electronic devices and circuit theory

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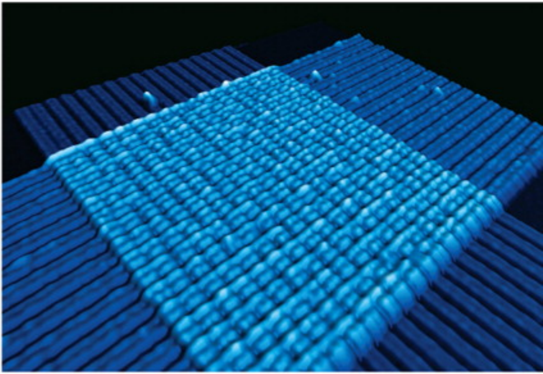

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SIGNIFICANT EQUATIONS

1 Semiconductor Diodes $W = QV$, 1 eV $= 1.6 \times 10^{-19}$ J, $I_D = I_s\,(e^{V_D/nV_T} - 1)$, $V_T = kT/q$, $T_{\text{K}} = T_{\text{C}} + 273^\circ$, $k = 1.38 \times 10^{-23}$ J/K, $V_K \cong 0.7$ V (Si), $V_K \cong 0.3$ V(Ge), $V_K \cong 1.2$ V (GaAs), $R_D = V_D/I_D$, $r_d = 26\text{ mV}/I_D$, $r_{\text{av}} = \Delta V_d/\Delta I_d|_{\text{pt. to pt.}}$, $P_D = V_D\,I_D$, $T_C = (\Delta V_Z/V_Z)/(T_1 - T_0) \times 100\%/^\circ\text{C}$

2 Diode Applications Silicon: $V_K \cong 0.7$ V, germanium: $V_K \cong 0.3$ V, GaAs: $V_K \cong 1.2$ V; half-wave: $V_{\text{dc}} = 0.318V_m$; full-wave: $V_{\text{dc}} = 0.636V_m$

3 Bipolar Junction Transistors $I_E = I_C + I_B$, $I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$, $I_C \cong I_E$, $V_{BE} = 0.7$ V, $\alpha_{\text{dc}} = I_C/I_E$, $I_C = \alpha I_E + I_{CBO}$, $\alpha_{\text{ac}} = \Delta I_C/\Delta I_E$, $I_{CEO} = I_{CBO}/(1 - \alpha)$, $\beta_{\text{dc}} = I_C/I_B$, $\beta_{\text{ac}} = \Delta I_C/\Delta I_B$, $\alpha = \beta/(\beta + 1)$, $\beta = \alpha/(1 - \alpha)$, $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$, $P_{C_{\max}} = V_{CE}I_C$

4 DC Biasing—BJTs In general: $V_{BE} = 0.7$ V, $I_C \cong I_E$, $I_C = \beta I_B$; fixed-bias: $I_B = (V_{CC} - V_{BE})/R_B$, $V_{CE} = V_{CC} - I_CR_C$, $I_{C_{\text{sat}}} = V_{CC}/R_C$; emitter-stabilized: $I_B = (V_{CC} - V_{BE})/(R_B + (\beta + 1)R_E)$, $R_i = (\beta + 1)R_E$, $V_{CE} = V_{CC} - I_C(R_C + R_E)$, $I_{C_{\text{sat}}} = V_{CC}/(R_C + R_E)$; voltage-divider: exact: $R_{\text{Th}} = R_1 \| R_2$, $E_{\text{Th}} = R_2V_{CC}/(R_1 + R_2)$, $I_B = (E_{\text{Th}} - V_{BE})/(R_{\text{Th}} + (\beta + 1)R_E)$, $V_{CE} = V_{CC} - I_C(R_C + R_E)$, approximate: $\beta R_E \geq 10R_2$, $V_B = R_2V_{CC}/(R_1 + R_2)$, $V_E = V_B - V_{BE}$, $I_C \cong I_E = V_E/R_E$; voltage-feedback: $I_B = (V_{CC} - V_{BE})/(R_B + \beta(R_C + R_E))$; common-base: $I_B = (V_{EE} - V_{BE})/R_E$; switching transistors: $t_{\text{on}} = t_r + t_d$, $t_{\text{off}} = t_s + t_f$; stability: $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$; fixed-bias: $S(I_{CO}) = \beta + 1$; emitter-bias: $S(I_{CO}) = (\beta + 1)(1 + R_B/R_E)/(1 + \beta + R_B/R_E)$; voltage-divider: $S(I_{CO}) = (\beta + 1)(1 + R_{\text{Th}}/R_E)/(1 + \beta + R_{\text{Th}}/R_E)$; feedback-bias: $S(I_{CO}) = (\beta + 1)(1 + R_B/R_C)/(1 + \beta + R_B/R_C)$, $S(V_{BE}) = \Delta I_C/\Delta V_{BE}$; fixed-bias: $S(V_{BE}) = -\beta/R_B$; emitter-bias: $S(V_{BE}) = -\beta/(R_B + (\beta + 1)R_E)$; voltage-divider: $S(V_{BE}) = -\beta/(R_{\text{Th}} + (\beta + 1)R_E)$; feedback bias: $S(V_{BE}) = -\beta/(R_B + (\beta + 1)R_C)$, $S(\beta) = \Delta I_C/\Delta\beta$; fixed-bias: $S(\beta) = I_{C_1}/\beta_1$; emitter-bias: $S(\beta) = I_{C_1}(1 + R_B/R_E)/(\beta_1(1 + \beta_2 + R_B/R_E))$; voltage-divider: $S(\beta) = I_{C_1}(1 + R_{\text{Th}}/R_E)/(\beta_1(1 + \beta_2 + R_{\text{Th}}/R_E))$; feedback-bias: $S(\beta) = I_{C_1}(1 + R_B/R_C)/(\beta_1(1 + \beta_2 + R_B/R_C))$, $\Delta I_C = S(I_{CO})\,\Delta I_{CO} + S(V_{BE})\,\Delta V_{BE} + S(\beta)\,\Delta\beta$

5 BJT AC Analysis $r_e = 26\text{ mV}/I_E$; CE fixed-bias: $Z_i \cong \beta r_e$, $Z_o \cong R_C$, $A_v = -R_C/r_e$; voltage-divider bias: $Z_i = R_1 \| R_2 \| \beta r_e$, $Z_o \cong R_C$, $A_v = -R_C/r_e$; CE emitter-bias: $Z_i \cong R_B \| \beta R_E$, $Z_o \cong R_C$, $A_v \cong -R_C/R_E$; emitter-follower: $Z_i \cong R_B \| \beta R_E$, $Z_o \cong r_e$, $A_v \cong 1$; common-base: $Z_i \cong R_E \| r_e$, $Z_o \cong R_C$, $A_v \cong R_C/r_e$; collector feedback: $Z_i \cong r_e/(1/\beta + R_C/R_F)$, $Z_o \cong R_C \| R_F$, $A_v = -R_C/r_e$; collector dc feedback: $Z_i \cong R_{F_1} \| \beta r_e$, $Z_o \cong R_C \| R_{F_2}$, $A_v = -(R_{F_2} \| R_C)/r_e$; effect of load impedance: $A_v = R_LA_{v_{\text{NL}}}/(R_L + R_o)$, $A_i = -A_vZ_i/R_L$; effect of source impedance: $V_i = R_iV_s/(R_i + R_s)$, $A_{v_s} = R_iA_{v_{\text{NL}}}/(R_i + R_s)$, $I_s = V_s/(R_s + R_i)$; combined effect of load and source impedance: $A_v = R_LA_{v_{\text{NL}}}/(R_L + R_o)$, $A_{v_s} = (R_i/(R_i + R_s))(R_L/(R_L + R_o))A_{v_{\text{NL}}}$, $A_i = -A_vR_i/R_L$, $A_{i_s} = -A_{v_s}(R_s + R_i)/R_L$; cascode connection: $A_v = A_{v_1}A_{v_2}$; Darlington connection: $\beta_D = \beta_1\beta_2$; emitter-follower configuration: $I_B = (V_{CC} - V_{BE})/(R_B + \beta_DR_E)$, $I_C \cong I_E \cong \beta_DI_B$, $Z_i = R_B \| \beta_1\beta_2R_E$, $A_i = \beta_DR_B/(R_B + \beta_DR_E)$, $A_v \cong 1$, $Z_o = r_{e_1}/\beta_2 + r_{e_2}$; basic amplifier configuration: $Z_i = R_1 \| R_2 \| Z_i'$, $Z_i' = \beta_1(r_{e_1} + \beta_2r_{e_2})$, $A_i = \beta_D(R_1 \| R_2)/(R_1 \| R_2 + Z_i')$, $A_v = \beta_DR_C/Z_i'$, $Z_o = R_C \| r_{o_2}$; feedback pair: $I_{B_1} = (V_{CC} - V_{BE_1})/(R_B + \beta_1\beta_2R_C)$, $Z_i = R_B \| Z_i'$, $Z_i' = \beta_1r_{e_1} + \beta_1\beta_2R_C$, $A_i = -\beta_1\beta_2R_B/(R_B + \beta_1\beta_2R_C)$ $A_v = \beta_2R_C/(r_e + \beta_2R_C) \cong 1$, $Z_o \cong r_{e_1}/\beta_2$.

6 Field-Effect Transistors $I_G = 0$ A, $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$, $I_D = I_S$, $V_{GS} = V_P\,(1 - \sqrt{I_D/I_{DSS}})$, $I_D = I_{DSS}/4$ (if $V_{GS} = V_P/2$), $I_D = I_{DSS}/2$ (if $V_{GS} \cong 0.3\,V_P$), $P_D = V_{DS}I_D$, $r_d = r_o/(1 - V_{GS}/V_P)^2$; MOSFET: $I_D = k(V_{GS} - V_T)^2$, $k = I_{D(\text{on})}/(V_{GS(\text{on})} - V_T)^2$

7 FET Biasing Fixed-bias: $V_{GS} = -V_{GG}$, $V_{DS} = V_{DD} - I_DR_D$; self-bias: $V_{GS} = -I_DR_S$, $V_{DS} = V_{DD} - I_D(R_S + R_D)$, $V_S = I_DR_S$; voltage-divider: $V_G = R_2V_{DD}/(R_1 + R_2)$, $V_{GS} = V_G - I_DR_S$, $V_{DS} = V_{DD} - I_D(R_D + R_S)$; common-gate configuration: $V_{GS} = V_{SS} - I_DR_S$, $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$; special case: $V_{GS_Q} = 0\ V$: $I_{I_Q} = I_{DSS}$, $V_{DS} = V_{DD} - I_DR_D$, $V_D = V_{DS}$, $V_S = 0$ V. enhancement-type MOSFET: $I_D = k(V_{GS} - V_{GS(\text{Th})})^2$, $k = I_{D(\text{on})}/(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$; feedback bias: $V_{DS} = V_{GS}$, $V_{GS} = V_{DD} - I_DR_D$; voltage-divider: $V_G = R_2V_{DD}/(R_1 + R_2)$, $V_{GS} = V_G - I_DR_S$; universal curve: $m = |V_P|/I_{DSS}R_S$, $M = m \times V_G/|V_P|$, $V_G = R_2V_{DD}/(R_1 + R_2)$

8 FET Amplifiers $g_m = y_{fs} = \Delta I_D/\Delta V_{GS}$, $g_{m0} = 2I_{DSS}/|V_P|$, $g_m = g_{m0}(1 - V_{GS}/V_P)$, $g_m = g_{m0}\sqrt{I_D/I_{DSS}}$, $r_d = 1/y_{os} = \Delta V_{DS}/\Delta I_D|_{V_{GS}=\text{constant}}$; fixed-bias: $Z_i = R_G$, $Z_o \cong R_D$, $A_v = -g_mR_D$; self-bias (bypassed Rs): $Z_i = R_G$, $Z_o \cong R_D$, $A_v = -g_mR_D$; self-bias (unbypassed Rs): $Z_i = R_G$, $Z_o = R_D$, $A_v \cong -g_mR_D/(1 + g_mR_s)$; voltage-divider bias: $Z_i = R_1 \| R_2$, $Z_o = R_D$, $A_v = -g_mR_D$; source follower: $Z_i = R_G$, $Z_o = R_S \| 1/g_m$, $A_v \cong g_mR_S/(1 + g_mR_S)$; common-gate: $Z_i = R_S \| 1/g_m$, $Z_o \cong R_D$, $A_v = g_mR_D$; enhancement-type MOSFETs: $g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$; drain-feedback configuration: $Z_i \cong R_F/(1 + g_mR_D)$, $Z_o \cong R_D$, $A_v \cong -g_mR_D$; voltage-divider bias: $Z_i = R_1 \| R_2$, $Z_o \cong R_D$, $A_v \cong -g_mR_D$.

9 BJT and JFET Frequency Response $\log_e a = 2.3 \log_{10} a$, $\log_{10} 1 = 0$, $\log_{10} a/b = \log_{10} a - \log_{10} b$, $\log_{10} 1/b = -\log_{10} b$, $\log_{10} ab = \log_{10} a + \log_{10} b$, $G_{\text{dB}} = 10 \log_{10} P_2/P_1$, $G_{\text{dBm}} = 10 \log_{10} P_2/1\text{ mW}|_{600\,\Omega}$, $G_{\text{dB}} = 20 \log_{10} V_2/V_1$, $G_{dB_T} = G_{dB_1} + G_{dB_2} + \cdots + G_{dB_n}$ $P_{o_{HPF}} = 0.5P_{o_{\text{mid}}}$, $\text{BW} = f_1 - f_2$; low frequency (BJT): $f_{L_S} = 1/2\pi(R_s + R_i)C_s$, $f_{L_C} = 1/2\pi(R_o + R_L)C_C$, $f_{L_E} = 1/2\pi R_e C_E$, $R_e = R_E \| (R_s'/\beta + r_e)$, $R_s' = R_s \| R_1 \| R_2$, FET: $f_{L_G} = 1/2\pi(R_{\text{sig}} + R_i)C_G$, $f_{L_C} = 1/2\pi(R_o + R_L)C_C$, $f_{L_S} = 1/2\pi R_{eq} C_S$, $R_{eq} = R_S \| 1/g_m (r_d \cong \infty\,\Omega)$; Miller effect: $C_{M_i} = (1 - A_v)C_f$, $C_{M_o} = (1 - 1/A_v)C_f$; high frequency (BJT): $f_{H_i} = 1/2\pi R_{\text{Th}_i} C_i$, $R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| R_i$, $C_i = C_{w_i} + C_{be} + (1 - A_v)C_{bc}$, $f_{H_o} = 1/2\pi R_{\text{Th}_o} C_o$, $R_{\text{Th}_o} = R_C \| R_L \| r_o$, $C_o = C_{W_o} + C_{ce} + C_{M_o}$, $f_\beta \cong 1/2\pi\beta_{\text{mid}} r_e (C_{be} + C_{bc})$, $f_T = \beta_{\text{mid}} f_\beta$; FET: $f_{H_i} = 1/2\pi R_{\text{Th}_i} C_i$, $R_{\text{Th}_i} = R_{\text{sig}} \| R_G$, $C_i = C_{W_i} + C_{gs} + C_{M_i}$, $C_{M_i} = (1 - A_v)C_{gd}$ $f_{H_o} = 1/2\pi R_{\text{Th}_o} C_o$, $R_{\text{Th}_o} = R_D \| R_L \| r_d$, $C_o = C_{W_o} + C_{ds} + C_{M_o}$; $C_{M_o} = (1 - 1/A_v)C_{gd}$; multistage: $f_1' = f_1/\sqrt{2^{1/n} - 1}$, $f_2' = (\sqrt{2^{1/n} - 1})f_2$; square-wave testing: $f_{H_i} = 0.35/t_r$, % tilt $= P\% = ((V - V')/V) \times 100\%$, $f_{L_o} = (P/\pi)f_s$

10 Operational Amplifiers $\text{CMRR} = A_d/A_c$; $\text{CMRR(log)} = 20 \log_{10}(A_d/A_c)$; constant-gain multiplier: $V_o/V_1 = -R_f/R_1$; noninverting amplifier: $V_o/V_1 = 1 + R_f/R_1$; unity follower: $V_o = V_1$; summing amplifier: $V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$; integrator: $v_o(t) = -(1/R_1C_1)\int v_1 dt$

11 Op-Amp Applications Constant-gain multiplier: $A = -R_f/R_1$; noninverting: $A = 1 + R_f/R_1$: voltage summing: $V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$; high-pass active filter: $f_{oL} = 1/2\pi R_1 C_1$; low-pass active filter: $f_{oH} = 1/2\pi R_1 C_1$

12 Power Amplifiers

Power in: $P_i = V_{CC}I_{CQ}$
power out: $P_o = V_{CE}I_C = I_C^2 R_C = V_{CE}^2/R_C$ rms
$= V_{CE}I_C/2 = (I_C^2/2)R_C = V_{CE}^2/(2R_C)$ peak
$= V_{CE}I_C/8 = (I_C^2/8)R_C = V_{CE}^2/(8R_C)$ peak-to-peak

efficiency: $\%\eta = (P_o/P_i) \times 100\%$; maximum efficiency: Class A, series-fed = 25%; Class A, transformer-coupled = 50%; Class B, push-pull = 78.5%; transformer relations: $V_2/V_1 = N_2/N_1 = I_1/I_2$, $R_2 = (N_2/N_1)^2 R_1$; power output: $P_o = [(V_{CE_{\text{max}}} - V_{CE_{\text{min}}})(I_{C_{\text{max}}} - I_{C_{\text{min}}})]/8$; class B power amplifier: $P_i = V_{CC}\left[(2/\pi)I_{\text{peak}}\right]$; $P_o = V_L^2(\text{peak})/(2R_L)$; $\%\eta = (\pi/4)\left[V_L(\text{peak})/V_{CC}\right] \times 100\%$; $P_Q = P_{2Q}/2 = (P_i - P_o)/2$; maximum $P_o = V_{CC}^2/2R_L$; maximum $P_i = 2V_{CC}^2/\pi R_L$; maximum $P_{2Q} = 2V_{CC}^2/\pi^2 R_L$; % total harmonic distortion (% THD) $= \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$; heat-sink: $T_J = P_D\theta_{JA} + T_A$, $\theta_{JA} = 40°\text{C/W}$ (free air); $P_D = (T_J - T_A)/(\theta_{JC} + \theta_{CS} + \theta_{SA})$

13 Linear-Digital ICs Ladder network: $V_o = [(D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + \cdots + D_n \times 2^n)/2^n]V_{\text{ref}}$; 555 oscillator: $f = 1.44(R_A + 2R_B)C$; 555 monostable: $T_{\text{high}} = 1.1R_A C$; VCO: $f_o = (2/R_1C_1)[(V^+ - V_C)/V^+]$; phase-locked loop (PLL): $f_o = 0.3/R_1C_1$, $f_L = \pm 8f_o/V$, $f_C = \pm(1/2\pi)\sqrt{2\pi f_L/(3.6 \times 10^3)C_2}$

14 Feedback and Oscillator Circuits $A_f = A/(1 + \beta A)$; series feedback; $Z_{if} = Z_i(1 + \beta A)$; shunt feedback: $Z_{if} = Z_i/(1 + \beta A)$; voltage feedback: $Z_{of} = Z_o/(1 + \beta A)$; current feedback; $Z_{of} = Z_o(1 + \beta A)$; gain stability: $dA_f/A_f = 1/(|1 + \beta A|)(dA/A)$; oscillator; $\beta A = 1$; phase shift: $f = 1/2\pi RC\sqrt{6}$, $\beta = 1/29$, $A > 29$; FET phase shift: $|A| = g_m R_L$, $R_L = R_D r_d/(R_D + r_d)$; transistor phase shift: $f = (1/2\pi RC)[1/\sqrt{6 + 4(R_C/R)}]$, $h_{fe} > 23 + 29(R_C/R) + 4(R/R_C)$; Wien bridge: $R_3/R_4 = R_1/R_2 + C_2/C_1$, $f_o = 1/2\pi\sqrt{R_1C_1R_2C_2}$; tuned: $f_o = 1/2\pi\sqrt{LC_{\text{eq}}}$, $C_{\text{eq}} = C_1C_2/(C_1 + C_2)$, Hartley: $L_{\text{eq}} = L_1 + L_2 + 2M$, $f_o = 1/2\pi\sqrt{L_{\text{eq}}C}$

15 Power Supplies (Voltage Regulators) Filters: $r = V_r(\text{rms})/V_{\text{dc}} \times 100\%$, $\text{V.R.} = (V_{NL} - V_{FL})/V_{FL} \times 100\%$, $V_{\text{dc}} = V_m - V_r(\text{p-p})/2$, $V_r(\text{rms}) = V_r(\text{p-p})/2\sqrt{3}$, $V_r(\text{rms}) \cong (I_{\text{dc}}/4\sqrt{3})(V_{\text{dc}}/V_m)$; full-wave, light load $V_r(\text{rms}) = 2.4I_{\text{dc}}/C$, $V_{\text{dc}} = V_m - 4.17I_{\text{dc}}/C$, $r = (2.4I_{\text{dc}}CV_{\text{dc}}) \times 100\% = 2.4/R_LC \times 100\%$, $I_{\text{peak}} = T/T_1 \times I_{\text{dc}}$; RC filter: $V_{\text{dc}}' = R_L V_{\text{dc}}/(R + R_L)$, $X_C = 2.653/C$(half-wave), $X_C = 1.326/C$ (full-wave), $V_r'(\text{rms}) = (X_C/\sqrt{R^2 + X_C^2})$; regulators: $IR = (I_{NL} - I_{FL})/I_{FL} \times 100\%$, $V_L = V_Z(1 + R_1/R_2)$, $V_o = V_{\text{ref}}(1 + R_2/R_1) + I_{\text{adj}}R_2$

16 Other Two-Terminal Devices Varactor diode: $C_T = C(0)/(1 + |V_r/V_T|)^n$, $TC_C = (\Delta C/C_o(T_1 - T_0)) \times 100\%$; photodiode: $W = \hbar f$, $\lambda = v/f$, 1 lm $= 1.496 \times 10^{-10}$ W, 1 Å $= 10^{-10}$ m, 1 fc $= 1\text{ lm/ft}^2 = 1.609 \times 10^{-9}\text{ W/m}^2$

17 *pnpn* and Other Devices Diac: $V_{BR_1} = V_{BR_2} \pm 0.1\, V_{BR_2}$ UJT: $R_{BB} = (R_{B_1} + R_{B_2})|_{I_E=0}$, $V_{R_{B_1}} = \eta V_{BB}|_{I_E=0}$, $\eta = R_{B_1}/(R_{B_1} + R_{B_2})|_{I_E=0}$, $V_P = \eta V_{BB} + V_D$; phototransistor: $I_C \cong h_{fe}I_\lambda$; PUT: $\eta = R_{B_1}/(R_{B_1} + R_{B_2})$, $V_P = \eta V_{BB} + V_D$

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DEDICATION

To Else Marie, Alison and Mark, Eric and Rachel, Stacey and Jonathan, and our eight granddaughters: Kelcy, Morgan, Codie, Samantha, Lindsey, Britt, Skylar, and Aspen.

To Katrin, Kira and Thomas, Larren and Patricia, and our six grandsons: Justin, Brendan, Owen, Tyler, Colin, and Dillon.

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PREFACE

The preparation of the preface for the 11th edition resulted in a bit of reflection on the 40 years since the first edition was published in 1972 by two young educators eager to test their ability to improve on the available literature on electronic devices. Although one may prefer the term *semiconductor* devices rather than *electronic* devices, the first edition was almost exclusively a survey of vacuum-tube devices—a subject without a single section in the new Table of Contents. The change from tubes to predominantly semiconductor devices took almost five editions, but today it is simply referenced in some sections. It is interesting, however, that when field-effect transistor (FET) devices surfaced in earnest, a number of the analysis techniques used for tubes could be applied because of the similarities in the ac equivalent models of each device.

We are often asked about the revision process and how the content of a new edition is defined. In some cases, it is quite obvious that the computer software has been updated, and the changes in application of the packages must be spelled out in detail. This text was the first to emphasize the use of computer software packages and provided a level of detail unavailable in other texts. With each new version of a software package, we have found that the supporting literature may still be in production, or the manuals lack the detail for new users of these packages. Sufficient detail in this text ensures that a student can apply each of the software packages covered without additional instructional material.

The next requirement with any new edition is the need to update the content reflecting changes in the available devices and in the characteristics of commercial devices. This can require extensive research in each area, followed by decisions regarding depth of coverage and whether the listed improvements in response are valid and deserve recognition. The classroom experience is probably one of the most important resources for defining areas that need expansion, deletion, or revision. The feedback from students results in marked-up copies of our texts with inserts creating a mushrooming copy of the material. Next, there is the input from our peers, faculty at other institutions using the text, and, of course, reviewers chosen by Pearson Education to review the text. One source of change that is less obvious is a simple rereading of the material following the passing of the years since the last edition. Rereading often reveals material that can be improved, deleted, or expanded.

For this revision, the number of changes far outweighs our original expectations. However, for someone who has used previous editions of the text, the changes will probably be less obvious. However, major sections have been moved and expanded, some 100-plus problems have been added, new devices have been introduced, the number of applications has been increased, and new material on recent developments has been added throughout the text. We believe that the current edition is a significant improvement over the previous editions.

As instructors, we are all well aware of the importance of a high level of accuracy required for a text of this kind. There is nothing more frustrating for a student than to work a problem over from many different angles and still find that the answer differs from the solution at the back of the text or that the problem seems undoable. We were pleased to find that there were fewer than half a dozen errors or misprints reported since the last edition. When you consider the number of examples and problems in the text along with the length of the text material, this statistic clearly suggests that the text is as error-free as possible. Any contributions from users to this list were quickly acknowledged, and the sources were thanked for taking the time to send the changes to the publisher and to us.

Although the current edition now reflects all the changes we feel it should have, we expect that a revised edition will be required somewhere down the line. We invite you to respond to this edition so that we can start developing a package of ideas and thoughts that will help us improve the content for the next edition. We promise a quick response to your comments, whether positive or negative.

NEW TO THIS EDITION

- Throughout the chapters, there are extensive changes in the problem sections. Over 100 new problems have been added, and a significant number of changes have been made to the existing problems.
- A significant number of computer programs were all rerun and the descriptions updated to include the effects of using OrCAD version 16.3 and Multisim version 11.1. In addition, the introductory chapters are now assuming a broader understanding of computer methods, resulting in a revised introduction to the two programs.
- Throughout the text, photos and biographies of important contributors have been added. Included among these are Sidney Darlington, Walter Schottky, Harry Nyquist, Edwin Colpitts, and Ralph Hartley.
- New sections were added throughout the text. There is now a discussion on the impact of combined dc and ac sources on diode networks, of multiple BJT networks, VMOS and UMOS power FETs, Early voltage, frequency impact on the basic elements, effect of R_S on an amplifier's frequency response, gain-bandwidth product, and a number of other topics.
- A number of sections were completely rewritten due to reviewers' comments or changing priorities. Some of the areas revised include bias stabilization, current sources, feedback in the dc and ac modes, mobility factors in diode and transistor response, transition and diffusion capacitive effects in diodes and transistor response characteristics, reverse-saturation current, breakdown regions (cause and effect), and the hybrid model.
- In addition to the revision of numerous sections described above, there are a number of sections that have been expanded to respond to changes in priorities for a text of this kind. The section on solar cells now includes a detailed examination of the materials employed, additional response curves, and a number of new practical applications. The coverage of the Darlington effect was totally rewritten and expanded to include detailed examination of the emitter-follower and collector gain configurations. The coverage of transistors now includes details on the cross-bar latch transistor and carbon nanotubes. The discussion of LEDs includes an expanded discussion of the materials employed, comparisons to today's other lighting options, and examples of the products defining the future of this important semiconductor device. The data sheets commonly included in a text of this type are now discussed in detail to ensure a well-established link when the student enters the industrial community.
- Updated material appears throughout the text in the form of photos, artwork, data sheets, and so forth, to ensure that the devices included reflect the components available today with the characteristics that have changed so rapidly in recent years. In addition, the parameters associated with the content and all the example problems are more in line with the device characteristics available today. Some devices, no longer available or used very infrequently, were dropped to ensure proper emphasis on the current trends.
- There are a number of important organizational changes throughout the text to ensure the best sequence of coverage in the learning process. This is readily apparent in the early dc chapters on diodes and transistors, in the discussion of current gain in the ac chapters for BJTs and JFETs, in the Darlington section, and in the frequency response chapters. It is particularly obvious in Chapter 16, where topics were dropped and the order of sections changed dramatically.

INSTRUCTOR SUPPLEMENTS

To download the supplements listed below, please visit: **http://www.pearsonhighered.com/irc** and enter “Electronic Devices and Circuit Theory” in the search bar. From there, you will be able to register to receive an instructor’s access code. Within 48 hours after registering, you will receive a confirming email, including an instructor access code. Once you have received your code, return to the site and log on for full instructions on how to download the materials you wish to use.

PowerPoint Presentation–(ISBN 0132783746). This supplement contains all figures from the text as well as a new set of lecture notes highlighting important concepts.

TestGen® Computerized Test Bank–(ISBN 013278372X). This electronic bank of test questions can be used to develop customized quizzes, tests, and/or exams.

Instructor’s Resource Manual–(ISBN 0132783738). This supplement contains the solutions to the problems in the text and lab manual.

STUDENT SUPPLEMENTS

Laboratory Manual–(ISBN 0132622459) . This supplement contains over 35 class-tested experiments for students to use to demonstrate their comprehension of course material.

Companion Website–Student study resources are available at **www.pearsonhighered.com/boylestad**

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BRIEF CONTENTS

Preface v

CHAPTER 1: Semiconductor Diodes 1

CHAPTER 2: Diode Applications 55

CHAPTER 3: Bipolar Junction Transistors 129

CHAPTER 4: DC Biasing—BJTs 160

CHAPTER 5: BJT AC Analysis 253

CHAPTER 6: Field-Effect Transistors 378

CHAPTER 7: FET Biasing 422

CHAPTER 8: FET Amplifiers 481

CHAPTER 9: BJT and JFET Frequency Response 545

CHAPTER 10: Operational Amplifiers 607

CHAPTER 11: Op-Amp Applications 653

CHAPTER 12: Power Amplifiers 683

CHAPTER 13: Linear-Digital ICs 722

CHAPTER 14: Feedback and Oscillator Circuits 751

CHAPTER 15: Power Supplies (Voltage Regulators) 783

CHAPTER 16: Other Two-Terminal Devices 811

CHAPTER 17: *pnpn* and Other Devices 841

Appendix A: Hybrid Parameters—Graphical Determinations and Conversion Equations (Exact and Approximate) 879

Appendix B: Ripple Factor and Voltage Calculations 885

Appendix C: Charts and Tables 891

Appendix D: Solutions to Selected Odd-Numbered Problems 893

Index 901

CONTENTS

Preface v

CHAPTER 1: Semiconductor Diodes 1
- **1.1** Introduction 1
- **1.2** Semiconductor Materials: Ge, Si, and GaAs 2
- **1.3** Covalent Bonding and Intrinsic Materials 3
- **1.4** Energy Levels 5
- **1.5** *n*-Type and *p*-Type Materials 7
- **1.6** Semiconductor Diode 10
- **1.7** Ideal Versus Practical 20
- **1.8** Resistance Levels 21
- **1.9** Diode Equivalent Circuits 27
- **1.10** Transition and Diffusion Capacitance 30
- **1.11** Reverse Recovery Time 31
- **1.12** Diode Specification Sheets 32
- **1.13** Semiconductor Diode Notation 35
- **1.14** Diode Testing 36
- **1.15** Zener Diodes 38
- **1.16** Light-Emitting Diodes 41
- **1.17** Summary 48
- **1.18** Computer Analysis 49

CHAPTER 2: Diode Applications 55
- **2.1** Introduction 55
- **2.2** Load-Line Analysis 56
- **2.3** Series Diode Configurations 61
- **2.4** Parallel and Series–Parallel Configurations 67
- **2.5** AND/OR Gates 70
- **2.6** Sinusoidal Inputs; Half-Wave Rectification 72
- **2.7** Full-Wave Rectification 75
- **2.8** Clippers 78
- **2.9** Clampers 85
- **2.10** Networks with a dc and ac Source 88

2.11 Zener Diodes **91**
2.12 Voltage-Multiplier Circuits **98**
2.13 Practical Applications **101**
2.14 Summary **111**
2.15 Computer Analysis **112**

CHAPTER 3: Bipolar Junction Transistors **129**
3.1 Introduction **129**
3.2 Transistor Construction **130**
3.3 Transistor Operation **130**
3.4 Common-Base Configuration **131**
3.5 Common-Emitter Configuration **136**
3.6 Common-Collector Configuration **143**
3.7 Limits of Operation **144**
3.8 Transistor Specification Sheet **145**
3.9 Transistor Testing **149**
3.10 Transistor Casing and Terminal Identification **151**
3.11 Transistor Development **152**
3.12 Summary **154**
3.13 Computer Analysis **155**

CHAPTER 4: DC Biasing—BJTs **160**
4.1 Introduction **160**
4.2 Operating Point **161**
4.3 Fixed-Bias Configuration **163**
4.4 Emitter-Bias Configuration **169**
4.5 Voltage-Divider Bias Configuration **175**
4.6 Collector Feedback Configuration **181**
4.7 Emitter-Follower Configuration **186**
4.8 Common-Base Configuration **187**
4.9 Miscellaneous Bias Configurations **189**
4.10 Summary Table **192**
4.11 Design Operations **194**
4.12 Multiple BJT Networks **199**
4.13 Current Mirrors **205**
4.14 Current Source Circuits **208**
4.15 *pnp* Transistors **210**
4.16 Transistor Switching Networks **211**
4.17 Troubleshooting Techniques **215**
4.18 Bias Stabilization **217**
4.19 Practical Applications **226**
4.20 Summary **233**
4.21 Computer Analysis **235**

CHAPTER 5: BJT AC Analysis 253
5.1 Introduction 253
5.2 Amplification in the AC Domain 253
5.3 BJT Transistor Modeling 254
5.4 The r_e Transistor Model 257
5.5 Common-Emitter Fixed-Bias Configuration 262
5.6 Voltage-Divider Bias 265
5.7 CE Emitter-Bias Configuration 267
5.8 Emitter-Follower Configuration 273
5.9 Common-Base Configuration 277
5.10 Collector Feedback Configuration 279
5.11 Collector DC Feedback Configuration 284
5.12 Effect of R_L and R_s 286
5.13 Determining the Current Gain 291
5.14 Summary Tables 292
5.15 Two-Port Systems Approach 292
5.16 Cascaded Systems 300
5.17 Darlington Connection 305
5.18 Feedback Pair 314
5.19 The Hybrid Equivalent Model 319
5.20 Approximate Hybrid Equivalent Circuit 324
5.21 Complete Hybrid Equivalent Model 330
5.22 Hybrid π Model 337
5.23 Variations of Transistor Parameters 338
5.24 Troubleshooting 340
5.25 Practical Applications 342
5.26 Summary 349
5.27 Computer Analysis 352

CHAPTER 6: Field-Effect Transistors 378
6.1 Introduction 378
6.2 Construction and Characteristics of JFETs 379
6.3 Transfer Characteristics 386
6.4 Specification Sheets (JFETs) 390
6.5 Instrumentation 394
6.6 Important Relationships 395
6.7 Depletion-Type MOSFET 396
6.8 Enhancement-Type MOSFET 402
6.9 MOSFET Handling 409
6.10 VMOS and UMOS Power and MOSFETs 410
6.11 CMOS 411
6.12 MESFETs 412
6.13 Summary Table 414

6.14 Summary **414**
6.15 Computer Analysis **416**

CHAPTER 7: FET Biasing 422

7.1 Introduction **422**
7.2 Fixed-Bias Configuration **423**
7.3 Self-Bias Configuration **427**
7.4 Voltage-Divider Biasing **431**
7.5 Common-Gate Configuration **436**
7.6 Special Case $V_{GS_Q} = 0\text{ V}$ **439**
7.7 Depletion-Type MOSFETs **439**
7.8 Enhancement-Type MOSFETs **443**
7.9 Summary Table **449**
7.10 Combination Networks **449**
7.11 Design **452**
7.12 Troubleshooting **455**
7.13 *p*-Channel FETs **455**
7.14 Universal JFET Bias Curve **458**
7.15 Practical Applications **461**
7.16 Summary **470**
7.17 Computer Analysis **471**

CHAPTER 8: FET Amplifiers 481

8.1 Introduction **481**
8.2 JFET Small-Signal Model **482**
8.3 Fixed-Bias Configuration **489**
8.4 Self-Bias Configuration **492**
8.5 Voltage-Divider Configuration **497**
8.6 Common-Gate Configuration **498**
8.7 Source-Follower (Common-Drain) Configuration **501**
8.8 Depletion-Type MOSFETs **505**
8.9 Enhancement-Type MOSFETs **506**
8.10 E-MOSFET Drain-Feedback Configuration **507**
8.11 E-MOSFET Voltage-Divider Configuration **510**
8.12 Designing FET Amplifier Networks **511**
8.13 Summary Table **513**
8.14 Effect of R_L and R_{sig} **516**
8.15 Cascade Configuration **518**
8.16 Troubleshooting **521**
8.17 Practical Applications **522**
8.18 Summary **530**
8.19 Computer Analysis **531**

CHAPTER 9: BJT and JFET Frequency Response **545**

9.1 Introduction **545**
9.2 Logarithms **545**
9.3 Decibels **550**
9.4 General Frequency Considerations **554**
9.5 Normalization Process **557**
9.6 Low-Frequency Analysis—Bode Plot **559**
9.7 Low-Frequency Response—BJT Amplifier with R_L **564**
9.8 Impact of R_s on the BJT Low-Frequency Response **568**
9.9 Low-Frequency Response—FET Amplifier **571**
9.10 Miller Effect Capacitance **574**
9.11 High-Frequency Response—BJT Amplifier **576**
9.12 High-Frequency Response—FET Amplifier **584**
9.13 Multistage Frequency Effects **586**
9.14 Square-Wave Testing **588**
9.15 Summary **591**
9.16 Computer Analysis **592**

CHAPTER 10: Operational Amplifiers **607**

10.1 Introduction **607**
10.2 Differential Amplifier Circuit **610**
10.3 BiFET, BiMOS, and CMOS Differential Amplifier Circuits **617**
10.4 Op-Amp Basics **620**
10.5 Practical Op-Amp Circuits **623**
10.6 Op-Amp Specifications—DC Offset Parameters **628**
10.7 Op-Amp Specifications—Frequency Parameters **631**
10.8 Op-Amp Unit Specifications **634**
10.9 Differential and Common-Mode Operation **639**
10.10 Summary **643**
10.11 Computer Analysis **644**

CHAPTER 11: Op-Amp Applications **653**

11.1 Constant-Gain Multiplier **653**
11.2 Voltage Summing **657**
11.3 Voltage Buffer **660**
11.4 Controlled Sources **661**
11.5 Instrumentation Circuits **663**
11.6 Active Filters **667**
11.7 Summary **670**
11.8 Computer Analysis **671**

CHAPTER 12: Power Amplifiers **683**

12.1 Introduction—Definitions and Amplifier Types **683**
12.2 Series-Fed Class A Amplifier **685**

12.3 Transformer-Coupled Class A Amplifier 688
12.4 Class B Amplifier Operation 695
12.5 Class B Amplifier Circuits 699
12.6 Amplifier Distortion 705
12.7 Power Transistor Heat Sinking 709
12.8 Class C and Class D Amplifiers 712
12.9 Summary 714
12.10 Computer Analysis 715

CHAPTER 13: Linear-Digital ICs 722
13.1 Introduction 722
13.2 Comparator Unit Operation 722
13.3 Digital–Analog Converters 729
13.4 Timer IC Unit Operation 732
13.5 Voltage-Controlled Oscillator 736
13.6 Phase-Locked Loop 738
13.7 Interfacing Circuitry 742
13.8 Summary 745
13.9 Computer Analysis 745

CHAPTER 14: Feedback and Oscillator Circuits 751
14.1 Feedback Concepts 751
14.2 Feedback Connection Types 752
14.3 Practical Feedback Circuits 758
14.4 Feedback Amplifier—Phase and Frequency Considerations 763
14.5 Oscillator Operation 766
14.6 Phase-Shift Oscillator 767
14.7 Wien Bridge Oscillator 770
14.8 Tuned Oscillator Circuit 771
14.9 Crystal Oscillator 774
14.10 Unijunction Oscillator 777
14.11 Summary 778
14.12 Computer Analysis 779

CHAPTER 15: Power Supplies (Voltage Regulators) 783
15.1 Introduction 783
15.2 General Filter Considerations 784
15.3 Capacitor Filter 786
15.4 *RC* Filter 789
15.5 Discrete Transistor Voltage Regulation 791
15.6 IC Voltage Regulators 798
15.7 Practical Applications 803
15.8 Summary 805
15.9 Computer Analysis 806

CHAPTER 16: Other Two-Terminal Devices 811
16.1 Introduction **811**
16.2 Schottky Barrier (Hot-Carrier) Diodes **811**
16.3 Varactor (Varicap) Diodes **815**
16.4 Solar Cells **819**
16.5 Photodiodes **824**
16.6 Photoconductive Cells **826**
16.7 IR Emitters **828**
16.8 Liquid-Crystal Displays **829**
16.9 Thermistors **831**
16.10 Tunnel Diodes **833**
16.11 Summary **837**

CHAPTER 17: *pnpn* and Other Devices 841
17.1 Introduction **841**
17.2 Silicon-Controlled Rectifier **841**
17.3 Basic Silicon-Controlled Rectifier Operation **842**
17.4 SCR Characteristics and Ratings **843**
17.5 SCR Applications **845**
17.6 Silicon-Controlled Switch **849**
17.7 Gate Turn-Off Switch **851**
17.8 Light-Activated SCR **852**
17.9 Shockley Diode **854**
17.10 Diac **854**
17.11 Triac **856**
17.12 Unijunction Transistor **857**
17.13 Phototransistors **865**
17.14 Opto-Isolators **867**
17.15 Programmable Unijunction Transistor **869**
17.16 Summary **874**

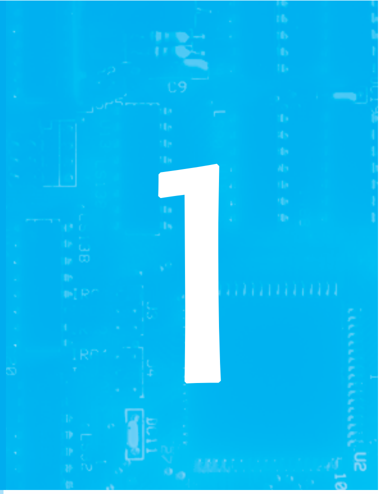
Appendix A: Hybrid Parameters—Graphical Determinations and Conversion Equations (Exact and Approximate) 879
A.1 Graphical Determination of the *h*-Parameters **879**
A.2 Exact Conversion Equations **883**
A.3 Approximate Conversion Equations **883**

Appendix B: Ripple Factor and Voltage Calculations 885
B.1 Ripple Factor of Rectifier **885**
B.2 Ripple Voltage of Capacitor Filter **886**
B.3 Relation of V_{dc} and V_m to Ripple r **887**
B.4 Relation of V_r(rms) and V_m to Ripple r **888**
B.5 Relation Connecting Conduction Angle, Percentage Ripple, and I_{peak}/I_{dc} for Rectifier-Capacitor Filter Circuits **889**

Appendix C: Charts and Tables 891

Appendix D: Solutions to Selected Odd-Numbered Problems 893

Index 901



1

Semiconductor Diodes

CHAPTER OBJECTIVES

- Become aware of the general characteristics of three important semiconductor materials: Si, Ge, GaAs.
- Understand conduction using electron and hole theory.
- Be able to describe the difference between *n*- and *p*-type materials.
- Develop a clear understanding of the basic operation and characteristics of a diode in the no-bias, forward-bias, and reverse-bias regions.
- Be able to calculate the dc, ac, and average ac resistance of a diode from the characteristics.
- Understand the impact of an equivalent circuit whether it is ideal or practical.
- Become familiar with the operation and characteristics of a Zener diode and light-emitting diode.

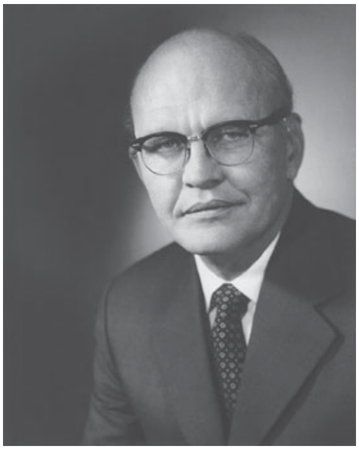
1.1 INTRODUCTION

One of the noteworthy things about this field, as in many other areas of technology, is how little the fundamental principles change over time. Systems are incredibly smaller, current speeds of operation are truly remarkable, and new gadgets surface every day, leaving us to wonder where technology is taking us. However, if we take a moment to consider that the majority of all the devices in use were invented decades ago and that design techniques appearing in texts as far back as the 1930s are still in use, we realize that most of what we see is primarily a steady improvement in construction techniques, general characteristics, and application techniques rather than the development of new elements and fundamentally new designs. The result is that most of the devices discussed in this text have been around for some time, and that texts on the subject written a decade ago are still good references with content that has not changed very much. The major changes have been in the understanding of how these devices work and their full range of capabilities, and in improved methods of teaching the fundamentals associated with them. The benefit of all this to the new student of the subject is that the material in this text will, we hope, have reached a level where it is relatively easy to grasp and the information will have application for years to come.

The miniaturization that has occurred in recent years leaves us to wonder about its limits. Complete systems now appear on wafers thousands of times smaller than the single element of earlier networks. The first integrated circuit (IC) was developed by Jack Kilby while working at Texas Instruments in 1958 (Fig. 1.1). Today, the Intel® Core™ i7 Extreme

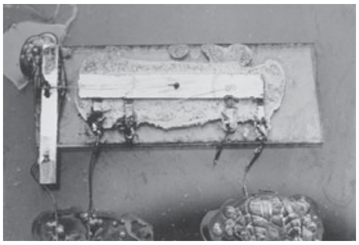
Edition Processor of Fig. 1.2 has 731 million transistors in a package that is only slightly larger than a 1.67 sq. inches. In 1965, Dr. Gordon E. Moore presented a paper predicting that the transistor count in a single IC chip would double every two years. Now, more than 45 years, later we find that his prediction is amazingly accurate and expected to continue for the next few decades. We have obviously reached a point where the primary purpose of the container is simply to provide some means for handling the device or system and to provide a mechanism for attachment to the remainder of the network. Further miniaturization appears to be limited by four factors: the quality of the semiconductor material, the network design technique, the limits of the manufacturing and processing equipment, and the strength of the innovative spirit in the semiconductor industry.

The first device to be introduced here is the simplest of all electronic devices, yet has a range of applications that seems endless. We devote two chapters to the device to introduce the materials commonly used in solid-state devices and review some fundamental laws of electric circuits.



Jack St. Clair Kilby, inventor of the integrated circuit and co-inventor of the electronic handheld calculator. (Courtesy of Texas Instruments.)

Born: Jefferson City, Missouri,1923. MS, University of Wisconsin. Director of Engineering and Technology, Components Group, Texas Instruments. Fellow of the IEEE. Holds more than 60 U.S. patents.



The first integrated circuit, a phase-shift oscillator, invented by Jack S. Kilby in 1958. (Courtesy of Texas Instruments.)

FIG. 1.1
Jack St. Clair Kilby.

1.2 SEMICONDUCTOR MATERIALS: Ge, Si, AND GaAs

The construction of every discrete (individual) solid-state (hard crystal structure) electronic device or integrated circuit begins with a semiconductor material of the highest quality.

Semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator.

In general, semiconductor materials fall into one of two classes: *single-crystal* and *compound.* Single-crystal semiconductors such as germanium (Ge) and silicon (Si) have a repetitive crystal structure, whereas compound semiconductors such as gallium arsenide (GaAs), cadmium sulfide (CdS), gallium nitride (GaN), and gallium arsenide phosphide (GaAsP) are constructed of two or more semiconductor materials of different atomic structures.

The three semiconductors used most frequently in the construction of electronic devices are Ge, Si, and GaAs.

In the first few decades following the discovery of the diode in 1939 and the transistor in 1947 germanium was used almost exclusively because it was relatively easy to find and was available in fairly large quantities. It was also relatively easy to refine to obtain very high levels of purity, an important aspect in the fabrication process. However, it was discovered in the early years that diodes and transistors constructed using germanium as the base material suffered from low levels of reliability due primarily to its sensitivity to changes in temperature. At the time, scientists were aware that another material, silicon, had improved temperature sensitivities, but the refining process for manufacturing silicon of very high levels of purity was still in the development stages. Finally, however, in 1954 the first silicon transistor was introduced, and silicon quickly became the semiconductor material of choice. Not only is silicon less temperature sensitive, but it is one of the most abundant materials on earth, removing any concerns about availability. The flood gates now opened to this new material, and the manufacturing and design technology improved steadily through the following years to the current high level of sophistication.

As time moved on, however, the field of electronics became increasingly sensitive to issues of speed. Computers were operating at higher and higher speeds, and communication systems were operating at higher levels of performance. A semiconductor material capable of meeting these new needs had to be found. The result was the development of the first GaAs transistor in the early 1970s. This new transistor had speeds of operation up to five times that of Si. The problem, however, was that because of the years of intense design efforts and manufacturing improvements using Si, Si transistor networks for most applications were cheaper to manufacture and had the advantage of highly efficient design strategies. GaAs was more difficult to manufacture at high levels of purity, was more expensive, and had little design support in the early years of development. However, in time the demand for increased speed resulted in more funding for GaAs research, to the point that today it is often used as the base material for new high-speed, very large scale integrated (VLSI) circuit designs.

This brief review of the history of semiconductor materials is not meant to imply that GaAs will soon be the only material appropriate for solid-state construction. Germanium devices are still being manufactured, although for a limited range of applications. Even though it is a temperature-sensitive semiconductor, it does have characteristics that find application in a limited number of areas. Given its availability and low manufacturing costs, it will continue to find its place in product catalogs. As noted earlier, Si has the benefit of years of development, and is the leading semiconductor material for electronic components and ICs. In fact, Si is still the fundamental building block for Intel's new line of processors.

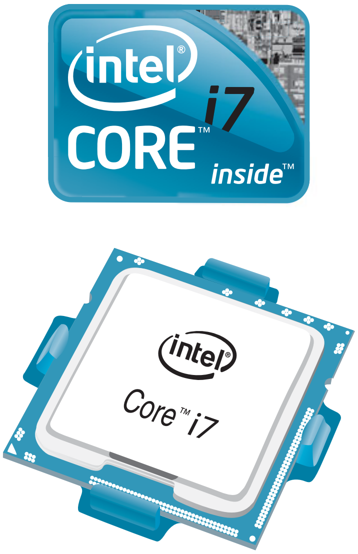
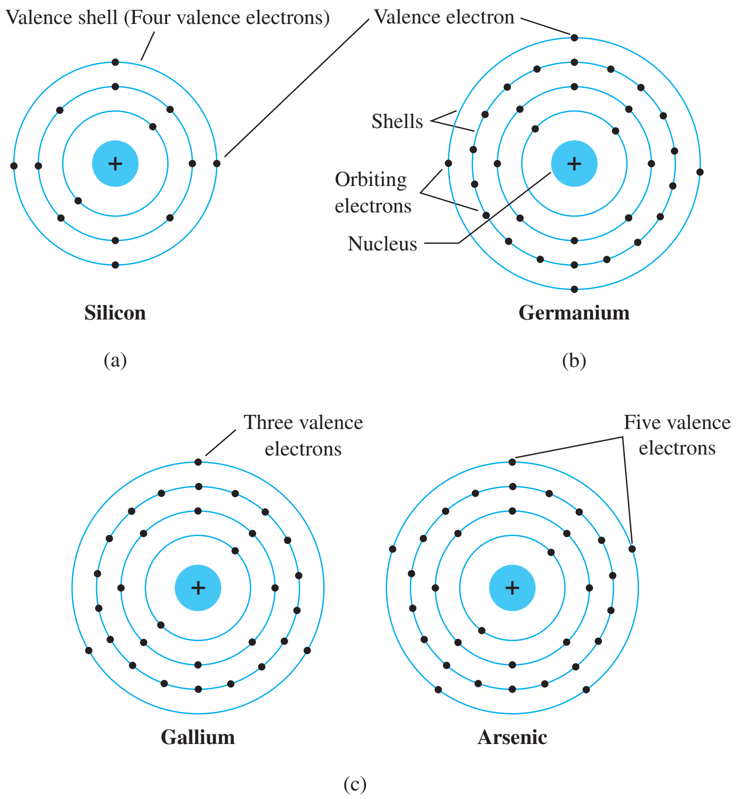


FIG. 1.2
Intel® Core™ i7 Extreme Edition Processor.

1.3 COVALENT BONDING AND INTRINSIC MATERIALS

To fully appreciate why Si, Ge, and GaAs are the semiconductors of choice for the electronics industry requires some understanding of the atomic structure of each and how the atoms are bound together to form a crystalline structure. The fundamental components of an atom are the electron, proton, and neutron. In the lattice structure, neutrons and protons form the nucleus and electrons appear in fixed orbits around the nucleus. The Bohr model for the three materials is provided in Fig. 1.3.



(a)

(b)

(c)

FIG. 1.3
Atomic structure of (a) silicon; (b) germanium; and (c) gallium and arsenic.

As indicated in Fig. 1.3, silicon has 14 orbiting electrons, germanium has 32 electrons, gallium has 31 electrons, and arsenic has 33 orbiting electrons (the same arsenic that is a very poisonous chemical agent). For germanium and silicon there are four electrons in the outermost shell, which are referred to as *valence electrons*. Gallium has three valence electrons and arsenic has five valence electrons. Atoms that have four valence electrons are called *tetravalent*, those with three are called *trivalent*, and those with five are called *pentavalent*. The term *valence* is used to indicate that the potential (ionization potential) required to remove any one of these electrons from the atomic structure is significantly lower than that required for any other electron in the structure.

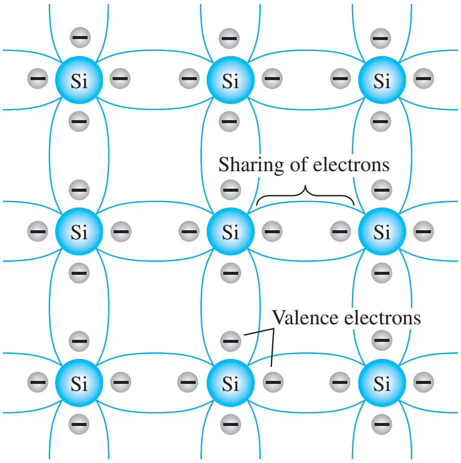


FIG. 1.4
Covalent bonding of the silicon atom.

In a pure silicon or germanium crystal the four valence electrons of one atom form a bonding arrangement with four adjoining atoms, as shown in Fig. 1.4.

This bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Because GaAs is a compound semiconductor, there is sharing between the two different atoms, as shown in Fig. 1.5. Each atom, gallium or arsenic, is surrounded by atoms of the complementary type. There is still a sharing of electrons similar in structure to that of Ge and Si, but now five electrons are provided by the As atom and three by the Ga atom.

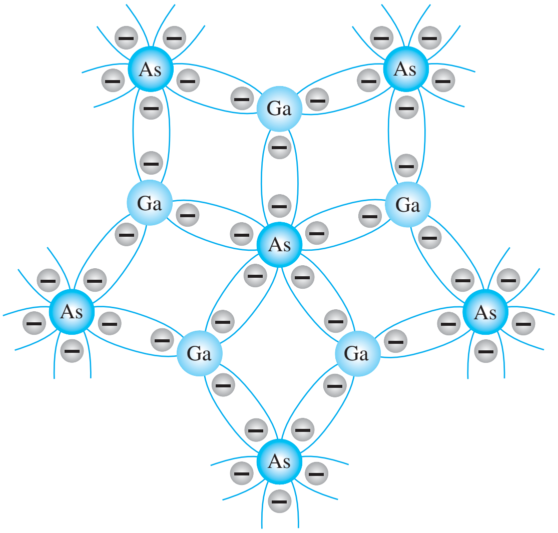


FIG. 1.5
Covalent bonding of the GaAs crystal.

Although the covalent bond will result in a stronger bond between the valence electrons and their parent atom, it is still possible for the valence electrons to absorb sufficient kinetic energy from external natural causes to break the covalent bond and assume the “free” state. The term *free* is applied to any electron that has separated from the fixed lattice structure and is very sensitive to any applied electric fields such as established by voltage sources or any difference in potential. *The external causes include effects such as light energy in the form of photons and thermal energy (heat) from the surrounding medium.* At room temperature there are approximately 1.5×10^{10} free carriers in 1 cm^3 of *intrinsic* silicon material, that is, 15,000,000,000 (15 billion) electrons in a space smaller than a small sugar cube—an enormous number.

The term* intrinsic *is applied to any semiconductor material that has been carefully refined to reduce the number of impurities to a very low level—essentially as pure as can be made available through modern technology.

The free electrons in a material due only to external causes are referred to as *intrinsic carriers.* Table 1.1 compares the number of intrinsic carriers per cubic centimeter (abbreviated n_i) for Ge, Si, and GaAs. It is interesting to note that Ge has the highest number and GaAs the lowest. In fact, Ge has more than twice the number as GaAs. The number of carriers in the intrinsic form is important, but other characteristics of the material are more significant in determining its use in the field. One such factor is the *relative mobility* (μ_n) of the free carriers in the material, that is, the ability of the free carriers to move throughout the material. Table 1.2 clearly reveals that the free carriers in GaAs have more than five times the mobility of free carriers in Si, a factor that results in response times using GaAs electronic devices that can be up to five times those of the same devices made from Si. Note also that free carriers in Ge have more than twice the mobility of electrons in Si, a factor that results in the continued use of Ge in high-speed radio frequency applications.

TABLE 1.1

Intrinsic Carriers n_i

Semiconductor	**Intrinsic Carriers (per cubic centimeter)**
GaAs	1.7×10^6
Si	1.5×10^{10}
Ge	2.5×10^{13}

TABLE 1.2

Relative Mobility Factor μ_n

Semiconductor	**μ_n (cm^2/V·s)**
Si	1500
Ge	3900
GaAs	8500

One of the most important technological advances of recent decades has been the ability to produce semiconductor materials of very high purity. Recall that this was one of the problems encountered in the early use of silicon—it was easier to produce germanium of the required purity levels. Impurity levels of 1 part in 10 billion are common today, with higher levels attainable for large-scale integrated circuits. One might ask whether these extremely high levels of purity are necessary. They certainly are if one considers that the addition of one part of impurity (of the proper type) per million in a wafer of silicon material can change that material from a relatively poor conductor to a good conductor of electricity. We obviously have to deal with a whole new level of comparison when we deal with the semiconductor medium. The ability to change the characteristics of a material through this process is called *doping*, something that germanium, silicon, and gallium arsenide readily and easily accept. The doping process is discussed in detail in Sections 1.5 and 1.6.

One important and interesting difference between semiconductors and conductors is their reaction to the application of heat. For conductors, the resistance increases with an increase in heat. This is because the numbers of carriers in a conductor do not increase significantly with temperature, but their vibration pattern about a relatively fixed location makes it increasingly difficult for a sustained flow of carriers through the material. Materials that react in this manner are said to have a *positive temperature coefficient.* Semiconductor materials, however, exhibit an increased level of conductivity with the application of heat. As the temperature rises, an increasing number of valence electrons absorb sufficient thermal energy to break the covalent bond and to contribute to the number of free carriers. Therefore:

Semiconductor materials have a negative temperature coefficient.

1.4 ENERGY LEVELS

Within the atomic structure of each and every *isolated* atom there are specific energy levels associated with each shell and orbiting electron, as shown in Fig. 1.6. The energy levels associated with each shell will be different for every element. However, in general:

The farther an electron is from the nucleus, the higher is the energy state, and any electron that has left its parent atom has a higher energy state than any electron in the atomic structure.

Note in Fig. 1.6a that only specific energy levels can exist for the electrons in the atomic structure of an isolated atom. The result is a series of gaps between allowed energy levels

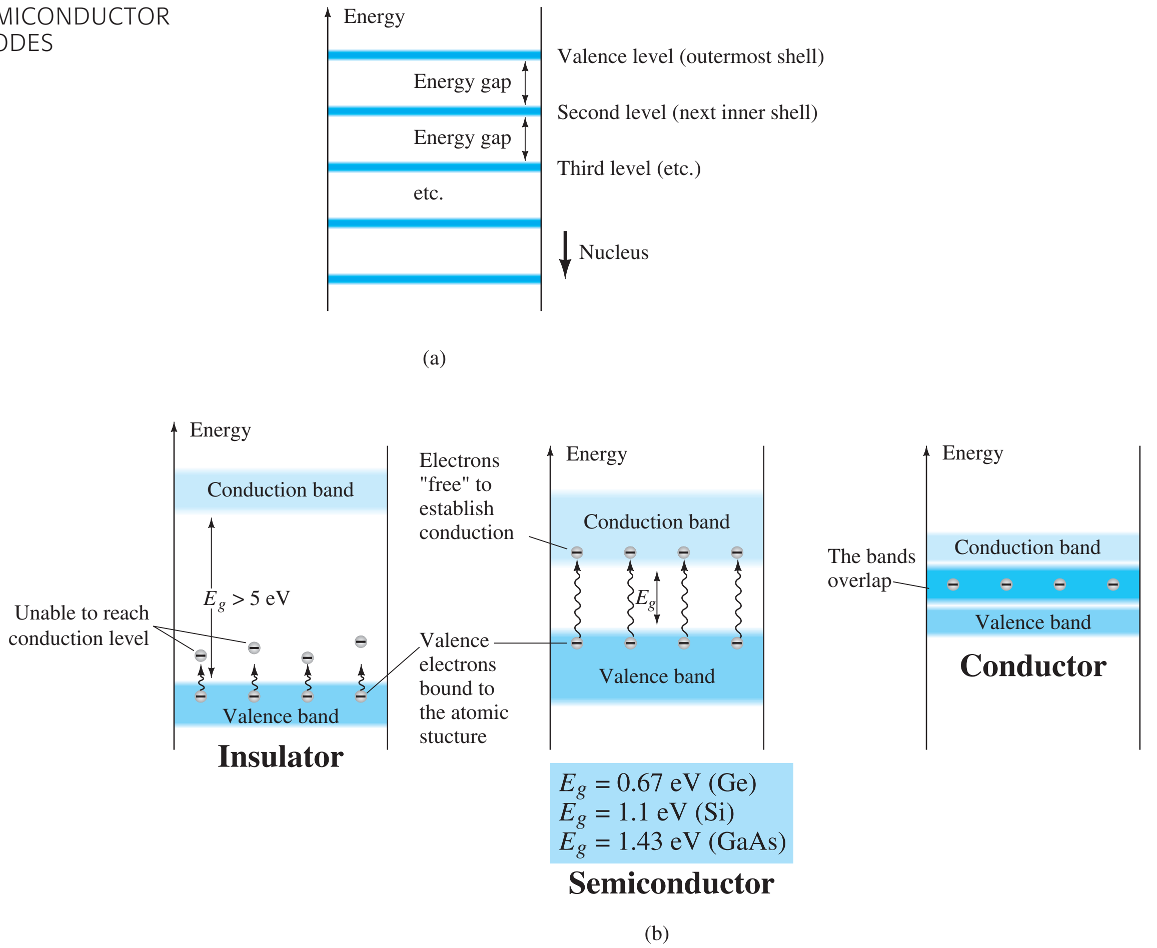

Energy
Valence level (outermost shell)
Energy gap
Second level (next inner shell)
Energy gap
Third level (etc.)
etc.
Nucleus
(a)
Energy
Conduction band
$E_g > 5$ eV
Unable to reach conduction level
Valence band
Insulator
Electrons "free" to establish conduction
Valence electrons bound to the atomic stucture
Energy
Conduction band
E_g
Valence band
E_g = 0.67 eV (Ge)
E_g = 1.1 eV (Si)
E_g = 1.43 eV (GaAs)
Semiconductor
Energy
The bands overlap
Conduction band
Valence band
Conductor
(b)

FIG. 1.6

Energy levels: (a) discrete levels in isolated atomic structures; (b) conduction and valence bands of an insulator, a semiconductor, and a conductor.

where carriers are not permitted. However, as the atoms of a material are brought closer together to form the crystal lattice structure, there is an interaction between atoms, which will result in the electrons of a particular shell of an atom having slightly different energy levels from electrons in the same orbit of an adjoining atom. The result is an expansion of the fixed, discrete energy levels of the valence electrons of Fig. 1.6a to bands as shown in Fig. 1.6b. In other words, the valence electrons in a silicon material can have varying energy levels as long as they fall within the band of Fig. 1.6b. Figure l.6b clearly reveals that there is a minimum energy level associated with electrons in the conduction band and a maximum energy level of electrons bound to the valence shell of the atom. Between the two is an energy gap that the electron in the valence band must overcome to become a free carrier. That energy gap is different for Ge, Si, and GaAs; Ge has the smallest gap and GaAs the largest gap. In total, this simply means that:

An electron in the valence band of silicon must absorb more energy than one in the valence band of germanium to become a free carrier. Similarly, an electron in the valence band of gallium arsenide must gain more energy than one in silicon or germanium to enter the conduction band.

This difference in energy gap requirements reveals the sensitivity of each type of semiconductor to changes in temperature. For instance, as the temperature of a Ge sample increases, the number of electrons that can pick up thermal energy and enter the conduction band will increase quite rapidly because the energy gap is quite small. However, the number of electrons entering the conduction band for Si or GaAs would be a great deal less. This sensitivity to changes in energy level can have positive and negative effects. The design of photodetectors sensitive to light and security systems sensitive to heat would appear to be an excellent area of application for Ge devices. However, for transistor networks, where stability is a high priority, this sensitivity to temperature or light can be a detrimental factor.

The energy gap also reveals which elements are useful in the construction of light-emitting devices such as light-emitting diodes (LEDs), which will be introduced shortly. The wider the energy gap, the greater is the possibility of energy being released in the form of visible or invisible (infrared) light waves. For conductors, the overlapping of valence and conduction bands essentially results in all the additional energy picked up by the electrons being dissipated in the form of heat. Similarly, for Ge and Si, because the energy gap is so small, most of the electrons that pick up sufficient energy to leave the valence band end up in the conduction band, and the energy is dissipated in the form of heat. However, for GaAs the gap is sufficiently large to result in significant light radiation. For LEDs (Section 1.9) the level of doping and the materials chosen determine the resulting color.

Before we leave this subject, it is important to underscore the importance of understanding the units used for a quantity. In Fig. 1.6 the units of measurement are *electron volts* (eV). The unit of measure is appropriate because W (energy) $= QV$ (as derived from the defining equation for voltage: $V = W/Q$). Substituting the charge of one electron and a potential difference of 1 V results in an energy level referred to as one *electron volt*.

That is,

$$\begin{aligned} W &= QV \\ &= (1.6 \times 10^{-19}\ \text{C})(1\ \text{V}) \\ &= 1.6 \times 10^{-19}\ \text{J} \end{aligned}$$

and

$$\boxed{1\ \text{eV} = 1.6 \times 10^{-19}\ \text{J}} \qquad \textbf{(1.1)}$$

1.5 *n*-TYPE AND *p*-TYPE MATERIALS

Because Si is the material used most frequently as the base (substrate) material in the construction of solid-state electronic devices, the discussion to follow in this and the next few sections deals solely with Si semiconductors. Because Ge, Si, and GaAs share a similar covalent bonding, the discussion can easily be extended to include the use of the other materials in the manufacturing process.

As indicated earlier, the characteristics of a semiconductor material can be altered significantly by the addition of specific impurity atoms to the relatively pure semiconductor material. These impurities, although only added at 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material.

A semiconductor material that has been subjected to the doping process is called an extrinsic material.

There are two extrinsic materials of immeasureable importance to semiconductor device fabrication: *n*-type and *p*-type materials. Each is described in some detail in the following subsections.

n-Type Material

Both *n*-type and *p*-type materials are formed by adding a predetermined number of impurity atoms to a silicon base. An *n*-type material is created by introducing impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony*, *arsenic*, and *phosphorus*. Each is a member of a subset group of elements in the Periodic Table of Elements referred to as Group V because each has five valence electrons. The effect of such impurity elements is indicated in Fig. 1.7 (using antimony as the impurity in a silicon base). Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n*-type material. Since the inserted impurity atom has donated a relatively "free" electron to the structure:

Diffused impurities with five valence electrons are called donor atoms.

It is important to realize that even though a large number of free carriers have been established in the *n*-type material, it is still electrically *neutral* since ideally the number of positively charged protons in the nuclei is still equal to the number of free and orbiting negatively charged electrons in the structure.

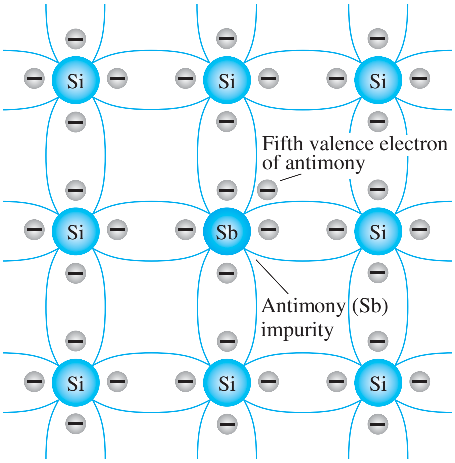


FIG. 1.7
Antimony impurity in n-type material.

The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.8. Note that a discrete energy level (called the *donor level*) appears in the forbidden band with an E_g significantly less than that of the intrinsic material. Those free electrons due to the added impurity sit at this energy level and have less difficulty absorbing a sufficient measure of thermal energy to move into the conduction band at room temperature. The result is that at room temperature, there are a large number of carriers (electrons) in the conduction level, and the conductivity of the material increases significantly. At room temperature in an intrinsic Si material there is about one free electron for every 10^{12} atoms. If the dosage level is 1 in 10 million (10^7), the ratio $10^{12}/10^7 = 10^5$ indicates that the carrier concentration has increased by a ratio of 100,000:1.

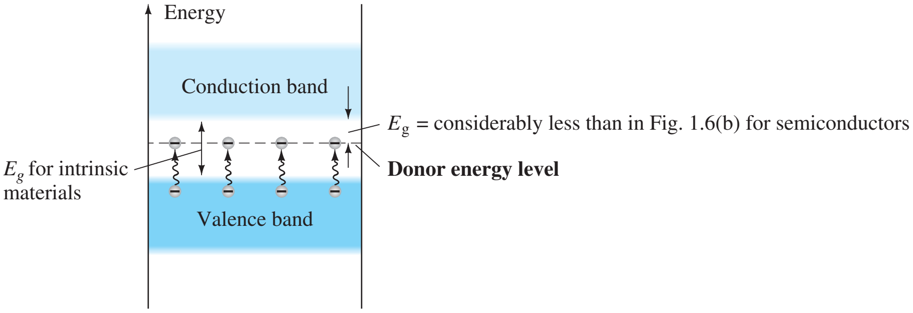

Energy
Conduction band
E_g = considerably less than in Fig. 1.6(b) for semiconductors
E_g for intrinsic materials
Donor energy level
Valence band

FIG. 1.8
Effect of donor impurities on the energy band structure.

p-Type Material

The *p*-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron*, *gallium*, and *indium*. Each is a member of a subset group of elements in the Periodic Table of Elements referred to as Group III because each has three valence electrons. The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.9.

Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or a plus sign, indicating the absence of a negative charge. Since the resulting vacancy will readily *accept* a free electron:

The diffused impurities with three valence electrons are called acceptor atoms.

The resulting *p*-type material is electrically neutral, for the same reasons described for the *n*-type material.

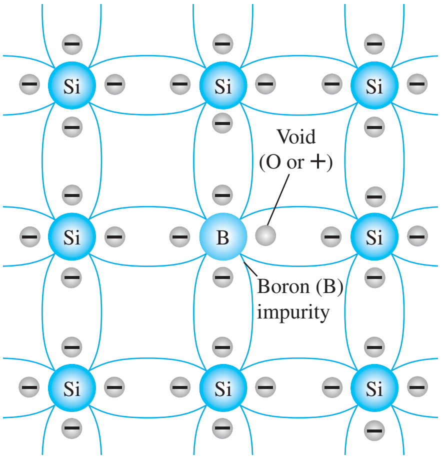


FIG. 1.9
Boron impurity in p-type material.

Electron versus Hole Flow

The effect of the hole on conduction is shown in Fig. 1.10. If a valence electron acquires sufficient kinetic energy to break its covalent bond and fills the void created by a hole, then a vacancy, or hole, will be created in the covalent bond that released the electron. There is, therefore, a transfer of holes to the left and electrons to the right, as shown in Fig. 1.10. The direction to be used in this text is that of *conventional flow*, which is indicated by the direction of hole flow.

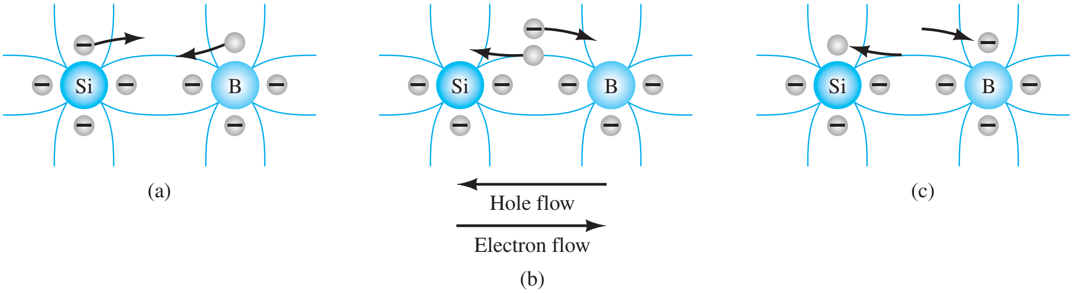


FIG. 1.10
Electron versus hole flow.

Majority and Minority Carriers

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence band that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes has not changed significantly from this intrinsic level. The net result, therefore, is that the number of electrons far outweighs the number of holes. For this reason:

In an n-type material (Fig. 1.11a) the electron is called the majority carrier and the hole the minority carrier.

For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Fig. 1.11b. Therefore:

In a p-type material the hole is the majority carrier and the electron is the minority carrier.

When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a net positive charge: hence the plus sign in the donor-ion representation. For similar reasons, the minus sign appears in the acceptor ion.

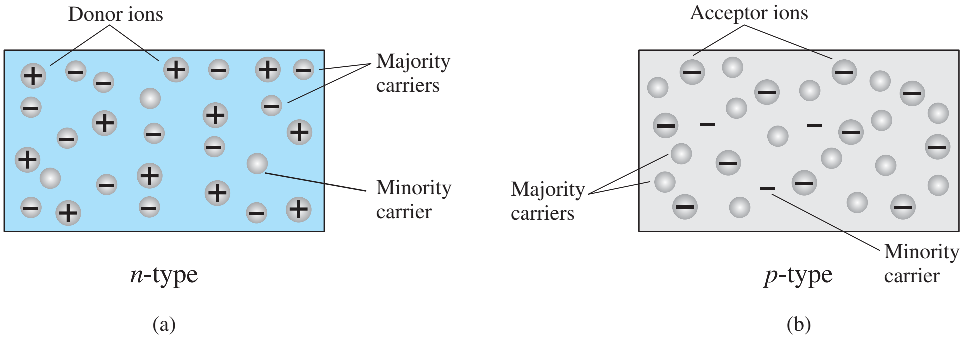


FIG. 1.11
(a) n-type material; (b) p-type material.

The *n*- and *p*-type materials represent the basic building blocks of semiconductor devices. We will find in the next section that the "joining" of a single *n*-type material with a *p*-type material will result in a semiconductor element of considerable importance in electronic systems.

1.6 SEMICONDUCTOR DIODE

Now that both *n*- and *p*-type materials are available, we can construct our first solid-state electronic device: The *semiconductor diode*, with applications too numerous to mention, is created by simply joining an *n*-type and a *p*-type material together, nothing more, just the joining of one material with a majority carrier of electrons to one with a majority carrier of holes. The basic simplicity of its construction simply reinforces the importance of the development of this solid-state era.

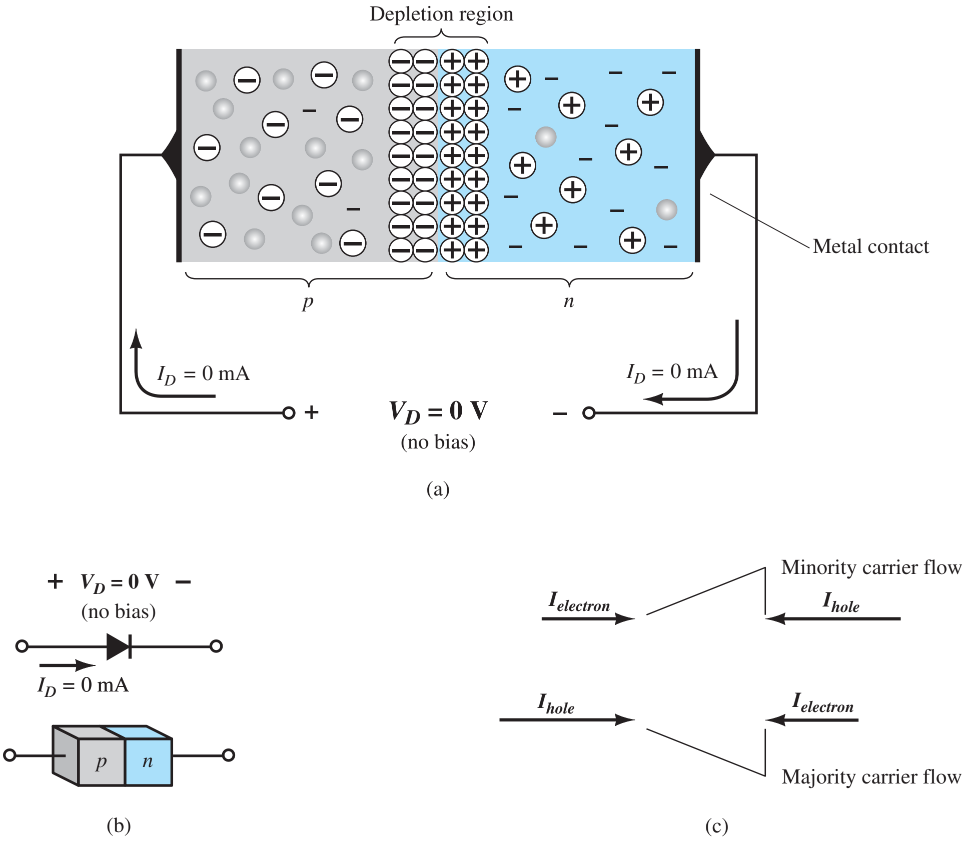
No Applied Bias ($V = 0$ V)

At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Fig. 1.12a. Note in Fig. 1.12a that the only particles displayed in this region are the positive and the negative ions remaining once the free carriers have been absorbed.

This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.

If leads are connected to the ends of each material, a *two-terminal device* results, as shown in Figs. 1.12a and 1.12b. Three options then become available: *no bias*, *forward bias*, and *reverse bias*. The term *bias* refers to the application of an external voltage across the two terminals of the device to extract a response. The condition shown in Figs. 1.12a and 1.12b is the no-bias situation because there is no external voltage applied. It is simply a diode with two leads sitting isolated on a laboratory bench. In Fig. 1.12b the symbol for a semiconductor diode is provided to show its correspondence with the *p–n* junction. In each figure it is clear that the applied voltage is 0 V (no bias) and the resulting current is 0 A, much like an isolated resistor. The absence of a voltage across a resistor results in zero current through it. Even at this early point in the discussion it is important to note the polarity of the voltage across the diode in Fig. 1.12b and the direction given to the current. Those polarities will be recognized as the *defined polarities* for the semiconductor diode. If a voltage applied across the diode has the same polarity across the diode as in Fig. 1.12b, it will be considered a positive voltage. If the reverse, it is a negative voltage. The same standards can be applied to the defined direction of current in Fig. 1.12b.

Under no-bias conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region for any reason whatsoever will pass quickly into the *p*-type material. The closer the minority carrier is to the junction, the greater is the attraction for the layer of negative ions and the less is the opposition offered by the positive ions in the depletion region of the *n*-type material. We will conclude, therefore, for future discussions, that any minority carriers of the *n*-type material that find themselves in the depletion region will pass directly into the *p*-type material. This carrier flow is indicated at the top of Fig. 1.12c for the minority carriers of each material.



(a)

(b)

(c)

FIG. 1.12

A p–n junction with no external bias: (a) an internal distribution of charge; (b) a diode symbol, with the defined polarity and the current direction; (c) demonstration that the net carrier flow is zero at the external terminal of the device when $V_D = 0$ V.

The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the *p*-type material. The resulting flow due to the majority carriers is shown at the bottom of Fig. 1.12c.

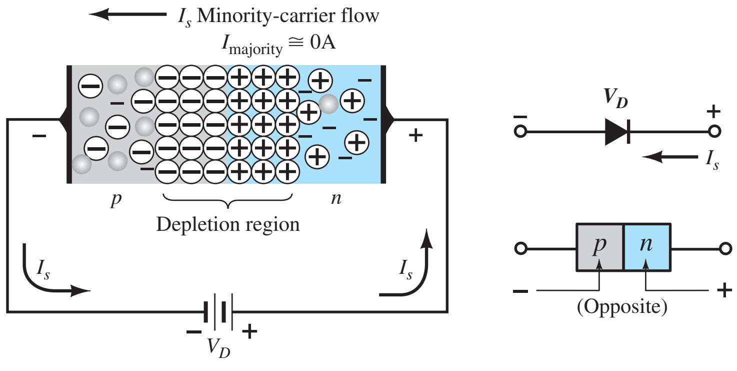
A close examination of Fig. 1.12c will reveal that the relative magnitudes of the flow vectors are such that the net flow in either direction is zero. This cancellation of vectors for each type of carrier flow is indicated by the crossed lines. The length of the vector representing hole flow is drawn longer than that of electron flow to demonstrate that the two magnitudes need not be the same for cancellation and that the doping levels for each material may result in an unequal carrier flow of holes and electrons. In summary, therefore:

In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.

In other words, the current under no-bias conditions is zero, as shown in Figs. 1.12a and 1.12b.

Reverse-Bias Condition ($V_D < 0$ V)

If an external potential of *V* volts is applied across the *p–n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig. 1.13, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a



(a) (b)

FIG. 1.13

Reverse-biased p–n junction: (a) internal distribution of charge under reverse-bias conditions; (b) reverse-bias polarity and direction of reverse saturation current.

widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero, as shown in Fig. 1.13a.

The number of minority carriers, however, entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 1.12c with no applied voltage.

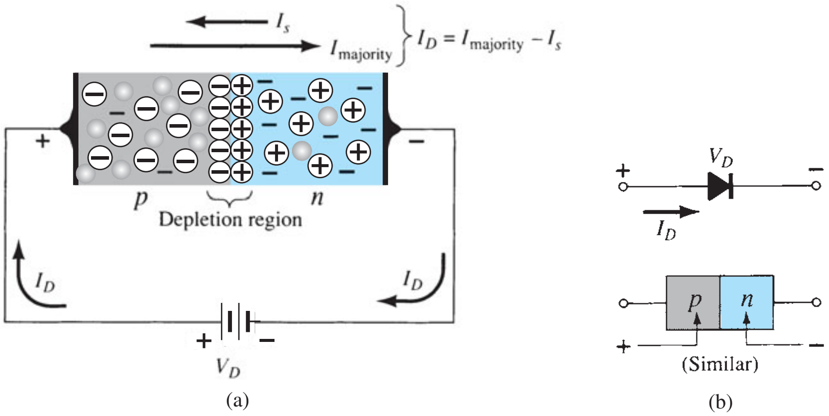
The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s.

The reverse saturation current is seldom more than a few microamperes and typically in nA, except for high-power devices. The term *saturation* comes from the fact that it reaches its maximum level quickly and does not change significantly with increases in the reverse-bias potential, as shown on the diode characteristics of Fig. 1.15 for $V_D < 0$ V. The reverse-biased conditions are depicted in Fig. 1.13b for the diode symbol and *p–n* junction. Note, in particular, that the direction of I_s is against the arrow of the symbol. Note also that the negative side of the applied voltage is connected to the *p*-type material and the positive side to the *n*-type material, the difference in underlined letters for each region revealing a reverse-bias condition.

Forward-Bias Condition ($V_D > 0$ V)

A *forward-bias* or "on" condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig. 1.14.

The application of a forward-bias potential V_D will "pressure" electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.14a. The resulting minority-carrier flow



(a) (b)

FIG. 1.14

Forward-biased p–n junction: (a) internal distribution of charge under forward-bias conditions; (b) forward-bias polarity and direction of resulting current.

of electrons from the *p*-type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the *n*-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. 1.15. Note that the vertical scale of Fig. 1.15 is measured in milliamperes (although some semiconductor diodes have a vertical scale measured in amperes), and the horizontal scale in the forward-bias region has a maximum of 1 V. Typically, therefore, the voltage across a forward-biased diode will be less than 1 V. Note also how quickly the current rises beyond the knee of the curve.

It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley's equation, for the forward- and reverse-bias regions:

$$\boxed{I_D = I_s(e^{V_D/nV_T} - 1)} \quad \text{(A)} \qquad \textbf{(1.2)}$$

where I_s is the reverse saturation current
V_D is the applied forward-bias voltage across the diode
n is an ideality factor, which is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending on a wide variety of factors ($n = 1$ will be assumed throughout this text unless otherwise noted).

The voltage V_T in Eq. (1.1) is called the *thermal voltage* and is determined by

$$\boxed{V_T = \frac{kT_K}{q}} \quad \text{(V)} \qquad \textbf{(1.3)}$$

where k is Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
T_K is the absolute temperature in kelvins $= 273 +$ the temperature in °C
q is the magnitude of electronic charge $= 1.6 \times 10^{-19}$ C

EXAMPLE 1.1 At a temperature of 27°C (common temperature for components in an enclosed operating system), determine the thermal voltage V_T.

Solution: Substituting into Eq. (1.3), we obtain

$$T = 273 + {}^\circ\text{C} = 273 + 27 = 300\ \text{K}$$

$$V_T = \frac{kT_K}{q} = \frac{(1.38 \times 10^{-23}\ \text{J/K})(30\ \text{K})}{1.6 \times 10^{-19}\ \text{C}}$$

$$= 25.875\ \text{mV} \cong 26\ \text{mV}$$

The thermal voltage will become an important parameter in the analysis to follow in this chapter and a number of those to follow.

Initially, Eq. (1.2) with all its defined quantities may appear somewhat complex. However, it will not be used extensively in the analysis to follow. It is simply important at this point to understand the source of the diode characteristics and which factors affect its shape.

A plot of Eq. (1.2) with $I_s = 10$ pA is provided in Fig. 1.15 as the dashed line. If we expand Eq. (1.2) into the following form, the contributing component for each region of Fig. 1.15 can be described with increased clarity:

$$I_D = I_s e^{V_D/nV_T} - I_s$$

For positive values of V_D the first term of the above equation will grow very quickly and totally overpower the effect of the second term. The result is the following equation, which only has positive values and takes on the exponential format e^x appearing in Fig. 1.16:

$$I_D \cong I_s e^{V_D/nV_T} \qquad (V_D \text{ positive})$$

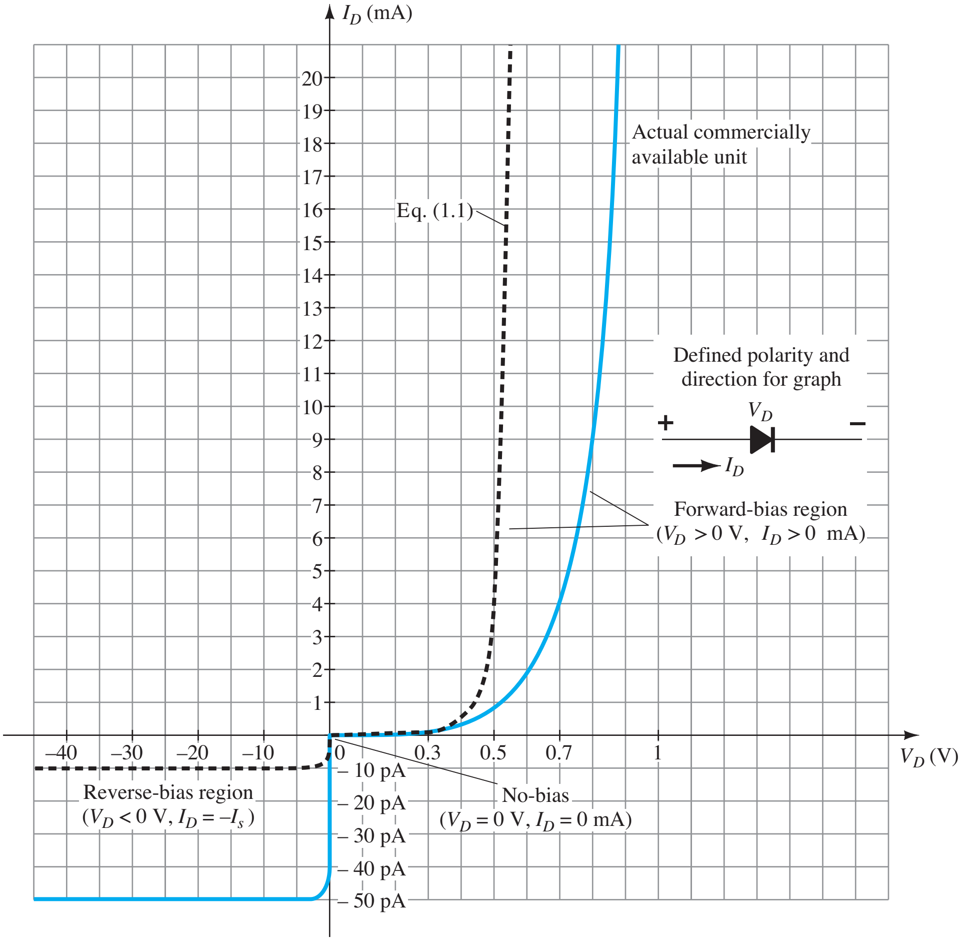


FIG. 1.15

Silicon semiconductor diode characteristics.

The exponential curve of Fig. 1.16 increases very rapidly with increasing values of x. At $x = 0$, $e^0 = 1$, whereas at $x = 5$, it jumps to greater than 148. If we continued to $x = 10$, the curve jumps to greater than 22,000. Clearly, therefore, as the value of x increases, the curve becomes almost vertical, an important conclusion to keep in mind when we examine the change in current with increasing values of applied voltage.

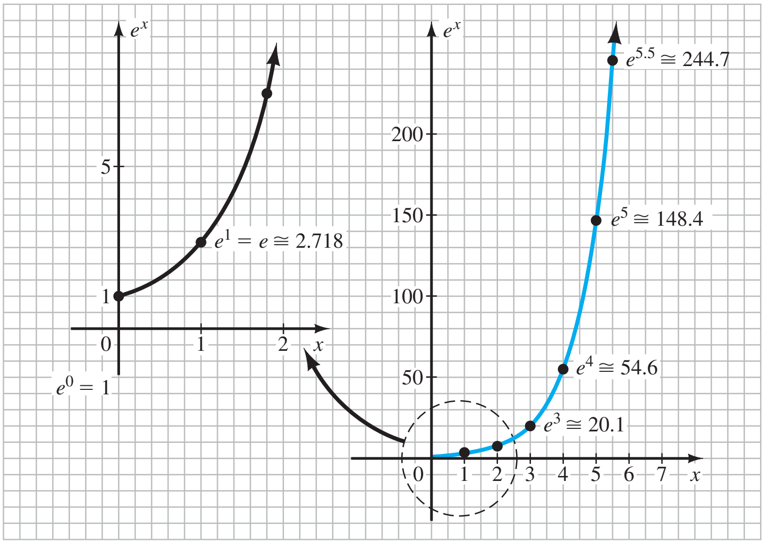


FIG. 1.16

Plot of e^x.

For negative values of V_D the exponential term drops very quickly below the level of I, and the resulting equation for I_D is simply

$$I_D \cong -I_s \qquad (V_D \text{ negative})$$

Note in Fig. 1.15 that for negative values of V_D the current is essentially horizontal at the level of $-I_s$.

At $V = 0$ V, Eq. (1.2) becomes

$$I_D = I_s(e^0 - 1) = I_s(1 - 1) = 0 \text{ mA}$$

as confirmed by Fig. 1.15.

The sharp change in direction of the curve at $V_D = 0$ V is simply due to the change in current scales from above the axis to below the axis. Note that above the axis the scale is in milliamperes (mA), whereas below the axis it is in picoamperes (pA).

Theoretically, with all things perfect, the characteristics of a silicon diode should appear as shown by the dashed line of Fig. 1.15. However, commercially available silicon diodes deviate from the ideal for a variety of reasons including the internal "body" resistance and the external "contact" resistance of a diode. Each contributes to an additional voltage at the same current level, as determined by Ohm's law, causing the shift to the right witnessed in Fig. 1.15.

The change in current scales between the upper and lower regions of the graph was noted earlier. For the voltage V_D there is also a measurable change in scale between the right-hand region of the graph and the left-hand region. For positive values of V_D the scale is in tenths of volts, and for the negative region it is in tens of volts.

It is important to note in Fig. 1.14b how:

The defined direction of conventional current for the positive voltage region matches the arrowhead in the diode symbol.

This will always be the case for a forward-biased diode. It may also help to note that the forward-bias condition is established when the bar representing the negative side of the applied voltage matches the side of the symbol with the vertical bar.

Going back a step further by looking at Fig. 1.14b, we find a forward-bias condition is established across a *p–n* junction when the positive side of the applied voltage is applied to the *p*-type material (noting the correspondence in the letter *p*) and the negative side of the applied voltage is applied to the *n*-type material (noting the same correspondence).

It is particularly interesting to note that the reverse saturation current of the commercial unit is significantly larger than that of I_s in Shockley's equation. In fact,

The actual reverse saturation current of a commercially available diode will normally be measurably larger than that appearing as the reverse saturation current in Shockley's equation.

This increase in level is due to a wide range of factors that include

- **leakage currents**
- **generation of carriers in the depletion region**
- **higher doping levels** that result in increased levels of reverse current
- **sensitivity to the intrinsic level of carriers** in the component materials by a squared factor—double the intrinsic level, and the contribution to the reverse current could increase by a factor of four.
- **a direct relationship with the junction area**—double the area of the junction, and the contribution to the reverse current could double. High-power devices that have larger junction areas typically have much higher levels of reverse current.
- **temperature sensitivity**—for every 5°C increase in current, the level of reverse saturation current in Eq. 1.2 will double, whereas a 10°C increase in current will result in doubling of the actual reverse current of a diode.

Note in the above the use of the terms reverse saturation current and reverse current. The former is simply due to the physics of the situation, whereas the latter includes all the other possible effects that can increase the level of current.

We will find in the discussions to follow that the ideal situation is for I_s to be 0 A in the reverse-bias region. The fact that it is typically in the range of 0.01 pA to 10 pA today as compared to 0.1 μA to 1 μA a few decades ago is a credit to the manufacturing industry. Comparing the common value of 1 nA to the 1-μA level of years past shows an improvement factor of 100,000.

Breakdown Region

Even though the scale of Fig. 1.15 is in tens of volts in the negative region, there is a point where the application of too negative a voltage with the reverse polarity will result in a sharp change in the characteristics, as shown in Fig. 1.17. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *breakdown potential* and is given the label V_{BV}.

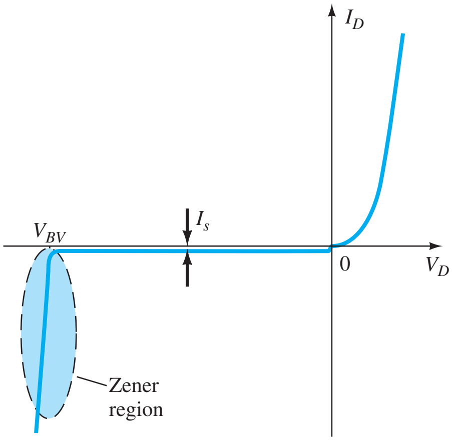


FIG. 1.17
Breakdown region.

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_s will also increase. Eventually, their velocity and associated kinetic energy ($W_K = \frac{1}{2}mv^2$) will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an *ionization* process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined.

The avalanche region (V_{BV}) can be brought closer to the vertical axis by increasing the doping levels in the *p*- and *n*-type materials. However, as V_{BV} decreases to very low levels, such as -5 V, another mechanism, called *Zener breakdown*, will contribute to the sharp change in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and “generate” carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of V_{BV}, this sharp change in the characteristic at any level is called the *Zener region*, and diodes employing this unique portion of the characteristic of a *p–n* junction are called *Zener diodes*. They are described in detail in Section 1.15.

The breakdown region of the semiconductor diode described must be avoided if the response of a system is not to be completely altered by the sharp change in characteristics in this reverse-voltage region.

The maximum reverse-bias potential that can be applied before entering the breakdown region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted the PRV rating).

If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.

In general, the breakdown voltage of GaAs diodes is about 10% higher those for silicon diodes but after 200% higher than levels for Ge diodes.

Ge, Si, and GaAs

The discussion thus far has solely used Si as the base semiconductor material. It is now important to compare it to the other two materials of importance: GaAs and Ge. A plot comparing the characteristics of Si, GaAs, and Ge diodes is provided in Fig. 1.18. The curves are not

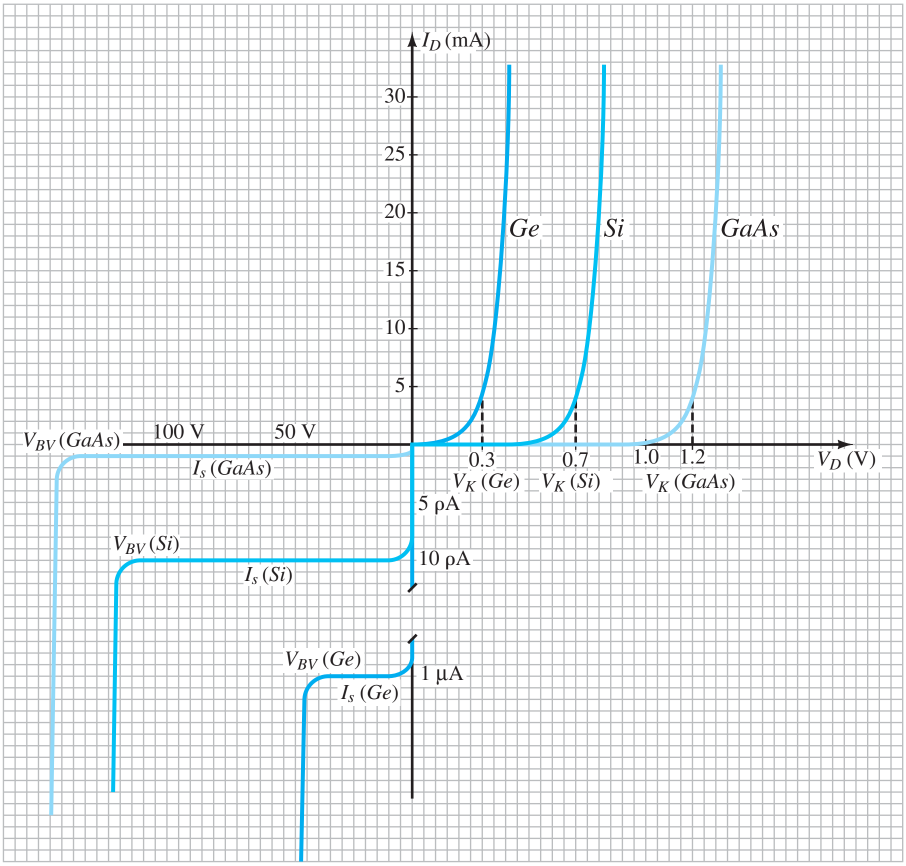


FIG. 1.18

Comparison of Ge, Si, and GaAs commercial diodes.

simply plots of Eq. 1.2 but the actual response of commercially available units. The total reverse current is shown and not simply the reverse saturation current. It is immediately obvious that the point of vertical rise in the characteristics is different for each material, although the general shape of each characteristic is quite similar. Germanium is closest to the vertical axis and GaAs is the most distant. As noted on the curves, the center of the knee (hence the *K* is the notation V_K) of the curve is about 0.3 V for Ge, 0.7 V for Si, and 1.2 V for GaAs (see Table 1.3).

The shape of the curve in the reverse-bias region is also quite similar for each material, but notice the measurable difference in the magnitudes of the typical reverse saturation currents. For GaAs, the reverse saturation current is typically about 1 pA, compared to 10 pA for Si and 1 μA for Ge, a significant difference in levels.

Also note the relative magnitudes of the reverse breakdown voltages for each material. GaAs typically has maximum breakdown levels that exceed those of Si devices of the same power level by about 10%, with both having breakdown voltages that typically extend between 50 V and 1 kV. There are Si power diodes with breakdown voltages as high as 20 kV. Germanium typically has breakdown voltages of less than 100 V, with maximums around 400 V. The curves of Fig. 1.18 are simply designed to reflect relative breakdown voltages for the three materials. When one considers the levels of reverse saturation currents and breakdown voltages, Ge certainly sticks out as having the least desirable characteristics.

A factor not appearing in Fig. 1.18 is the operating speed for each material—an important factor in today's market. For each material, the electron mobility factor is provided in Table 1.4. It provides an indication of how fast the carriers can progress through the material and therefore the operating speed of any device made using the materials. Quite obviously, GaAs stands out, with a mobility factor more than five times that of silicon and twice that of germanium. The result is that GaAs and Ge are often used in high-speed applications. However, through proper design, careful control of doping levels, and so on, silicon is also found in systems operating in the gigahertz range. Research today is also looking at compounds in groups III–V that have even higher mobility factors to ensure that industry can meet the demands of future high-speed requirements.

TABLE 1.3

Knee Voltages V_K

Semiconductor	V_K(V)
Ge	0.3
Si	0.7
GaAs	1.2

TABLE 1.4

Electron Mobility μ_n

Semiconductor	μ_n(cm^2/V·s)
Ge	3900
Si	1500
GaAs	8500

EXAMPLE 1.2 Using the curves of Fig 1.18:

a. Determine the voltage across each diode at a current of 1 mA.
b. Repeat for a current of 4 mA.
c. Repeat for a current of 30 mA.
d. Determine the average value of the diode voltage for the range of currents listed above.
e. How do the average values compare to the knee voltages listed in Table 1.3?

Solution:

a. $V_D(\text{Ge}) = 0.2\text{ V}$, $V_D(\text{Si}) = 0.6\text{ V}$, $V_D\ (\text{GaAs}) = 1.1\text{ V}$
b. $V_D(\text{Ge}) = 0.3\text{ V}$, $V_D(\text{Si}) = 0.7\text{ V}$, $V_D\ (\text{GaAs}) = 1.2\text{ V}$
c. $V_D(\text{Ge}) = 0.42\text{ V}$, $V_D(\text{Si}) = 0.82\text{ V}$, $V_D\ (\text{GaAs}) = 1.33\text{ V}$
d. Ge: $V_{\text{av}} = (0.2\text{ V} + 0.3\text{ V} + 0.42\text{ V})/3 = 0.307\text{ V}$
Si: $V_{\text{av}} = (0.6\text{ V} + 0.7\text{ V} + 0.82\text{ V})/3 = 0.707\text{ V}$
GaAs: $V_{\text{av}} = (1.1\text{ V} + 1.2\text{ V} + 1.33\text{ V})/3 = 1.21\text{ V}$
e. Very close correspondence. Ge: 0.307 V vs. 0.3, V, Si: 0.707 V vs. 0.7 V, GaAs: 1.21 V vs. 1.2 V.

Temperature Effects

Temperature can have a marked effect on the characteristics of a semiconductor diode, as demonstrated by the characteristics of a silicon diode shown in Fig. 1.19:

In the forward-bias region the characteristics of a silicon diode shift to the left at a rate of 2.5 mV per centigrade degree increase in temperature.

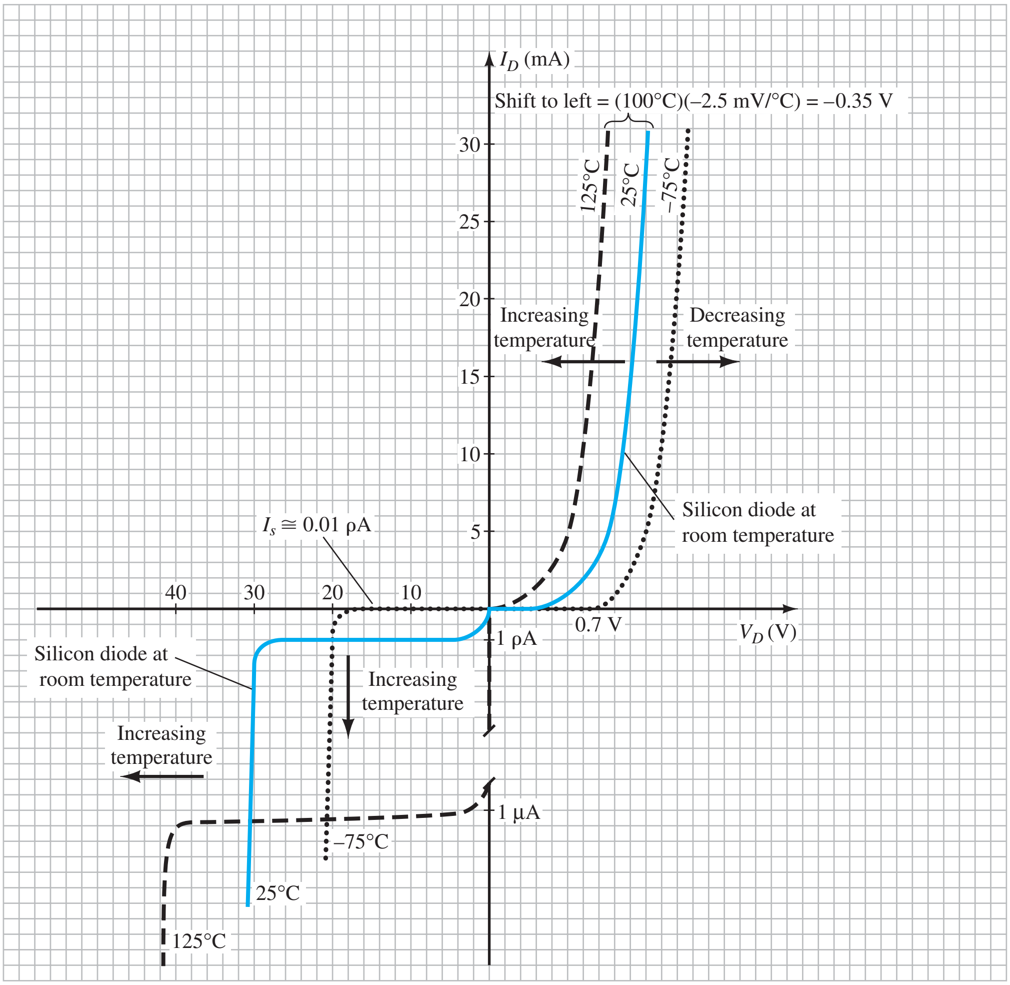


FIG. 1.19
Variation in Si diode characteristics with temperature change.

An increase from room temperature (20°C) to 100°C (the boiling point of water) results in a drop of $80(2.5 \text{ mV}) = 200 \text{ mV}$, or 0.2 V, which is significant on a graph scaled in tenths of volts. A decrease in temperature has the reverse effect, as also shown in the figure:

In the reverse-bias region the reverse current of a silicon diode doubles for every 10°C rise in temperature.

For a change from 20°C to 100°C, the level of I_s increases from 10 nA to a value of 2.56 μA, which is a significant, 256-fold increase. Continuing to 200°C would result in a monstrous reverse saturation current of 2.62 mA. For high-temperature applications one would therefore look for Si diodes with room-temperature I_s closer to 10 pA, a level commonly available today, which would limit the current to 2.62 μA. It is indeed fortunate that both Si and GaAs have relatively small reverse saturation currents at room temperature. GaAs devices are available that work very well in the −200°C to +200°C temperature range, with some having maximum temperatures approaching 400°C. Consider, for a moment, how huge the reverse saturation current would be if we started with a Ge diode with a saturation current of 1 μA and applied the same doubling factor.

Finally, it is important to note from Fig. 1.19 that:

The reverse breakdown voltage of a semiconductor diode will increase or decrease with temperature.

However, if the initial breakdown voltage is less than 5 V, the breakdown voltage may actually decrease with temperature. The sensitivity of the breakdown potential to changes of temperature will be examined in more detail in Section 1.15.

Summary

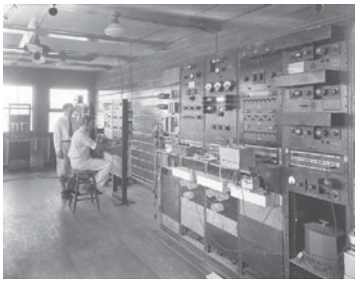
A great deal has been introduced in the foregoing paragraphs about the construction of a semiconductor diode and the materials employed. The characteristics have now been presented and the important differences between the response of the materials discussed. It is now time to compare the *p–n* junction response to the desired response and reveal the primary functions of a semiconductor diode.

Table 1.5 provides a synopsis of material regarding the three most frequently used semiconductor materials. Figure 1.20 includes a short biography of the first research scientist to discover the *p–n* junction in a semiconductor material.

TABLE 1.5

The Current Commercial Use of Ge, Si, and GaAs

Ge:	Germanium is in limited production due to its temperature sensitivity and high reverse saturation current. It is still commercially available but is limited to some high-speed applications (due to a relatively high mobility factor) and applications that use its sensitivity to light and heat such as photodetectors and security systems.
Si:	Without question the semiconductor used most frequently for the full range of electronic devices. It has the advantage of being readily available at low cost and has relatively low reverse saturation currents, good temperature characteristics, and excellent breakdown voltage levels. It also benefits from decades of enormous attention to the design of large-scale integrated circuits and processing technology.
GaAs:	Since the early 1990s the interest in GaAs has grown in leaps and bounds, and it will eventually take a good share of the development from silicon devices, especially in very large scale integrated circuits. Its high-speed characteristics are in more demand every day, with the added features of low reverse saturation currents, excellent temperature sensitivities, and high breakdown voltages. More than 80% of its applications are in optoelectronics with the development of light-emitting diodes, solar cells, and other photodetector devices, but that will probably change dramatically as its manufacturing costs drop and its use in integrated circuit design continues to grow; perhaps the semiconductor material of the future.



Russell Ohl (1898–1987)

American (Allentown, PA; Holmdel, NJ; Vista, CA) Army Signal Corps, University of Colorado, Westinghouse, AT&T, Bell Labs Fellow, Institute of Radio Engineers—1955 (Courtesy of AT&T Archives History Center.)

Although vacuum tubes were used in all forms of communication in the 1930s, Russell Ohl was determined to demonstrate that the future of the field was defined by semiconductor crystals. Germanium was not immediately available for his research, so he turned to silicon, and found a way to raise its level of purity to 99.8%, for which he received a patent. The actual discovery of the *p–n* junction, as often happens in scientific research, was the result of a set of circumstances that were not planned. On February 23, 1940, Ohl found that a silicon crystal with a crack down the middle would produce a significant rise in current when placed near a source of light. This discovery led to further research, which revealed that the purity levels on each side of the crack were different and that a barrier was formed at the junction that allowed the passage of current in only one direction—the first solid-state diode had been identified and explained. In addition, this sensitivity to light was the beginning of the development of solar cells. The results were quite instrumental in the development of the transistor in 1945 by three individuals also working at Bell Labs.

FIG. 1.20

1.7 IDEAL VERSUS PRACTICAL

In the previous section we found that a *p–n* junction will permit a generous flow of charge when forward-biased and a very small level of current when reverse-biased. Both conditions are reviewed in Fig. 1.21, with the heavy current vector in Fig. 1.21a matching the direction of the arrow in the diode symbol and the significantly smaller vector in the opposite direction in Fig. 1.21b representing the reverse saturation current.

An analogy often used to describe the behavior of a semiconductor diode is a mechanical switch. In Fig. 1.21a the diode is acting like a closed switch permitting a generous flow of charge in the direction indicated. In Fig. 1.21b the level of current is so small in most cases that it can be approximated as 0 A and represented by an open switch.

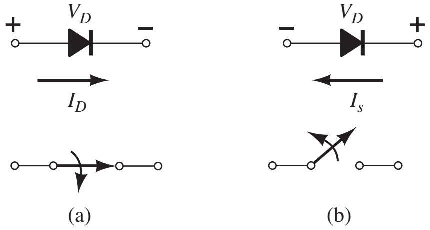


FIG. 1.21
Ideal semiconductor diode: (a) forward-biased; (b) reverse-biased.

In other words:

The semiconductor diode behaves in a manner similar to a mechanical switch in that it can control whether current will flow between its two terminals.

However, it is important to also be aware that:

The semiconductor diode is different from a mechanical switch in the sense that when the switch is closed it will only permit current to flow in one direction.

Ideally, if the semiconductor diode is to behave like a closed switch in the forward-bias region, the resistance of the diode should be 0 Ω. In the reverse-bias region its resistance should be ∞Ω to represent the open-circuit equivalent. Such levels of resistance in the forward- and reverse-bias regions result in the characteristics of Fig. 1.22.

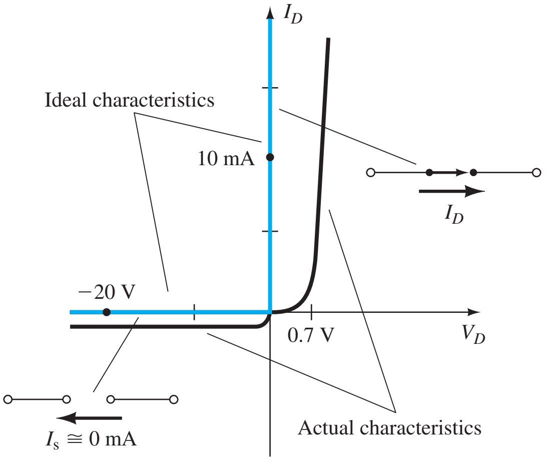


FIG. 1.22
Ideal versus actual semiconductor characteristics.

The characteristics have been superimposed to compare the ideal Si diode to a real-world Si diode. First impressions might suggest that the commercial unit is a poor impression of the ideal switch. However, when one considers that the only major difference is that the commercial diode rises at a level of 0.7 V rather than 0 V, there are a number of similarities between the two plots.

When a switch is closed the resistance between the contacts is assumed to be 0 Ω. At the plot point chosen on the vertical axis the diode current is 5 mA and the voltage across the diode is 0 V. Substituting into Ohm's law results in

$$R_F = \frac{V_D}{I_D} = \frac{0\text{ V}}{5\text{ mA}} = \mathbf{0\ \Omega} \qquad \text{(short-circuit equivalent)}$$

In fact:

At any current level on the vertical line, the voltage across the ideal diode is 0 V and the resistance is 0 Ω.

For the horizontal section, if we again apply Ohm's law, we find

$$R_R = \frac{V_D}{I_D} = \frac{20\text{ V}}{0\text{ mA}} \cong \infty\,\Omega \qquad \text{(open-circuit equivalent)}$$

Again:

Because the current is 0 mA anywhere on the horizontal line, the resistance is considered to be infinite ohms (an open-circuit) at any point on the axis.

Due to the shape and the location of the curve for the commercial unit in the forward-bias region there will be a resistance associated with the diode that is greater than 0 Ω. However, if that resistance is small enough compared to other resistors of the network in series with the diode, it is often a good approximation to simply assume the resistance of the commercial unit is 0 Ω. In the reverse-bias region, if we assume the reverse saturation current is so small it can be approximated as 0 mA, we have the same open-circuit equivalence provided by the open switch.

The result, therefore, is that there are sufficient similarities between the ideal switch and the semiconductor diode to make it an effective electronic device. In the next section the various resistance levels of importance are determined for use in the next chapter, where the response of diodes in an actual network is examined.

1.8 RESISTANCE LEVELS

As the operating point of a diode moves from one region to another the resistance of the diode will also change due to the nonlinear shape of the characteristic curve. It will be demonstrated in the next few paragraphs that the type of applied voltage or signal will define the resistance level of interest. Three different levels will be introduced in this section, which will appear again as we examine other devices. It is therefore paramount that their determination be clearly understood.

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.23 and applying the following equation:

$$\boxed{R_D = \frac{V_D}{I_D}} \qquad \textbf{(1.4)}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few milliamperes).

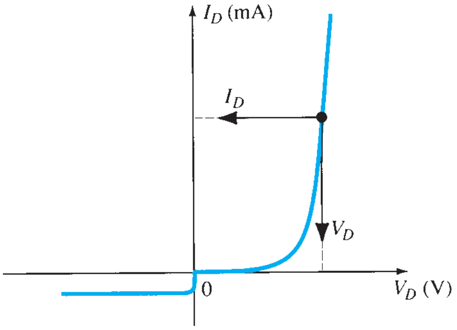


FIG. 1.23

Determining the dc resistance of a diode at a particular operating point.

In general, therefore, the higher the current through a diode, the lower is the dc resistance level.

Typically, the dc resistance of a diode in the active (most utilized) will range from about 10 Ω to 80 Ω.

EXAMPLE 1.3 Determine the dc resistance levels for the diode of Fig. 1.24 at

a. $I_D = 2$ mA (low level)
b. $I_D = 20$ mA (high level)
c. $V_D = -10$ V (reverse-biased)

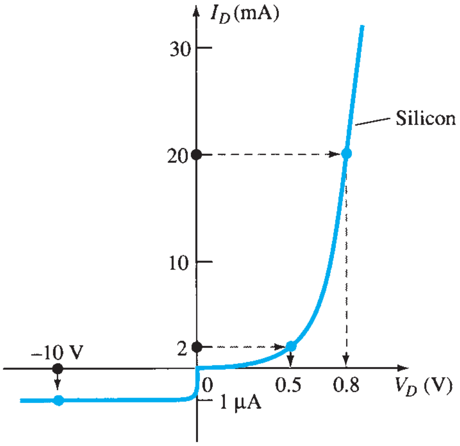


FIG. 1.24

Example 1.3.

Solution:

a. At $I_D = 2$ mA, $V_D = 0.5$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5\text{ V}}{2\text{ mA}} = \mathbf{250\ \Omega}$$

b. At $I_D = 20$ mA, $V_D = 0.8$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.8\text{ V}}{20\text{ mA}} = \mathbf{40\ \Omega}$$

c. At $V_D = -10$ V, $I_D = -I_s = -1\ \mu$A (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{10\text{ V}}{1\ \mu\text{A}} = \mathbf{10\ M\Omega}$$

clearly supporting some of the earlier comments regarding the dc resistance levels of a diode.

AC or Dynamic Resistance

Eq. (1.4) and Example 1.3 reveal that

the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest.

If a sinusoidal rather than a dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.25. With no applied varying signal, the point of operation would be the *Q*-point appearing on Fig. 1.25, determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent*, which means “still or unvarying.”

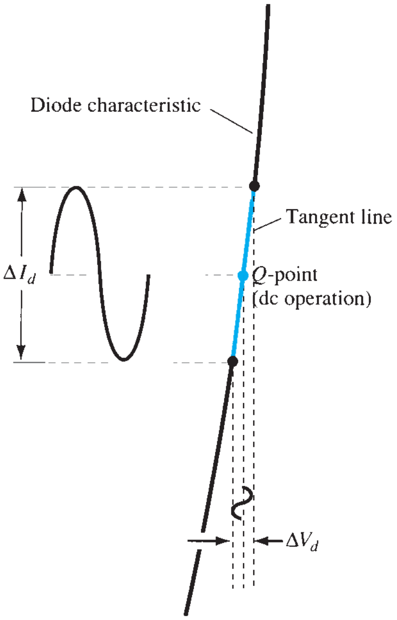


FIG. 1.25
Defining the dynamic or ac resistance.

A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 1.26 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. An effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the *Q*-point. In equation form,

$$\boxed{r_d = \frac{\Delta V_d}{\Delta I_d}} \tag{1.5}$$

where Δ signifies a finite change in the quantity.

The steeper the slope, the lower is the value of ΔV_d for the same change in ΔI_d and the lower is the resistance. The ac resistance in the vertical-rise region of the characteristic is therefore quite small, whereas the ac resistance is much higher at low current levels.

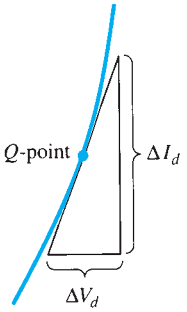


FIG. 1.26
Determining the ac resistance at a Q-point.

In general, therefore, the lower the Q-point of operation (smaller current or lower voltage), the higher is the ac resistance.

EXAMPLE 1.4 For the characteristics of Fig. 1.27:

a. Determine the ac resistance at $I_D = 2$ mA.
b. Determine the ac resistance at $I_D = 25$ mA.
c. Compare the results of parts (a) and (b) to the dc resistances at each current level.

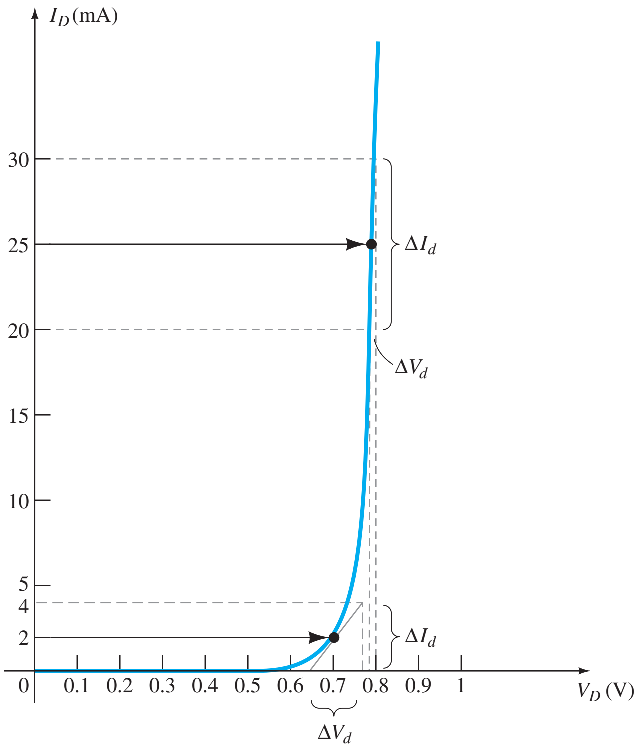


FIG. 1.27
Example 1.4.

Solution:

a. For $I_D = 2$ mA, the tangent line at $I_D = 2$ mA was drawn as shown in Fig. 1.27 and a swing of 2 mA above and below the specified diode current was chosen. At $I_D = 4$ mA, $V_D = 0.76$ V, and at $I_D = 0$ mA, $V_D = 0.65$ V. The resulting changes in current and voltage are, respectively,

$$\Delta I_d = 4\text{ mA} - 0\text{ mA} = 4\text{ mA}$$

and

$$\Delta V_d = 0.76\text{ V} - 0.65\text{ V} = 0.11\text{ V}$$

and the ac resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11\text{ V}}{4\text{ mA}} = \mathbf{27.5\ \Omega}$$

b. For $I_D = 25$ mA, the tangent line at $I_D = 25$ mA was drawn as shown in Fig. 1.27 and a swing of 5 mA above and below the specified diode current was chosen. At $I_D = 30$ mA, $V_D = 0.8$ V, and at $I_D = 20$ mA, $V_D = 0.78$ V. The resulting changes in current and voltage are, respectively,

$$\Delta I_d = 30\text{ mA} - 20\text{ mA} = 10\text{ mA}$$

and

$$\Delta V_d = 0.8\text{ V} - 0.78\text{ V} = 0.02\text{ V}$$

and the ac resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02\text{ V}}{10\text{ mA}} = \mathbf{2\ \Omega}$$

c. For $I_D = 2$ mA, $V_D = 0.7$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.7\text{ V}}{2\text{ mA}} = \mathbf{350\ \Omega}$$

which far exceeds the r_d of 27.5 Ω.

For $I_D = 25$ mA, $V_D = 0.79$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.79\text{ V}}{25\text{ mA}} = \mathbf{31.62\ \Omega}$$

which far exceeds the r_d of 2 Ω.

We have found the dynamic resistance graphically, but there is a basic definition in differential calculus that states:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

Equation (1.5), as defined by Fig. 1.26, is, therefore, essentially finding the derivative of the function at the *Q*-point of operation. If we find the derivative of the general equation (1.2) for the semiconductor diode with respect to the applied forward bias and then invert the result, we will have an equation for the dynamic or ac resistance in that region. That is, taking the derivative of Eq. (1.2) with respect to the applied bias will result in

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV_D}\left[I_s(e^{V_D/nV_T} - 1)\right]$$

and

$$\frac{dI_D}{dV_D} = \frac{1}{nV_T}(I_D + I_s)$$

after we apply differential calculus. In general, $I_D \gg I_s$ in the vertical-slope section of the characteristics and

$$\frac{dI_D}{dV_D} \cong \frac{I_D}{nV_T}$$

Flipping the result to define a resistance ratio ($R = V/I$) gives

$$\frac{dV_D}{dI_D} = r_d = \frac{nV_T}{I_D}$$

Substituting $n = 1$ and $V_T \cong 26$ mV from Example 1.1 results in

$$\boxed{r_d = \frac{26\text{ mV}}{I_D}} \qquad \textbf{(1.6)}$$

The significance of Eq. (1.6) must be clearly understood. It implies that

the dynamic resistance can be found simply by substituting the quiescent value of the diode current into the equation.

There is no need to have the characteristics available or to worry about sketching tangent lines as defined by Eq. (1.5). It is important to keep in mind, however, that Eq. (1.6) is accurate only for values of I_D in the vertical-rise section of the curve. For lesser values of I_D, $n = 2$ (silicon) and the value of r_d obtained must be multiplied by a factor of 2. For small values of I_D below the knee of the curve, Eq. (1.6) becomes inappropriate.

All the resistance levels determined thus far have been defined by the *p–n* junction and do not include the resistance of the semiconductor material itself (called *body* resistance) and the resistance introduced by the connection between the semiconductor material and the external metallic conductor (called *contact* resistance). These additional resistance levels can be included in Eq. (1.6) by adding a resistance denoted r_B:

$$\boxed{r'_d = \frac{26\text{ mV}}{I_D} + r_B}\ \text{ohms} \qquad \textbf{(1.7)}$$

The resistance r'_d, therefore, includes the dynamic resistance defined by Eq. (1.6) and the resistance r_B just introduced. The factor r_B can range from typically 0.1 Ω for high-power devices to 2 Ω for some low-power, general-purpose diodes. For Example 1.4 the ac resistance at 25 mA was calculated to be 2 Ω. Using Eq. (1.6), we have

$$r_d = \frac{26\text{ mV}}{I_D} = \frac{26\text{ mV}}{25\text{ mA}} = \mathbf{1.04\ \Omega}$$

The difference of about 1 Ω could be treated as the contribution of r_B.

For Example 1.4 the ac resistance at 2 mA was calculated to be 27.5 Ω. Using Eq. (1.6) but multiplying by a factor of 2 for this region (in the knee of the curve $n = 2$),

$$r_d = 2\left(\frac{26\text{ mV}}{I_D}\right) = 2\left(\frac{26\text{ mV}}{2\text{ mA}}\right) = 2(13\ \Omega) = \mathbf{26\ \Omega}$$

The difference of 1.5 Ω could be treated as the contribution due to r_B.

In reality, determining r_d to a high degree of accuracy from a characteristic curve using Eq. (1.5) is a difficult process at best and the results have to be treated with skepticism. At low levels of diode current the factor r_B is normally small enough compared to r_d to permit ignoring its impact on the ac diode resistance. At high levels of current the level of r_B may approach that of r_d, but since there will frequently be other resistive elements of a much larger magnitude in series with the diode, we will assume in this book that the ac resistance is determined solely by r_d, and the impact of r_B will be ignored unless otherwise noted. Technological improvements of recent years suggest that the level of r_B will continue to decrease in magnitude and eventually become a factor that can certainly be ignored in comparison to r_d.

The discussion above centered solely on the forward-bias region. In the reverse-bias region we will assume that the change in current along the I_s line is nil from 0 V to the Zener region and the resulting ac resistance using Eq. (1.5) is sufficiently high to permit the open-circuit approximation.

Typically, the ac resistance of a diode in the active region will range from about 1 Ω to 100 Ω.

Average AC Resistance

If the input signal is sufficiently large to produce a broad swing such as indicated in Fig. 1.28, the resistance associated with the device for this region is called the *average ac resistance*. The average ac resistance is, by definition, the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage. In equation form (note Fig. 1.28),

$$\boxed{r_{\text{av}} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}} \qquad \textbf{(1.8)}$$

For the situation indicated by Fig. 1.28,

$$\Delta I_d = 17\text{ mA} - 2\text{ mA} = 15\text{ mA}$$

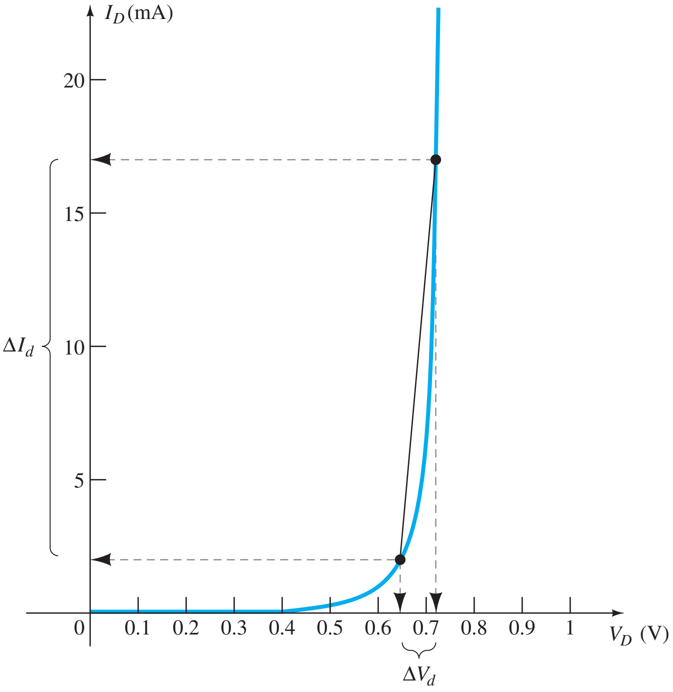


FIG. 1.28

Determining the average ac resistance between indicated limits.

and $$\Delta V_d = 0.725\text{ V} - 0.65\text{ V} = 0.075\text{ V}$$

with $$r_{\text{av}} = \frac{\Delta V_d}{\Delta I_d} = \frac{0.075\text{ V}}{15\text{ mA}} = \mathbf{5\ \Omega}$$

If the ac resistance (r_d) were determined at $I_D = 2$ mA, its value would be more than 5 Ω, and if determined at 17 mA, it would be less. In between, the ac resistance would make the transition from the high value at 2 mA to the lower value at 17 mA. Equation (1.7) defines a value that is considered the average of the ac values from 2 mA to 17 mA. The fact that one resistance level can be used for such a wide range of the characteristics will prove quite useful in the definition of equivalent circuits for a diode in a later section.

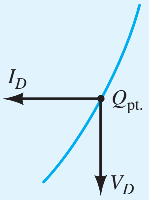
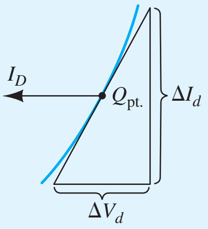
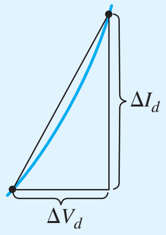
As with the dc and ac resistance levels, the lower the level of currents used to determine the average resistance, the higher is the resistance level.

Summary Table

Table 1.6 was developed to reinforce the important conclusions of the last few pages and to emphasize the differences among the various resistance levels. As indicated earlier, the content of this section is the foundation for a number of resistance calculations to be performed in later sections and chapters.

TABLE 1.6

Resistance Levels

Type	Equation	Special Characteristics	Graphical Determination
DC or static	$R_D = \frac{V_D}{I_D}$	Defined as a point on the characteristics	
AC or dynamic	$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\text{ mV}}{I_D}$	Defined by a tangent line at the Q-point	
Average ac	$r_{\text{av}} = \left.\frac{\Delta V_d}{\Delta I_d}\right\vert_{\text{pt. to pt.}}$	Defined by a straight line between limits of operation	

1.9 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating region.

In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.29. The resulting equivalent circuit is called a *piecewise-linear equivalent circuit.* It should be obvious from Fig. 1.29 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device. For the sloping section of the equivalence the average ac resistance as introduced in Section 1.8 is the resistance level appearing in the equivalent circuit of Fig. 1.28 next to the actual device. In essence, it defines the resistance level of the device when it is in the "on" state. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open-circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.29), a battery V_K opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.30. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established the resistance of the diode will be the specified value of r_{av}.

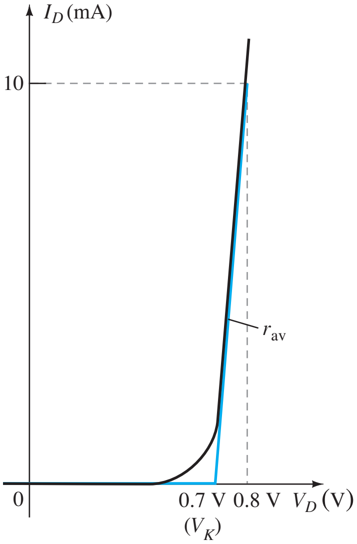


FIG. 1.29

Defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve.

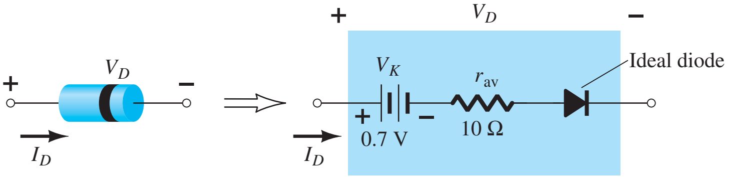


FIG. 1.30

Components of the piecewise-linear equivalent circuit.

Keep in mind, however, that V_K in the equivalent circuit is not an independent voltage source. If a voltmeter is placed across an isolated diode on the top of a laboratory bench, a reading of 0.7 V will not be obtained. The battery simply represents the horizontal offset of the characteristics that must be exceeded to establish conduction.

The approximate level of r_{av} can usually be determined from a specified operating point on the specification sheet (to be discussed in Section 1.10). For instance, for a silicon semiconductor diode, if $I_F = 10$ mA (a forward conduction current for the diode) at

$V_D = 0.8$ V, we know that for silicon a shift of 0.7 V is required before the characteristics rise, and we obtain

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} = \frac{0.8\text{ V} - 0.7\text{ V}}{10\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{10\text{ mA}} = \mathbf{10\ \Omega}$$

as obtained for Fig. 1.29.

If the characteristics or specification sheet for a diode is not available the resistance r_{av} can be approximated by the ac resistance r_d.

Simplified Equivalent Circuit

For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. Removing r_{av} from the equivalent circuit is the same as implying that the characteristics of the diode appear as shown in Fig. 1.31. Indeed, this approximation is frequently employed in semiconductor circuit analysis as demonstrated in Chapter 2. The reduced equivalent circuit appears in the same figure. It states that a forward-biased silicon diode in an electronic system under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current (within rated values, of course).

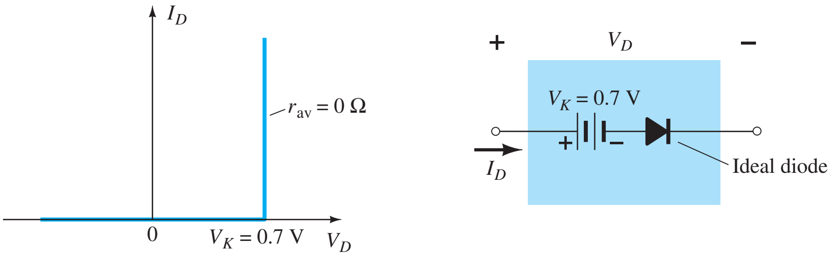


FIG. 1.31

Simplified equivalent circuit for the silicon semiconductor diode.

Ideal Equivalent Circuit

Now that r_{av} has been removed from the equivalent circuit, let us take the analysis a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level. In this case the equivalent circuit will be reduced to that of an ideal diode as shown in Fig. 1.32 with its characteristics. In Chapter 2 we will see that this approximation is often made without a serious loss in accuracy.

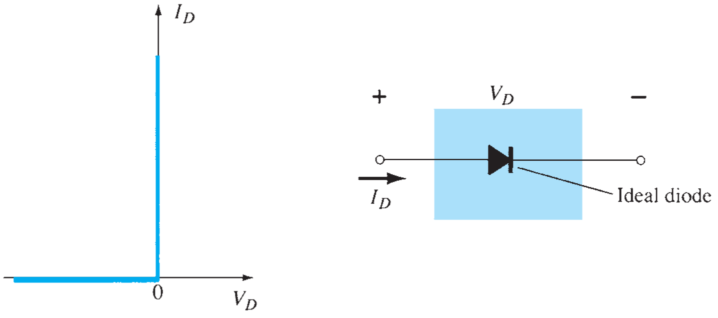


FIG. 1.32

Ideal diode and its characteristics.

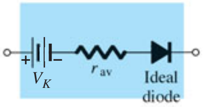
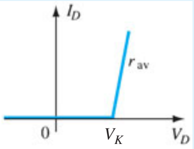
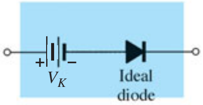
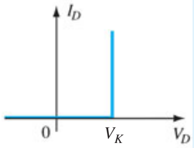
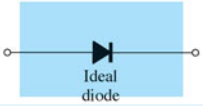
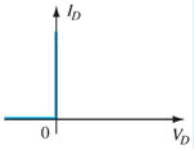
In industry a popular substitution for the phrase "diode equivalent circuit" is diode *model*—a model by definition being a representation of an existing device, object, system, and so on. In fact, this substitute terminology will be used almost exclusively in the chapters to follow.

Summary Table

For clarity, the diode models employed for the range of circuit parameters and applications are provided in Table 1.7 with their piecewise-linear characteristics. Each will be investigated in greater detail in Chapter 2. There are always exceptions to the general rule, but it

TABLE 1.7

Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{\text{network}} \gg r_{\text{av}}$		
Ideal device	$R_{\text{network}} \gg r_{\text{av}}$ $E_{\text{network}} \gg V_K$		

is fairly safe to say that the simplified equivalent model will be employed most frequently in the analysis of electronic systems, whereas the ideal diode is frequently applied in the analysis of power supply systems where larger voltages are encountered.

1.10 TRANSITION AND DIFFUSION CAPACITANCE

It is important to realize that:

Every electronic or electrical device is frequency sensitive.

That is, the terminal characteristics of any device will change with frequency. Even the resistance of a basic resistor, as of any construction, will be sensitive to the applied frequency. At low to mid-frequencies most resistors can be considered fixed in value. However, as we approach high frequencies, stray capacitive and inductive effects start to play a role and will affect the total impedance level of the element.

For the diode it is the stray capacitance levels that have the greatest effect. At low frequencies and relatively small levels of capacitance the reactance of a capacitor, determined by $X_C = 1/2\pi fC$, is usually so high it can be considered infinite in magnitude, represented by an open circuit, and ignored. At high frequencies, however, the level of X_C can drop to the point where it will introduce a low-reactance "shorting" path. If this shorting path is across the diode, it can essentially keep the diode from affecting the response of the network.

In the *p–n* semiconductor diode, there are two capacitive effects to be considered. Both types of capacitance are present in the forward- and reverse-bias regions, but one so outweighs the other in each region that we consider the effects of only one in each region.

Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In a diode the depletion region (free of carriers) behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease, as shown in Fig. 1.33. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. In fact, in Chapter 16 the varactor diode will be introduced whose operation is wholly dependent on this phenomenon.

This capacitance, called the transition (C_T), barriers, or depletion region capacitance, is determined by

$$\boxed{C_T = \frac{C(0)}{(1 + |V_R/V_K|)^n}} \tag{1.9}$$

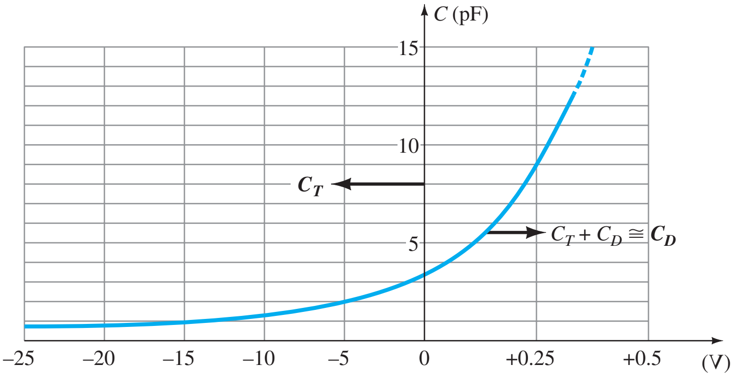


FIG. 1.33

Transition and diffusion capacitance versus applied bias for a silicon diode.

where $C(0)$ is the capacitance under no-bias conditions and V_R is the applied reverse bias potential. The power n is ½ or ⅓ depending on the manufacturing process for the diode.

Although the effect described above will also be present in the forward-bias region, it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The result is that increased levels of current will result in increased levels of diffusion capacitance (C_D) as demonstrated by the following equation:

$$\boxed{C_D = \left(\frac{\tau_T}{V_K}\right) I_D} \tag{1.10}$$

where τ_T is the minority carrier lifetime—the time is world take for a minority carrier such as a hole to recombine with an electron in the n-type material. However, increased levels of current result in a reduced level of associated resistance (to be demonstrated shortly), and the resulting time constant ($\tau = RC$), which is very important in high-speed applications, does not become excessive.

In general, therefore,

the transition capacitance is the predominant capacitive effect in the reverse-bias region whereas the diffusion capacitance is the predominant capacitive effect in the forward-bias region.

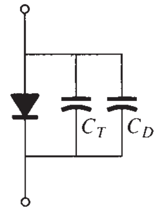


FIG. 1.34

Including the effect of the transition or diffusion capacitance on the semiconductor diode.

The capacitive effects described above are represented by capacitors in parallel with the ideal diode, as shown in Fig. 1.34. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

1.11 REVERSE RECOVERY TIME

There are certain pieces of data that are normally provided on diode specification sheets provided by manufacturers. One such quantity that has not been considered yet is the reverse recovery time, denoted by t_{rr}. In the forward-bias state it was shown earlier that there are a large number of electrons from the n-type material progressing through the p-type material and a large number of holes in the n-type material—a requirement for conduction. The electrons in the p-type material and holes progressing through the n-type material establish a large number of minority carriers in each material. If the applied voltage should be reversed to establish a reverse-bias situation, we would ideally like to see the diode change instantaneously from the conduction state to the nonconduction state. However, because of the large number of minority carriers in each material, the diode current will simply reverse as shown in Fig. 1.35 and stay at this measurable level for the period of time t_s (storage time) required for the minority carriers to return to their majority-carrier state in the opposite material. In essence, the diode will remain in the short-circuit state with a current I_{reverse} determined by the network parameters. Eventually, when this storage phase has passed, the current will be reduced in level to that associated with the nonconduction state. This second period of time is denoted by t_t (transition interval). The reverse recovery time is the sum of these two intervals: $t_{rr} = t_s + t_t$. This is an important consideration in

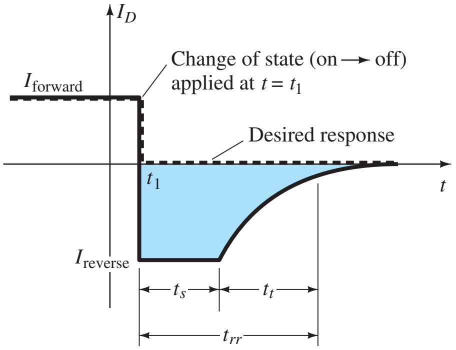


FIG. 1.35
Defining the reverse recovery time.

high-speed switching applications. Most commercially available switching diodes have a t_{rr} in the range of a few nanoseconds to 1 μs. Units are available, however, with a t_{rr} of only a few hundred picoseconds (10^{-12} s).

1.12 DIODE SPECIFICATION SHEETS

Data on specific semiconductor devices are normally provided by the manufacturer in one of two forms. Most frequently, they give a very brief description limited to perhaps one page. At other times, they give a thorough examination of the characteristics using graphs, artwork, tables, and so on. In either case, there are specific pieces of data that must be included for proper use of the device. They include:

1. The forward voltage V_F (at a specified current and temperature)
2. The maximum forward current I_F (at a specified temperature)
3. The reverse saturation current I_R (at a specified voltage and temperature)
4. The reverse-voltage rating [PIV or PRV or V(BR), where BR comes from the term "breakdown" (at a specified temperature)]
5. The maximum power dissipation level at a particular temperature
6. Capacitance levels
7. Reverse recovery time t_{rr}
8. Operating temperature range

Depending on the type of diode being considered, additional data may also be provided, such as frequency range, noise level, switching time, thermal resistance levels, and peak repetitive values. For the application in mind, the significance of the data will usually be self-apparent. If the maximum power or dissipation rating is also provided, it is understood to be equal to the following product:

$$\boxed{P_{D\max} = V_D I_D} \tag{1.11}$$

where I_D and V_D are the diode current and voltage, respectively, at a particular point of operation.

If we apply the simplified model for a particular application (a common occurrence), we can substitute $V_D = V_T = 0.7$ V for a silicon diode in Eq. (1.11) and determine the resulting power dissipation for comparison against the maximum power rating. That is,

$$\boxed{P_{\text{dissipated}} \cong (0.7\ \text{V})I_D} \tag{1.12}$$

The data provided for a high-voltage/low-leakage diode appear in Figs. 1.36 and 1.37. This example would represent the expanded list of data and characteristics. The term *rectifier* is applied to a diode when it is frequently used in a *rectification* process, described in Chapter 2.

Specific areas of the specification sheet are highlighted in blue, with letters corresponding to the following description:

A The data sheet highlights the fact that the silicon high-voltage diode has a *minimum* reverse-bias voltage of 125 V at a specified reverse-bias current.

B Note the wide range of temperature operation. Always be aware that data sheets typically use the centigrade scale, with 200°C = 392°F and −65°C = −85°F.

C The maximum power dissipation level is given by $P_D = V_D I_D = 500\text{ mW} = 0.5\text{ W}$. The effect of the linear derating factor of 3.33 mW/°C is demonstrated in Fig. 1.37a. Once the temperature exceeds 25°C the maximum power rating will drop by 3.33 mW for each 1°C increase in temperature. At a temperature of 100°C, which is the boiling point of water, the maximum power rating has dropped to one half of its original value. An initial temperature of 25°C is typical inside a cabinet containing operating electronic equipment in a low-power situation.

D The maximum sustainable current is 500 mA. The plot of Fig. 1.37b reveals that the forward current at 0.5 V is about 0.01 mA, but jumps to 1 mA (100 times greater) at about 0.65 V. At 0.8 V the current is more than 10 mA, and just above 0.9 V it is close

DIFFUSED SILICON PLANAR

A **• BV . . . 125 V (MIN) @ 100 μA (BAY73)**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperatures

B	Storage Temperature Range	−65°C to +200°C
	Maximum Junction Operating Temperature	+175°C
	Lead Temperature	+260°C

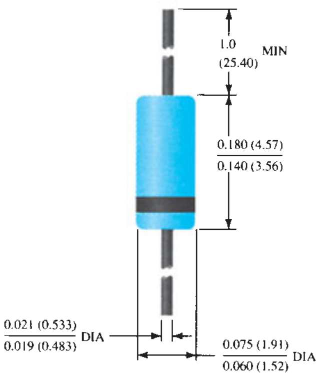
Power Dissipation (Note 2)

C	Maximum Total Power Dissipation at 25°C Ambient	500 mW
	Linear Power Derating Factor (from 25°C)	3.33 mW/°C

Maximum Voltage and Currents

	WIV	Working Inverse Voltage	BAY73	100 V
	I_O	Average Rectified Current		200 mA
D	I_F	Continuous Forward Current		500 mA
	i_f	Peak Repetitive Forward Current		600 mA
	$i_{f\,(\text{surge})}$	Peak Forward Surge Current		
		Pulse Width = 1 s		1.0 A
		Pulse Width = 1 μs		4.0 A

DO-35 OUTLINE



NOTES:
Copper clad steel leads, tin plated
Gold plated leads available
Hermetically sealed glass package
Package weight is 0.14 gram

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

	SYMBOL	CHARACTERISTIC	BAY73		UNITS	TEST CONDITIONS
			MIN	MAX		
E	V_F	Forward Voltage	0.85	1.00	V	I_F = 200 mA
			0.81	0.94	V	I_F = 100 mA
			0.78	0.88	V	I_F = 50 mA
			0.69	0.80	V	I_F = 10 mA
			0.67	0.75	V	I_F = 5.0 mA
			0.60	0.68	V	I_F = 1.0 mA
F	I_R	Reverse Current		500	nA	V_R = 20 V, T_A = 125°C
				1.0	μA	V_R = 100 V, T_A = 125°C
				0.2	nA	V_R = 20 V, T_A = 25°C
				0.5	nA	V_R = 100 V, T_A = 25°C
	BV	Breakdown Voltage	125		V	I_R = 100 μA
G	C	Capacitance		5.0	pF	V_R = 0, f = 1.0 MHz
H	t_{rr}	Reverse Recovery Time		3.0	μs	I_F = 10 mA, V_R = 35 V R_L = 1.0 to 100 kΩ C_L = 10 pF, JAN 256

NOTES
1 These ratings are limiting values above which the serviceability of the diode may be impaired.
2 These are steady state limits. The factory should be consulted on applications involving pulses or low duty-cycle operation.

FIG. 1.36

Electrical characteristics of a high-voltage, low-leakage diode.

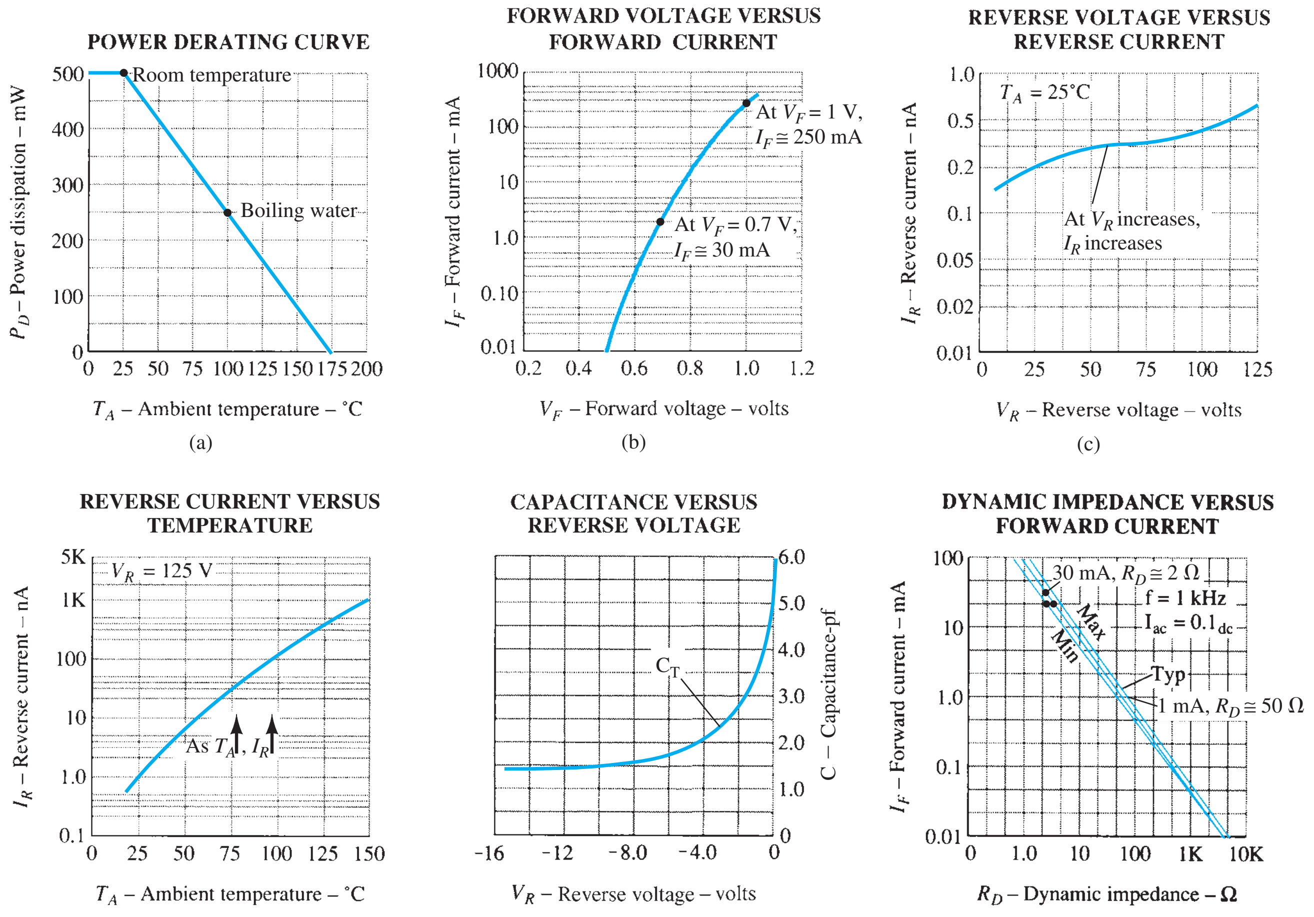


FIG. 1.37

Terminal characteristics of a high-voltage diode.

to 100 mA. The curve of Fig. 1.37b certainly looks nothing like the characteristic curves appearing in the last few sections. This is a result of using a log scale for the current and a linear scale for the voltage.

Log scales are often used to provide a broader range of values for a variable in a limited amount of space.

If a linear scale was used for the current, it would be impossible to show a range of values from 0.01 mA to 1000 mA. If the vertical divisions were in 0.01-mA increments, it would take 100,000 equal intervals on the vertical axis to reach 1000 mA. For the moment recognize that the voltage level at given levels of current can be found by using the intersection with the curve. For vertical values above a level such as 1.0 mA, the next level is 2 mA, followed by 3 mA, 4 mA, and 5 mA. The levels of 6 mA to 10 mA can be determined by simply dividing the distance into equal intervals (not the true distribution, but close enough for the provided graphs). For the next level it would be 10 mA, 20 mA, 30 mA, and so on. The graph of Fig. 1.37b is called a *semi-log plot* to reflect the fact that only one axis uses a log scale. A great deal more will be said about log scales in Chapter 9.

E The data provide a range of V_F (forward-bias voltages) for each current level. The higher the forward current, the higher is the applied forward bias. At 1 mA we find V_F can range from 0.6 V to 0.68 V, but at 200 mA it can be as high as 0.85 V to 1.00 V. For the full range of current levels with 0.6 V at 1 mA and 0.85 V at 200 mA it is certainly a reasonable approximation to use 0.7 V as the average value.

F The data provided clearly reveal how the reverse saturation current increases with applied reverse bias at a fixed temperature. At 25°C the maximum reverse-bias current increases from 0.2 nA to 0.5 nA due to an increase in reverse-bias voltage by the same factor of 5. At 125°C it jumps by a factor of 2 to the high level of 1 μA. Note the extreme change in reverse saturation current with temperature as the maximum current rating jumps from 0.2 nA at 25°C to 500 nA at 125°C (at a fixed reverse-bias voltage of 20 V). A similar increase occurs at a reverse-bias potential of 100 V. The semi-log plots of Figs. 1.37c and 1.37d provide an indication of how the reverse saturation current changes with changes in reverse voltage and temperature. At first glance Fig. 1.37c might suggest that the reverse saturation current is fairly steady for changes in reverse voltage. However, this can sometimes be the effect of using a log scale for the vertical axis. The current has actually changed from a level of 0.2 nA to a level of 0.7 nA for the range of voltages representing a change of almost 6 to 1. The dramatic effect of temperature on the reverse saturation current is clearly displayed in Fig. 1.37d. At a reverse-bias voltage of 125 V the reverse-bias current increases from a level of about 1 nA at 25°C to about 1 μA at 150°C, an increase of a factor of 1000 over the initial value.

Temperature and applied reverse bias are very important factors in designs sensitive to the reverse saturation current.

G As shown in the data listing and on Fig. 1.37e, the transition capacitance at a reverse-bias voltage of 0 V is 5 pF at a test frequency of 1 MHz. Note the severe change in capacitance level as the reverse-bias voltage is increased. As mentioned earlier, this sensitive region can be put to good use in the design of a device (Varactor; Chapter 16) whose terminal capacitance is sensitive to the applied voltage.

H The reverse recovery time is 3 μs for the test conditions shown. This is not a fast time for some of the current high-performance systems in use today. However, for a variety of low- and mid-frequency applications it is acceptable.

The curves of Fig. 1.37f provide an indication of the magnitude of the ac resistance of the diode versus forward current. Section 1.8 clearly demonstrated that the dynamic resistance of a diode decreases with increase in current. As we go up the current axis of Fig. 1.37f it is clear that if we follow the curve, the dynamic resistance will decrease. At 0.1 mA it is close to 1 kΩ; at 10 mA, 10 Ω; and at 100 mA, only 1 Ω; this clearly supports the earlier discussion. Unless one has had experience reading log scales, the curve is challenging to read for levels between those indicated because it is a *log–log* plot. Both the vertical axis and the horizontal axis employ a log scale.

The more one is exposed to specification sheets, the “friendlier” they will become, especially when the impact of each parameter is clearly understood for the application under investigation.

1.13 SEMICONDUCTOR DIODE NOTATION

The notation most frequently used for semiconductor diodes is provided in Fig. 1.38. For most diodes any marking such as a dot or band, as shown in Fig. 1.38, appears at the cathode end. The terminology anode and cathode is a carryover from vacuum-tube notation. The anode refers to the higher or positive potential, and the cathode refers to the lower or negative terminal. This combination of bias levels will result in a forward-bias or “on” condition for the diode. A number of commercially available semiconductor diodes appear in Fig. 1.39.

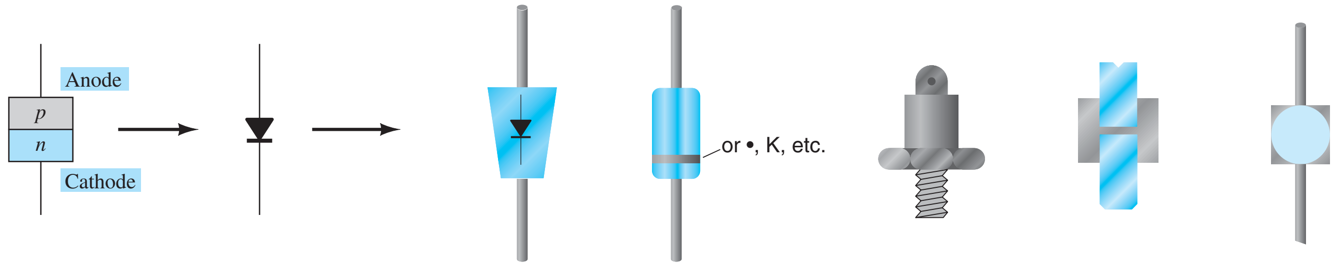
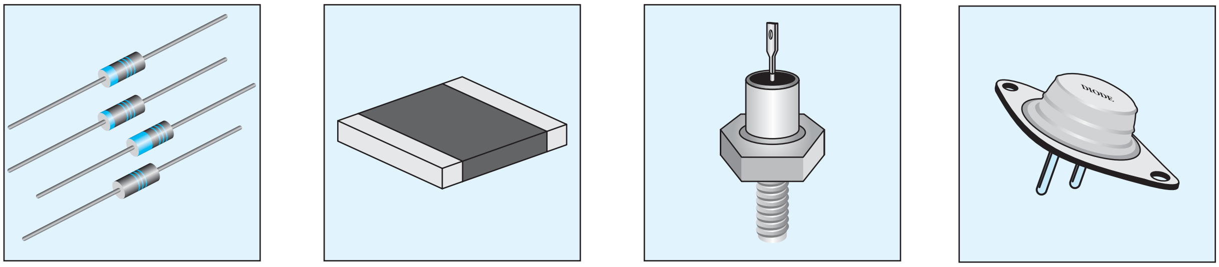
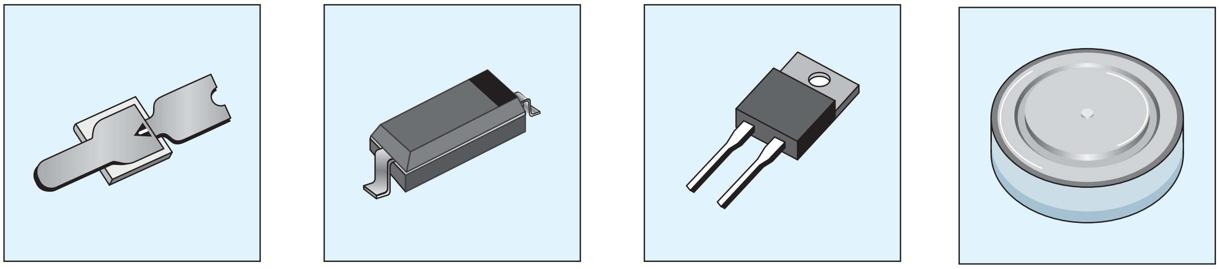


FIG. 1.38
Semiconductor diode notation.



General purpose diode Surface mount high-power PIN diode Power (stud) diode Power (planar) diode



Beam lead pin diode Flat chip surface mount diode Power diode Power (disc, puck) diode

FIG. 1.39
Various types of junction diodes.

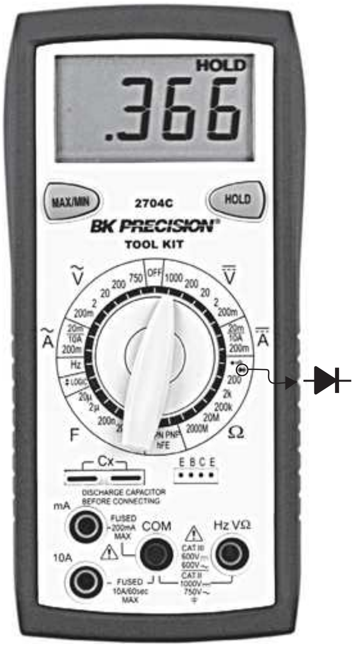


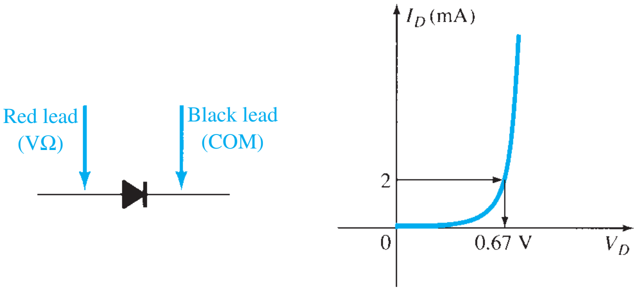
FIG. 1.40
Digital display meter. (Courtesy of B&K Precision Corporation.)

1.14 DIODE TESTING

The condition of a semiconductor diode can be determined quickly using (1) a digital display meter (DDM) with a *diode checking function*, (2) the *ohmmeter section* of a multimeter, or (3) a *curve tracer.*

Diode Checking Function

A digital display meter with a diode checking capability appears in Fig. 1.40. Note the small diode symbol at the top right of the rotating dial. When set in this position and hooked up as shown in Fig. 1.41a, the diode should be in the "on" state and the display will provide an indication of the forward-bias voltage such as 0.67 V (for Si). The meter has an internal constant-current source (about 2 mA) that will define the voltage level as indicated in Fig. 1.41b. An OL indication with the hookup of Fig. 1.41a reveals an open (defective) diode. If the leads are reversed, an OL indication should result due to the expected open-circuit equivalence for the diode. In general, therefore, an OL indication in both directions is an indication of an open or defective diode.



(a) (b)

FIG. 1.41
Checking a diode in the forward-bias state.

Ohmmeter Testing

In Section 1.8 we found that the forward-bias resistance of a semiconductor diode is quite low compared to the reverse-bias level. Therefore, if we measure the resistance of a diode using the connections indicated in Fig. 1.42, we can expect a relatively low level. The resulting ohmmeter indication will be a function of the current established through the diode by the internal battery (often 1.5 V) of the ohmmeter circuit. The higher the current, the lower is the resistance level. For the reverse-bias situation the reading should be quite high, requiring a high resistance scale on the meter, as indicated in Fig. 1.42b. A high resistance reading in both directions indicates an open (defective-device) condition, whereas a very low resistance reading in both directions will probably indicate a shorted device.

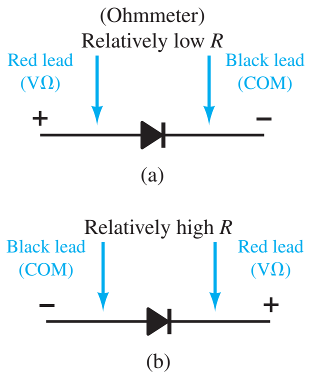


FIG. 1.42

Checking a diode with an ohmmeter.

Curve Tracer

The curve tracer of Fig. 1.43 can display the characteristics of a host of devices, including the semiconductor diode. By properly connecting the diode to the test panel at the bottom center of the unit and adjusting the controls, one can obtain the display of Fig. 1.44. Note that the vertical scaling is 1 mA/div, resulting in the levels indicated. For the horizontal axis the scaling is 100 mV/div, resulting in the voltage levels indicated. For a 2-mA level as defined for a DDM, the resulting voltage would be about 625 mV = 0.625 V. Although the instrument initially appears quite complex, the instruction manual and a few moments of exposure will reveal that the desired results can usually be obtained without an excessive amount of effort and time. The display of the instrument will appear on more than one occasion in the chapters to follow as we investigate the characteristics of the variety of devices.

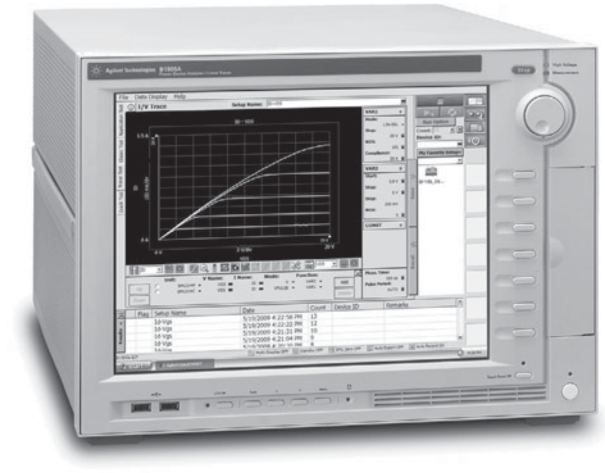


FIG. 1.43

Curve tracer. (© Agilent Technologies, Inc. Reproduced with Permission, Courtesy of Agilent Technologies, Inc.)

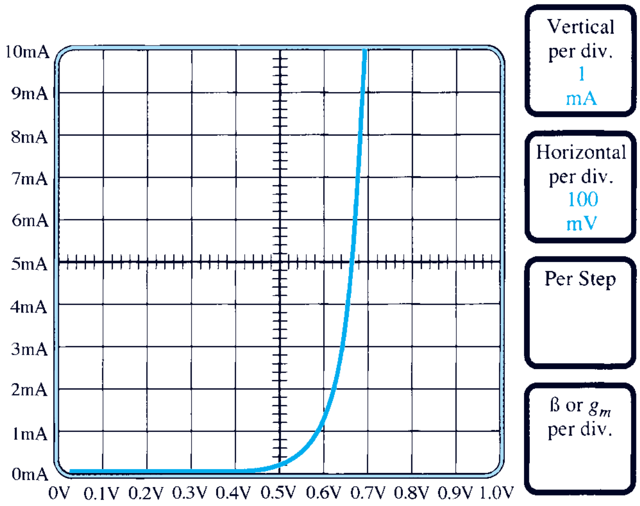


FIG. 1.44

Curve tracer response to IN4007 silicon diode.

1.15 ZENER DIODES

The Zener region of Fig. 1.45 was discussed in some detail in Section 1.6. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive-V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode. The slight slope to the curve in the Zener region reveals that there is a level of resistance to be associated with the Zener diode in the conduction mode.

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in Fig. 1.46a. The semiconductor diode and the Zener diode are presented side by side in Fig. 1.46 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol, as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element as shown in Fig. 1.46c.

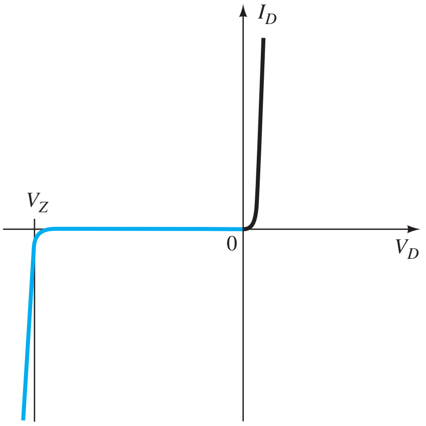


FIG. 1.45

Reviewing the Zener region.

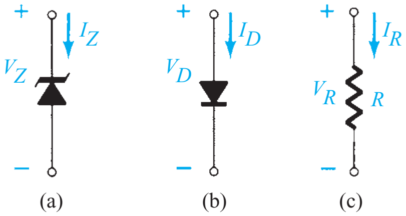


FIG. 1.46

Conduction direction: (a) Zener diode; (b) semiconductor diode; (c) resistive element.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping that produces an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 V to 200 V with power ratings from ¼ W to 50 W. Because of its excellent temperature and current capabilities, silicon is the preferred material in the manufacture of Zener diodes.

It would be nice to assume the Zener diode is ideal with a straight vertical line at the Zener potential. However, there is a slight slope to the characteristics requiring the piecewise equivalent model appearing in Fig. 1.47 for that region. For most of the applications appearing in this text the series resistive element can be ignored and the reduced equivalent model of just a dc battery of V_Z volts employed. Since some applications of Zener diodes swing between the Zener region and the forward-bias region, it is important to understand the operation of the Zener diode in all regions. As shown in Fig. 1.47, the equivalent model for a Zener diode in the reverse-bias region below V_Z is a very large resistor (as for the standard diode). For most applications this resistance is so large it can be ignored and the open-circuit equivalent employed. For the forward-bias region the piecewise equivalent is the same as described in earlier sections.

The specification sheet for a 10-V, 500-mW, 20% Zener diode is provided as Table 1.8, and a plot of the important parameters is given in Fig. 1.48. The term *nominal* used in the specification of the Zener voltage simply indicates that it is a typical average value. Since this is a 20% diode, the Zener potential of the unit one picks out of a *lot* (a term used to describe a package of diodes) can be expected to vary as 10 V + 20%, or from 8 V to 12 V. Both 10% and 50% diodes are also readily available. The test current I_{ZT} is the current defined by the

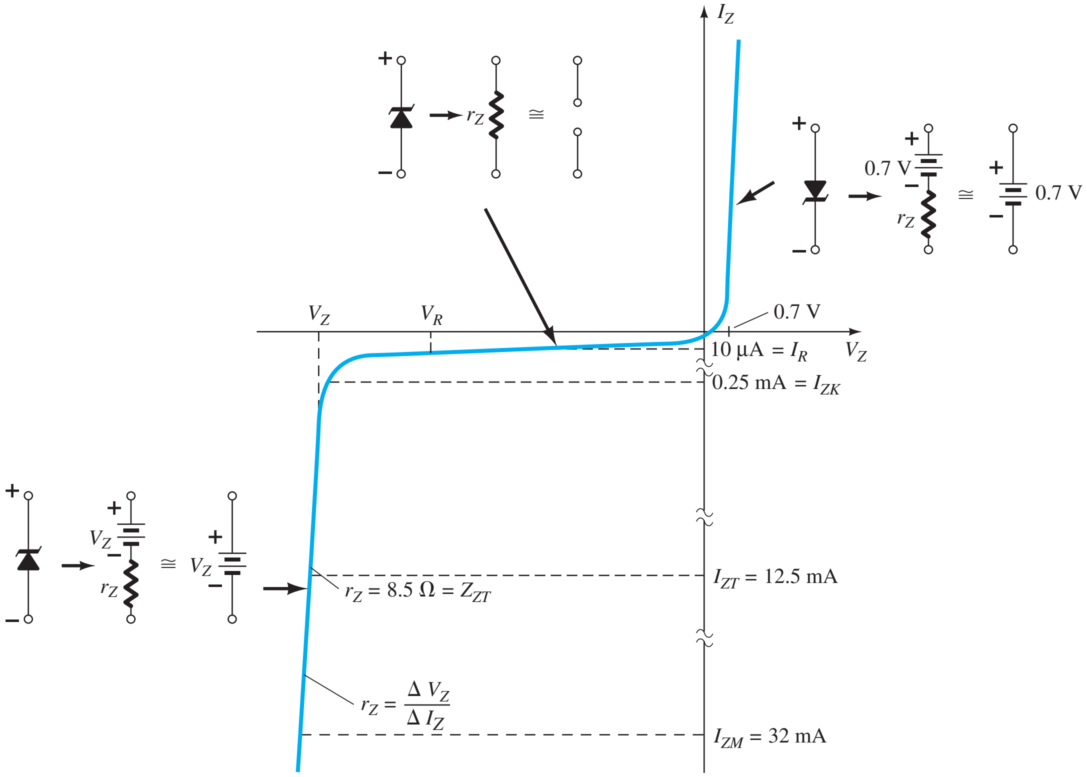

I_Z
r_Z
$\cong$
0.7 V
r_Z
$\cong$
0.7 V
V_Z
V_R
0.7 V
V_Z
10 µA = I_R
0.25 mA = I_{ZK}
V_Z
r_Z
$\cong$
V_Z
$r_Z = 8.5\ \Omega = Z_{ZT}$
I_{ZT} = 12.5 mA
$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$
I_{ZM} = 32 mA

FIG. 1.47
Zener diode characteristics with the equivalent model for each region.

TABLE 1.8
Electrical Characteristics (25°C Ambient Temperature)

Zener Voltage Nominal V_Z (V)	Test Current I_{ZT} (mA)	Maximum Dynamic Impedance Z_{ZT} at I_{ZT} (Ω)	Maximum Knee Impedance Z_{ZK} at I_{ZK} (Ω)	(mA)	Maximum Reverse Current I_R at V_R (μA)	Test Voltage V_R (V)	Maximum Regulator Current I_{ZM} (mA)	Typical Temperature Coefficient (%/°C)
10	12.5	8.5	700	0.25	10	7.2	32	+0.072

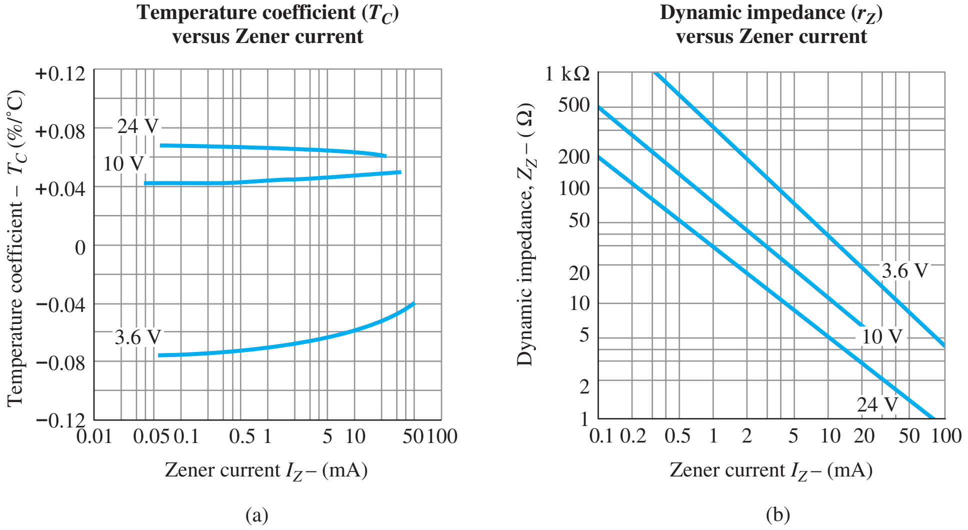


FIG. 1.48
Electrical characteristics for a 10-V, 500-mW Zener diode.

¼-power level. It is the current that will define the dynamic resistance Z_{ZT} and appears in the general equation for the power rating of the device. That is,

$$\boxed{P_{Z_{\max}} = 4I_{ZT}V_Z} \qquad \textbf{(1.13)}$$

Substituting I_{ZT} into the equation with the nominal Zener voltage results in

$$P_{Z_{\max}} = 4I_{ZT}V_Z = 4(12.5\text{ mA})(10\text{ V}) = 500\text{ mW}$$

which matches the 500-mW label appearing above. For this device the dynamic resistance is 8.5 Ω, which is usually small enough to be ignored in most applications. The maximum knee impedance is defined at the center of the knee at a current of $I_{ZK} = 0.25$ mA. Note that in all the above the letter T is used in subscripts to indicate test values and the letter K to indicate knee values. For any level of current below 0.25 mA the resistance will only get larger in the reverse-bias region. The knee value therefore reveals when the diode will start to show very high series resistance elements that one may not be able to ignore in an application. Certainly 500 Ω = 0.5 kΩ may be a level that can come into play. At a reverse-bias voltage the application of a test voltage of 7.2 V results in a reverse saturation current of 10 μA, a level that could be of some concern in some applications. The maximum regulator current is the maximum continuous current one would want to support in the use of the Zener diode in a regulator configuration. Finally, we have the temperature coefficient (T_C) in percent per degree centigrade.

The Zener potential of a Zener diode is very sensitive to the temperature of operation.

The temperature coefficient can be used to find the change in Zener potential due to a change in temperature using the following equation:

$$\boxed{T_C = \frac{\Delta V_Z/V_Z}{T_1 - T_0} \times 100\%/^\circ\text{C}} \quad (\%/^\circ\text{C}) \qquad \textbf{(1.14)}$$

where T_1 is the new temperature level
T_0 is room temperature in an enclosed cabinet (25°C)
T_C is the temperature coefficient
and V_Z is the nominal Zener potential at 25°C.

To demonstrate the effect of the temperature coefficient on the Zener potential, consider the following example.

EXAMPLE 1.5 Analyze the 10-V Zener diode described by Table 1.7 if the temperature is increased to 100°C (the boiling point of water).

Solution: Substituting into Eq. (1.14), we obtain

$$\Delta V_Z = \frac{T_C V_Z}{100\%}(T_1 - T_0)$$

$$= \frac{(0.072\%/^\circ\text{C})(10\text{ V})}{100\%}(100^\circ\text{C} - 25^\circ\text{C})$$

and $$\Delta V_Z = 0.54\text{ V}$$

The resulting Zener potential is now

$$V_Z' = V_Z + 0.54\text{ V} = \mathbf{10.54\text{ V}}$$

which is not an insignificant change.

It is important to realize that in this case the temperature coefficient was positive. For Zener diodes with Zener potentials less than 5 V it is very common to see negative temperature coefficients, where the Zener voltage drops with an increase in temperature. Figure 1.48a provides a plot of T versus Zener current for three different levels of diodes. Note that the 3.6-V diode has a negative temperature coefficient, whereas the others have positive values.

The change in dynamic resistance with current for the Zener diode in its avalanche region is provided in Fig. 1.48b. Again, we have a log–log plot, which has to be carefully read.

Initially it would appear that there is an inverse linear relationship between the dynamic resistance because of the straight line. That would imply that if one doubles the current, one cuts the resistance in half. However, it is only the log–log plot that gives this impression, because if we plot the dynamic resistance for the 24-V Zener diode versus current using linear scales we obtain the plot of Fig. 1.49, which is almost exponential in appearance. Note on both plots that the dynamic resistance at very low currents that enter the knee of the curve is fairly high at about 200 Ω. However, at higher Zener currents, away from the knee, at, say 10 mA, the dynamic resistance drops to about 5 Ω.

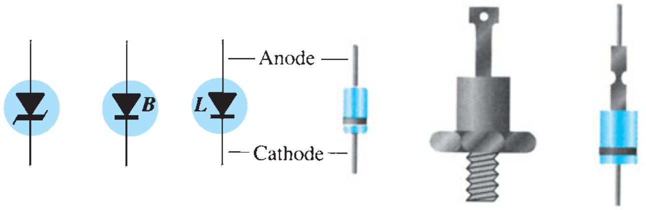


FIG. 1.49
Zener terminal identification and symbols.

The terminal identification and the casing for a variety of Zener diodes appear in Fig. 1.49. Their appearance is similar in many ways to that of the standard diode. Some areas of application for the Zener diode will be examined in Chapter 2.

1.16 LIGHT-EMITTING DIODES

The increasing use of digital displays in calculators, watches, and all forms of instrumentation has contributed to an extensive interest in structures that emit light when properly biased. The two types in common use to perform this function are the light-emitting diode (LED) and the liquid-crystal display (LCD). Since the LED falls within the family of *p–n* junction devices and will appear in some of the networks of the next few chapters, it will be introduced in this chapter. The LCD display is described in Chapter 16.

As the name implies, the light-emitting diode is a diode that gives off visible or invisible (infrared) light when energized. In any forward-biased *p–n* junction there is, within the structure and primarily close to the junction, a recombination of holes and electrons. This recombination requires that the energy possessed by the unbound free electrons be transferred to another state. In all semiconductor *p–n* junctions some of this energy is given off in the form of heat and some in the form of photons.

In Si and Ge diodes the greater percentage of the energy converted during recombination at the junction is dissipated in the form of heat within the structure, and the emitted light is insignificant.

For this reason, silicon and germanium are not used in the construction of LED devices. On the other hand:

Diodes constructed of GaAs emit light in the infrared (invisible) zone during the recombination process at the p–n junction.

Even though the light is not visible, infrared LEDs have numerous applications where visible light is not a desirable effect. These include security systems, industrial processing, optical coupling, safety controls such as on garage door openers, and in home entertainment centers, where the infrared light of the remote control is the controlling element.

Through other combinations of elements a coherent visible light can be generated. Table 1.9 provides a list of common compound semiconductors and the light they generate. In addition, the typical range of forward bias potentials for each is listed.

The basic construction of an LED appears in Fig. 1.50 with the standard symbol used for the device. The external metallic conducting surface connected to the *p*-type material is smaller to permit the emergence of the maximum number of photons of light energy when the device is forward-biased. Note in the figure that the recombination of the injected carriers due to the forward-biased junction results in emitted light at the site of the recombination.

TABLE 1.9

Light-Emitting Diodes

Color	Construction	Typical Forward Voltage (V)
Amber	AlInGaP	2.1
Blue	GaN	5.0
Green	GaP	2.2
Orange	GaAsP	2.0
Red	GaAsP	1.8
White	GaN	4.1
Yellow	AlInGaP	2.1

There will, of course, be some absorption of the packages of photon energy in the structure itself, but a very large percentage can leave, as shown in the figure.

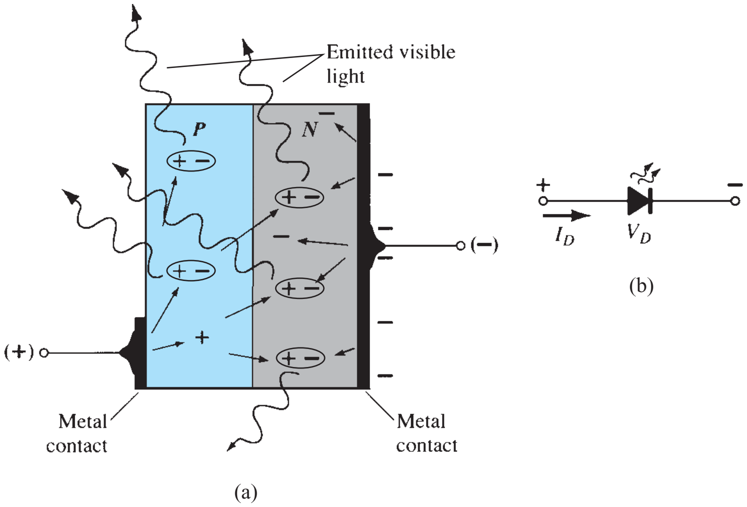


FIG. 1.50

(a) Process of electroluminescence in the LED; (b) graphic symbol.

Just as different sounds have different frequency spectra (high-pitched sounds generally have high-frequency components, and low sounds have a variety of low-frequency components), the same is true for different light emissions.

The frequency spectrum for infrared light extends from about 100 THz (T = tera = 10^{12}) to 400 THz, with the visible light spectrum extending from about 400 to 750 THz.

It is interesting to note that invisible light has a lower frequency spectrum than visible light.

In general, when one talks about the response of electroluminescent devices, one references their wavelength rather than their frequency.

The two quantities are related by the following equation:

$$\boxed{\lambda = \frac{c}{f}} \quad \text{(m)} \tag{1.15}$$

where $c = 3 \times 10^8$ m/s (the speed of light in a vacuum)
f = frequency in Hertz
λ = wavelength in meters.

EXAMPLE 1.6 Using Eq. (1.15), find the range of wavelength for the frequency range of visible light (400 THz–750 THz).

Solution:

$$c = 3 \times 10^8 \frac{\cancel{\text{m}}}{\text{s}}\left[\frac{10^9\ \text{nm}}{\cancel{\text{m}}}\right] = 3 \times 10^{17}\ \text{nm/s}$$

$$\lambda = \frac{c}{f} = \frac{3 \times 10^{17}\ \text{nm/s}}{400\ \text{THz}} = \frac{3 \times 10^{17}\ \text{nm/s}}{400 \times 10^{12}\ \text{Hz}} = 750\ \text{nm}$$

$$\lambda = \frac{c}{f} = \frac{3 \times 10^{17}\ \text{nm/s}}{750\ \text{THz}} = \frac{3 \times 10^{17}\ \text{nm/s}}{750 \times 10^{12}\ \text{Hz}} = 400\ \text{nm}$$

400 nm to 750 nm

Note in the above example the resulting inversion from higher frequency to smaller wavelength. That is, the higher frequency results in the smaller wavelength. Also, most charts use either nanometers (nm) or angstrom (Å) units. One angstrom unit is equal to 10^{-10} m.

The response of the average human eye as provided in Fig. 1.51 extends from about 350 nm to 800 nm with a peak near 550 nm.

It is interesting to note that the peak response of the eye is to the color green, with red and blue at the lower ends of the bell curve. The curve reveals that a red or a blue LED must have a much stronger efficiency than a green one to be visible at the same intensity. In other words, the eye is more sensitive to the color green than to other colors. Keep in mind that the wavelengths shown are for the peak response of each color. All the colors indicated on the plot will have a bell-shaped curve response, so green, for example, is still visible at 600 nm, but at a lower intensity level.

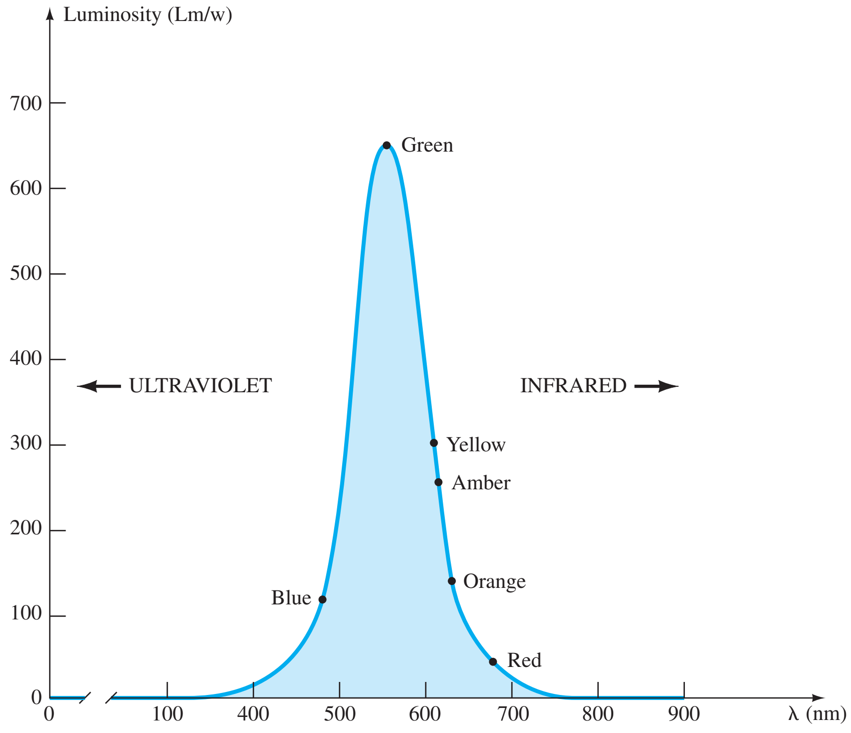


FIG. 1.51

Standard response curve of the human eye, showing the eye's response to light energy peaks at green and falls off for blue and red.

In Section 1.4 it was mentioned briefly that GaAs with its higher energy gap of 1.43 eV made it suitable for electromagnetic radiation of visible light, whereas Si at 1.1 eV resulted primarily in heat dissipation on recombination. The effect of this difference in energy gaps can be explained to some degree by realizing that to move an electron from one discrete energy level to another requires a specific amount of energy. The amount of energy involved is given by

$$\boxed{E_g = \frac{hc}{\lambda}} \tag{1.16}$$

with E_g = joules (J) [1 eV = 1.6×10^{-19} J]
h = Planck's constant = 6.626×10^{-34} J • s.
$c = 3 \times 10^8$ m/s
λ = wavelength in meters

If we substitute the energy gap level of 1.43 eV for GaAs into the equation, we obtain the following wavelength:

$$1.43\ \cancel{\text{eV}}\left[\frac{1.6 \times 10^{-19}\ \text{J}}{1\ \cancel{\text{eV}}}\right] = 2.288 \times 10^{-19}\ \text{J}$$

and

$$\lambda = \frac{hc}{E_g} = \frac{(6.626 \times 10^{-34}\ \text{J} \cdot \text{s})(3 \times 10^8\ \text{m/s})}{2.288 \times 10^{-19}\ \text{J}}$$
$$= 869\ \mathbf{nm}$$

For silicon, with $E_g = 1.1$ eV

$$\lambda = \mathbf{1130\ nm}$$

which is well beyond the visible range of Fig. 1.51.

The wavelength of 869 nm places GaAs in the wavelength zone typically used in infrared devices. For a compound material such as GaAsP with a band gap of 1.9 eV the resulting wavelength is 654 nm, which is in the center of the red zone, making it an excellent compound semiconductor for LED production. In general, therefore:

The wavelength and frequency of light of a specific color are directly related to the energy band gap of the material.

A first step, therefore, in the production of a compound semiconductor that can be used to generate light is to come up with a combination of elements that will generate the desired energy band gap.

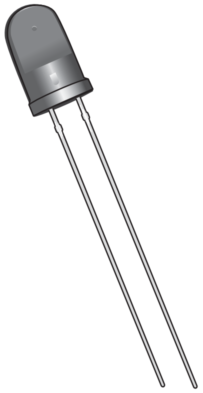
The appearance and characteristics of a subminiature high-efficiency red LED manufactured by Hewlett-Packard are given in Fig. 1.52. Note in Fig. 1.52b that the peak forward current is 60 mA, with 20 mA the typical average forward current. The text conditions listed in Fig. 1.52c, however, are for a forward current of 10 mA. The level of V_D under forward-bias conditions is listed as V_F and extends from 2.2 V to 3 V. In other words, one can expect a typical operating current of about 10 mA at 2.3 V for good light emission, as shown in Fig. 1.52e. In particular, note the typical diode characteristics for an LED, permitting similar analysis techniques to be described in the next chapter.

Two quantities yet undefined appear under the heading Electrical/Optical Characteristics at $T_A = 25°\text{C}$. They are the *axial luminous intensity* (I_V) and the *luminous efficacy* (η_V). Light intensity is measured in *candelas.* One candela (cd) corresponds to a light flux of 4π lumens (lm) and is equivalent to an illumination of *1 footcandle* on a 1-ft^2 area 1 ft from the light source. Even if this description may not provide a clear understanding of the candela as a unit of measure, it should be enough to allow its level to be compared between similar devices. Figure 1.52f is a normalized plot of the relative luminous intensity versus forward current. The term *normalized* is used frequently on graphs to give comparisons of response to a particular level.

A normalized plot is one where the variable of interest is plotted with a specific level defined as the reference value with a magnitude of one.

In Fig. 1.52f the normalized level is taken at $I_F = 10$ mA. Note that the relative luminous intensity is 1 at $I_F = 10$ mA. The graph quickly reveals that the intensity of the light is almost doubled at a current of 15 mA and is almost three times as much at a current of 20 mA. It is important to therefore note that:

The light intensity of an LED will increase with forward current until a point of saturation arrives where any further increase in current will not effectively increase the level of illumination.



(a)

Absolute Maximum Ratings at T_A = 25°C

Parameter	*High-Efficiency Red 4160*	*Units*
Power dissipation	120	mW
Average forward current	20[1]	mA
Peak forward current	60	mA
Operating and storage temperature range	−55°C to 100°C	
Lead soldering temperature [1.6 mm (0.063 in.) from body]	230°C for 3 s	

NOTE: 1. Derate from 50°C at 0.2 mV/°C.

(b)

Electrical/Optical Characteristics at T_A = 25°C

		High-Efficiency Red 4160				
Symbol	*Description*	*Min.*	*Typ.*	*Max.*	*Units*	*Test Conditions*
						I_F = 10 mA
I_V	Axial luminous intensity	1.0	3.0		mcd	
$2\theta_{1/2}$	Included angle between half luminous intensity points		80		degree	Note 1
λ_{peak}	Peak wavelength		635		nm	Measurement at peak
λ_d	Dominant wavelength		628		nm	Note 2
τ_s	Speed of response		90		ns	
C	Capacitance		11		pF	V_F = 0; f = 1 Mhz
θ_{JC}	Thermal resistance		120		°C/W	Junction to cathode lead at 0.79 mm (0.031 in.) from body
V_F	Forward voltage		2.2	3.0	V	I_F = 10 mA
BV_R	Reverse breakdown voltage	5.0			V	I_R = 100 μA
η_v	Luminous efficacy		147		lm/W	Note 3

NOTES:

1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength that defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

(c)

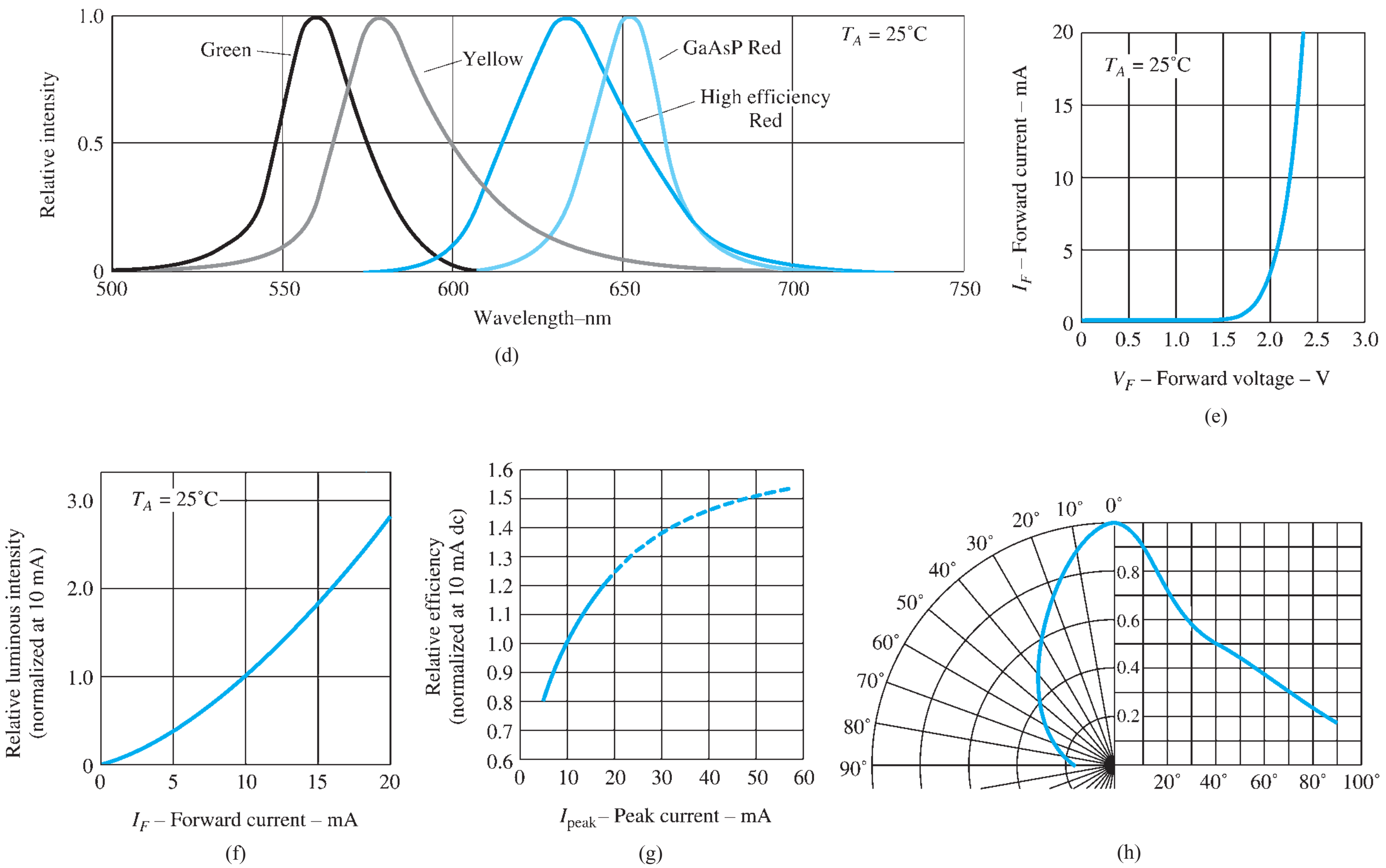
FIG. 1.52

Hewlett-Packard subminiature high-efficiency red solid-state lamp: (a) appearance; (b) absolute maximum ratings; (c) electrical/optical characteristics; (d) relative intensity versus wavelength; (e) forward current versus forward voltage; (f) relative luminous intensity versus forward current; (g) relative efficiency versus peak current; (h) relative luminous intensity versus angular displacement.

For instance, note in Fig. 1.52g that the increase in relative efficiency starts to level off as the current exceeds 50 mA.

The term *efficacy* is, by definition, a measure of the ability of a device to produce the desired effect. For the LED this is the ratio of the number of lumens generated per applied watt of electrical power.

The plot of Fig. 1.52d supports the information appearing on the eye-response curve of Fig. 1.51. As indicated above, note the bell-shaped curve for the range of wavelengths that will result in each color. The peak value of this device is near 630 nm, very close to the peak value of the GaAsP red LED. The curves of green and yellow are only provided for reference purposes.



(d)

(e)

(f)

(g)

(h)

FIG. 1.52
Continued.

Figure 1.52h is a graph of light intensity versus angle measured from 0° (head on) to 90° (side view). Note that at 40° the intensity has already dropped to 50% of the head-on intensity.

One of the major concerns when using an LED is the reverse-bias breakdown voltage, which is typically between 3 V and 5 V (an occasional device has a 10-V level).

This range of values is significantly less than that of a standard commercial diode, where it can extend to thousands of volts. As a result one has to be acutely aware of this severe limitation in the design process. In the next chapter one protective approach will be introduced.

In the analysis and design of networks with LEDs it is helpful to have some idea of the voltage and current levels to be expected.

For many years the only colors available were green, yellow, orange, and red, permitting the use of the average values of $V_F = 2$ V and $I_F = 20$ mA for obtaining an approximate operating level.

However, with the introduction of blue in the early 1990s and white in the late 1990s the magnitude of these two parameters has changed. For blue the average forward bias voltage can be as high as 5 V, and for white about 4.1 V, although both have a typical operating current of 20 mA or more. In general, therefore:

Assume an average forward-bias voltage of 5 V for blue and 4 V for white LEDs at currents of 20 mA to initiate an analysis of networks with these types of LEDs.

Every once in a while a device is introduced that seems to open the door to a slue of possibilities. Such is the case with the introduction of white LEDs. The slow start for white LEDs is primarily due to the fact that it is not a primary color like green, blue, and red. Every other color that one requires, such as on a TV screen, can be generated from these three colors (as in virtually all monitors available today). Yes, the right combination of these three colors can give white—hard to believe, but it works. The best evidence is the human eye, which only has cones sensitive to red, green, and blue. The brain is responsible for processing the input and perceiving the "white" light and color we see in our everyday lives. The same reasoning was used to generate some of the first white LEDs, by combining the right proportions of a red, a green, and a blue LED in a single package. Today, however, most white LEDs are constructed of a blue *gallium nitride* LED below a film *of yttrium-aluminum garnet* (YAG) phosphor. When the blue light hits the phosphor, a yellow light is generated. The mix of this yellow emission with that of the central blue LED forms a white light—incredible, but true.

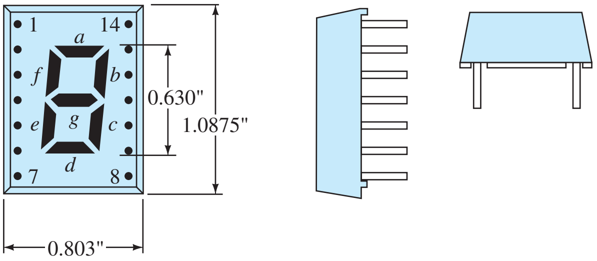
Since most of the lighting for homes and offices is white light, we now have another option to consider versus incandescent and fluorescent lighting. The rugged characteristics of LED white light along with lifetimes that exceed 25,000 hours, clearly suggest that this will be a true competitor in the near future. Various companies are now providing replacement LED bulbs for almost every possible application. Some have efficacy ratings as high as 135.7 lumens per watt, far exceeding the 25 lumens per watt of a few years ago. It is forecast that 7 W of power will soon be able to generate 1,000 lm of light, which exceeds the illumination of a 60 W bulb and can run off four D cell batteries. Imagine the same lighting with less than 1/8 the power requirement. At the present time entire offices, malls, street lighting, sporting facilities, and so on are being designed using solely LED lighting. Recently, LEDs are the common choice for flashlights and many high-end automobiles due to the sharp intensity at lower dc power requirements. The tube light of Fig. 1.53a replaces the standard fluorescent bulb typically found in the ceiling fixtures of both the home and industry. Not only do they draw 20% less energy while providing 25% additional light but they also last twice as long as a standard fluorescent bulb. The flood light of Fig. 1.53b draws 1.7 watts for each 140 lumens of light resulting in an enormous 90% savings in energy compared to the incandescent variety. The chandelier bulbs of Fig. 1.53c have a lifetime of 50,000 hours and only draw 3 watts of power while generating 200 lumens of light.

(a) (b) (c)

FIG. 1.53
LED residential and commercial lighting.

Before leaving the subject, let us look at a seven-segment digital display housed in a typical dual in-line integrated circuit package as shown in Fig. 1.54. By energizing the proper pins with a typical 5-V dc level, a number of the LEDs can be energized and the desired numeral displayed. In Fig. 1.54a the pins are defined by looking at the face of the display and counting counterclockwise from the top left pin. Most seven-segment displays are either common-anode or common-cathode displays, with the term *anode* referring to the defined positive side of each diode and the *cathode* referring to the negative side. For the common-cathode option the pins have the functions listed in Fig. 1.54b and appear as in Fig. 1.54c. In the common-cathode configuration all the cathodes are connected together to form a common point for the negative side of each LED. Any LED with a positive 5 V applied to the anode or numerically numbered pin side will turn on and produce light for that segment. In Fig. 1.54c, 5 V has been applied to the terminals that generate the numeral 5. For this particular unit the average forward turn-on voltage is 2.1 V at a current of 10 mA.

Various LED configurations are examined in the next chapter.

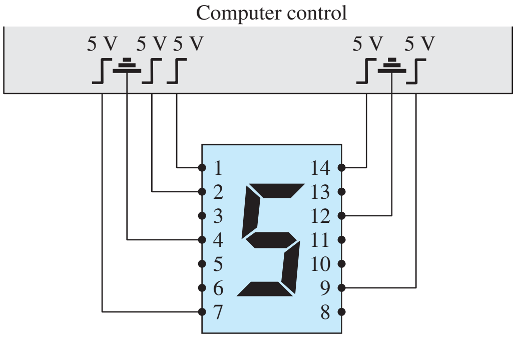


(a)

COMMON CATHODE

PIN #	FUNCTION
1.	Anode f
2.	ANODE g
3.	NO PIN
4.	COMMON CATHODE
5.	NO PIN
6.	ANODE e
7.	ANODE d
8.	ANODE c
9.	ANODE d
10.	NO PIN
11.	NO PIN
12.	COMMON CATHODE
13.	ANODE b
14.	ANODE a

(b)



(c)

FIG. 1.54

Seven-segment display: (a) face with pin idenfication; (b) pin function; (c) displaying the numeral 5.

1.17 SUMMARY

Important Conclusions and Concepts

1. The characteristics of an ideal diode are a close match with those of a **simple switch** except for the important fact that an ideal diode can **conduct in only one direction**.
2. The ideal diode is a **short** in the region of conduction and an **open circuit** in the region of nonconduction.
3. A semiconductor is a material that has a conductivity level somewhere **between** that of a good conductor and that of an insulator.
4. A bonding of atoms, strengthened by the **sharing of electrons** between neighboring atoms, is called covalent bonding.
5. Increasing temperatures can cause a **significant increase** in the number of free electrons in a semiconductor material.
6. Most semiconductor materials used in the electronics industry have **negative temperature coefficients**; that is, the resistance drops with an increase in temperature.
7. Intrinsic materials are those semiconductors that have a very **low level of impurities**, whereas extrinsic materials are semiconductors that have been **exposed to a doping process**.
8. An *n*-type material is formed by adding **donor** atoms that have **five** valence electrons to establish a high level of relatively free electrons. In an *n*-type material, the **electron is the majority carrier** and the hole is the minority carrier.
9. A *p*-type material is formed by adding **acceptor** atoms with **three** valence electrons to establish a high level of holes in the material. In a *p*-type material, the hole is the majority carrier and the electron is the minority carrier.
10. The region near the junction of a diode that has very few carriers is called the **depletion** region.
11. In the **absence** of any externally applied bias, the diode current is zero.
12. In the forward-bias region the diode current **increases exponentially** with increase in voltage across the diode.

13. In the reverse-bias region the diode current is the **very small reverse saturation current** until Zener breakdown is reached and current will flow in the opposite direction through the diode.
14. The reverse saturation current I_s will just about **double** in magnitude for every 10-fold increase in temperature.
15. The dc resistance of a diode is determined by the **ratio** of the diode voltage and current at the point of interest and is **not sensitive** to the shape of the curve. The dc resistance **decreases** with increase in diode current or voltage.
16. The ac resistance of a diode is sensitive to the shape of the curve in the region of interest and decreases for higher levels of diode current or voltage.
17. The threshold voltage is about **0.7 V** for silicon diodes and **0.3 V** for germanium diodes.
18. The maximum power dissipation level of a diode is equal to the **product** of the diode voltage and current.
19. The capacitance of a diode **increases exponentially** with increase in the forward-bias voltage. Its lowest levels are in the reverse-bias region.
20. The direction of conduction for a Zener diode is **opposite** to that of the arrow in the symbol, and the Zener voltage has a polarity opposite to that of a forward-biased diode.
21. Light emitting diodes (LEDs) emit light under **forward-bias conditions** but require 2 V to 4 V for good emission.

Equations

$$I_D = I_s(e^{V_D/nV_T} - 1) \qquad V_T = \frac{kT}{q} \qquad T_K = T_C + 273^\circ \qquad k = 1.38 \times 10^{-23}\ \text{J/K}$$

$$V_K \cong 0.7\ \text{V (Si)}$$

$$V_K \cong 1.2\ \text{V (GaAs)}$$

$$V_K \cong 0.3\ \text{V (Ge)}$$

$$R_D = \frac{V_D}{I_D}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\ \text{mV}}{I_D}$$

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}$$

$$P_{D_{\max}} = V_D I_D$$

1.18 COMPUTER ANALYSIS

Two software packages designed to analyze electronic circuits will be introduced and applied throughout the text. They include **Cadence OrCAD, version 16.3** (Fig. 1.55), and **Multisim, version 11.0.1** (Fig. 1.56). The content was written with sufficient detail to ensure that the reader will not need to reference any other computer literature to apply both programs.

NI Circuit Design Suite 11
NI Multisim • NI Ultiboard
Academic Edition
ni.com/academic/circuits
NATIONAL INSTRUMENTS

FIG. 1.55
Cadence OrCAD Design package version 16.3.
(Photo by Dan Trudden/Pearson.)

ELECTRONIC DESIGN SOFTWARE
cādence

FIG. 1.56
Multisim 11.0.1.
(Photo by Dan Trudden/Pearson.)

Those of you who have used either program in the past will find that the changes are minor and appear primarily in the front end and in the generation of specific data and plots.

The reason for including two programs stems from the fact that both are used throughout the educational community. You will find that the OrCAD software has a broader area of investigation but the Multisim software generates displays that are a better match to the actual laboratory experience.

The demo version of OrCAD is free from Cadence Design Systems, Inc., and can be downloaded directly from the EMA Design Automation, Inc., web site, **info@emaeda.com**. Multisim must be purchased from the **National Instruments Corporation** using their web site, **ni.com/multisim**.

In previous editions, the OrCAD package was referred to as a **PSpice** program primarily because it is a subset of a more sophisticated version used extensively in industry called **SPICE**. The result is the use of the term PSpice in the descriptions to follow when initiating an analysis using the OrCAD software.

The downloading process for each software package will now be introduced along with the general appearance of the resulting screen.

OrCAD

Installation:

Insert the **OrCAD Release 16.3** DVD into the disk drive to open the **Cadence OrCAD 16.3** software screen.

Select **Demo Installation** and the **Preparing Setup** dialog box will open, followed by the message **Welcome to the Installation Wizard for OrCAD 16.3 Demo**. Select **Next**, and the **License Agreement** dialog box opens. Choose **I accept** and select **Next**, and the **Choose Destination** dialog box will open with **Install OrCAD 16.3 Demo Accept C:\OrCAD\OrCAD_16.3 Demo.**

Select **Next**, and the **Start Copying Files** dialog box opens. Choose **Select** again, and the **Ready to Install Program** dialog box opens. Click **Install**, and the **Installing Crystal Report Xii** box will appear. The **Setup** dialog box opens with the prompt: **Setup status installs program**. The **Install Wizard** is now installing the OrCAD 16.3 Demo.

At completion, a message will appear: **Searching for and adding programs to the Windows firewall exception list. Generating indexes for Cadence Help. This may take some time.**

When the process has completed, select **Finish** and the **Cadence OrCAD 16.3** screen will appear. The software has been installed.

Screen Icon: The screen icon can be established (if it does not appear automatically) by applying the following sequence. **START-All Programs-Cadence-OrCAD 16.3 Demo-OrCAD Capture CIS Demo**, followed by a right-click of the mouse to obtain a listing where **Send to** is chosen, followed by **Desktop (create shortcut)**. The OrCAD icon will then appear on the screen and can be moved to the appropriate location.

Folder Creation: Starting with the OrCAD opening screen, right-click on the **Start** option at the bottom left of the screen. Then choose **Explore** followed by **Hard Drive (C:)**. Then place the mouse on the folder listing, and a right-click will result in a listing in which **New** is an option. Choose **New** followed by **Folder**, and then type in **OrCAD 11.3** in the provided area of the screen, followed by a right-click of the mouse. A location for all the files generated using OrCAD has now been established.

Multisim

Installation:

Insert the Multisim disk into the DVD disk drive to obtain the **Autoplay** dialog box.

Then select **Always do this for software and games**, followed by the selection of **Auto-run** to open the **NI Circuit Design Suite 11.0** dialog box.

Enter the full name to be used and provide the serial number. (The serial number appears in the Certificate of Ownership document that came with the NI Circuit Design Suite packet.)

Selecting **Next** will result in the **Destination Directory** dialog box from which one will **Accept** the following: **C:\Program Files(X86) National Instruments**. Select **Next** to open the **Features** dialog box and then select **NI Circuit Design Suite 11.0.1 Education.**

Selecting **Next** will result in the **Product Notification** dialog box with a succeeding **Next** resulting in the **License Agreement** dialog box. A left-click of the mouse on **I accept** can then be followed by choosing **Next** to obtain the **Start Installation** dialog box. Another left-click and the installation process begins, with the progress being displayed. The process takes between 15 and 20 minutes.

At the conclusion of the installation, you will be asked to install the **NI Elvismx driver DVD**. This time **Cancel** will be selected, and the **NI Circuit Design Suite 11.0.1** dialog box will appear with the following message: **NI Circuit Design Suite 11.0.1 has been installed.** Click **Finish**, and the response will be to restart the computer to complete the operation. Select **Restart**, and the computer will shut down and start up again, followed by the appearance of the **Multisim Screen** dialog box.

Select **Activate** and then **Activate through secure Internet connection**, and the **Activation Wizard** dialog box will open. Enter the **serial number** followed by **Next** to enter all the information into the **NI Activation Wizard** dialog box. Selecting **Next** will result in the option of **Send me an email confirmation of this activation**. Select this option and the message **Product successfully activated** will appear. Selecting **Finish** will complete the process.

Screen Icon: The process described for the OrCAD program will produce the same results for Multisim.

Folder Creation: Following the procedure introduced above for the OrCAD program, a folder labeled OrCAD 16.3 was established for the Multisim files.

The computer section of the next chapter will cover the details of opening both the OrCAD and Multisim analysis packages, setting up a specific circuit, and generating a variety of results.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

1.3 Covalent Bonding and Intrinsic Materials

1. Sketch the atomic structure of copper and discuss why it is a good conductor and how its structure is different from that of germanium, silicon, and gallium arsenide.
2. In your own words, define an intrinsic material, a negative temperature coefficient, and covalent bonding.
3. Consult your reference library and list three materials that have a negative temperature coefficient and three that have a positive temperature coefficient.

1.4 Energy Levels

4. **a.** How much energy in joules is required to move a charge of $12\ \mu\text{C}$ through a difference in potential of 6 V?
   b. For part (a), find the energy in electron-volts.
5. If 48 eV of energy is required to move a charge through a potential difference of 3.2 V, determine the charge involved.
6. Consult your reference library and determine the level of E_g for GaP, ZnS, and GaAsP, three semiconductor materials of practical value. In addition, determine the written name for each material.

1.5 *n*-Type and *p*-Type Materials

7. Describe the difference between *n*-type and *p*-type semiconductor materials.
8. Describe the difference between donor and acceptor impurities.
9. Describe the difference between majority and minority carriers.

C9
J3
J4
DC11
RA3

10. Sketch the atomic structure of silicon and insert an impurity of arsenic as demonstrated for silicon in Fig. 1.7.

11. Repeat Problem 10, but insert an impurity of indium.

12. Consult your reference library and find another explanation of hole versus electron flow. Using both descriptions, describe in your own words the process of hole conduction.

1.6 Semiconductor Diode

13. Describe in your own words the conditions established by forward- and reverse-bias conditions on a *p–n* junction diode and how the resulting current is affected.

14. Describe how you will remember the forward- and reverse-bias states of the *p–n* junction diode. That is, how will you remember which potential (positive or negative) is applied to which terminal?

15. **a.** Determine the thermal voltage for a diode at a temperature of 20°C.
b. For the same diode of part (a), find the diode current using Eq. 1.2 if $I_s = 40$ nA, $n = 2$ (low value of V_D), and the applied bias voltage is 0.5 V.

16. Repeat Problem 15 for $T = 100°\text{C}$ (boiling point of water). Assume that I_s has increased to 5.0 μA.

17. **a.** Using Eq. (1.2), determine the diode current at 20°C for a silicon diode with $n = 2$, $I_s = 0.1$ μA at a reverse-bias potential of -10 V.
b. Is the result expected? Why?

18. Given a diode current of 8 mA and $n = 1$, find I_s if the applied voltage is 0.5 V and the temperature is room temperature (25°C).

***19.** Given a diode current of 6 mA, $V_T = 26$ mV, $n = 1$, and $I_s = 1$ nA, find the applied voltage V_D.

20. **a.** Plot the function $y = e^x$ for x from 0 to 10. Why is it difficult to plot?
b. What is the value of $y = e^x$ at $x = 0$?
c. Based on the results of part (b), why is the factor -1 important in Eq. (1.2)?

21. In the reverse-bias region the saturation current of a silicon diode is about 0.1 μA ($T = 20°\text{C}$). Determine its approximate value if the temperature is increased 40°C.

22. Compare the characteristics of a silicon and a germanium diode and determine which you would prefer to use for most practical applications. Give some details. Refer to a manufacturer's listing and compare the characteristics of a germanium and a silicon diode of similar maximum ratings.

23. Determine the forward voltage drop across the diode whose characteristics appear in Fig. 1.19 at temperatures of $-75°\text{C}$, 25°C, 125°C and a current of 10 mA. For each temperature, determine the level of saturation current. Compare the extremes of each and comment on the ratio of the two.

1.7 Ideal versus Practical

24. Describe in your own words the meaning of the word *ideal* as applied to a device or a system.

25. Describe in your own words the characteristics of the *ideal* diode and how they determine the on and off states of the device. That is, describe why the short-circuit and open-circuit equivalents are appropriate.

26. What is the one important difference between the characteristics of a simple switch and those of an ideal diode?

1.8 Resistance Levels

27. Determine the static or dc resistance of the commercially available diode of Fig. 1.15 at a forward current of 4 mA.

28. Repeat Problem 27 at a forward current of 15 mA and compare results.

29. Determine the static or dc resistance of the commercially available diode of Fig. 1.15 at a reverse voltage of -10 V. How does it compare to the value determined at a reverse voltage of -30 V?

30. Calculate the dc and ac resistances for the diode of Fig. 1.15 at a forward current of 10 mA and compare their magnitudes.

31. **a.** Determine the dynamic (ac) resistance of the commercially available diode of Fig. 1.15 at a forward current of 10 mA using Eq. (1.5).
b. Determine the dynamic (ac) resistance of the diode of Fig. 1.15 at a forward current of 10 mA using Eq. (1.6).
c. Compare solutions of parts (a) and (b).

32. Using Eq. (1.5), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.15. Compare the solutions and develop a general conclusion regarding the ac resistance and increasing levels of diode current.

33. Using Eq. (1.6), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.15. Modify the equation as necessary for low levels of diode current. Compare to the solutions obtained in Problem 32.

34. Determine the average ac resistance for the diode of Fig. 1.15 for the region between 0.6 V and 0.9 V.

35. Determine the ac resistance for the diode of Fig. 1.15 at 0.75 V and compare it to the average ac resistance obtained in Problem 34.

1.9 Diode Equivalent Circuits

36. Find the piecewise-linear equivalent circuit for the diode of Fig. 1.15. Use a straight-line segment that intersects the horizontal axis at 0.7 V and best approximates the curve for the region greater than 0.7 V.

37. Repeat Problem 36 for the diode of Fig. 1.27.

38. Find the piecewise-linear equivalent circuit for the germanium and gallium arsenide diodes of Fig. 1.18.

1.10 Transition and Diffusion Capacitance

***39.** **a.** Referring to Fig. 1.33, determine the transition capacitance at reverse-bias potentials of -25 V and -10 V. What is the ratio of the change in capacitance to the change in voltage?

b. Repeat part (a) for reverse-bias potentials of -10 V and -1 V. Determine the ratio of the change in capacitance to the change in voltage.

c. How do the ratios determined in parts (a) and (b) compare? What does this tell you about which range may have more areas of practical application?

40. Referring to Fig. 1.33, determine the diffusion capacitance at 0 V and 0.25 V.

41. Describe in your own words how diffusion and transition capacitances differ.

42. Determine the reactance offered by a diode described by the characteristics of Fig. 1.33 at a forward potential of 0.2 V and a reverse potential of -20 V if the applied frequency is 6 MHz.

43. The no-bias transition capacitance of a silicon diode is 8 pF with $V_K = 0.7$ V and $n = 1/2$. What is the transition capacitance if the applied reverse bias potential is 5 V?

44. Find the applied reverse bias potential if the transition capacitance of a silicon diode is 4 pF but the no-bias level is 10 pF with $n = 1/3$ and $V_K = 0.7$ V.

1.11 Reverse Recovery Time

45. Sketch the waveform for i of the network of Fig. 1.57 if $t_t = 2t_s$ and the total reverse recovery time is 9 ns.

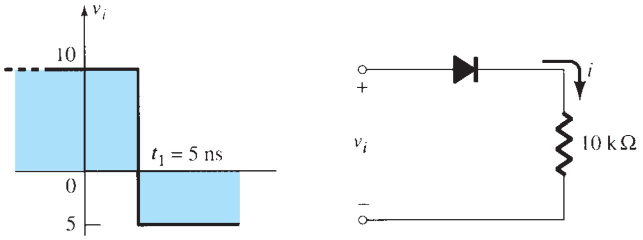


FIG. 1.57
Problem 45.

1.12 Diode Specification Sheets

***46.** Plot I_F versus V_F using linear scales for the diode of Fig. 1.37. Note that the provided graph employs a log scale for the vertical axis (log scales are covered in Sections 9.2 and 9.3).

47. **a.** Comment on the change in capacitance level with increase in reverse-bias potential for the diode of Fig. 1.37.

b. What is the level of $C(0)$?

c. Using $V_K = 0.7$ V, find the level of n in Eq. 1.9.

48. Does the reverse saturation current of the diode of Fig. 1.37 change significantly in magnitude for reverse-bias potentials in the range -25 V to -100 V?

***49.** For the diode of Fig. 1.37 determine the level of I_R at room temperature (25°C) and the boiling point of water (100°C). Is the change significant? Does the level just about double for every 10°C increase in temperature?

50. For the diode of Fig. 1.37, determine the maximum ac (dynamic) resistance at a forward current of 0.1, 1.5, and 20 mA. Compare levels and comment on whether the results support conclusions derived in earlier sections of this chapter.

51. Using the characteristics of Fig. 1.37, determine the maximum power dissipation levels for the diode at room temperature (25°C) and 100°C. Assuming that V_F remains fixed at 0.7 V, how has the maximum level of I_F changed between the two temperature levels?

52. Using the characteristics of Fig. 1.37, determine the temperature at which the diode current will be 50% of its value at room temperature (25°C).

1.15 Zener Diodes

53. The following characteristics are specified for a particular Zener diode: $V_Z = 29$ V, $V_R = 16.8$ V, $I_{ZT} = 10$ mA, $I_R = 20\ \mu$A, and $I_{ZM} = 40$ mA. Sketch the characteristic curve in the manner displayed in Fig. 1.47.

***54.** At what temperature will the 10-V Zener diode of Fig. 1.47 have a nominal voltage of 10.75 V? (*Hint:* Note the data in Table 1.7.)

55. Determine the temperature coefficient of a 5-V Zener diode (rated 25°C value) if the nominal voltage drops to 4.8 V at a temperature of 100°C.

56. Using the curves of Fig. 1.48a, what level of temperature coefficient would you expect for a 20-V diode? Repeat for a 5-V diode. Assume a linear scale between nominal voltage levels and a current level of 0.1 mA.

57. Determine the dynamic impedance for the 24-V diode at $I_Z = 10$ mA for Fig. 1.48b. Note that it is a log scale.

***58.** Compare the levels of dynamic impedance for the 24-V diode of Fig. 1.48b at current levels of 0.2, 1, and 10 mA. How do the results relate to the shape of the characteristics in this region?

1.16 Light-Emitting Diodes

59. Referring to Fig. 1.52e, what would appear to be an appropriate value of V_K for this device? How does it compare to the value of V_K for silicon and germanium?

60. Given that $E_g = 0.67$ eV for germanium, find the wavelength of peak solar response for the material. Do the photons at this wavelength have a lower or higher energy level?

61. Using the information provided in Fig. 1.52, determine the forward voltage across the diode if the relative luminous intensity is 1.5.

***62.** **a.** What is the percentage increase in relative efficiency of the device of Fig. 1.52 if the peak current is increased from 5 mA to 10 mA?
  b. Repeat part (a) for 30 mA to 35 mA (the same increase in current).
  c. Compare the percentage increase from parts (a) and (b). At what point on the curve would you say there is little to be gained by further increasing the peak current?

63. **a.** If the luminous intensity at 0° angular displacement is 3.0 mcd for the device of Fig. 1.52, at what angle will it be 0.75 mcd?
  b. At what angle does the loss of luminous intensity drop below the 50% level?

***64.** Sketch the current derating curve for the average forward current of the high-efficiency red LED of Fig. 1.52 as determined by temperature. (Note the absolute maximum ratings.)

2

Diode Applications

CHAPTER OBJECTIVES

- Understand the concept of load-line analysis and how it is applied to diode networks.
- Become familiar with the use of equivalent circuits to analyze series, parallel, and series-parallel diode networks.
- Understand the process of rectification to establish a dc level from a sinusoidal ac input.
- Be able to predict the output response of a clipper and clamper diode configuration.
- Become familiar with the analysis of and the range of applications for Zener diodes.

2.1 INTRODUCTION

The construction, characteristics, and models of semiconductor diodes were introduced in Chapter 1. This chapter will develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application. By chapter's end, the fundamental behavior pattern of diodes in dc and ac networks should be clearly understood. The concepts learned in this chapter will have significant carryover in the chapters to follow. For instance, diodes are frequently employed in the description of the basic construction of transistors and in the analysis of transistor networks in the dc and ac domains.

This chapter demonstrates an interesting and very useful aspect of the study of a field such as electronic devices and systems:

Once the basic behavior of a device is understood, its function and response in an infinite variety of configurations can be examined.

In other words, now that we have a basic knowledge of the characteristics of a diode along with its response to applied voltages and currents, we can use this knowledge to examine a wide variety of networks. There is no need to reexamine the response of the device for each application.

In general:

The analysis of electronic circuits can follow one of two paths: using the actual characteristics or applying an approximate model for the device.

For the diode the initial discussion will include the actual characteristics to clearly demonstrate how the characteristics of a device and the network parameters interact. Once there is confidence in the results obtained, the approximate piecewise model will be employed to verify the results found using the complete characteristics. It is important that the role and the response of various elements of an electronic system be understood without continually having to resort to lengthy mathematical procedures. This is usually accomplished through the approximation process, which can develop into an art itself. Although the results obtained using the actual characteristics may be slightly different from those obtained using a series of approximations, keep in mind that the characteristics obtained from a specification sheet may be slightly different from those of the device in actual use. In other words, for example, the characteristics of a 1N4001 semiconductor diode may vary from one element to the next in the same lot. The variation may be slight, but it will often be sufficient to justify the approximations employed in the analysis. Also consider the other elements of the network: Is the resistor labeled 100 Ω exactly 100 Ω? Is the applied voltage exactly 10 V or perhaps 10.08 V? All these tolerances contribute to the general belief that a response determined through an appropriate set of approximations can often be "as accurate" as one that employs the full characteristics. In this book the emphasis is toward developing a working knowledge of a device through the use of appropriate approximations, thereby avoiding an unnecessary level of mathematical complexity. Sufficient detail will normally be provided, however, to permit a detailed mathematical analysis if desired.

2.2 LOAD-LINE ANALYSIS

The circuit of Fig. 2.1 is the simplest of diode configurations. It will be used to describe the analysis of a diode circuit using its actual characteristics. In the next section we will replace the characteristics by an approximate model for the diode and compare solutions. Solving the circuit of Fig. 2.1 is all about finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

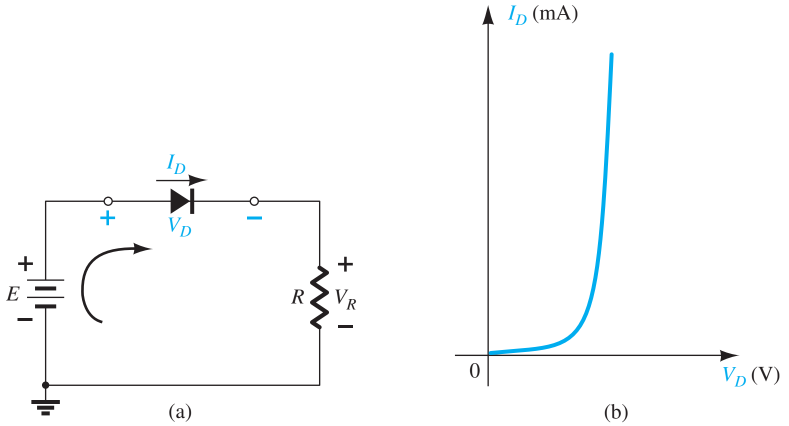


FIG. 2.1

Series diode configuration: (a) circuit; (b) characteristics.

In Fig. 2.2 the diode characteristics are placed on the same set of axes as a straight line defined by the parameters of the network. The straight line is called a *load line* because the intersection on the vertical axis is defined by the applied load R. The analysis to follow is therefore called *load-line analysis.* The intersection of the two curves will define the solution for the network and define the current and voltage levels for the network.

Before reviewing the details of drawing the load line on the characteristics, we need to determine the expected response of the simple circuit of Fig. 2.1. Note in Fig. 2.1 that the effect of the "pressure" established by the dc supply is to establish a conventional current in the direction indicated by the clockwise arrow. The fact that the direction of this current has the same direction as the arrow in the diode symbol reveals that the diode is in the "on" state and will conduct a high level of current. The polarity of the applied voltage has resulted in a forward-bias situation. With the current direction established, the polarities for the voltage across the diode and resistor can be superimposed. The polarity of V_D and the direction of I_D clearly reveal that the diode is indeed in the forward-bias state, resulting in a voltage across the diode in the neighborhood of 0.7 V and a current on the order of 10 mA or more.

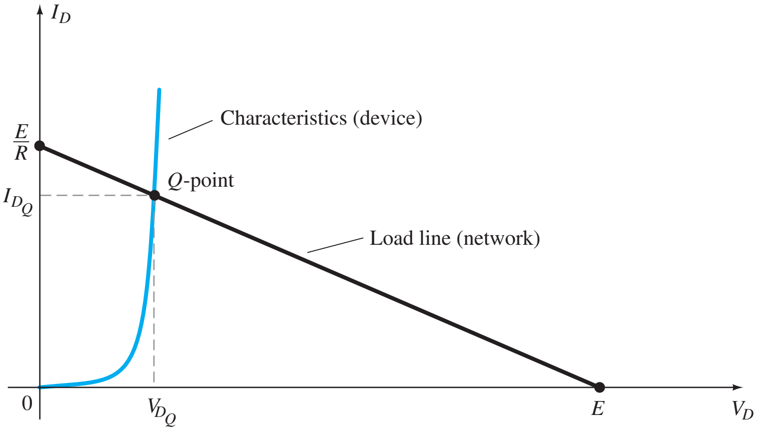


FIG. 2.2
Drawing the load line and finding the point of operation.

The intersections of the load line on the characteristics of Fig. 2.2 can be determined by first applying Kirchhoff's voltage law in the clockwise direction, which results in

$$+E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1), V_D and I_D, are the same as the diode axis variables of Fig. 2.2. This similarity permits plotting Eq. (2.1) on the same characteristics of Fig. 2.2.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\text{ V} + I_D R \end{aligned}$$

and

$$\boxed{I_D = \frac{E}{R}\bigg|_{V_D = 0\text{ V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\text{ A})R \end{aligned}$$

and

$$\boxed{V_D = E\big|_{I_D = 0\text{ A}}} \tag{2.3}$$

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of operation for this circuit. By simply drawing a line down to the horizontal axis, we can determine the diode voltage V_{D_Q}, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}. The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "*Q*-point") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same as would be obtained by a simultaneous mathematical solution of

$$I_D = \frac{E}{R} - \frac{V_D}{R} \qquad \left[\text{derived from Eq. (2.1)}\right]$$

and $$I_D = I_s(e^{V_D/nV_T} - 1)$$

Since the curve for a diode has nonlinear characteristics, the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_Q} and I_{D_Q} were obtained. The next example demonstrates the techniques introduced above and reveals the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

a. V_{D_Q} and I_{D_Q}.
b. V_R.

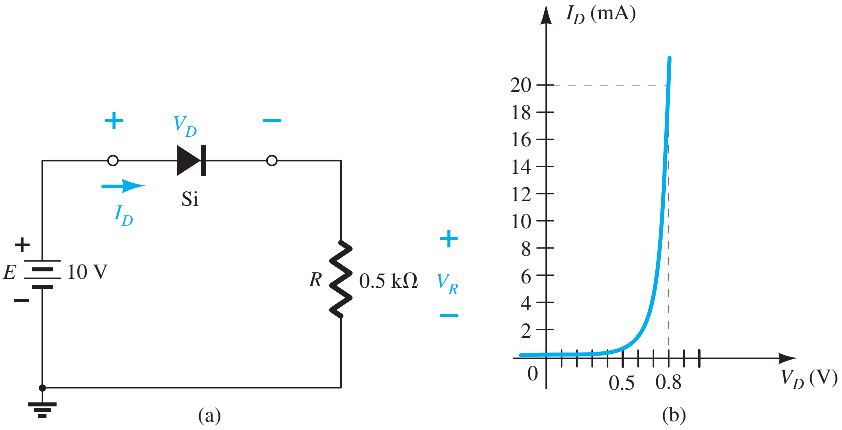


FIG. 2.3
(a) Circuit; (b) characteristics.

Solution:

a. Eq. (2.2): $$I_D = \frac{E}{R}\bigg|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$$

Eq. (2.3): $$V_D = E\big|_{I_D=0\text{ A}} = 10\text{ V}$$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$
$$I_{D_Q} \cong \mathbf{18.5\text{ mA}}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

As noted in the example above,

the load line is determined solely by the applied network, whereas the characteristics are defined by the chosen device.

Changing the model we use for the diode will not disturb the network so the load line to be drawn will be exactly the same as appearing in the example above.

Since the network of Example 2.1 is a dc network the Q-point of Fig.2.4 will remain fixed with $V_{D_Q} = 0.78$ V and $I_{D_Q} = 18.5$ mA. In Chapter 1 a dc resistance was defined at any point on the characteristics by $R_{DC} = V_D/I_D$.

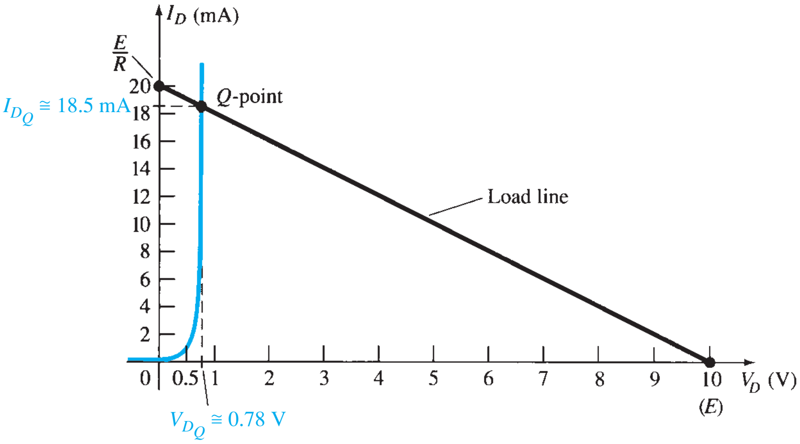


FIG. 2.4

Solution to Example 2.1.

Using the Q-point values, the dc resistance for Example 2.1 is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.78\text{ V}}{18.5\text{ mA}} = 42.16\ \Omega$$

An equivalent network (for these operating conditions only) can then be drawn as shown in Fig. 2.5.

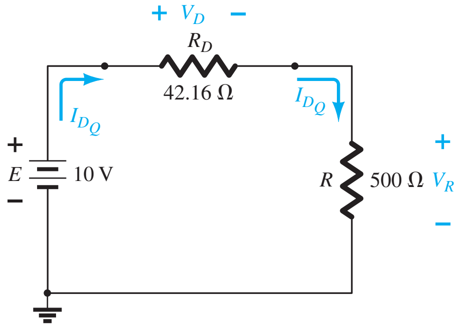


FIG. 2.5

Network quivalent to Fig. 2.4.

The current

$$I_D = \frac{E}{R_D + R} = \frac{10\text{ V}}{42.16\ \Omega + 500\ \Omega} = \frac{10\text{ V}}{542.16\ \Omega} \cong \mathbf{18.5\ mA}$$

and
$$V_R = \frac{RE}{R_D + R} = \frac{(500\ \Omega)(10\text{ V})}{42.16\ \Omega + 500\ \Omega} = \mathbf{9.22\ V}$$

matching the results of Example 2.1.

In essence, therefore, once a dc Q-point has been determined the diode can be replaced by its dc resistance equivalent. This concept of replacing a characteristic by an equivalent model is an important one and will be used when we consider ac inputs and equivalent models for transistors in the chapters to follow. Let us now see what effect different equivalent models for the diode will have on the response in Example 2.1

EXAMPLE 2.2 Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution: The load line is redrawn as shown in Fig. 2.6 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting Q-point is

$$V_{D_Q} = \mathbf{0.7\ V}$$
$$I_{D_Q} = \mathbf{18.5\ mA}$$

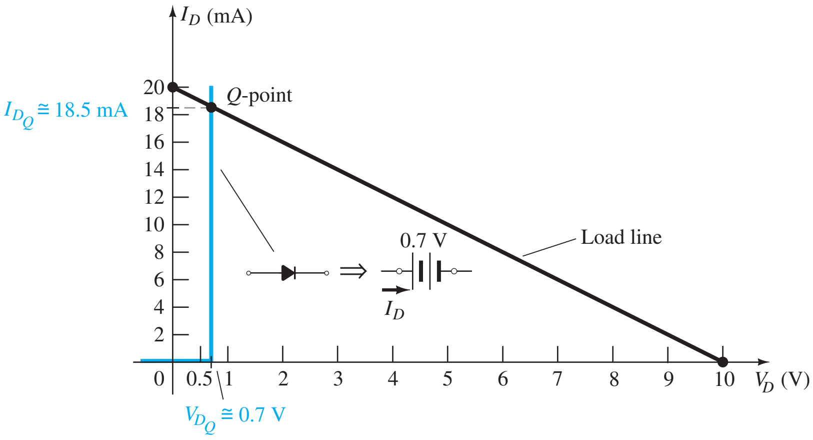


FIG. 2.6

Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.2 are quite interesting. The level of I_{D_Q} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The $V_D = 0.7$ V here and the 0.78 V from Example 2.1 are of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

For this situation the dc resistance of the Q-point is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.7\text{ V}}{18.5\text{ mA}} = 37.84\ \Omega$$

which is still relatively close to that obtained for the full characteristics.

In the next example we go a step further and substitute the ideal model. The results will reveal the conditions that must be satisfied to apply the ideal equivalent properly.

EXAMPLE 2.3 Repeat Example 2.1 using the ideal diode model.

Solution: As shown in Fig. 2.7, the load line is the same, but the ideal characteristics now intersect the load line on the vertical axis. The Q-point is therefore defined by

$$V_{D_Q} = \mathbf{0\ V}$$
$$I_{D_Q} = \mathbf{20\ mA}$$

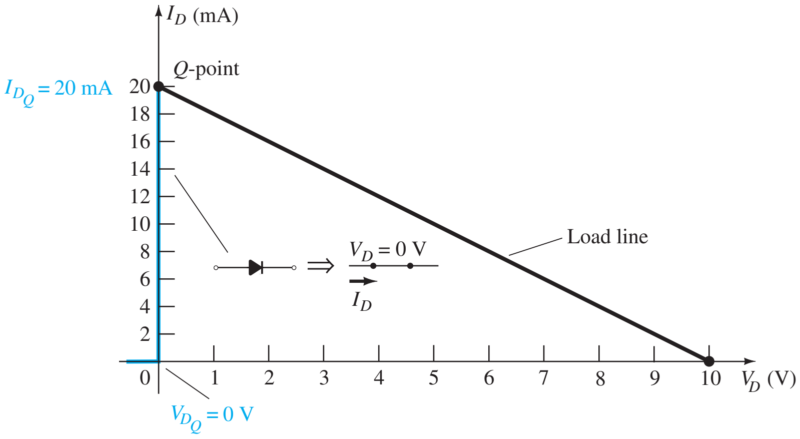


FIG. 2.7

Solution to Example 2.1 using the ideal diode model.

The results are sufficiently different from the solutions of Example 2.1 to cause some concern about their accuracy. Certainly, they do provide some indication of the level of voltage and current to be expected relative to the other voltage levels of the network, but the additional effort of simply including the 0.7-V offset suggests that the approach of Example 2.2 is more appropriate.

Use of the ideal diode model therefore should be reserved for those occasions when the role of a diode is more important than voltage levels that differ by tenths of a volt and in those situations where the applied voltages are considerably larger than the threshold voltage V_K. In the next few sections the approximate model will be employed exclusively since the voltage levels obtained will be sensitive to variations that approach V_K. In later sections the ideal model will be employed more frequently since the applied voltages will frequently be quite a bit larger than V_K and the authors want to ensure that the role of the diode is correctly and clearly understood.

In this case,

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0\text{ V}}{20\text{ mA}} = 0\ \Omega \text{ (or a short-circuit equivalent)}$$

2.3 SERIES DIODE CONFIGURATIONS

In the last section we found that the results obtained using the approximate piecewise-linear equivalent model were quite close, if not equal, to the response obtained using the full characteristics. In fact, if one considers all the variations possible due to tolerances, temperature, and so on, one could certainly consider one solution to be "as accurate" as the other. Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified. Recall the following:

The primary purpose of this text is to develop a general knowledge of the behavior, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.

For all the analysis to follow in this chapter it is assumed that

The forward resistance of the diode is usually so small compared to the other series elements of the network that it can be ignored.

This is a valid approximation for the vast majority of applications that employ diodes. Using this fact will result in the approximate equivalents for a silicon diode and an ideal diode that appear in Table 2.1. For the conduction region the only difference between the silicon diode and the ideal diode is the vertical shift in the characteristics, which is accounted for in the equivalent model by a dc supply of 0.7 V opposing the direction of forward current through the device. For voltages less than 0.7 V for a silicon diode and 0 V for the ideal diode the resistance is so high compared to other elements of the network that its equivalent is the open circuit.

For a Ge diode the offset voltage is 0.3 V and for a GaAs diode it is 1.2 V. Otherwise the equivalent networks are the same. For each diode the label Si, Ge, or GaAs will appear along with the diode symbol. For networks with ideal diodes the diode symbol will appear as shown in Table 2.1 without any labels.

The approximate models will now be used to investigate a number of series diode configurations with dc inputs. This will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

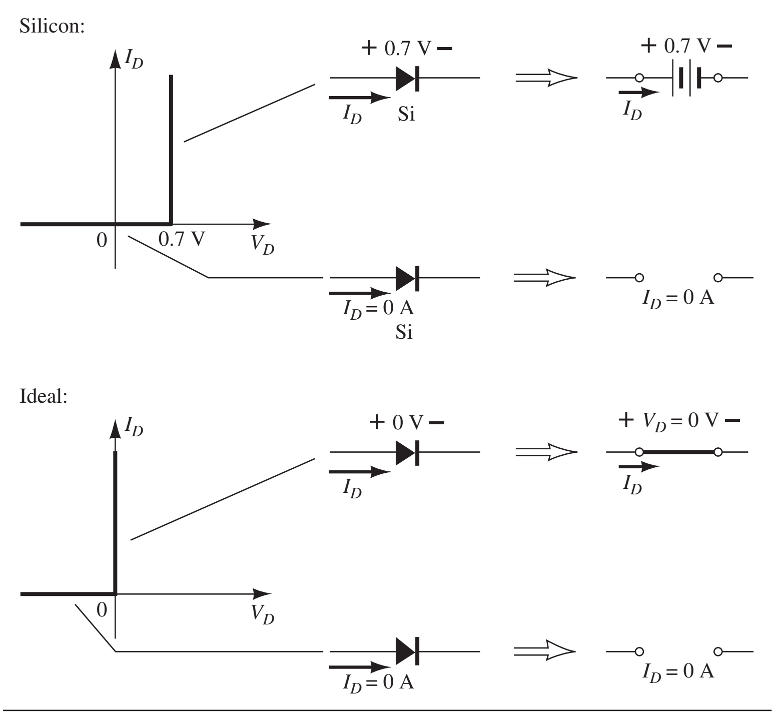
For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon, $V_D \geq 0.3$ V for germanium, and $V_D \geq 1.2$ V for gallium arsenide.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting

TABLE 2.1

Approximate and Ideal Semiconductor Diode Models.



direction is a “match” with the arrow in the diode symbol, conduction through the diode will occur and the device is in the “on” state. The description above is, of course, contingent on the supply having a voltage greater than the “turn-on” voltage (V_K) of each diode.

If a diode is in the “on” state, one can either place a 0.7-V drop across the element or redraw the network with the V_K equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each “on” diode and to draw a diagonal line through each diode in the “off” or open state. Initially, however, the substitution method will be used to ensure that the proper voltage and current levels are determined.

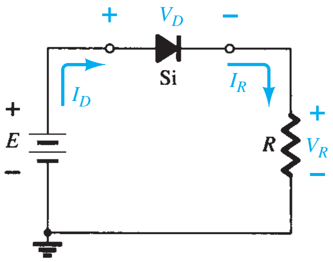


FIG. 2.8

Series diode configuration.

The series circuit of Fig. 2.8 described in some detail in Section 2.2 will be used to demonstrate the approach described in the above paragraphs. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.9a. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_K$, the diode is in the “on” state. The network is then redrawn as shown in Fig. 2.9b with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

$$\boxed{V_D = V_K} \tag{2.4}$$

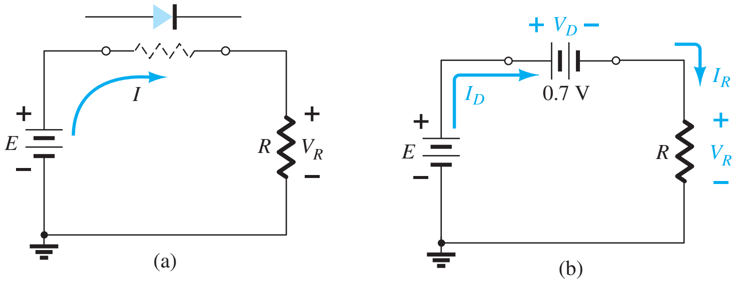


FIG. 2.9

(a) Determining the state of the diode of Fig. 2.8; (b) substituting the equivalent model for the “on” diode of Fig. 2.9a.

$$\boxed{V_R = E - V_K} \tag{2.5}$$

$$\boxed{I_D = I_R = \frac{V_R}{R}} \tag{2.6}$$

In Fig. 2.10 the diode of Fig. 2.7 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.11 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.12. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\ V}$$

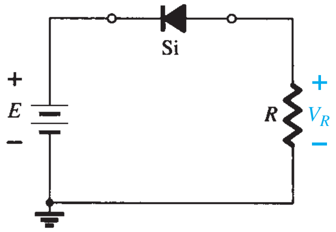


FIG. 2.10
Reversing the diode of Fig. 2.8.

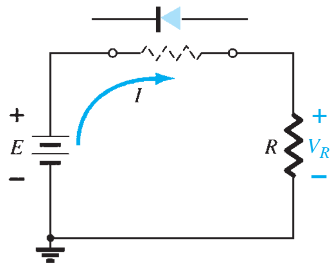


FIG. 2.11
Determining the state of the diode of Fig. 2.10.

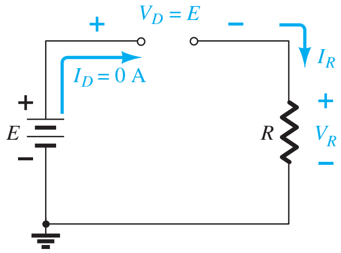


FIG. 2.12
Substituting the equivalent model for the "off" diode of Fig. 2.10.

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13, determine V_D, V_R, and I_D.

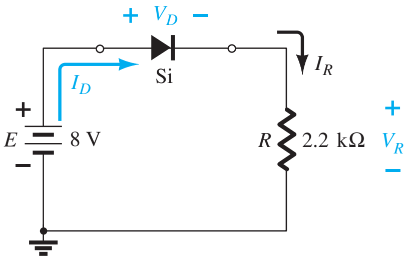


FIG. 2.13
Circuit for Example 2.4.

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\ V}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = \mathbf{7.3\ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{3.32\ mA}$$

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.14, where $I_D = \mathbf{0\ A}$ due to the open circuit. Since $V_R = I_R R$, we have $V_R = (0)R = \mathbf{0\ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = 8\ \text{V}$$

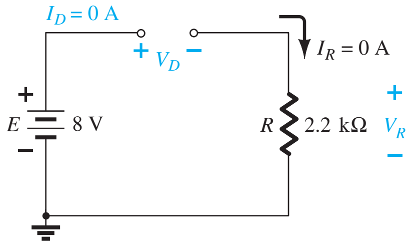


FIG. 2.14
Determining the unknown quantities for Example 2.5.

In particular, note in Example 2.5 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

An open circuit can have any voltage across its terminals, but the current is always 0 A.

A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.15 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

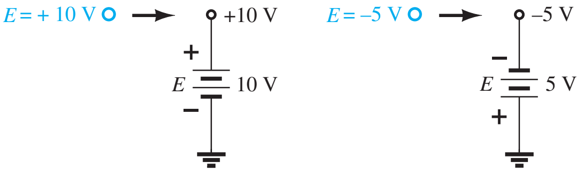


FIG. 2.15
Source notation.

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

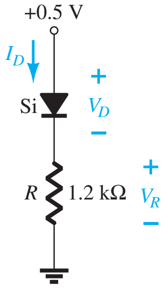


FIG. 2.16
Series diode circuit for Example 2.6.

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})\,1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

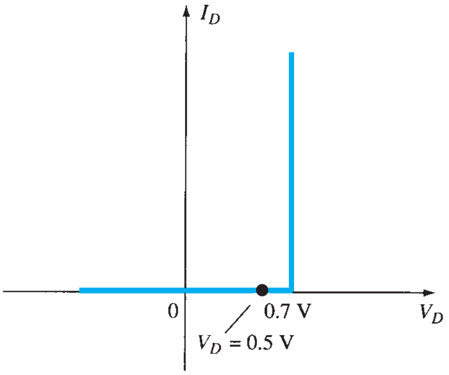


FIG. 2.17
Operating point with E = 0.5 V.

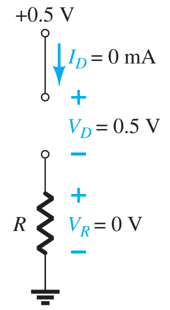


FIG. 2.18
Determining I_D, V_R, and V_D for the circuit of Fig. 2.16.

EXAMPLE 2.7 Determine V_o and I_D for the series circuit of Fig. 2.19.

Solution: An attack similar to that applied in Example 2.4 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.20 results because $E = 12\text{ V} > (0.7\text{ V} + 1.8\text{ V [Table 1.8]}) = 2.5\text{ V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 680-Ω resistor. The resulting voltage is

$$V_o = E - V_{K_1} - V_{K_2} = 12\text{ V} - 2.5\text{ V} = \mathbf{9.5\text{ V}}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\text{ V}}{680\ \Omega} = \mathbf{13.97\text{ mA}}$$

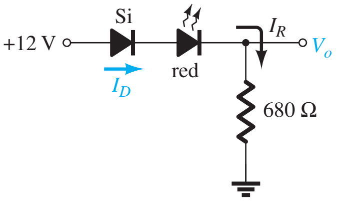


FIG. 2.19
Circuit for Example 2.7.

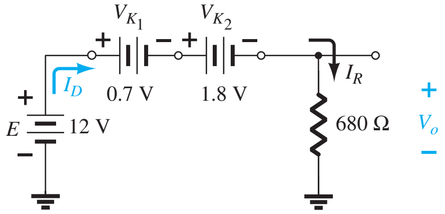


FIG. 2.20
Determining the unknown quantities for Example 2.7.

EXAMPLE 2.8 Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.21.

Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22. There is a match in current direction for one silicon diode but not for the other silicon diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\text{ A}}$, as shown in Fig. 2.23.

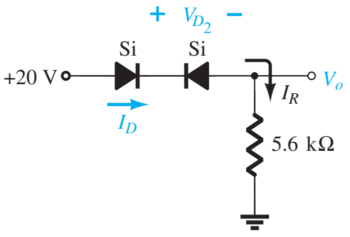


FIG. 2.21
Circuit for Example 2.8.

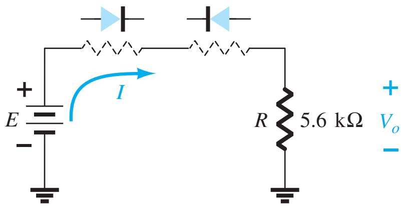


FIG. 2.22
Determining the state of the diodes of Fig. 2.21.

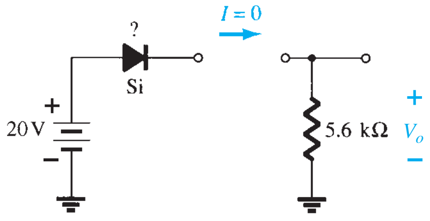


FIG. 2.23
Substituting the equivalent state for the open diode.

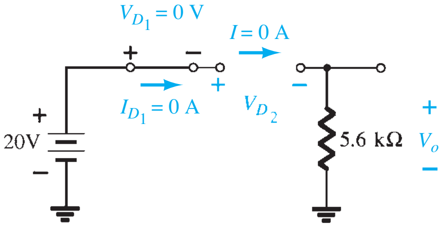


FIG. 2.24
Determining the unknown quantities for the circuit of Example 2.8.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.24. We have

$$V_o = I_R R = I_D R = (0\text{ A})R = \mathbf{0\ V}$$

and
$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{20\ V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and
$$V_{D_2} = E - V_{D_1} - V_o = 20\text{ V} - 0 - 0$$
$$= \mathbf{20\ V}$$

with
$$V_o = \mathbf{0\ V}$$

EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

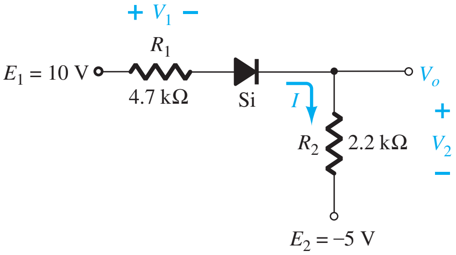


FIG. 2.25
Circuit for Example 2.9.

Solution: The sources are drawn and the current direction indicated as shown in Fig. 2.26. The diode is in the "on" state and the notation appearing in Fig. 2.27 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V on the figure. This eliminates the need to redraw the network and avoids any confusion that may

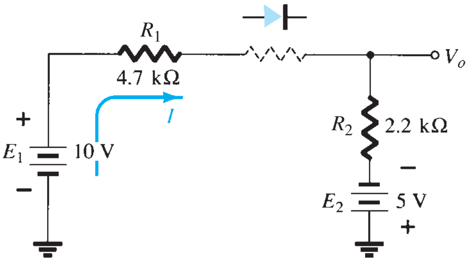


FIG. 2.26
Determining the state of the diode for the network of Fig. 2.25.

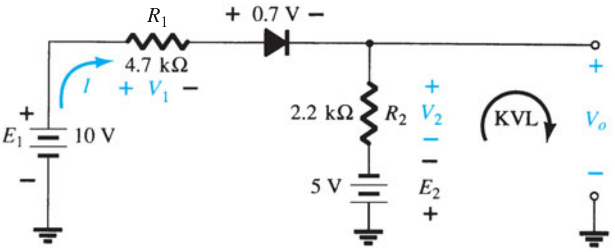


FIG. 2.27
Determining the unknown quantities for the network of Fig. 2.25. KVL, Kirchhoff voltage loop.

result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$
$$\cong \mathbf{2.07\text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.07\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.73\text{ V}}$$
$$V_2 = IR_2 = (2.07\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.55\text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction results in

$$-E_2 + V_2 - V_o = 0$$

and $$V_o = V_2 - E_2 = 4.55\text{ V} - 5\text{ V} = \mathbf{-0.45\text{ V}}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.25.

2.4 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.3 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.10 Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.28.

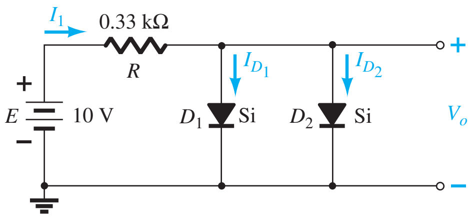


FIG. 2.28
Network for Example 2.10.

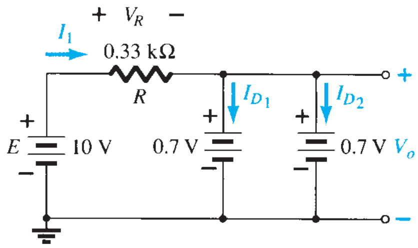


FIG. 2.29
Determining the unknown quantities for the network of Example 2.10.

Solution: For the applied voltage the "pressure" of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\text{ V}}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

This example demonstrates one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.28 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.28. By placing two in parallel, we limit the current to a safe value of 14.09 mA with the same terminal voltage.

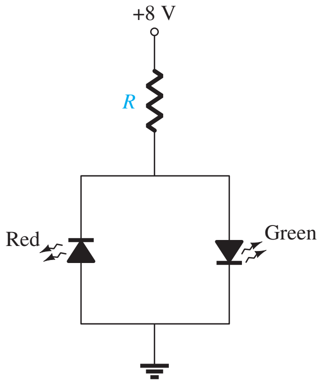


FIG. 2.30
Network for Example 2.11.

EXAMPLE 2.11 In this example there are two LEDs that can be used as a polarity detector. Apply a positive source voltage and a green light results. Negative supplies result in a red light. Packages of such combinations are commercially available.

Find the resistor R to ensure a current of 20 mA through the "on" diode for the configuration of Fig. 2.30. Both diodes have a reverse breakdown voltage of 3 V and an average turn-on voltage of 2 V.

Solution: The application of a positive supply voltage results in a conventional current that matches the arrow of the green diode and turns it on.

The polarity of the voltage across the green diode is such that it reverse biases the red diode by the same amount. The result is the equivalent network of Fig. 2.31.

Applying Ohm's law, we obtain

$$I = 20\text{ mA} = \frac{E - V_{\text{LED}}}{R} = \frac{8\text{ V} - 2\text{ V}}{R}$$

and

$$R = \frac{6\text{ V}}{20\text{ mA}} = \mathbf{300\ \Omega}$$

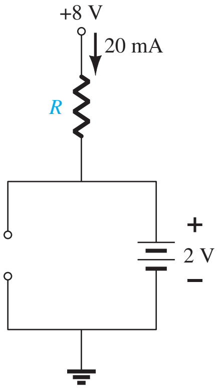


FIG. 2.31
Operating conditions for the network of Fig. 2.30.

Note that the reverse breakdown voltage across the red diode is 2 V, which is fine for an LED with a reverse breakdown voltage of 3 V.

However, if the green diode were to be replaced by a blue diode, problems would develop, as shown in Fig. 2.32. Recall that the forward bias required to turn on a blue diode is about 5 V. The result would appear to require a smaller resistor R to establish the current of 20 mA. However, note that the reverse bias voltage of the red LED is 5 V, but the reverse breakdown voltage of the diode is only 3 V. The result is the voltage across the red LED would lock in at 3 V as shown in Fig. 2.33. The voltage across R would be 5 V and the current limited to 20 mA with a 250 Ω resistor but neither LED would be on.

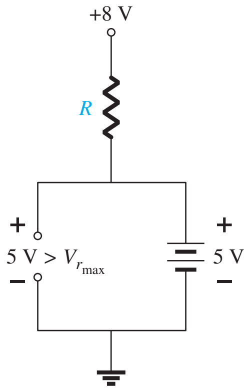


FIG. 2.32
Network of Fig. 2.31 with a blue diode.

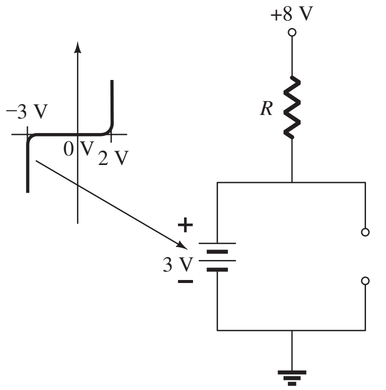


FIG. 2.33
Demonstrating damage to the red LED if the reverse breakdown voltage is exceeded.

A simple solution to the above is to add the appropriate resistance level in series with each diode to establish the desired 20 mA and to include another diode to add to the reverse-bias total reverse breakdown voltage rating, as shown in Fig. 2.34. When the blue LED is on, the diode in series with the blue LED will also be on, causing a total voltage drop of 5.7 V across the two series diodes and a voltage of 2.3 V across the resistor R_1, establishing a high emission current of 19.17 mA. At the same time the red LED diode and

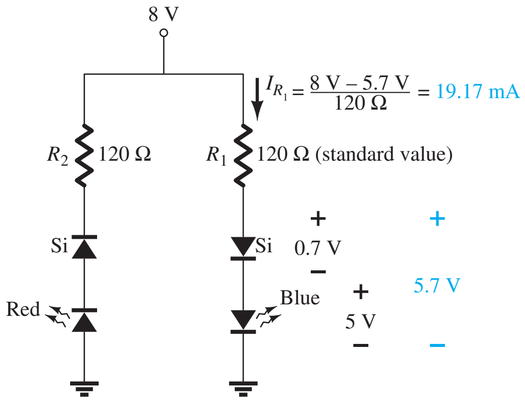

8 V
$I_{R_1} = \frac{8\text{ V} - 5.7\text{ V}}{120\ \Omega} = 19.17\text{ mA}$
R_2 120 Ω
R_1 120 Ω (standard value)
Si
Si
0.7 V
Red
Blue
5 V
5.7 V

FIG. 2.34
Protective measure for the red LED of Fig. 2.33.

its series diode will also be reverse biased, but now the standard diode with a reverse breakdown voltage of 20 V will prevent the full reverse-bias voltage of 8 V from appearing across the red LED. When forward biased, the resistor R_2 will establish a current of 19.63 mA to ensure a high level of intensity for the red LED.

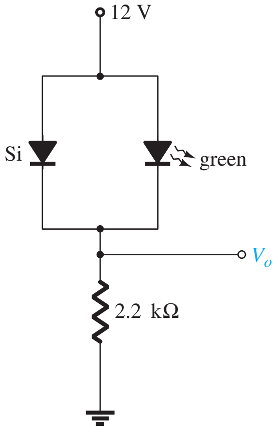


FIG. 2.35
Network for Example 2.12.

EXAMPLE 2.12 Determine the voltage V_o for the network of Fig. 2.35.

Solution: Initially, it might appear that the applied voltage will turn both diodes "on" because the applied voltage ("pressure") is trying to establish a conventional current through each diode that would suggest the "on" state. However, if both were on, there would be more than one voltage across the parallel diodes, violating one of the basic rules of network analysis: The voltage must be the same across parallel elements.

The resulting action can best be explained by remembering that there is a period of build-up of the supply voltage from 0 V to 12 V even though it may take milliseconds or microseconds. At the instant the increasing supply voltage reaches 0.7 V the silicon diode will turn "on" and maintain the level of 0.7 V since the characteristic is vertical at this voltage—the current of the silicon diode will simply rise to the defined level. The result is that the voltage across the green LED will never rise above 0.7 V and will remain in the equivalent open-circuit state as shown in Fig. 2.36.

The result is

$$V_o = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\ V}$$

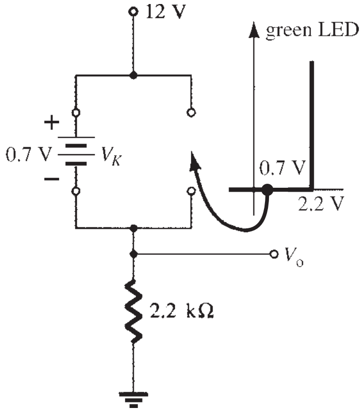


FIG. 2.36
Determining V_o for the network of Fig. 2.35.

EXAMPLE 2.13 Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.37.

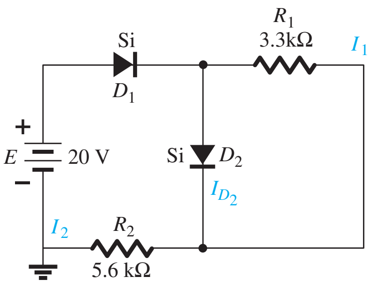


FIG. 2.37
Network for Example 2.13.

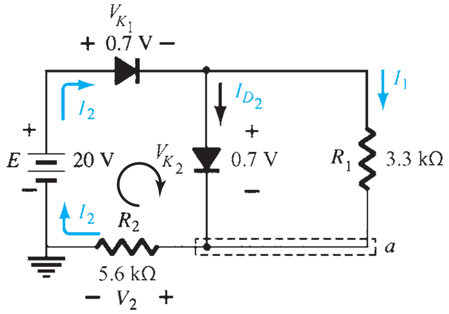


FIG. 2.38
Determining the unknown quantities for Example 2.13.

Solution: The applied voltage (pressure) is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series–parallel networks. We have

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and
$$V_2 = E - V_{K_1} - V_{K_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{18.6\text{ V}}$$

with
$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node a,

$$I_{D_2} + I_1 = I_2$$

and
$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} \cong \mathbf{3.11\text{ mA}}$$

2.5 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.14 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.39 is assigned a "1" for Boolean algebra and the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

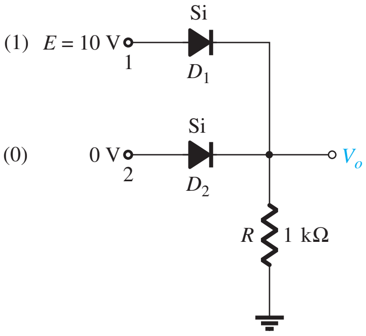


FIG. 2.39
Positive logic OR gate.

EXAMPLE 2.14 Determine V_o for the network of Fig. 2.39.

Solution: First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of

Fig. 2.40. Figure 2.40 "suggests" that D_1 is probably in the "on" state due to the applied 10 V, whereas D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.41.

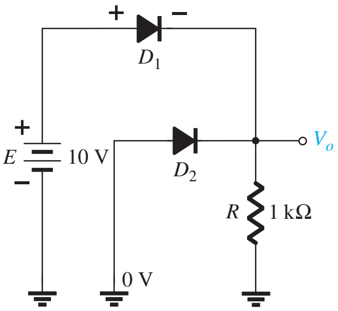


FIG. 2.40
Redrawn network of Fig. 2.39.

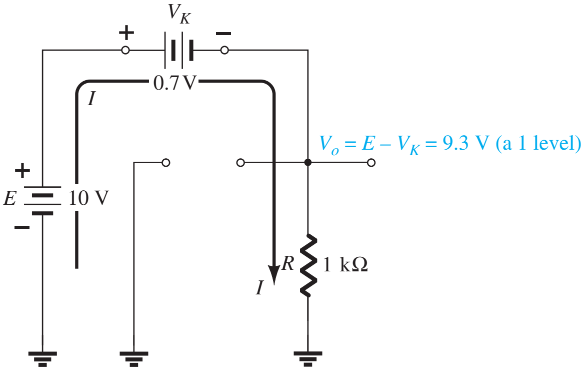


FIG. 2.41
Assumed diode states for Fig. 2.40.

The next step is simply to check that there is no contradiction in our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.41 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.15 Determine the output level for the positive logic AND gate of Fig. 2.42. An AND gate is one where a 1 output is only obtained when a 1 input appears at each and every input.

Solution: Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious, it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.43 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor.

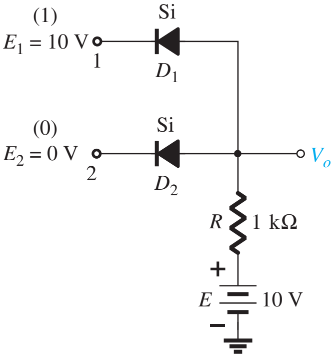


FIG. 2.42
Positive logic AND gate.

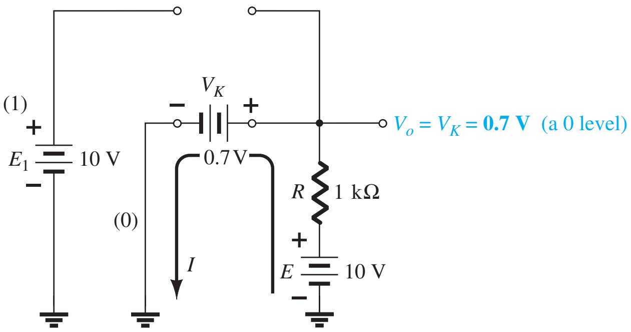


FIG. 2.43
Substituting the assumed states for the diodes of Fig. 2.42.

However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.43 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.43 and a magnitude equal to

$$I = \frac{E - V_K}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\ mA}$$

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.44. For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.

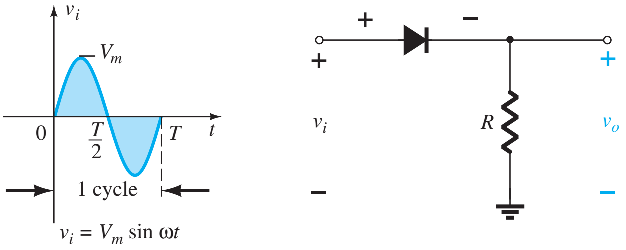


FIG. 2.44
Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.44, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.44, called a *half-wave rectifier*, will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier*. Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.44 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.45, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.46, and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o are sketched together in Fig. 2.47 for comparison purposes. The output signal v_o now has a net positive area above the axis over

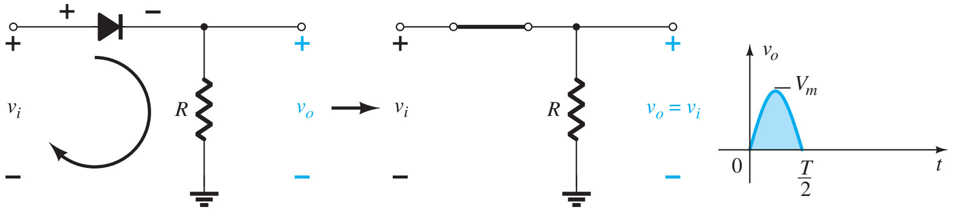

+
−
+
−
v_i
R
+
v_o
−
+
v_i
−
R
+
$v_o = v_i$
−
v_o
V_m
0
$\frac{T}{2}$
t

FIG. 2.45
Conduction region ($0 \rightarrow T/2$).

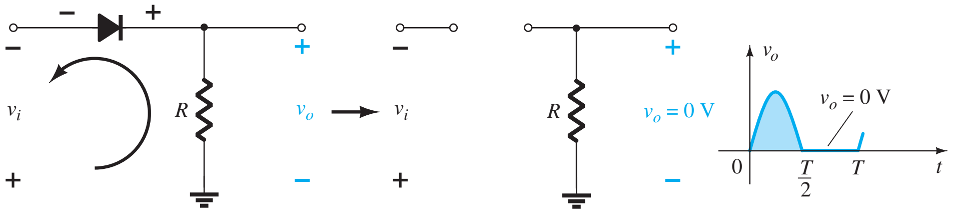

−
+
−
v_i
+
R
+
v_o
−
−
v_i
+
R
+
$v_o = 0$ V
−
v_o
$v_o = 0$ V
0
$\frac{T}{2}$
T
t

FIG. 2.46
Nonconduction region ($T/2 \rightarrow T$).

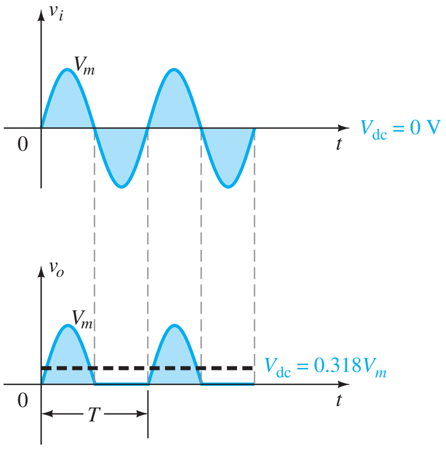


FIG. 2.47
Half-wave rectified signal.

a full period and an average value determined by

$$\boxed{V_{dc} = 0.318\ V_m} \quad \text{half-wave} \tag{2.7}$$

The process of removing one-half the input signal to establish a dc level is called *half-wave rectification*.

The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V, as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed

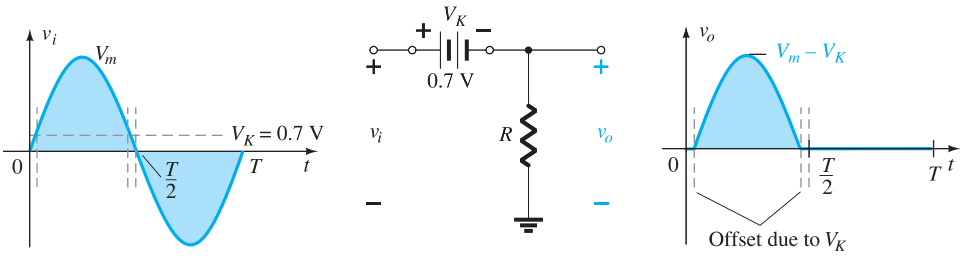

v_i
V_m
$V_K = 0.7$ V
0
$\frac{T}{2}$
T
t
V_K
+
−
0.7 V
+
v_i
−
R
+
v_o
−
v_o
$V_m - V_K$
0
$\frac{T}{2}$
T
t
Offset due to V_K

FIG. 2.48
Effect of V_K on half-wave rectified signal.

level of $V_K = 0.7$ V and $v_o = v_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m \gg V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$\boxed{V_{\text{dc}} \cong 0.318(V_m - V_K)} \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_K, Eq. (2.7) is often applied as a first approximation for V_{dc}.

EXAMPLE 2.16

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

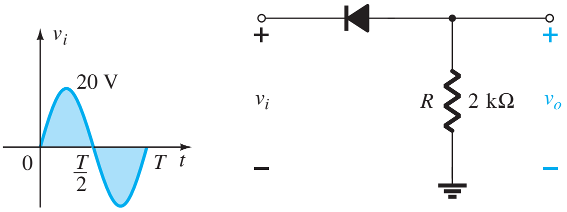


FIG. 2.49
Network for Example 2.16.

Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{\text{dc}} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

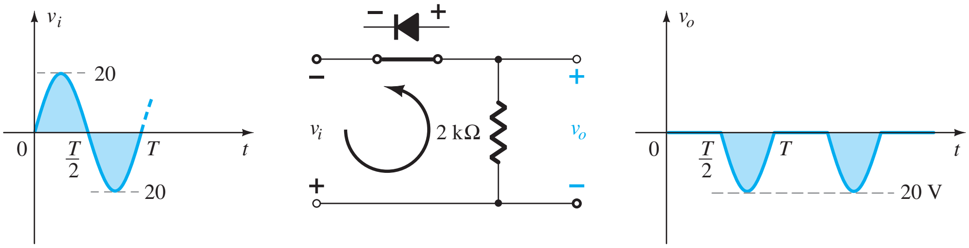


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

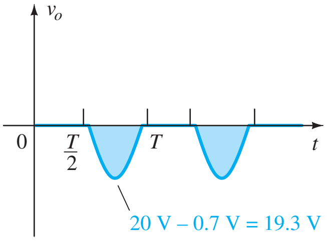


FIG. 2.51
Effect of V_K on output of Fig. 2.50.

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{\text{dc}} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

c. Eq. (2.7): $V_{\text{dc}} = -0.318\,V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{\text{dc}} = -0.318(V_m - V_K) = -0.318(200\text{ V} - 0.7\text{ V})$

$$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$$

which is a difference that can certainly be ignored for most applications. For part (c) the offset and drop in amplitude due to V_K would not be discernible on a typical oscilloscope if the full pattern is displayed.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.52, which displays the reverse-biased diode of Fig. 2.44 with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\boxed{\text{PIV rating} \geqq V_m} \quad \text{half-wave rectifier} \tag{2.9}$$

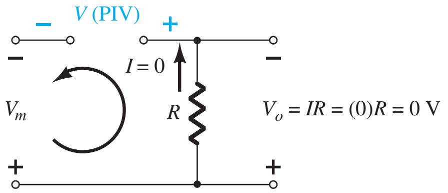


FIG. 2.52
Determining the required PIV rating for the half-wave rectifier.

2.7 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.54. The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D_2 and D_3 are conducting, whereas D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.55, with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.

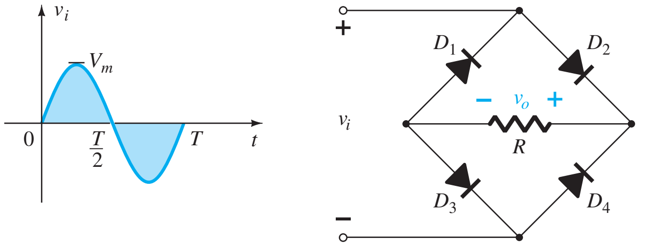


FIG. 2.53
Full-wave bridge rectifier.

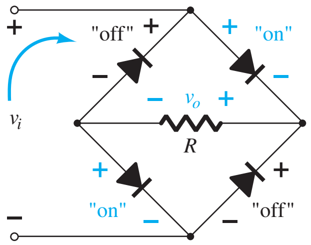


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i.

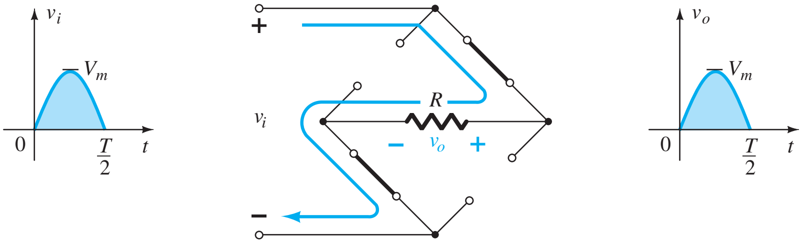


FIG. 2.55
Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.56. The important result is that the polarity across the load resistor R is the same as in Fig. 2.54, establishing a second positive pulse, as shown in Fig. 2.56. Over one full cycle the input and output voltages will appear as shown in Fig. 2.57.

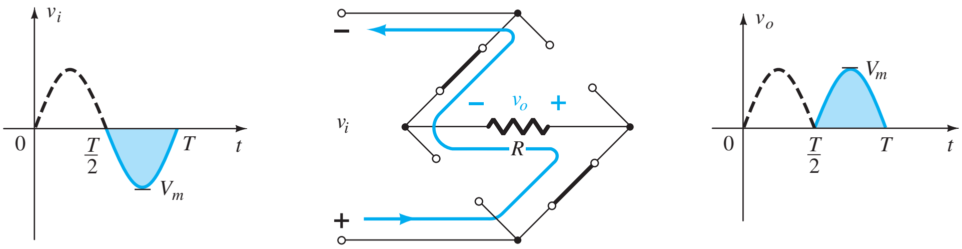


FIG. 2.56

Conduction path for the negative region of v_i.

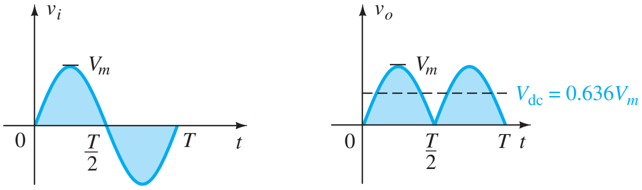


FIG. 2.57

Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2[\text{Eq. (2.7)}] = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636\ V_m} \quad \text{full-wave} \tag{2.10}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.58, the application of Kirchhoff's voltage law around the conduction path results in

$$v_i - V_K - v_o - V_K = 0$$

and

$$v_o = v_i - 2V_K$$

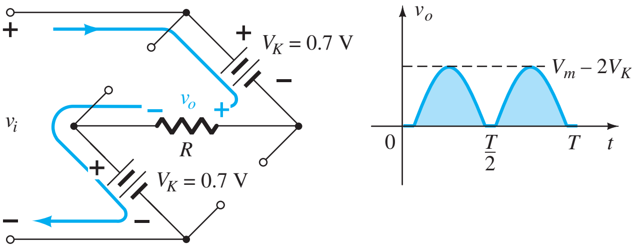


FIG. 2.58

Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_K$$

For situations where $V_m \gg 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_K)} \tag{2.11}$$

Then again, if V_m is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

PIV The required PIV of each diode (ideal) can be determined from Fig. 2.59 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\boxed{\text{PIV} \geqq V_m} \quad \text{full-wave bridge rectifier} \tag{2.12}$$

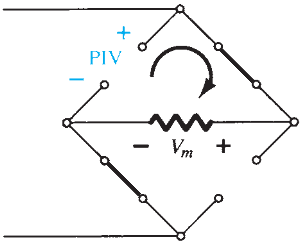


FIG. 2.59
Determining the required PIV for the bridge configuration.

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61.

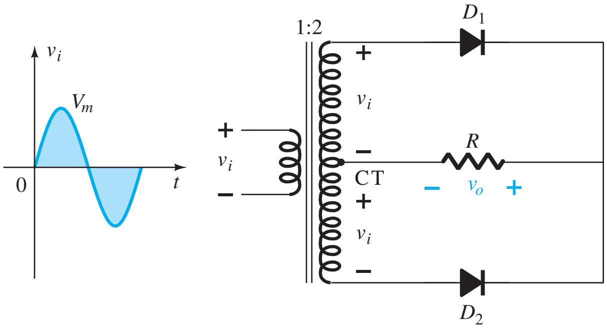


FIG. 2.60
Center-tapped transformer full-wave rectifier.

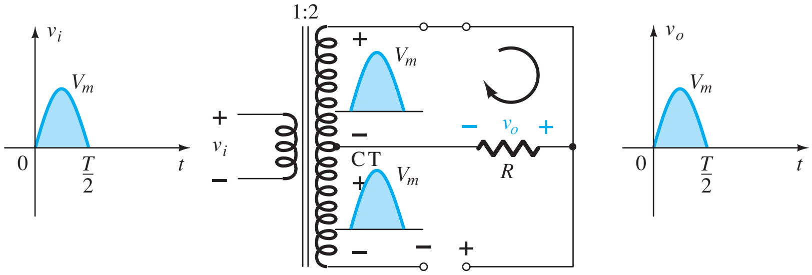


FIG. 2.61
Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.62, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R. The net effect is the same output as that appearing in Fig. 2.57 with the same dc levels.

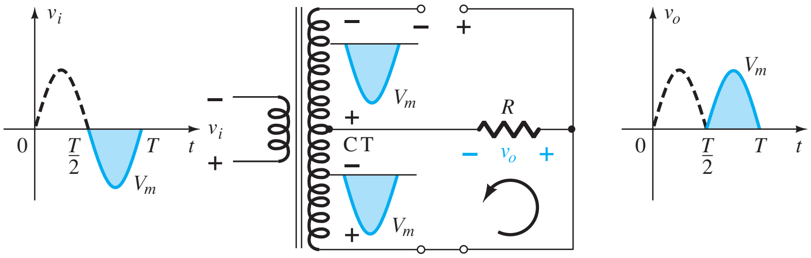


FIG. 2.62
Network conditions for the negative region of v_i.

PIV The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

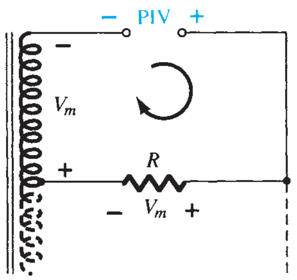


FIG. 2.63
Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

$$\begin{aligned}\text{PIV} &= V_{\text{secondary}} + V_R \\ &= V_m + V_m\end{aligned}$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

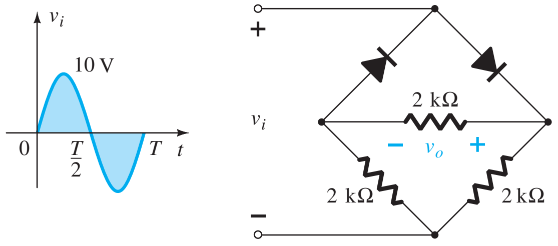


FIG. 2.64
Bridge network for Example 2.17.

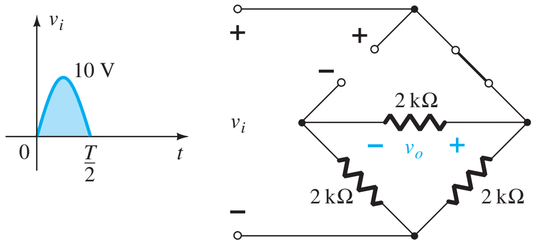


FIG. 2.65
Network of Fig. 2.64 for the positive region of v_i.

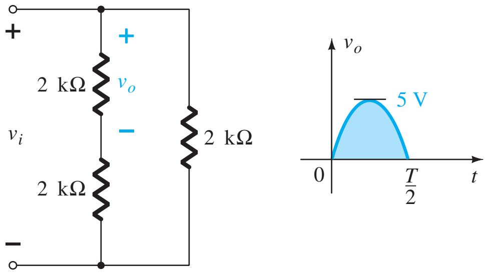


FIG. 2.66
Redrawn network of Fig. 2.65.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\text{max}}} = \frac{1}{2}V_{i_{\text{max}}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.66. For the negative part of the input, the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

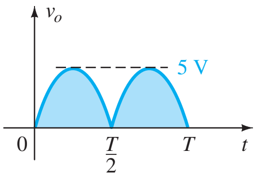


FIG. 2.67
Resulting output for Example 2.17.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R, which is 5 V, or half of that required for a half-wave rectifier with the same input.

2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clampers will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

The half-wave rectifier of Section 2.6 is an example of the simplest form of diode clipper—one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel.* The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.68a to a variety of alternating waveforms is provided in Fig. 2.68b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

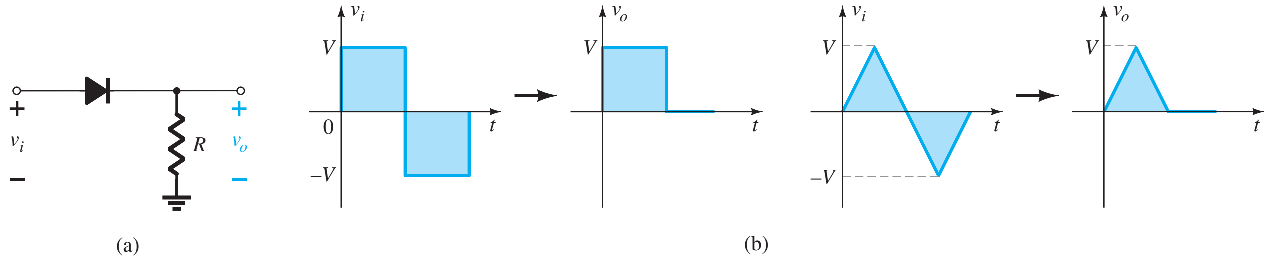


FIG. 2.68
Series clipper.

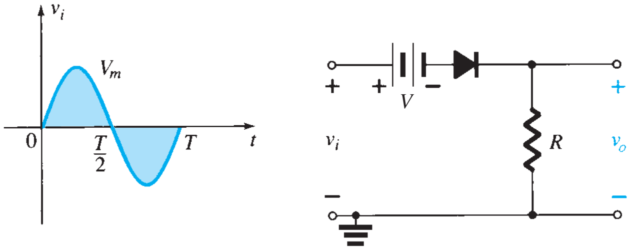


FIG. 2.69
Series clipper with a dc supply.

The addition of a dc supply to the network as shown in Fig. 2.69 can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.

There is no general procedure for analyzing networks such as the type in Fig. 2.69, but there are some things one can do to give the analysis some direction.

First and most important:

1. Take careful note of where the output voltage is defined.

In Fig. 2.69 it is directly across the resistor *R*. In some cases it may be across a combination of series elements.

Next:

2. Try to develop an overall sense of the response by simply noting the "pressure" established by each supply and the effect it will have on the conventional current direction through the diode.

In Fig. 2.69, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply *V* will oppose that applied voltage and try to keep the diode in the "off" state. The result is that any supply voltage greater than *V* volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the diode will be on for any voltage v_i that is greater than V volts and off for any lesser voltage. For the "off" condition, the output would be 0 V due to the lack of current, and for the "on" condition it would simply be $v_o = v_i - V$ as determined by Kirchhoff's voltage law.

3. **Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.**

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when $V_D = 0$ V and $I_D = 0$ mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and $I_D = 0$ mA.

This exercise was applied to the network of Fig. 2.69 as shown in Fig. 2.70. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is $v_i - V = 0$, and so

$$\boxed{v_i = V} \tag{2.14}$$

is the transition voltage.

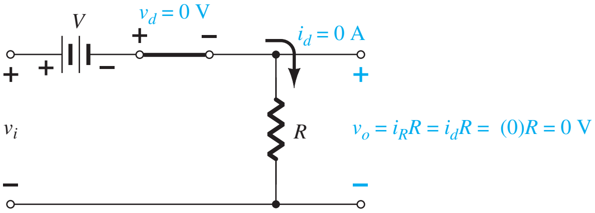


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

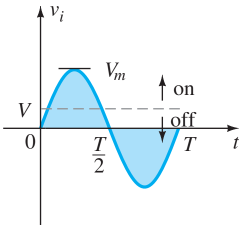


FIG. 2.71
Using the transition voltage to define the "on" and "off" regions.

This permits drawing a line on the sinusoidal supply voltage as shown in Fig. 2.71 to define the regions where the diode is on and off.

For the "on" region, as shown in Fig. 2.72, the diode is replaced by a short-circuit equivalent, and the output voltage is defined by

$$\boxed{v_o = v_i - V} \tag{2.15}$$

For the "off" region, the diode is an open circuit, $I_D = 0$ mA, and the output voltage is

$$\boxed{v_o = 0\text{ V}}$$

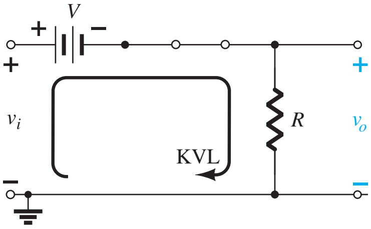


FIG. 2.72
Determining v_o for the diode in the "on" state.

4. **It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.**

Using this last piece of information, we can establish the 0-V level on the plot of Fig. 2.73 for the region indicated. For the "on" condition, Eq. (2.15) can be used to find the output voltage when the applied voltage has its peak value:

$$v_{o_{\text{peak}}} = V_m - V$$

and this can be added to the plot of Fig. 2.73. It is then simple to fill in the missing section of the output curve.

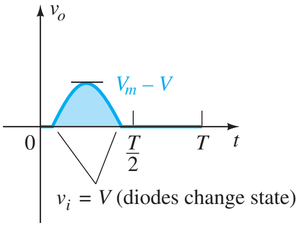


FIG. 2.73
Sketching the waveform of v_o using the results obtained for v_o above and below the transition level.

EXAMPLE 2.18 Determine the output waveform for the sinusoidal input of Fig. 2.74.

Solution:

Step 1: The output is again directly across the resistor R.

Step 2: The positive region of v_i and the dc supply are both applying "pressure" to turn the diode on. The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for v_i. Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode off.

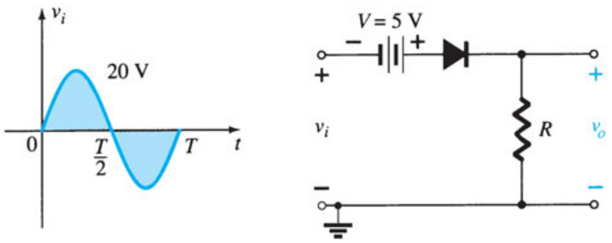


FIG. 2.74
Series clipper for Example 2.18.

Step 3: The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5\text{ V} = 0\text{ V}$$

or
$$v_i = -5\text{ V}$$

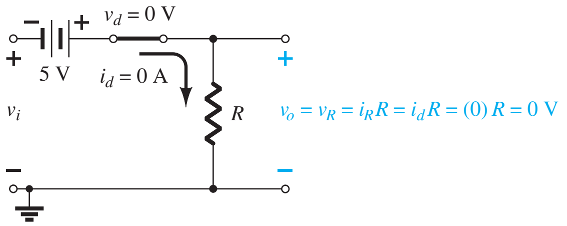


FIG. 2.75
Determining the transition level for the clipper of Fig. 2.74.

Step 4: In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than −5 V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of v_o. Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5\text{ V}$$

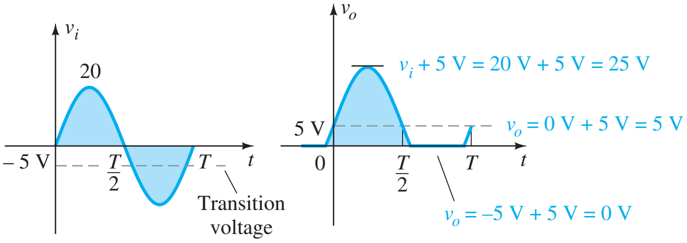


FIG. 2.76
Sketching v_o for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting v_o plotted in the proper time frame. The next example demonstrates the procedure.

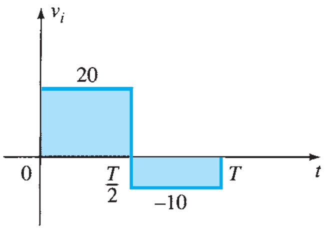


FIG. 2.77
Applied signal for Example 2.19.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20\text{ V}$ ($0 \rightarrow T/2$) the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$. For $v_i = -10\text{ V}$ the network of Fig. 2.79

results, placing the diode in the “off” state, and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.80.

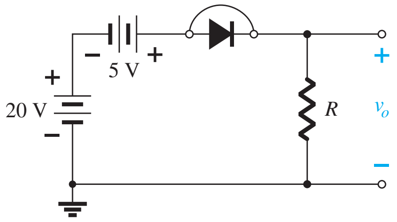


FIG. 2.78
v_o at $v_i = +20$ V.

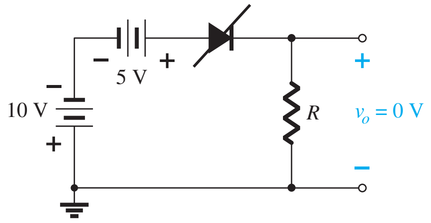


FIG. 2.79
v_o at $v_i = -10$ V.

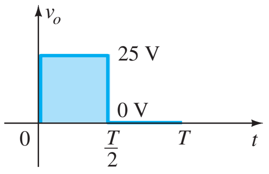


FIG. 2.80
Sketching v_o for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

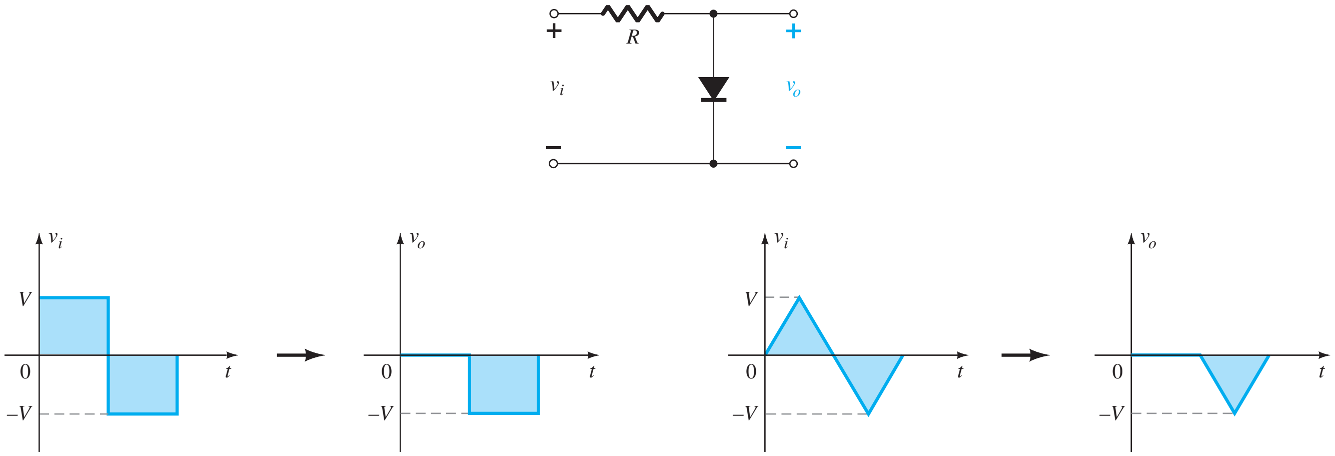


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor *R*.

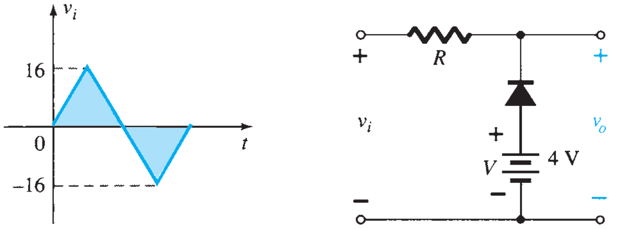


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4\text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4\text{ V}$ when the diode is on. For $v_i \geq 4\text{ V}$, $v_o = 4\text{ V}$, and the waveform is simply repeated on the output plot.

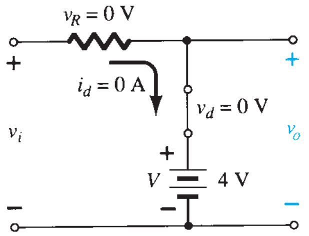


FIG. 2.83
Determining the transition level for Example 2.20.

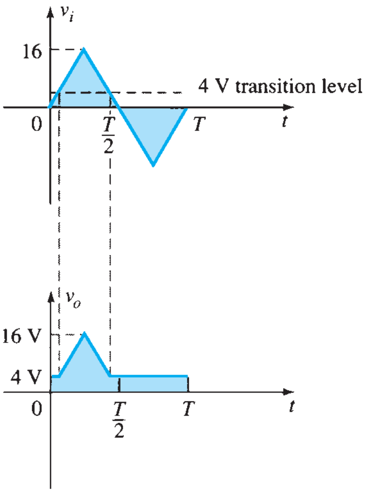


FIG. 2.84
Sketching v_o for Example 2.20.

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

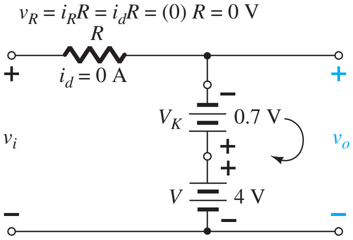


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7\text{ V}$.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0\text{ A}$ at $v_d = V_D = 0.7\text{ V}$ and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and $$v_i = V - V_K = 4\text{ V} - 0.7\text{ V} = \mathbf{3.3\text{ V}}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.86 results, where

$$v_o = 4\text{ V} - 0.7\text{ V} = \mathbf{3.3\text{ V}}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

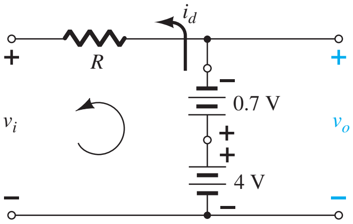


FIG. 2.86
Determining v_o for the diode of Fig. 2.82 in the "on" state.

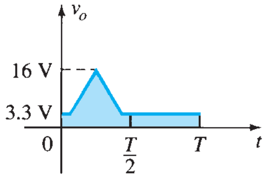


FIG. 2.87
Sketching v_o for Example 2.21.

There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K, will not be that difficult.

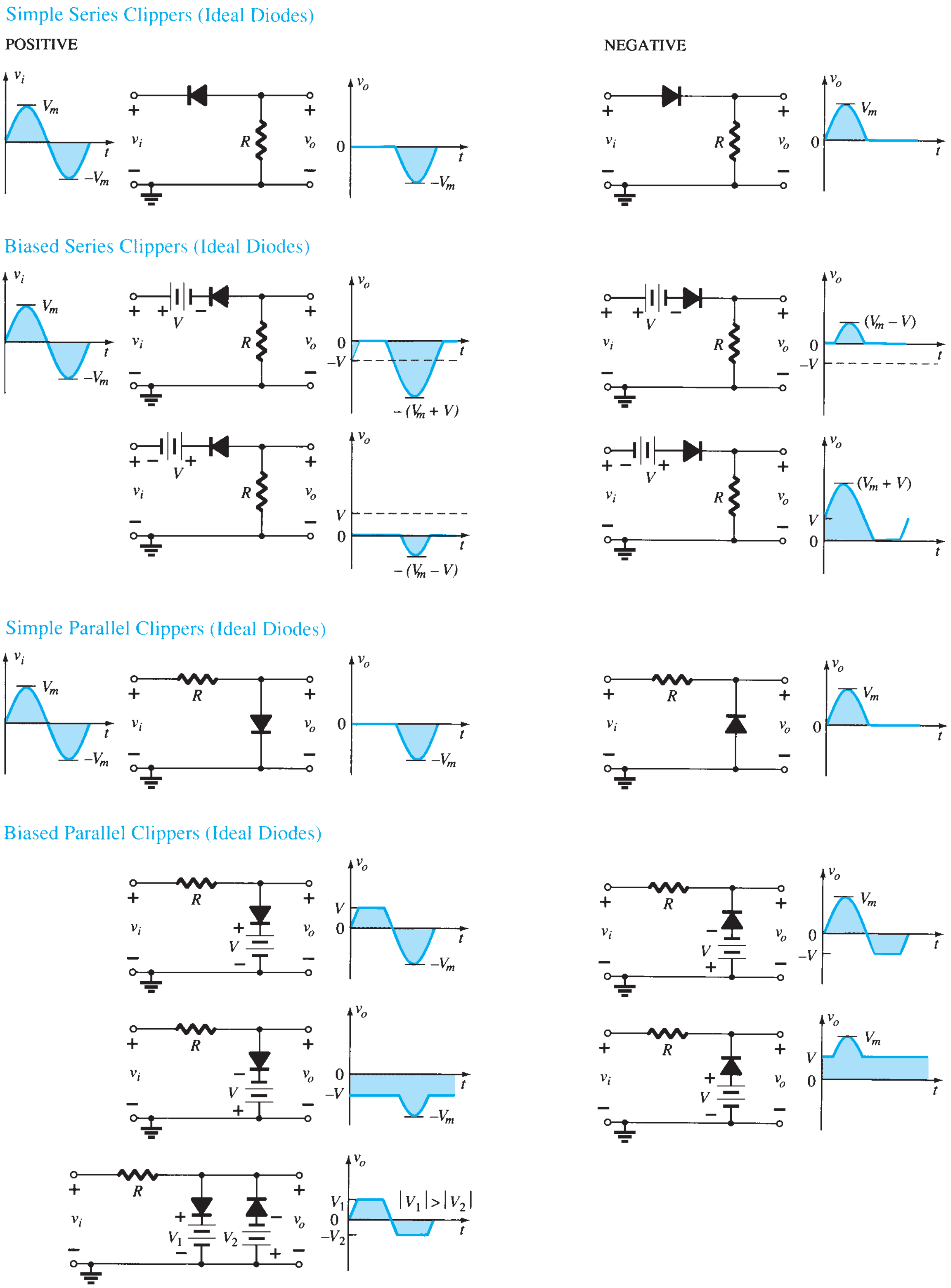

Simple Series Clippers (Ideal Diodes)
POSITIVE
NEGATIVE
v_i
V_m
$-V_m$
t
R
v_o
0
Biased Series Clippers (Ideal Diodes)
V
$-V$
$-(V_m + V)$
$-(V_m - V)$
$(V_m - V)$
$(V_m + V)$
Simple Parallel Clippers (Ideal Diodes)
Biased Parallel Clippers (Ideal Diodes)
V_1
V_2
$-V_2$
$|V_1| > |V_2|$

FIG. 2.88

Clipping circuits.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

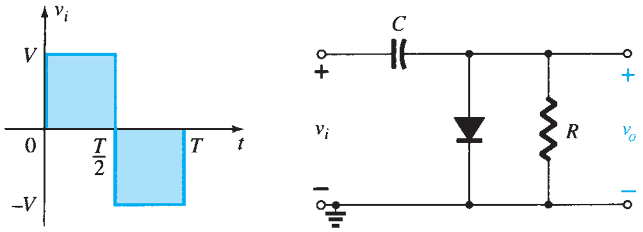


FIG. 2.89
Clamper.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to $T/2$ the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in $v_o = 0$ V for this time interval, as shown in the sketch of v_o in Fig. 2.92. During this same interval of time, the time constant determined by $\tau = RC$ is very small because the resistor R has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of V volts as shown in Fig. 2.90 with the polarity indicated.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

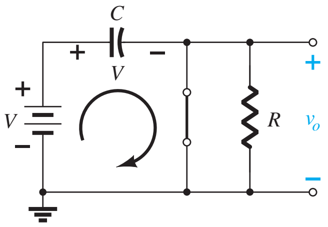


FIG. 2.90
Diode "on" and the capacitor charging to V volts.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ, much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

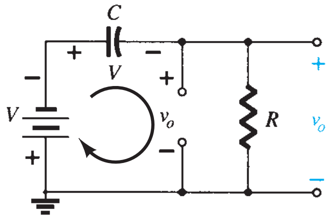


FIG. 2.91
Determining v_o with the diode "off."

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and
$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

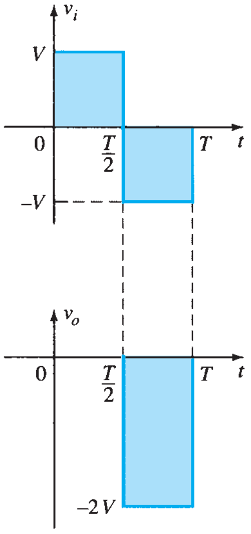


FIG. 2.92
Sketching v_o for the network of Fig. 2.91.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.

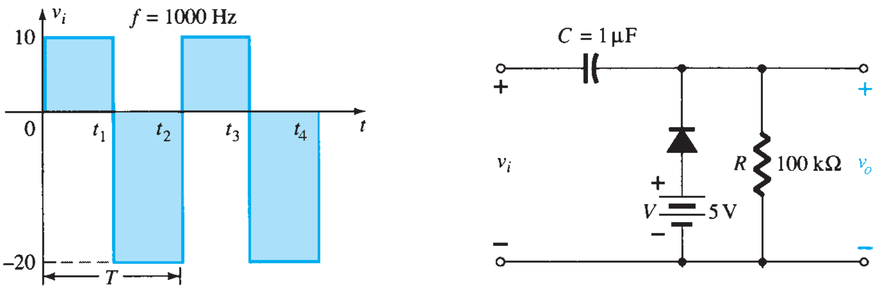


FIG. 2.93
Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R, but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop results in

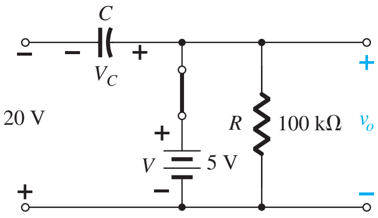


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and
$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

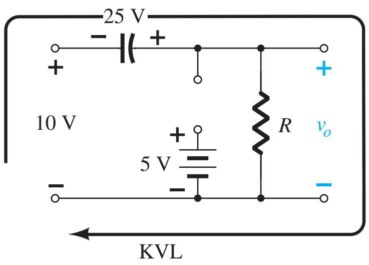


FIG. 2.95
Determining v_o with the diode in the "off" state.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and
$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

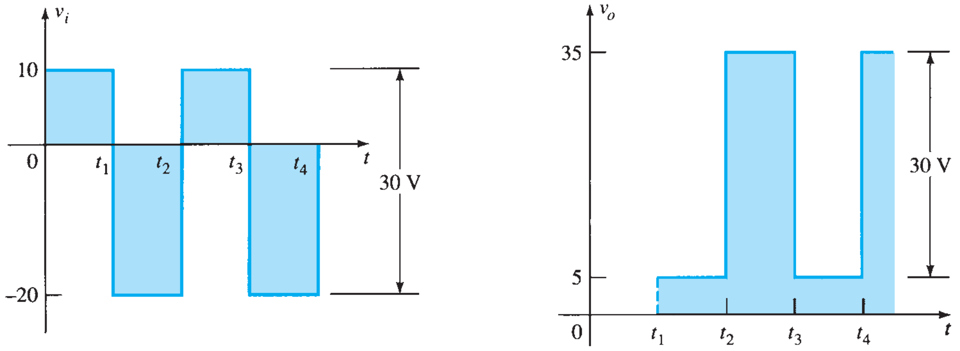


FIG. 2.96

v_i and v_o for the clamper of Fig. 2.93.

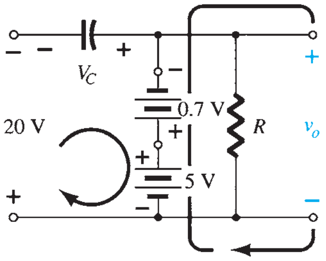


FIG. 2.97

Determining v_o and V_C with the diode in the "on" state.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7$ V.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and
$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law results in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and
$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and
$$v_o = 34.3\ \text{V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

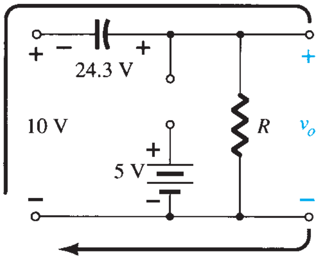


FIG. 2.98

Determining v_o with the diode in the open state.

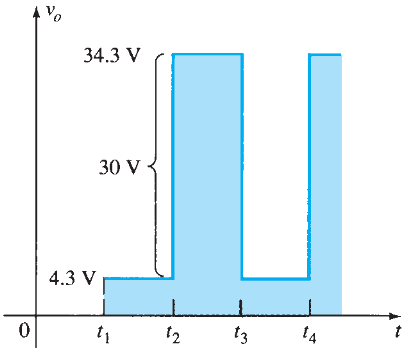


FIG. 2.99

Sketching v_o for the clamper of Fig. 2.93 with a silicon diode.

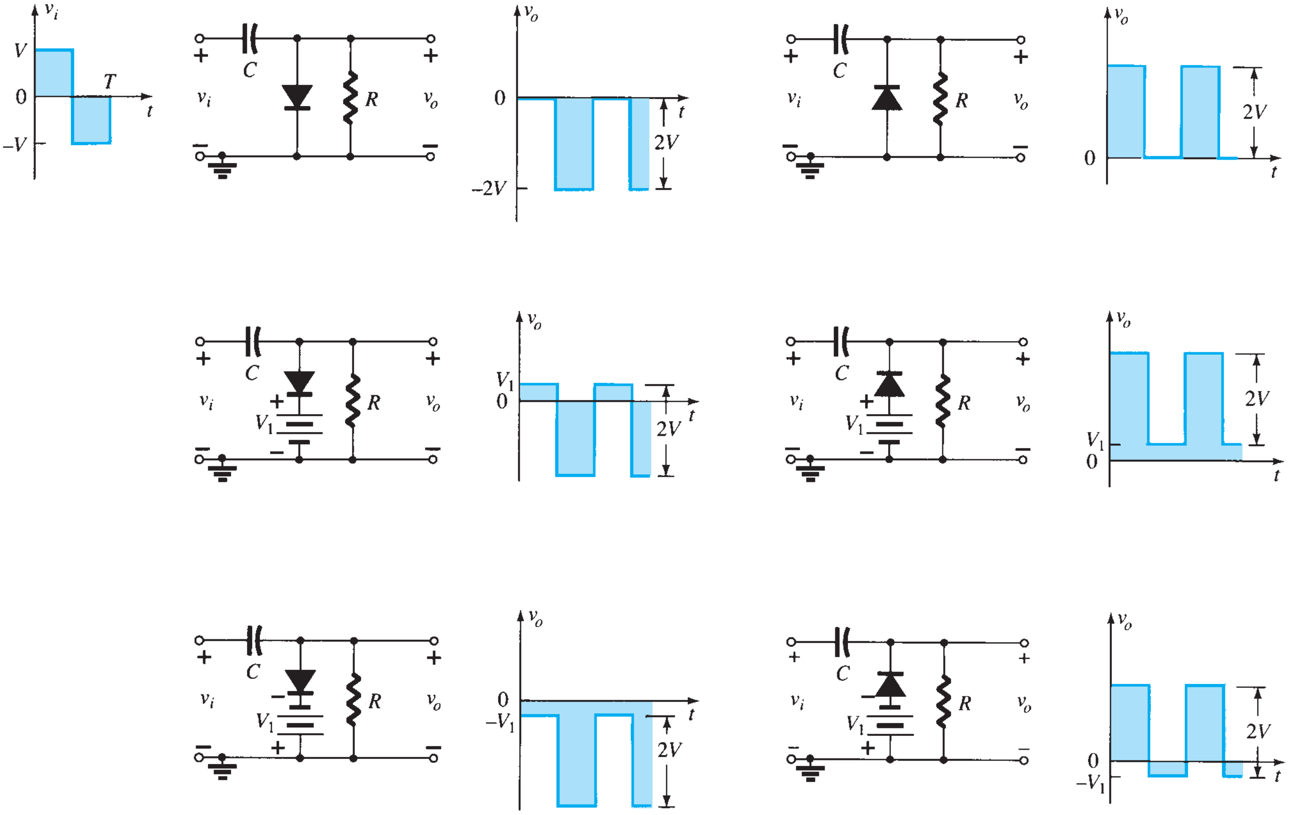


FIG. 2.100

Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

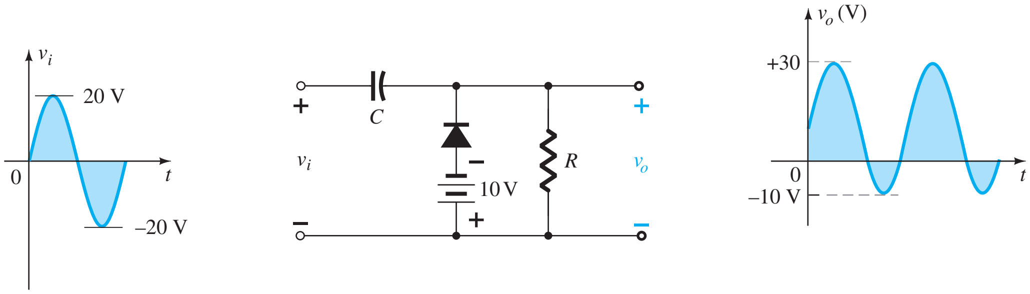


FIG. 2.101

Clamping network with a sinusoidal input.

2.10 NETWORKS WITH A DC AND AC SOURCE

The analysis thus far has been limited to circuits with a single dc, ac, or square wave input. This section will expand that analysis to include both an ac and a dc source in the same configuration. In Fig. 2.102 the simplest of two-source networks has been constructed.

For such a system it is especially important that the Superposition Theorem can be applied. That is,

The response of any network with both an ac and a dc source can be found by finding the response to each source independently and then combining the results.

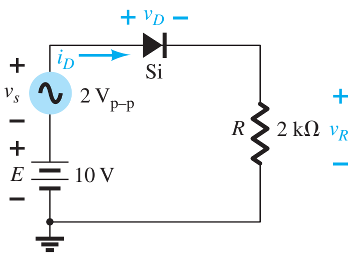


FIG. 2.102
Network with a dc and ac supply.

DC Source

The network is redrawn as shown in Fig. 2.103 for the dc source. Note that the ac source was removed by simply replacing it with a short-circuit equivalent to the condition $v_s = 0$ V.

Using the approximate equivalent circuit for the diode, the output voltage is

$$V_R = E - V_D = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$$

and the currents are $$I_D = I_R = \frac{9.3\text{ V}}{2\text{ k}\Omega} = 4.65\text{ mA}$$

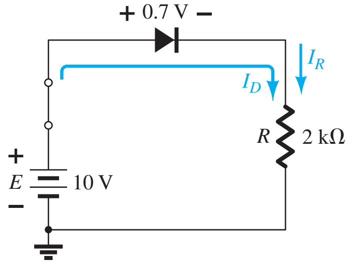


FIG. 2.103
Applying superposition to determine effects of the dc source.

AC Source

The dc source is also replaced by a short-circuit equivalent, as shown in Fig. 2.104. The diode will be replaced by the ac resistance, as determined by Eq. 1.5 in Chapter 1—the current in the equation being the quiescent or dc value. For this case,

$$r_d = \frac{26\text{ mV}}{I_D} = \frac{26\text{ mV}}{4.65\text{ mA}} = 5.59\ \Omega$$

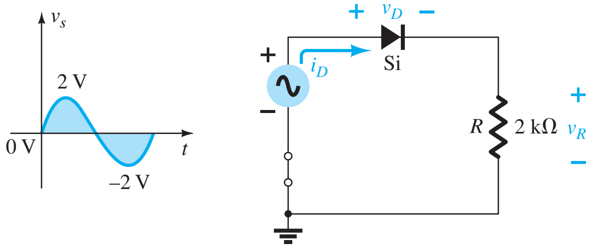


FIG. 2.104
Determing the response of v_R to the applied ac source.

Replacing the diode by this resistance will result in the circuit of Fig. 2.105. For the peak value of the applied voltage, the peak values of v_R and v_D will be

$$v_{R_\text{peak}} = \frac{2\text{ k}\Omega\,(2\text{ V})}{2\text{ k}\Omega + 5.59\ \Omega} \cong 1.99\text{ V}$$

and $$v_{D_\text{peak}} = v_{s_\text{peak}} - v_{R_\text{peak}} = 2\text{ V} - 1.99\text{ V} = 0.01\text{ V} = 10\text{ mV}$$

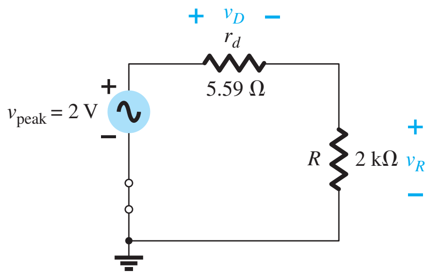


FIG. 2.105
Replacing the diode of Fig. 2.104 by its equivalent ac resistance.

Combining the results of the dc and ac analysis will result in the waveforms of Fig. 2.106 for v_R and v_D.

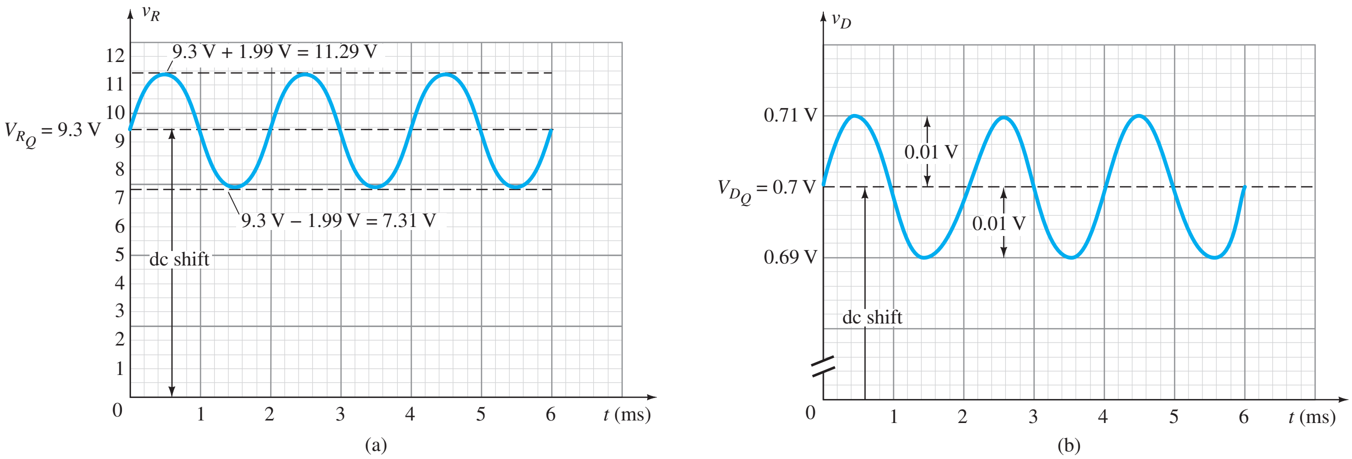


FIG. 2.106

(a) v_R and (b) v_D for the network of Fig. 2.102.

Note that the diode has an important impact on the resulting output voltage v_R but very little impact on the ac swing.

For comparison purposes the same system will now be analyzed using the actual characteristics and a load-line analysis. In Fig. 2.107 the dc load line has been drawn as described in Section 2.2. The resulting dc current is now slightly less due to a voltage drop across the diode that is slightly more than the approximate value of 0.7 V. For the peak value of the input voltage the load line will have intersections of $E = 12$ V and $I = \frac{E}{R} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6$ mA. For the negative peak the intersections are at 8 V and 4 mA. Take particular note of the region of the diode characteristics traversed by the ac swing. It defines the region for which the diode resistance was determined in the analysis above. In this case, however, the quiescent value of dc current is ≅4.6 mA so the new ac resistance is

$$r_d = \frac{26\text{ mV}}{4.6\text{ mA}} = 5.65\ \Omega$$

which is very close to the above value.

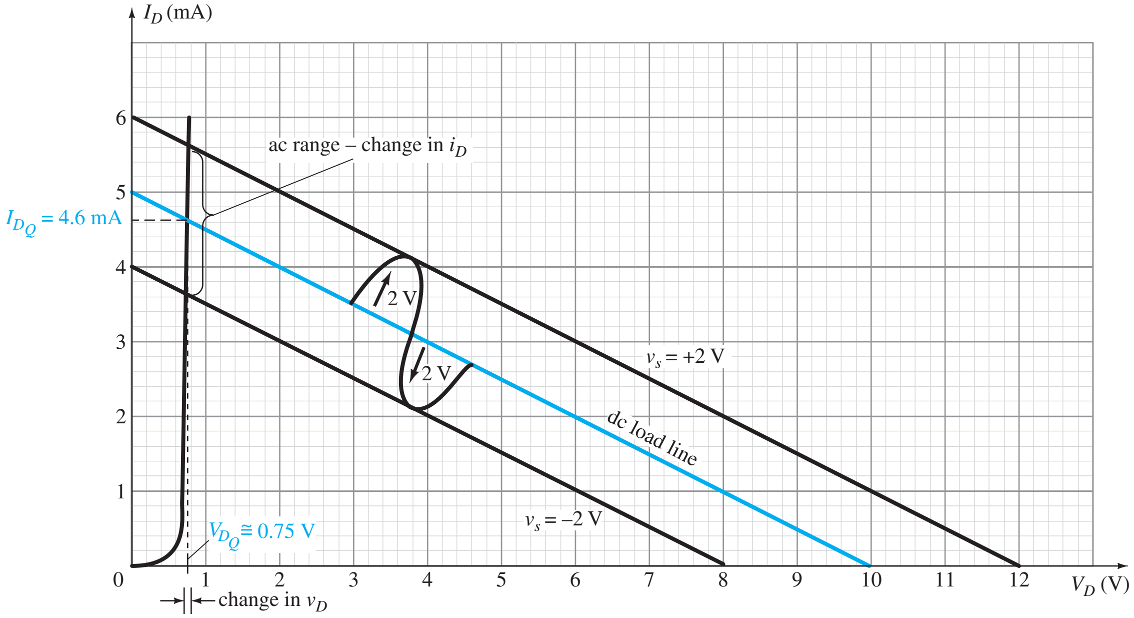


FIG. 2.107

Shifting load line due to v_s source.

In any event, it is now clear that the change in diode voltage for this region is very small, resulting in minimum impact on the output voltage. In general, the diode had a strong impact on the dc level of the output voltage but very little impact on the ac swing of the output. The diode was clearly close to ideal for the ac voltage and 0.7 V off for the dc level. This is all due primarily to the almost vertical rise of the diode once conduction is fully established through the diode. In most cases, diodes in the "on" state that are in series with loads will have some effect on the dc level but very little effect on the ac swing if the diode is fully conducting for the full cycle.

For the future, when dealing with diodes and an ac signal the dc level through the diode is first determined and the ac resistance level determined by Eq. 1.3. This ac resistance can then be substituted in place of the diode for the required analysis.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure 2.108 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also.

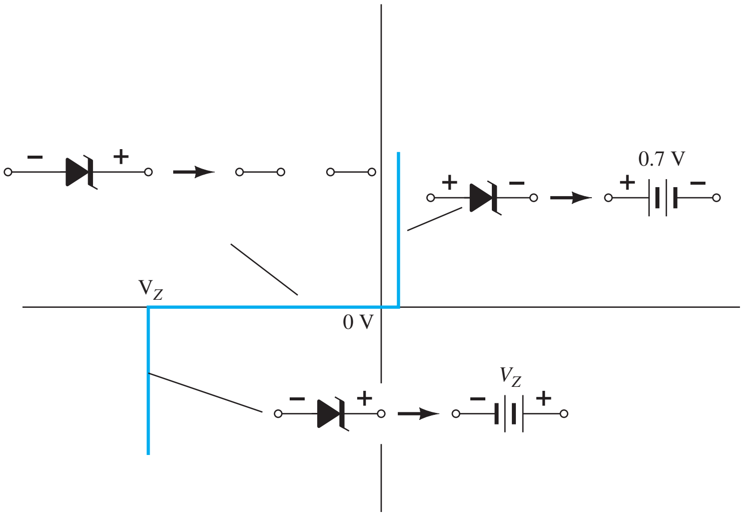


FIG. 2.108

Approximate equivalent circuits for the Zener diode in the three possible regions of application.

The first two examples will demonstrate how a Zener diode can be used to establish reference voltage levels and act as a protection device. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.109, which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

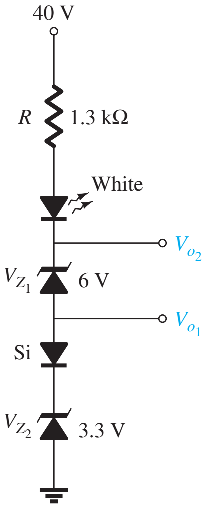


FIG. 2.109

Reference setting circuit for Example 2.24.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_2} + V_K = 3.3\text{ V} + 0.7\text{ V} = \mathbf{4.0\ V}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4\text{ V} + 6\text{ V} = \mathbf{10\ V}$$

Finally, the 4 V across the white LED will leave a voltage of 40 V – 14 V = 26 V across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40\text{ V} - V_{o_2} - V_{\text{LED}}}{1.3\text{ k}\Omega} = \frac{40\text{ V} - 10\text{ V} - 4\text{ V}}{1.3\text{ k}\Omega} = \frac{26\text{ V}}{1.3\text{ k}\Omega} = \mathbf{20\ mA}$$

which should establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40\text{ V})(20\text{ mA}) = \mathbf{800\ mW}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4\text{ V})(20\text{ mA}) = \mathbf{80\ mW}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6\text{ V})(20\text{ mA}) = \mathbf{120\ mW}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

EXAMPLE 2.25 The network of Fig. 2.110 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network.

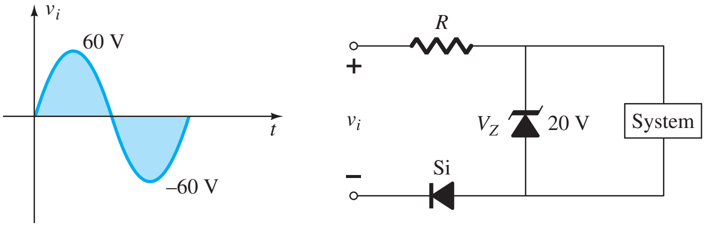


FIG. 2.110

Controlling network for Example 2.25.

Solution: For positive applied voltages less than the Zener potential of 20 V the Zener diode will be in its approximate open-circuit state, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.111a and the voltage across the system will lock in at 20 V. Further increases in the applied voltage will simply appear across the series resistor with the voltage across the system and the forward-biased diode remaining fixed at 20 V and 0.7 V, respectively. The voltage across the system is fixed at 20 V, as shown in Fig. 2.111a, because the 0.7 V of the diode is not between the defined output terminals. The system is therefore safe from any further increases in applied voltage.

For the negative region of the applied signal the silicon diode is reverse biased and presents an open circuit to the series combination of elements. The result is that the full negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.111b.

The voltage across the system will therefore appear as shown in Fig. 2.111c.

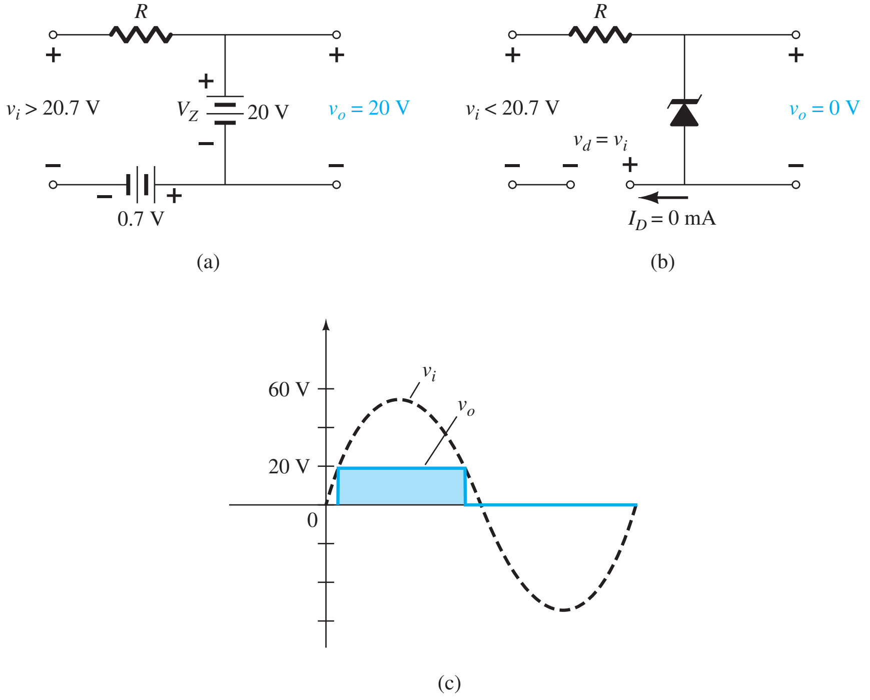


FIG. 2.111
Response of the network of Fig. 2.110 to the application of a 60-V sinusoidal signal.

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.112. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

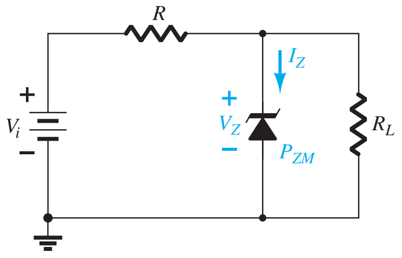


FIG. 2.112
Basic Zener regulator.

V_i and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.112. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. ***Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.***

Applying step 1 to the network of Fig. 2.112 results in the network of Fig. 2.113, where an application of the voltage divider rule results in

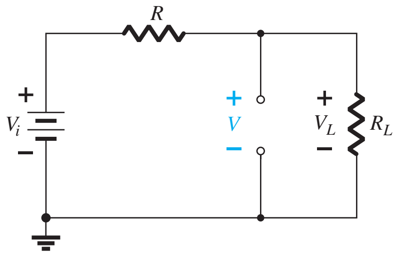


FIG. 2.113
Determining the state of the Zener diode.

$$\boxed{V = V_L = \frac{R_L V_i}{R + R_L}} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted. If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. ***Substitute the appropriate equivalent circuit and solve for the desired unknowns.***

For the network of Fig. 2.112, the "on" state will result in the equivalent network of Fig. 2.114. Since voltages across parallel elements must be the same, we find that

$$\boxed{V_L = V_Z} \tag{2.17}$$

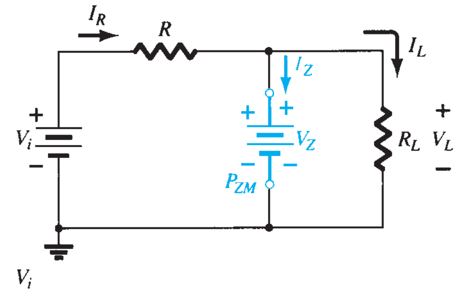


FIG. 2.114

Substituting the Zener equivalent for the "on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and
$$\boxed{I_Z = I_R - I_L} \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$\boxed{P_Z = V_Z I_Z} \tag{2.19}$$

that must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode.* If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

EXAMPLE 2.26

a. For the Zener diode network of Fig. 2.115, determine V_L, V_R, I_Z, and P_Z.
b. Repeat part (a) with $R_L = 3\text{ k}\Omega$.

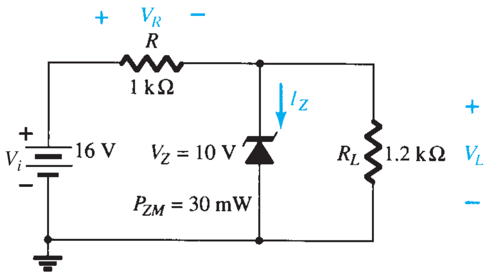


FIG. 2.115

Zener diode regulator for Example 2.26.

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.116. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\text{ k}\Omega(16\text{ V})}{1\text{ k}\Omega + 1.2\text{ k}\Omega} = 8.73\text{ V}$$

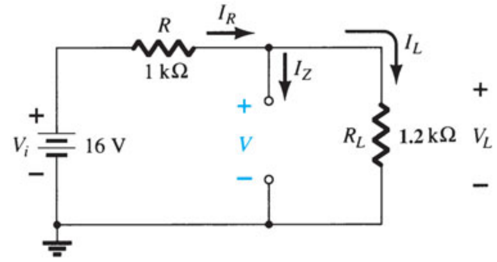


FIG. 2.116
Determining V for the regulator of Fig. 2.115.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state, as shown on the characteristics of Fig. 2.117. Substituting the open-circuit equivalent results in the same network as in Fig. 2.116, where we find that

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ \text{V} - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

and $$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

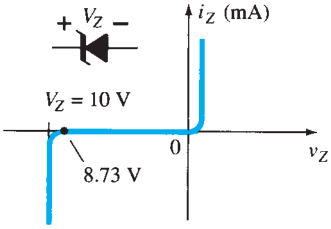


FIG. 2.117
Resulting operating point for the network of Fig. 2.115.

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega\ +\ 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.118 results. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and $$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with $$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and $$I_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that $$\begin{aligned} I_Z &= I_R - I_L\ [\text{Eq. (2.18)}] \\ &= 6\ \text{mA} - 3.33\ \text{mA} \\ &= \mathbf{2.67\ mA} \end{aligned}$$

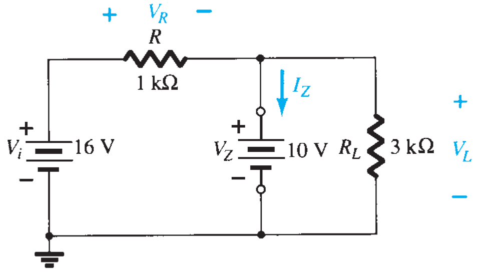


FIG. 2.118
Network of Fig. 2.115 in the "on" state.

The power dissipated is

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.112 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$\boxed{R_{L_{\min}} = \frac{R V_Z}{V_i - V_Z}} \qquad \textbf{(2.20)}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L, but in turn specifies the maximum I_L as

$$\boxed{I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}}} \qquad \textbf{(2.21)}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$\boxed{V_R = V_i - V_Z} \qquad \textbf{(2.22)}$$

and I_R remains fixed at

$$\boxed{I_R = \frac{V_R}{R}} \qquad \textbf{(2.23)}$$

The Zener current

$$\boxed{I_Z = I_R - I_L} \qquad \textbf{(2.24)}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$\boxed{I_{L_{\min}} = I_R - I_{ZM}} \qquad \textbf{(2.25)}$$

and the maximum load resistance as

$$\boxed{R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}}} \qquad \textbf{(2.26)}$$

EXAMPLE 2.27

a. For the network of Fig. 2.119, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
b. Determine the maximum wattage rating of the diode.

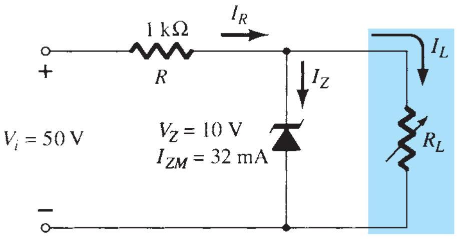


FIG. 2.119
Voltage regulator for Example 2.27.

Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

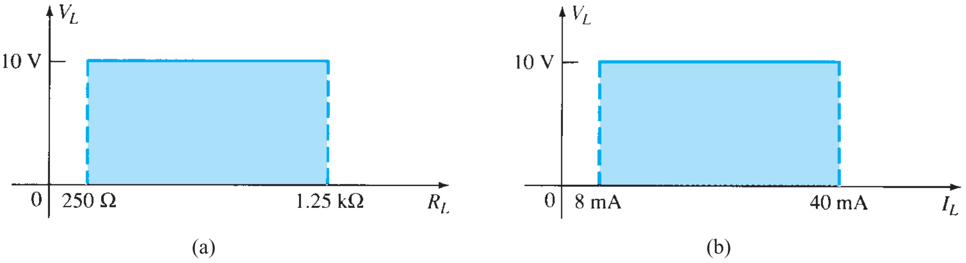
The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.120a and for V_L versus I_L in Fig. 2.120b.



(a) (b)

FIG. 2.120

V_L versus R_L and I_L for the regulator of Fig. 2.119.

b. $P_{\max} = V_Z I_{ZM}$

$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.112, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{\min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L}} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{\max}} = I_{ZM} + I_L} \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{\max}} = V_{R_{\max}} + V_Z$$

$$\boxed{V_{i_{\max}} = I_{R_{\max}}R + V_Z} \tag{2.29}$$

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.121 in the "on" state.

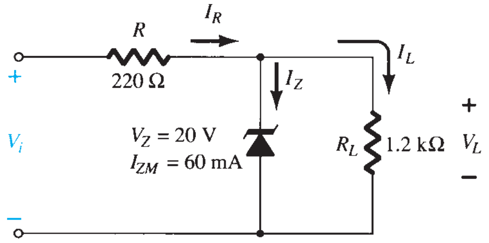


FIG. 2.121
Regulator for Example 2.28.

Solution:

Eq. (2.27): $$V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

Eq. (2.28): $$\begin{aligned} I_{R_{\max}} &= I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA} \\ &= 76.67\ \text{mA} \end{aligned}$$

Eq. (2.29): $$\begin{aligned} V_{i_{\max}} &= I_{R_{\max}} R + V_Z \\ &= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V} \\ &= 16.87\ \text{V} + 20\ \text{V} \\ &= \mathbf{36.87\ V} \end{aligned}$$

A plot of V_L versus V_i is provided in Fig. 2.122.

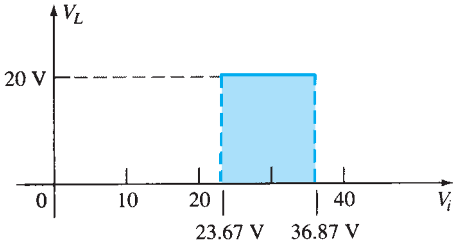


FIG. 2.122
V_L versus V_i for the regulator of Fig. 2.121.

The results of Example 2.28 reveal that for the network of Fig. 2.121 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 V to 36.87 V.

2.12 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Fig. 2.123 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.124a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.124b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$
$$-V_m - V_m + V_{C_2} = 0$$

from which we obtain

$$V_{C_2} = 2V_m$$

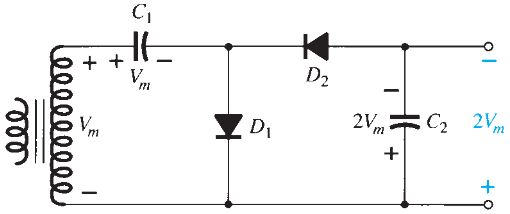
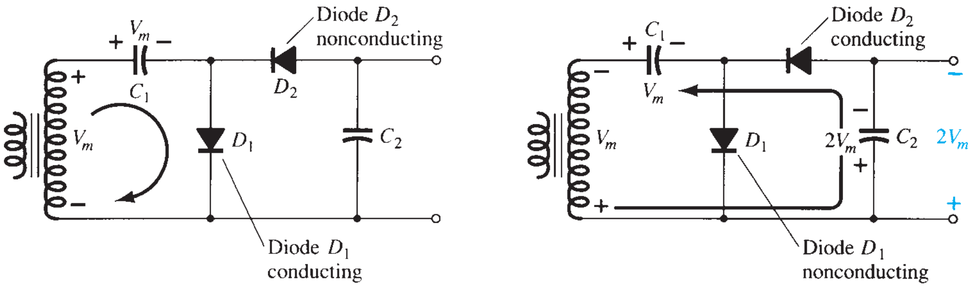


FIG. 2.123
Half-wave voltage doubler.



(a)
(b)

FIG. 2.124
Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half-cycle.

On the next positive half-cycle, diode D_2 is nonconducting and capacitor C_2 will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Another doubler circuit is the full-wave doubler of Fig. 2.125. During the positive half-cycle of transformer secondary voltage (see Fig. 2.126a) diode D_1 conducts, charging capacitor C_1 to a peak voltage V_m. Diode D_2 is nonconducting at this time.

During the negative half-cycle (see Fig. 2.126b) diode D_2 conducts, charging capacitor C_2, while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is $2V_m$. If load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

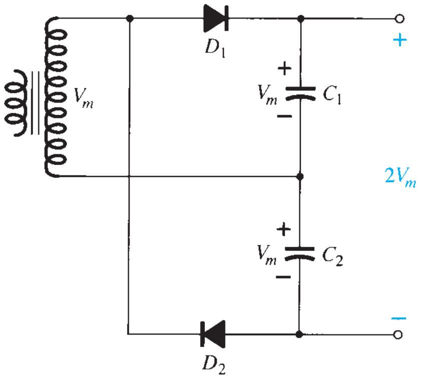

D1
+
Vm
C1
−
Vm
+
2Vm
+
Vm
C2
−
−
D2

FIG. 2.125

Full-wave voltage doubler.

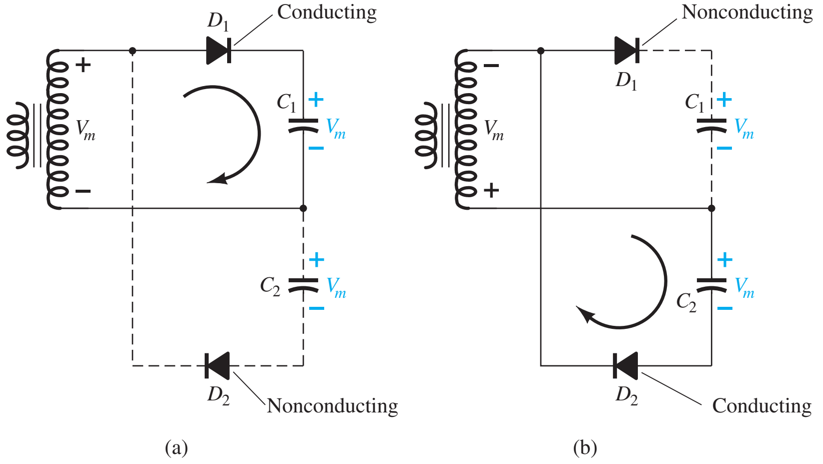

D1
Conducting
+
Vm
−
C1
+
Vm
−
C2
+
Vm
−
D2
Nonconducting
(a)
Nonconducting
D1
−
Vm
+
C1
+
Vm
−
C2
+
Vm
−
D2
Conducting
(b)

FIG. 2.126

Alternate half-cycles of operation for full-wave voltage doubler.

The peak inverse voltage across each diode is $2V_m$, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only $2V_m$ PIV rating for the diodes.

Voltage Tripler and Quadrupler

Figure 2.127 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit

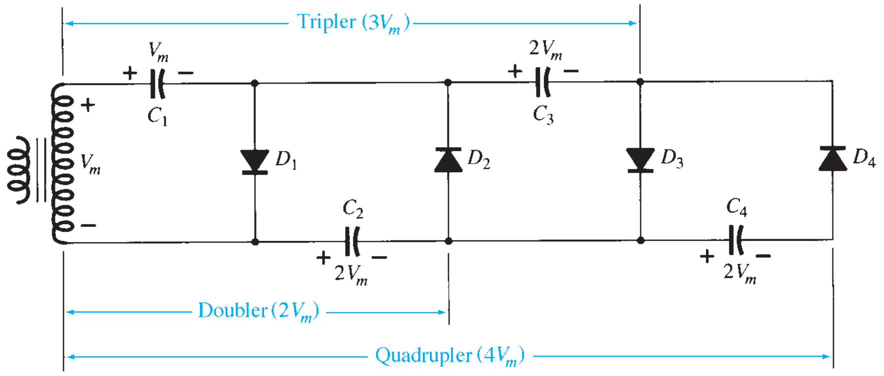

Tripler (3Vm)
Vm
+
−
C1
2Vm
+
−
C3
+
Vm
−
D1
D2
D3
D4
C2
+
−
2Vm
C4
+
−
2Vm
Doubler (2Vm)
Quadrupler (4Vm)

FIG. 2.127

Voltage tripler and quadrupler.

connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_m).

In operation, capacitor C_1 charges through diode D_1 to a peak voltage V_m during the positive half-cycle of the transformer secondary voltage. Capacitor C_2 charges to twice the peak voltage, $2V_m$, developed by the sum of the voltages across capacitor C_1 and the transformer during the negative half-cycle of the transformer secondary voltage.

During the positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges capacitor C_3 to the same $2V_m$ peak voltage. On the negative half-cycle, diodes D_2 and D_4 conduct with capacitor C_3, charging C_4 to $2V_m$.

The voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 it is $3V_m$, and across C_2 and C_4 it is $4V_m$. If additional sections of diode and capacitor are used, each capacitor will be charged to $2V_m$. Measuring from the top of the transformer winding (Fig. 2.127) will provide odd multiples of V_m at the output, whereas measuring the output voltage from the bottom of the transformer will provide even multiples of the peak voltage V_m.

The transformer rating is only V_m, maximum, and each diode in the circuit must be rated at $2V_m$ PIV. If the load is small and the capacitors have little leakage, extremely high dc voltages may be developed by this type of circuit, using many sections to step up the dc voltage.

2.13 PRACTICAL APPLICATIONS

The range of practical applications for diodes is so broad that it would be virtually impossible to consider all the options in one section. However, to develop some sense for the use of the device in everyday networks, a number of common areas of application are introduced below. In particular, note that the use of diodes extends well beyond the important switching characteristic that was introduced earlier in this chapter.

Rectification

Battery chargers are a common household piece of equipment used to charge everything from small flashlight batteries to heavy-duty, marine, lead-acid batteries. Since all are plugged into a 120-V ac outlet such as found in the home, the basic construction of each is quite similar. In every charging system a *transformer* must be included to cut the ac voltage to a level appropriate for the dc level to be established. A *diode* (also called *rectifier*) arrangement must be included to convert the ac voltage, which varies with time, to a fixed dc level such as described in this chapter. Some dc chargers also include a *regulator* to provide an improved dc level (one that varies less with time or load). Since the car battery charger is one of the most common, it will be described in the next few paragraphs.

The outside appearance and the internal construction of a Sears 6/2 AMP Manual Battery Charger are provided in Fig. 2.128. Note in Fig. 2.128b that the transformer (as in most chargers) takes up most of the internal space. The additional air space and the holes in the casing are there to ensure an outlet for the heat that develops due to the resulting current levels.

The schematic of Fig. 2.129 includes all the basic components of the charger. Note first that the 120 V from the outlet are applied directly across the primary of the transformer. The charging rate of 6 A or 2 A is determined by the switch, which simply controls how many windings of the primary will be in the circuit for the chosen charging rate. If the battery is charging at the 2-A level, the full primary will be in the circuit, and the ratio of the turns in the primary to the turns in the secondary will be a maximum. If it is charging at the 6-A level, fewer turns of the primary are in the circuit, and the ratio drops. When you study transformers, you will find that the voltage at the primary and secondary is directly related to the *turns ratio*. If the ratio from primary to secondary drops, then the voltage drops also. The reverse effect occurs if the turns on the secondary exceed those on the primary.

The general appearance of the waveforms appears in Fig. 2.129 for the 6-A charging level. Note that so far, the ac voltage has the same wave shape across the primary and the secondary. The only difference is in the peak value of the waveforms. Now the diodes take

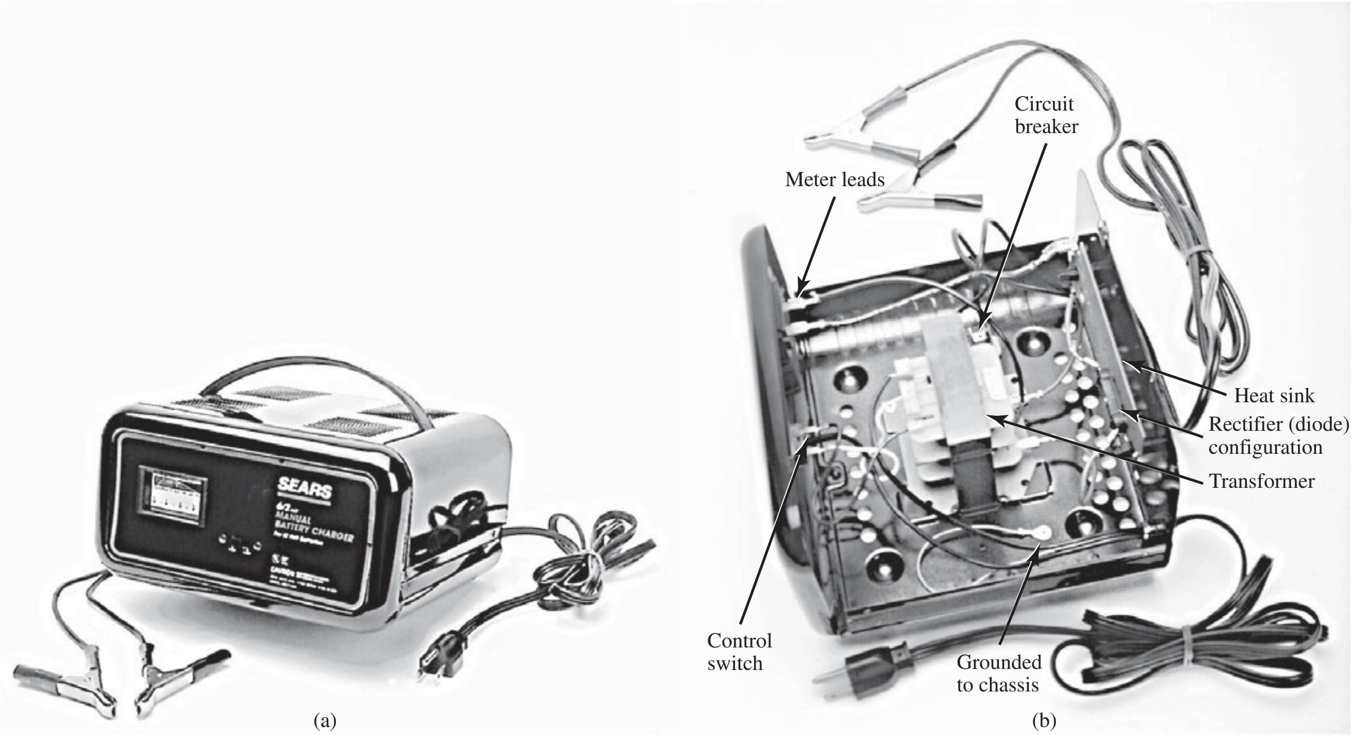

Circuit breaker
Meter leads
Heat sink
Rectifier (diode) configuration
Transformer
Control switch
Grounded to chassis
(a)
(b)

FIG. 2.128
Battery charger: (a) external appearance; (b) internal construction.

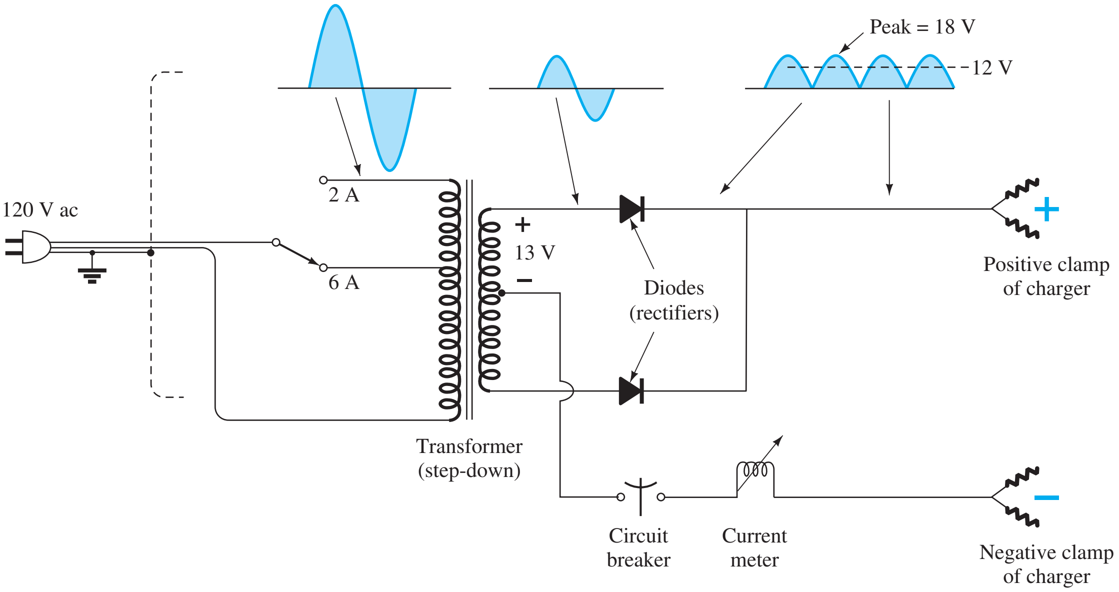

Peak = 18 V
12 V
120 V ac
2 A
6 A
+
13 V
−
Diodes (rectifiers)
Transformer (step-down)
Positive clamp of charger
+
Circuit breaker
Current meter
Negative clamp of charger
−

FIG. 2.129
Electrical schematic for the battery charger of Fig. 2.128.

over and convert the ac waveform, which has zero average value (the waveform above equals the waveform below), to one that has an average value (all above the axis) as shown in the same figure. For the moment simply recognize that diodes are semiconductor electronic devices that permit only conventional current to flow through them in the direction indicated by the arrow in the symbol. Even though the waveform resulting from the diode action has a pulsing appearance with a peak value of about 18 V, it will charge the 12-V battery whenever its voltage is greater than that of the battery, as shown by the shaded area.

Below the 12-V level the battery cannot discharge back into the charging network because the diodes permit current flow in only one direction.

In particular, note in Fig. 2.128b the large plate that carries the current from the rectifier (diode) configuration to the positive terminal of the battery. Its primary purpose is to provide a *heat sink* (a place for the heat to be distributed to the surrounding air) for the diode configuration. Otherwise the diodes would eventually melt down and self-destruct due to the resulting current levels. Each component of Fig. 2.129 has been carefully labeled in Fig. 2.128b for reference.

When current is first applied to a battery at the 6-A charge rate, the current demand, as indicated by the meter on the face of the instrument, may rise to 7 A or almost 8 A. However, the level of current will decrease as the battery charges until it drops to a level of 2 A or 3 A. For units such as this that do not have an automatic shutoff, it is important to disconnect the charger when the current drops to the fully charged level; otherwise, the battery will become overcharged and may be damaged. A battery that is at its 50% level can take as long as 10 hours to charge, so one should not expect it to be a 10-minute operation. In addition, if a battery is in very bad shape, with a lower than normal voltage, the initial charging current may be too high for the design. To protect against such situations, the circuit breaker will open and stop the charging process. Because of the high current levels, it is important that the directions provided with the charger be carefully read and applied.

In an effort to compare the theoretical world with the real world, a load (in the form of a headlight) was applied to the charger to permit a viewing of the actual output waveform. It is important to note and remember that **a diode with zero current through it will not display its rectifying capabilities**. In other words, the output from the charger of Fig. 2.129 will not be a rectified signal unless a load is applied to the system to draw current through the diode. Recall from the diode characteristics that when $I_D = 0$ A, $V_D = 0$ V.

By applying the headlamp as a load, however, sufficient current is drawn through the diode for it to behave like a switch and convert the ac waveform to a pulsating one as shown in Fig. 2.130 for the 6-A setting. First note that the waveform is slightly distorted by the nonlinear characteristics of the transformer and the nonlinear characteristics of the diode at low currents. The waveform, however, is certainly close to what is expected when we compare it to the theoretical patterns of Fig. 2.129. The peak value is determined from the vertical sensitivity as

$$V_{\text{peak}} = (3.3 \text{ divisions})(5 \text{ V/division}) = 16.5 \text{ V vs. the 18 V of Fig. 1.129}$$

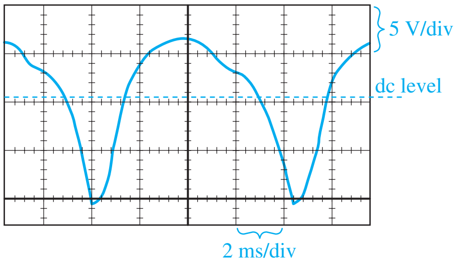


FIG. 2.130
Pulsating response of the charger of Fig. 2.129 to the application of a headlamp as a load.

with a dc level of

$$V_{\text{dc}} = 0.636V_{\text{peak}} = 0.636(16.5 \text{ V}) = 10.49 \text{ V}$$

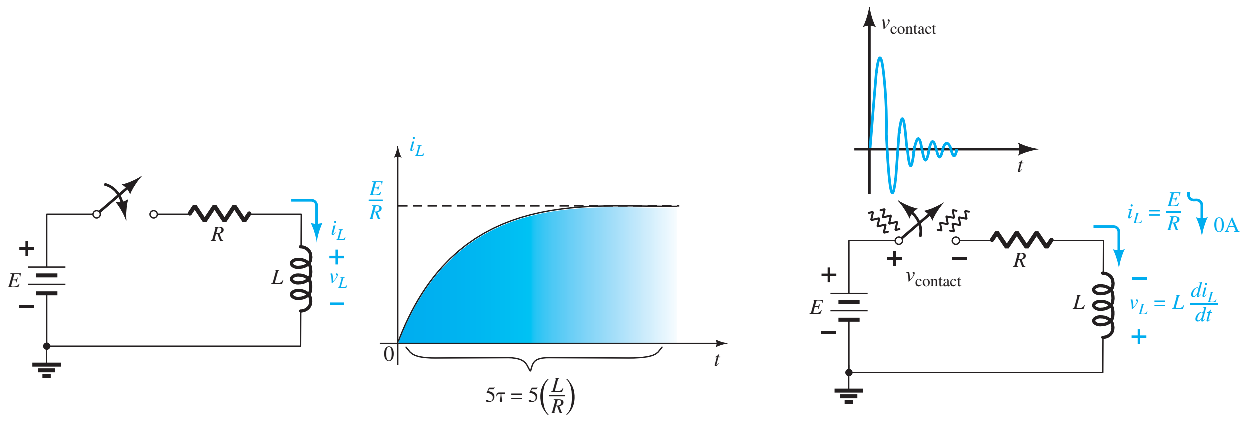
A dc meter connected across the load registered 10.41 V, which is very close to the theoretical average (dc) level of 10.49 V.

One may wonder how a charger having a dc level of 10.49 V can charge a 12-V battery to a typical level of 14 V. It is simply a matter of realizing that (as shown in Fig. 2.130) for a good deal of each pulse, the voltage across the battery will be greater than 12 V and the battery will be charging—a process referred to as **trickle charging**. In other words, charging does not occur during the entire cycle, but only when the charging voltage is more than the voltage of the battery.

Protective Configurations

Diodes are used in a variety of ways to protect elements and systems from excessive voltages or currents, polarity reversals, arcing, and shorting, to name a few. In Fig. 2.131a, the switch on a simple *RL* circuit has been closed, and the current will rise to a level determined by the applied voltage and series resistor *R* as shown on the plot. Problems arise when the switch is quickly opened as in Fig. 2.131b to essentially tell the circuit that the current must drop to zero almost instantaneously. You will remember from your basic circuits courses, however, that the inductor will not permit an instantaneous change in current through the coil. A conflict results, which will establish arcing across the contacts of the switch as the coil tries to find a path for discharge. Recall also that the voltage across an inductor is directly related to the rate of change in current through the coil ($v_L = L\,di_L/dt$). When the switch is opened, it is trying to dictate that the current change almost instantaneously, causing a very high voltage to develop across the coil that will then appear across the contacts to establish this arcing current. Levels in the thousands of volts will develop across the contacts, which will soon, if not immediately, damage the contacts and thereby the switch. The effect is referred to as an “inductive kick.” Note also that the polarity of the voltage across the coil during the “build-up” phase is opposite to that during the “release” phase. This is due to the fact that the current must maintain the same direction before and after the switch is opened. During the “build-up” phase, the coil appears as a load, whereas during the release phase, it has the characteristics of a source. In general, therefore, always keep in mind that

Trying to change the current through an inductive element too quickly may result in an inductive kick that could damage surrounding elements or the system itself.



(a)

(b)

FIG. 2.131

(a) Transient phase of a simple RL circuit; (b) arcing that results across a switch when opened in series with an RL circuit.

In Fig. 2.132a the simple network above may be controlling the action of a relay. When the switch is closed, the coil will be energized, and steady-state current levels will be established. However, when the switch is opened to deenergize the network, we have the problem introduced above because the electromagnet controlling the relay action will appear as a coil to the energizing network. One of the cheapest but most effective ways to protect the switching system is to place a capacitor (called a “snubber”) across the terminals of the coil as shown in Fig. 2.132b. When the switch is opened, the capacitor will initially appear as a short to the coil and will provide a current path that will bypass the dc supply and switch. The capacitor has the characteristics of a short (very low resistance) because of the high-frequency characteristics of the surge voltage, as shown in Fig. 2.131b. Recall that the reactance of a capacitor is determined by $X_C = 1/2\pi fC$, so the higher the frequency, the less is the resistance. Normally, because of the high surge voltages and relatively low cost, ceramic capacitors of about 0.01 μF are used. You don’t want to use large capacitors because the voltage across the capacitor will build up too slowly and will essentially slow down the

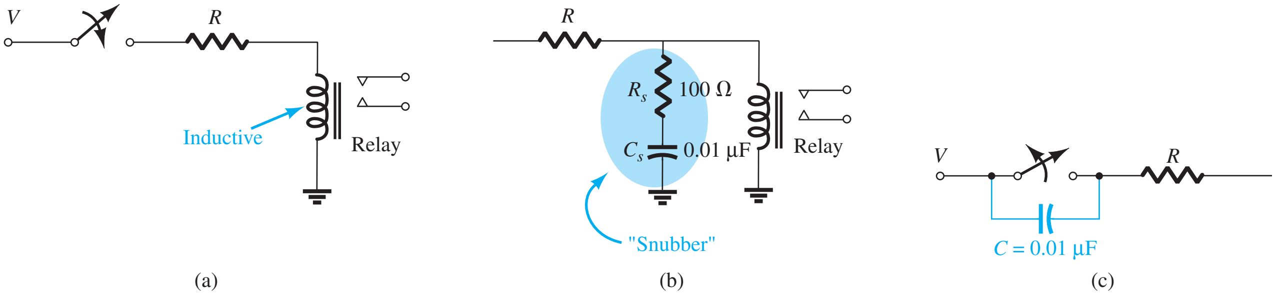


FIG. 2.132

(a) Inductive characteristics of a relay; (b) snubber protection for the configuration of part (a); (c) capacitive protection for a switch.

performance of the system. The resistor of 100 Ω in series with the capacitor is introduced solely to limit the surge current that will result when a change in state is called for. Often, the resistor does not appear because of the internal resistance of the coil as established by many turns of fine wire. On occasion, you may find the capacitor across the switch as shown in Fig. 2.132c. In this case, the shorting characteristics of the capacitor at high frequencies will bypass the contacts with the switch and extend its life. Recall that the voltage across a capacitor cannot change instantaneously. In general, therefore,

Capacitors in parallel with inductive elements or across switches are often there to act as protective elements, not as typical network capacitive elements.

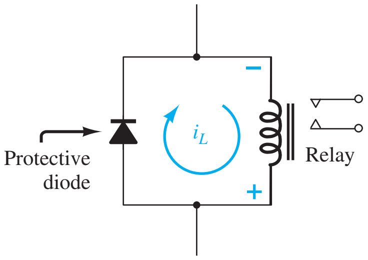


FIG. 2.133

Diode protection for an RL circuit.

Finally, the diode is often used as a protective device for situations such as above. In Fig. 2.133, a diode has been placed in parallel with the inductive element of the relay configuration. When the switch is opened or the voltage source quickly disengaged, the polarity of the voltage across the coil is such as to turn the diode on and conduct in the direction indicated. The inductor now has a conduction path through the diode rather than through the supply and switch, thereby saving both. Since the current established through the coil must now switch directly to the diode, the diode must be able to carry **the same level of current** that was passing through the coil before the switch was opened. The rate at which the current collapses will be controlled by the resistance of the coil and the diode. It can be reduced by placing an additional resistor in series with the diode. The advantage of the diode configuration over that of the snubber is that the diode reaction and behavior are not frequency dependent. However, the protection offered by the diode will not work if the applied voltage is an alternating one such as ac or a square wave since the diode will conduct for one of the applied polarities. For such alternating systems, the "snubber" arrangement would be the best option.

In the next chapter we will find that the base-to-emitter junction of a transistor is forward-biased. That is, the voltage V_{BE} of Fig. 2.134a will be about 0.7 V positive. To prevent a situation where the emitter terminal would be made more positive than the base terminal by a voltage that could damage the transistor, the diode shown in Fig. 2.134a is added. The diode will prevent the reverse-bias voltage V_{EB} from exceeding 0.7 V. On

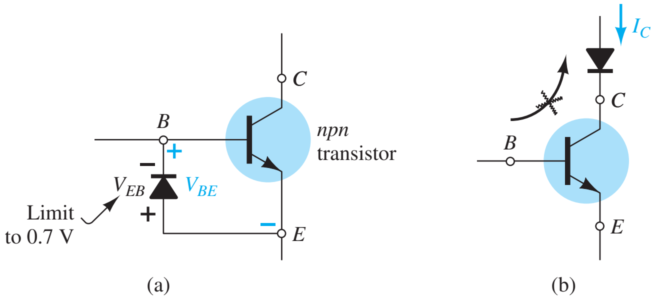


FIG. 2.134

(a) Diode protection to limit the emitter-to-base voltage of a transistor; (b) diode protection to prevent a reversal in collector current.

occasion, you may also find a diode in series with the collector terminal of a transistor as shown in Fig. 2.134b. Normal transistor action requires that the collector be more positive than the base or emitter terminal to establish a collector current in the direction shown. However, if a situation arises where the emitter or base terminal is at a higher potential than the collector terminal, the diode will prevent conduction in the opposite direction. In general, therefore,

Diodes are often used to prevent the voltage between two points from exceeding 0.7 V or to prevent conduction in a particular direction.

As shown in Fig. 2.135, diodes are often used at the input terminals of systems such as op-amps to limit the swing of the applied voltage. For the 400-mV level the signal will pass undisturbed to the input terminals of the op-amp. However, if the voltage jumps to a level of 1 V, the top and bottom peaks will be clipped off before appearing at the input terminals of the op-amp. Any clipped-off voltage will appear across the series resistor R_1.

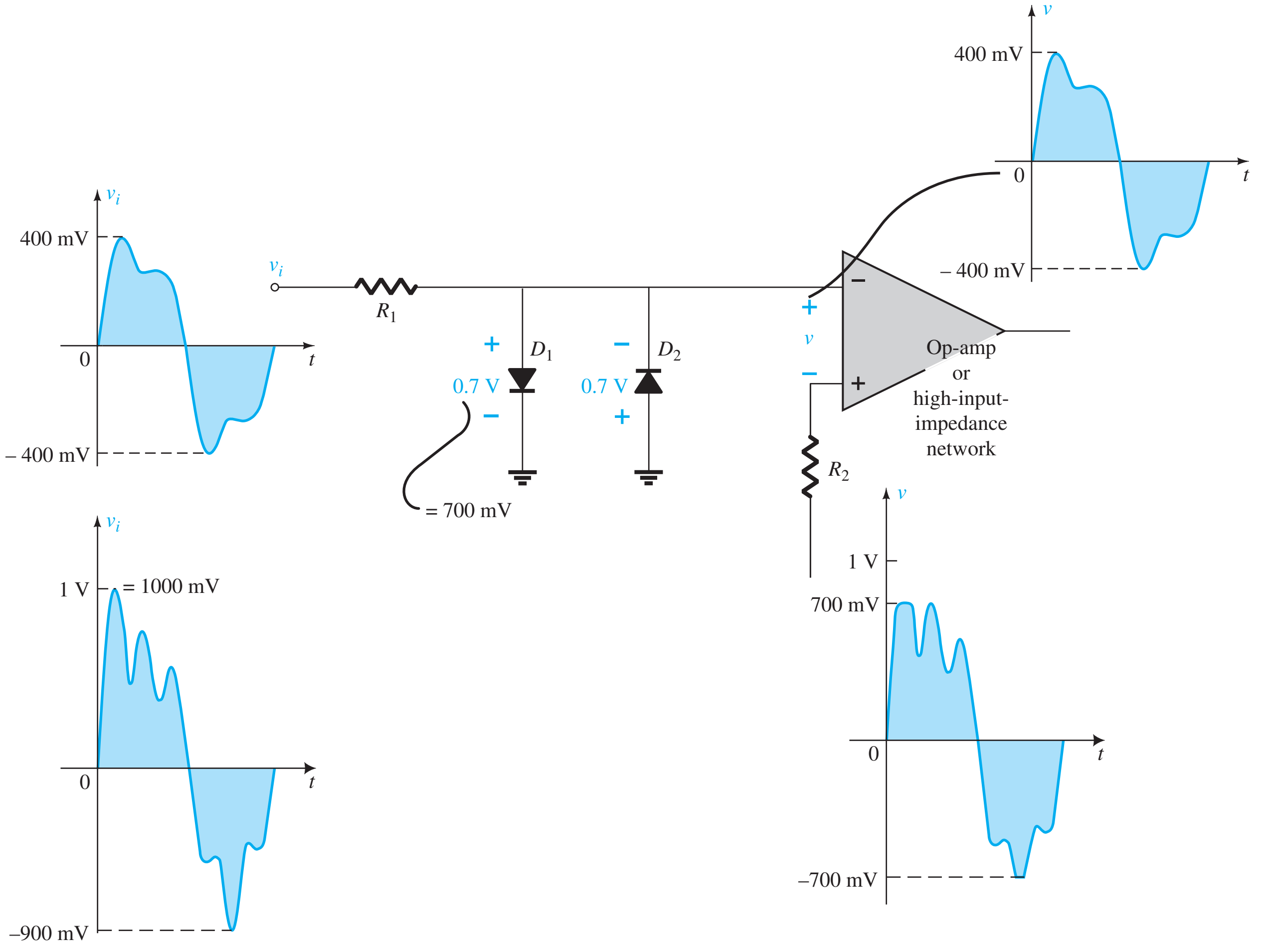


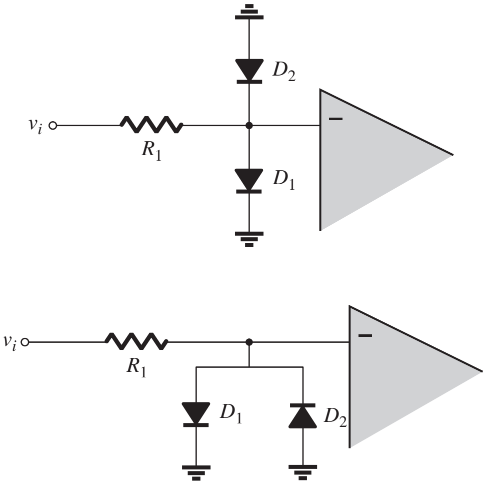
FIG. 2.135

Diode control of the input swing to an op-amp or a high-input-impedance network.

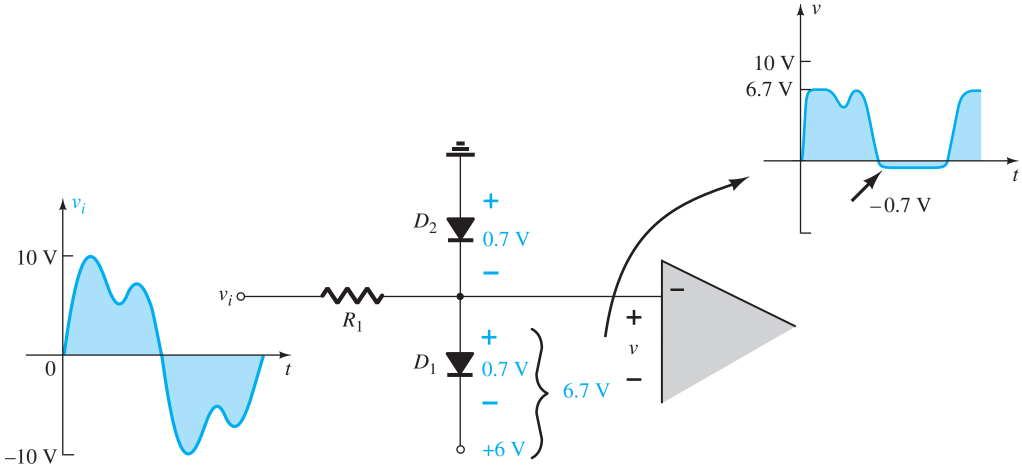
The controlling diodes of Fig. 2.135 may also be drawn as shown in Fig. 2.136 to control the signal appearing at the input terminals of the op-amp. In this example, the diodes are acting more like shaping elements than as limiters as in Fig. 2.135. However, the point is that

The placement of elements may change, but their function may still be the same. Do not expect every network to appear exactly as you studied it for the first time.

In general, therefore, don't always assume that diodes are used simply as switches. There is a wide variety of uses for diodes as protective and limiting devices.


v_i
R_1
D_2
D_1
−
v_i
R_1
D_1
D_2
−

(a)


v_i
10 V
0
−10 V
t
v_i
R_1
D_2
+
0.7 V
−
D_1
+
0.7 V
−
+6 V
6.7 V
+
v
−
−
v
10 V
6.7 V
t
−0.7 V

(b)

FIG. 2.136

(a) Alternate appearances for the network of Fig. 2.135; (b) establishing random levels of control with separate dc supplies.

Polarity Insurance

There are numerous systems that are very sensitive to the polarity of the applied voltage. For instance, in Fig. 2.137a, assume for the moment that there is a very expensive piece of equipment that would be damaged by an incorrectly applied bias. In Fig. 2.137b the correct applied bias is shown on the left. As a result, the diode is reverse-biased, but the system works just fine—the diode has no effect. However, if the wrong polarity is applied as

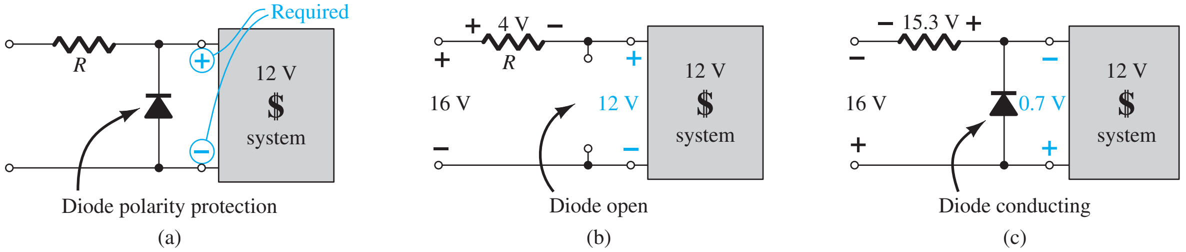

R
Required
+
−
12 V
$
system
Diode polarity protection
(a)
+ 4 V −
R
+
16 V
−
+
12 V
−
12 V
$
system
Diode open
(b)
− 15.3 V +
−
16 V
+
−
0.7 V
+
12 V
$
system
Diode conducting
(c)

FIG. 2.137

(a) Polarity protection for an expensive, sensitive piece of equipment; (b) correctly applied polarity; (c) application of the wrong polarity.

shown in Fig. 2.137c, the diode will conduct and ensure that no more than 0.7 V will appear across the terminals of the system, protecting it from excessive voltages of the wrong polarity. For either polarity, the difference between the applied voltage and the load or diode voltage will appear across the series source or network resistance.

In Fig. 2.138 a sensitive measuring movement cannot withstand voltages greater than 1 V of the wrong polarity. With this simple design the sensitive movement is protected from voltages of the wrong polarity of more than 0.7 V.

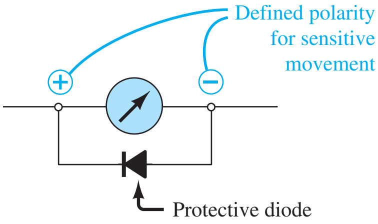


FIG. 2.138
Protection for a sensitive meter movement.

Controlled Battery-Powered Backup

In numerous situations a system should have a backup power source to ensure that the system will still be operational in case of a loss of power. This is especially true of security systems and lighting systems that must turn on during a power failure. It is also important when a system such as a computer or a radio is disconnected from its ac-to-dc power conversion source to a portable mode for traveling. In Fig. 2.139 the 12-V car radio operating off the 12-V dc power source has a 9-V battery backup system in a small compartment in the back of the radio ready to take over the role of saving the clock mode and the channels stored in memory when the radio is removed from the car. With the full 12 V available from the car, D_1 is conducting, and the voltage at the radio is about 11.3 V. D_2 is reverse-biased (an open circuit), and the reserve 9-V battery inside the radio is disengaged. However, when the radio is removed from the car, D_1 will no longer be conducting because the 12-V source is no longer available to forward-bias the diode. However, D_2 will be forward-biased by the 9-V battery, and the radio will continue to receive about 8.3 V to maintain the memory that has been set for components such as the clock and the channel selections.

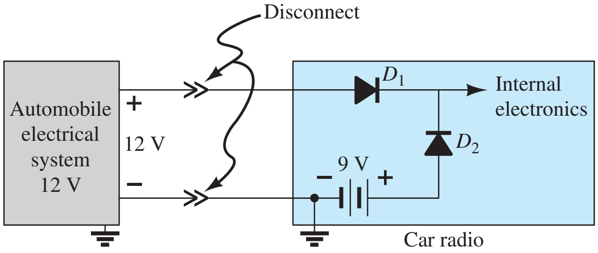


FIG. 2.139
Backup system designed to prevent the loss of memory in a car radio when the radio is removed from the car.

Polarity Detector

Through the use of LEDs of different colors, the simple network of Fig. 2.140 can be used to check the polarity at any point in a dc network. When the polarity is as indicated for the applied 6 V, the top terminal is positive, D_1 will conduct along with LED1, and a green light will result. Both D_2 and LED2 will be back-biased for the above polarity. However, if the polarity at the input is reversed, D_2 and LED2 will conduct, and a red light will appear, defining the top lead as the lead at the negative potential. It would appear that the

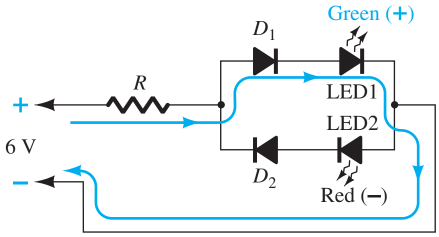


FIG. 2.140
Polarity detector using diodes and LEDs.

network would work without diodes D_1 and D_2. However, in general, LEDs do not like to be reverse-biased because of sensitivity built in during the doping process. Diodes D_1 and D_2 offer a series open-circuit condition that provides some protection to the LEDs. In the forward-bias state, the additional diodes D_1 and D_2 reduce the voltage across the LEDs to more common operating levels.

Displays

Some of the primary concerns of using electric light bulbs in exit signs are their limited lifetime (requiring frequent replacement); their sensitivity to heat, fire, and so on; their durability factor when catastrophic accidents occur; and their high voltage and power requirements. For this reason LEDs are often used to provide the longer life span, higher durability levels, and lower demand voltage and power levels (especially when the reserve dc battery system has to take over).

In Fig. 2.141 a control network determines when the EXIT light should be on. When it is on, all the LEDs in series will be on, and the EXIT sign will be fully lit. Obviously, if one of the LEDs should burn out and open up, the entire section will turn off. However, this situation can be improved by simply placing parallel LEDs between every two points. Lose one, and you will still have the other parallel path. Parallel diodes will, of course, reduce the current through each LED, but two at a lower level of current can have a luminescence similar to one at twice the current. Even though the applied voltage is ac, which means that the diodes will turn on and off as the 60-Hz voltage swings positive and negative, the persistence of the LEDs will provide a steady light for the sign.

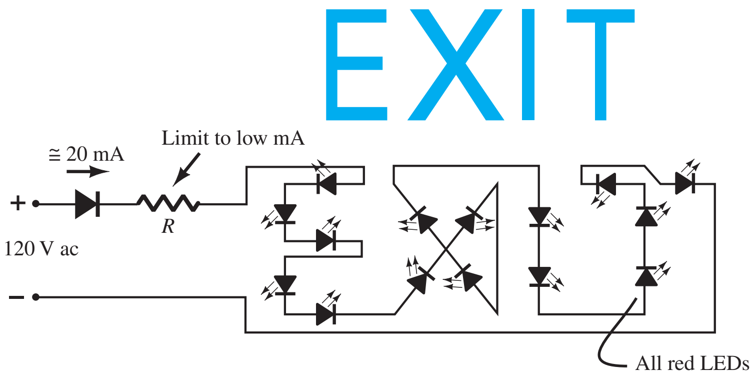


FIG. 2.141
EXIT sign using LEDs.

Setting Voltage Reference Levels

Diodes and Zeners can be used to set reference levels as shown in Fig. 2.142. The network, through the use of two diodes and one Zener diode, is providing three different voltage levels.

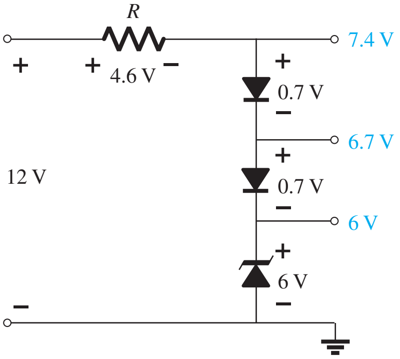


FIG. 2.142
Providing different reference levels using diodes.

Establishing a Voltage Level Insensitive to the Load Current

As an example that clearly demonstrates the difference between a resistor and a diode in a voltage-divider network, consider the situation of Fig. 2.143a, where a load requires about 6 V to operate properly but a 9-V battery is all that is available. For the moment let us assume that operating conditions are such that the load has an internal resistance of 1 kΩ. Using the voltage-divider rule, we can easily determine that the series resistor should be 470 Ω (commercially available value) as shown in Fig. 2.143b. The result is a voltage across the load of 6.1 V, an acceptable situation for most 6-V loads. However, if the operating conditions of the load change and the load now has an internal resistance of only 600 Ω, the load voltage will drop to about 4.9 V, and the system will not operate correctly. This sensitivity to the load resistance can be eliminated by connecting four diodes in series with the load as shown in Fig. 2.143c. When all four diodes conduct, the load voltage will be

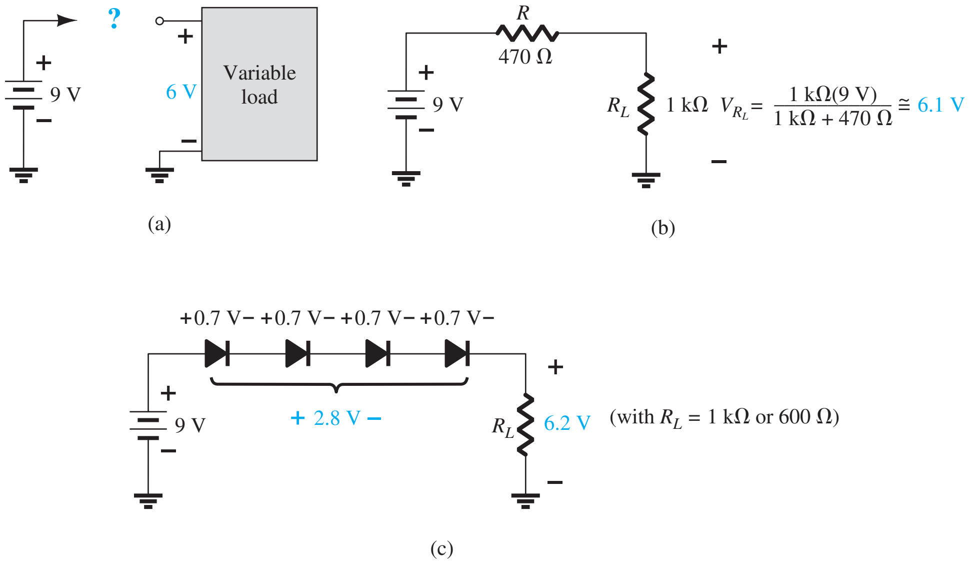

?
+
9 V
−
+
6 V
Variable load
−
(a)
R
470 Ω
+
9 V
−
R_L
1 kΩ
+
−
$V_{R_L} = \frac{1\ \text{k}\Omega(9\ \text{V})}{1\ \text{k}\Omega + 470\ \Omega} \cong 6.1\ \text{V}$
(b)
+0.7 V− +0.7 V− +0.7 V− +0.7 V−
+
9 V
−
+ 2.8 V −
+
R_L
6.2 V
(with R_L = 1 kΩ or 600 Ω)
−
(c)

FIG. 2.143

(a) How to drive a 6-V load with a 9-V supply (b) using a fixed resistor value. (c) Using a series combination of diodes.

about 6.2 V, irrespective of the load impedance (within device limits, of course)—the sensitivity to the changing load characteristics has been removed.

AC Regulator and Square-Wave Generator

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.144a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.144b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, whereas the impedance of Z_2 is quite large, corresponding to the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and the output will continue to duplicate each other until v_i reaches 20 V. Then Z_2 will “turn on” (as a Zener diode), whereas Z_1 will be in a region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a

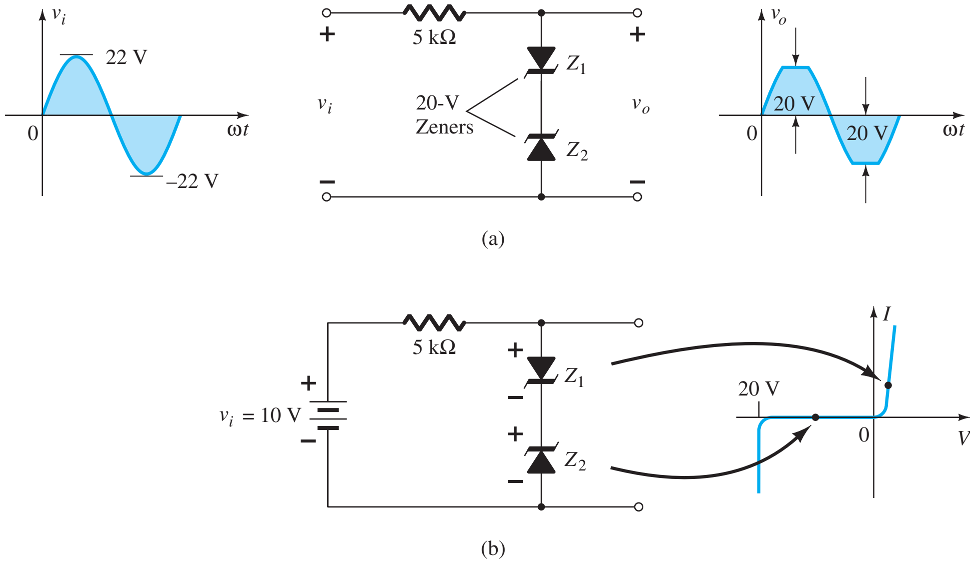

v_i
22 V
0
ωt
−22 V
5 kΩ
+
+
v_i
20-V Zeners
Z_1
Z_2
v_o
−
−
v_o
20 V
0
20 V
ωt
(a)
5 kΩ
+
v_i = 10 V
−
+
Z_1
−
+
Z_2
−
I
20 V
0
V
(b)

FIG. 2.144

Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

short circuit. The resulting output for the full range of v_i is provided in Fig. 2.144a. Note that the waveform is not purely sinusoidal, but its root mean square (rms) value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.144b can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.145 with the resulting output waveform.

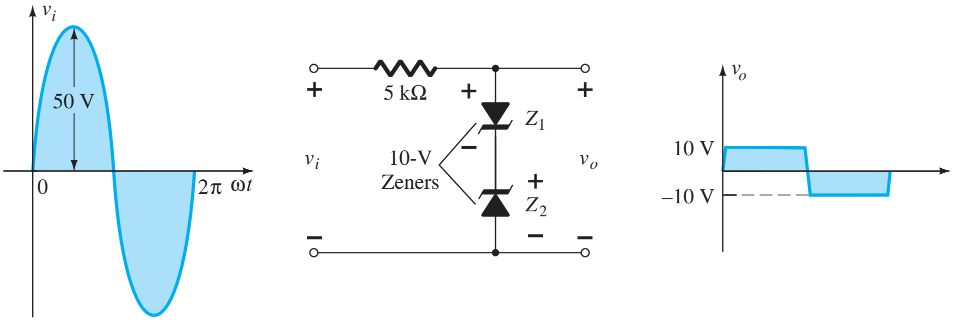


FIG. 2.145
Simple square-wave generator.

2.14 SUMMARY

Important Conclusions and Concepts

1. The characteristics of a diode are **unaltered** by the network in which it is employed. The network simply determines the point of operation of the device.
2. The operating point of a network is determined by the **intersection** of the network equation and an equation defining the characteristics of the device.
3. For most applications, the characteristics of a diode can be defined simply by the **threshold voltage in the forward-bias region** and an open circuit for applied voltages less than the threshold value.
4. To determine the state of a diode, simply **think of it initially as a resistor**, and find the polarity of the voltage across it and the direction of conventional current through it. If the voltage across it has a forward-bias polarity and the **current has a direction that matches the arrow in the symbol**, the diode is conducting.
5. To determine the state of diodes used in a logic gate, first make an **educated guess** about the state of the diodes, and then **test your assumptions**. If your estimate is incorrect, refine your guess and try again until the analysis verifies the conclusions.
6. Rectification is a process whereby an applied waveform of **zero average value** is changed to one that **has a dc level**. For applied signals of more than a few volts, the ideal diode approximations can normally be applied.
7. It is very important that the PIV rating of a diode be checked when choosing a diode for a particular application. Simply determine the **maximum voltage** across the diode under **reverse-bias conditions**, and compare it to the nameplate rating. For the typical half-wave and full-wave bridge rectifiers, it is the peak value of the applied signal. For the CT transformer full-wave rectifier, it is twice the peak value (which can get quite high).
8. Clippers are networks that "**clip**" away part of the applied signal either to create a specific type of signal or to limit the voltage that can be applied to a network.
9. Clampers are networks that "**clamp**" the input signal to a different dc level. In any event, the peak-to-peak swing of the applied signal will remain the same.
10. Zener diodes are diodes that make effective use of the **Zener breakdown potential** of an ordinary p–n junction characteristic to provide a device of wide importance and application. For Zener conduction, the direction of conventional flow is **opposite to the arrow in the symbol**. The polarity under conduction is also **opposite to that of the conventional diode**.

11. To determine the state of a Zener diode in a dc network, simply remove the Zener from the network, and determine the **open-circuit voltage** between the two points where the Zener diode was originally connected. If it is **more than the Zener potential** and has the correct polarity, the Zener diode is in the "on" state.
12. A half-wave or full-wave voltage doubler employs two capacitors; a tripler, three capacitors; and a quadrupler, four capacitors. In fact, for each, the number of diodes equals the number of capacitors.

Equations

Approximate:

Silicon: $V_K = 0.7\text{ V}$; I_D is determined by network.
Germanium: $V_K = 0.3\text{ V}$; I_D is determined by network.
Gallium arsenide: $V_K = 1.2\text{ V}$; I_D is determined by network.

Ideal:

$V_K = 0\text{ V}$; I_D is determined by network.

For conduction:

$$V_D \geq V_K$$

Half-wave rectifier:

$$V_{\text{dc}} = 0.318V_m$$

Full-wave rectifier:

$$V_{\text{dc}} = 0.636V_m$$

2.15 COMPUTER ANALYSIS

Cadence OrCAD

Series Diode Configuration In the previous chapter the OrCAD 16.3 folder was established as the location for our projects. This section will define the name of our project, set up the software for the analysis to be performed, describe how to build a simple circuit, and, finally, perform the analysis. The coverage will be quite extensive since this will be the first true exposure to the mechanics associated with using the software package. In the chapters to follow you will find the analysis can be performed quite rapidly to obtain results that confirm the long-hand solutions.

Our first project can now be initiated by double-clicking on the **OrCAD Capture CIS Demo** icon on the screen, or you can use the sequence **Start–All Programs–Cadence–OrCAD 16.3 Demo**. The resulting screen has only a few active keys on the top toolbar. The first at the top left is the **Create document** key (or you can use the sequence **File-New-Project**). Selecting the key will result in a **New Project** dialog box, in which the **Name** of the project must be entered. For our purposes we will choose **OrCAD 2-1** as shown in the heading of Fig. 2.146, and select **Analog or Mixed A/D** (to be used for all the analyses of this text). Note at the bottom of the dialog box that the **Location** appears as **C:\OrCAD 16.3** as set earlier. Click **OK**, and another dialog box will appear titled **Create PSpice Project**. Select **Create a blank project** (again, for all the analyses to be performed in this text). Click **OK**, and additional keys will be turned on along with additional toolbars. A **Project Manager Window** will appear with **OrCAD 2-1** as its heading. The new project listing will appear with an icon and an associated + sign in a small square. Clicking on the + sign will take the listing a step further to **SCHEMATIC1**. Click + again (to the left of SCHEMATIC1), and **PAGE1** will appear; clicking on a − sign will reverse the process. Double-clicking on **PAGE1** will create a working window titled **SCHEMATIC1: PAGE1**, revealing that a project can have more than one schematic file and more than one associated page. The width and the height of the window can be adjusted by grabbing an edge to obtain a double-headed arrow and dragging the border to the desired location. Either window on the screen can be moved by clicking on the top heading to make it dark blue and then dragging it to any location.

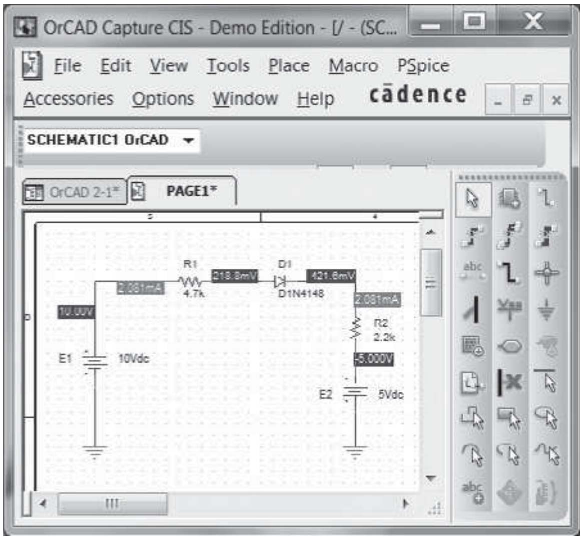

OrCAD Capture CIS - Demo Edition - [/ - (SC...
File Edit View Tools Place Macro PSpice
Accessories Options Window Help
cādence
SCHEMATIC1 OrCAD
OrCAD 2-1*
PAGE1*
R1
4.7k
218.8mV
D1
D1N4148
421.6mV
2.081mA
10.00V
E1
10Vdc
2.081mA
R2
2.2k
-5.000V
E2
5Vdc

FIG. 2.146
Cadence OrCAD analysis of a series diode configuration.

Now we are ready to build the simple circuit of Fig. 2.146. Select the **Place part** key (the top key on the far right vertical toolbar that looks like an integrated circuit with a positive sign in the bottom right corner) to obtain the **Place Part** dialog box. Since this is the first circuit to be constructed, we must ensure that the parts appear in the list of active libraries. Go to **Libraries** and select the **Add Library** key (looks like a dashed rectangular box with a yellow star in the top left corner). The result is a **Browse File** in which **analog.olb** can be selected, followed by **Open** to place it in the active list of **Libraries**. Repeat the process to add the **eval.olb** and **source.olb** libraries. All three libraries will be required to build the networks appearing in this text. However, it is important to realize that:

Once the library files have been selected, they will appear in the active listing for each new project without having to add them each time—a step, such as the Folder step above, that does not have to be repeated with each similar project.

Click the small X in the top right corner of the dialog box to remove the **Place Part** dialog box. We can now place components on the screen. For the dc voltage source, first select the **Place Part** key and then select **SOURCE** in the library listing. Under **Part List**, a list of available sources will appear; select **VDC** for this project. Once **VDC** has been selected, its symbol, label, and value will appear on the picture window at the bottom left of the dialog box. Click the **Place Part** key on the top of the dialog box, and the **VDC** source will follow the cursor across the screen. Move it to a convenient location, left-click the mouse, and it will be set in place as shown in Fig. 2.146.

Since a second source is present in Fig. 2.146, move the cursor to the general area of the second source and click it in place. Since this is the last source to appear in the network, execute a right click of the mouse and select **End Mode**. Choosing this option will end the procedure, leaving the last source in a red dashed box. The fact that it is red indicates that it is still in the active mode and can be operated on. One more click of the mouse, and the second source will be in place and the red active status removed. The second source can be rotated 180° to match Fig. 2.146 by first clicking the source to make it red (active) to obtain a long list of options and select **Rotate**. Since each rotation only turns it 90° counterclockwise, two rotations will be required. The rotations can also be accomplished using the sequence **Ctrl-R**.

One of the most important steps in the procedure is to ensure that a 0-V ground potential is defined for the network so that voltages at any point in the network have a reference point. *The result is a requirement that every network must have a ground defined.* For our purposes, the **0/SOURCE** option will be our choice when the **GND** key is selected. It is obtained by selecting the ground symbol in the middle of the far right toolbar to obtain the **Place Ground** dialog box. Scroll down until **0/SOURCE** is selected and click **OK**. The result is a ground that can be placed anywhere on the screen. As with the voltage source, multiple grounds can be added by simply going from one point to another. The process is ended with a right click and the **End Mode** option.

The next step will be to place the resistors of the network of Fig. 2.146. This is accomplished by selecting the **Place Part** key again and then selecting the **ANALOG** library. Scrolling the options, note that **R** will appear and should be selected. Click the **Place Part** key, and the resistor will appear next to the cursor on the screen. Move it to the desired location and click it in place. The second resistor can be placed by simply moving to the general area of its location in Fig. 2.146 and clicking it in place. Since there are only two resistors, the process can be ended by making a right click of the mouse and selecting **End Mode**. The second resistor will have to be rotated to the vertical position using the same procedure described for the second voltage source.

The last element to be placed is the diode. Selecting the **Place Part** keypad will again result in the **Place Part** dialog box, in which the **EVAL** library is chosen from the **Libraries** listing. Then type **D** under **Part** heading and select **D14148** under **Part List** followed by the **Place Part** command to place on the screen in the same manner described for the source and resistors.

Now that all the components are on the screen you may want to move them to positions corresponding directly with Fig. 2.146. This is accomplished by simply clicking on the element and holding the left-click down as you move the element.

All the required elements are on the screen, but they need to be connected. This is accomplished by selecting the **Place wire** key, which looks like a step, near the top of the toolbar to the left of the toolbar with the **Place Part** key. The result is a crosshair with a center that should be placed at the point to be connected. Place the crosshair at the top of the voltage source, and left-click it once to connect it to that point. Then draw a line to the end of the next element, and click the mouse again when the crosshair is at the correct point. A red line will result with a square at each end to confirm that the connection has been made. Then move the crosshair to the other elements, and build the circuit. Once everything is connected, a right click will provide the **End Mode** option. Don't forget to connect the source to ground as shown in Fig. 2.146.

Now we have all the elements in place, but their labels and values are wrong. To change any parameter, simply double-click on the parameter (the label or the value) to obtain the **Display Properties** dialog box. Type in the correct label or value, click **OK**, and the quantity is changed on the screen. The labels and values can be moved by simply clicking on the center of the parameter until it is closely surrounded by the four small squares and then dragging it to the new location. Another left click, and it is deposited in its new location.

Finally, we can initiate the analysis process, called **Simulation**, by selecting the **New Simulation Profile** key near the top left of the display—it resembles a data page with a star in the top right corner. A **New Simulation** dialog box will result that first asks for the **Name** of the simulation. **OrCAD 2-1** is entered, and **none** is left in the **Inherit From** request. Then select **Create**, and a **Simulation Setting** dialog box will appear in which **Analysis-Analysis Type-Bias Point** is sequentially selected. Click **OK**, and select the **Run** key (which looks like an isolated arrowhead in a green background) or choose **PSpice-Run** from the menu bar. An **Output Window** will result that appears to be somewhat inactive. It will not be used in the current analysis, so close (X) the window, and the circuit of Fig. 2.146 will appear with the voltage and current levels of the network. The voltage, current, or power levels can be removed (or replaced) from the display by simply selecting the **V**, **I**, or **W** in the third toolbar from the top. Individual values can be removed by simply selecting the value and pressing the **Delete** key. Resulting values can be moved by simply left-clicking the value and dragging it to the desired location.

The results of Fig. 2.146 show that the current through the series configuration is 2.081 mA through each element, compared to the 2.072 mA of Example 2.9. The voltage across the diode is 218.8 mV $-$ ($-$421.6 mV) $\cong$ 0.64 V, compared to the 0.7 V applied in the long-hand solution of Example 2.9. The voltage across R_1 is 10 V $-$ 218.8 mV $\cong$ 9.78 V, compared to 9.74 V in the long-hand solution. The voltage across the resistor R_2 is 5 V $-$ 421.6 mV $\cong$ 4.58 V, compared to 4.56 V in Example 2.9.

To understand the differences between the two solutions, one must be aware that the diode has internal characteristics that affect its behavior such as the reverse saturation current and its resistance levels at different current levels. Those characteristics can be viewed through the sequence **Edit-PSpice Model** resulting in the **PSpice Model Editor Demo** dialog box.

You will find that the default value of the reverse saturation current is 2.682 nA—a quantity that can have an important effect on the characteristics of the device. If we choose I_s = 3.5E-15A (a value determined by trial and error) and delete the other parameters for the device, a new simulation of the network will result in the response of Fig. 2.147. Now the current through the circuit is 2.072 mA, which is an exact match with the result of Example 2.9. The voltage across the diode is 260.2 mV + 440.9 mV ≅ 0.701 V, or essentially 0.7 V, and the voltage across each resistor is exactly as obtained in the long-hand solution. In other words, by choosing this value of reverse saturation current, we created a diode with characteristics that permitted the approximation that $V_D = 0.7$ V when in the "on" state.

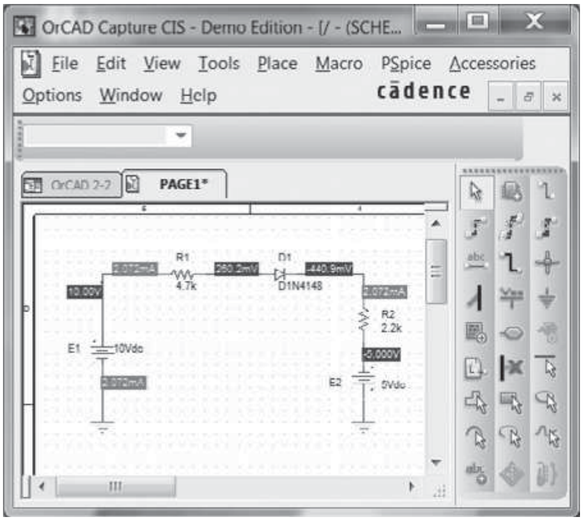


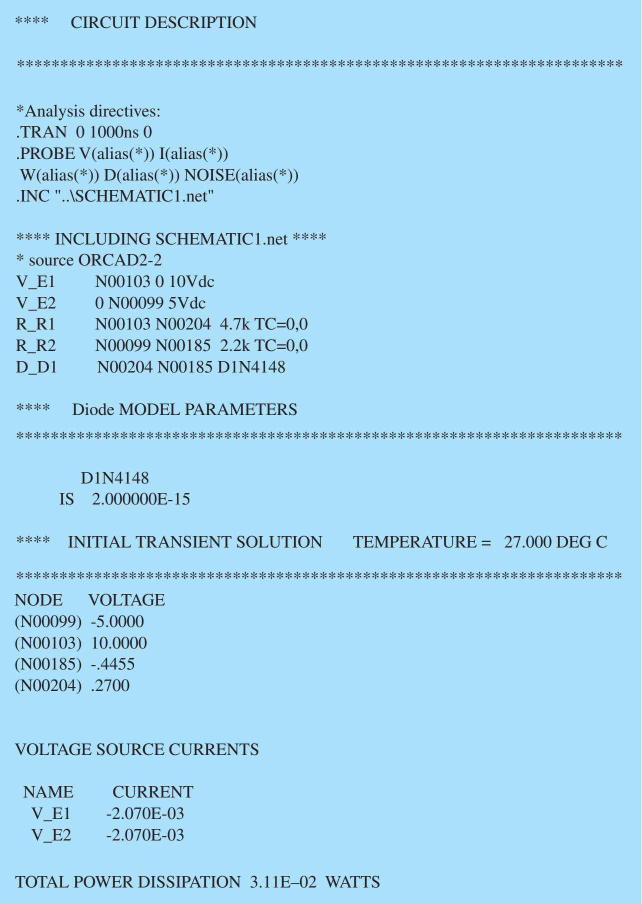
FIG. 2.147

The circuit of Fig. 2.146 reexamined with I_s set at 3.5E-15A.

The results can also be viewed in tabulated form by selecting **PSpice** at the head of the screen followed by **View Output File**. The result is the listing of Fig. 2.148 (modified to conserve space), which includes the **CIRCUIT DESCRIPTION** with all the components of the network, the **Diode MODEL PARAMETERS** with the chosen **Is** value, and the **INITIAL TRANSIENT SOLUTION** with the dc voltage levels, current levels, and total power dissipation.

The analysis is now complete for the diode circuit of interest. Granted, there was a wealth of information provided to establish and investigate this rather simple network. However, the vast majority of this material will not be repeated in the PSpice examples to follow, which will have a dramatic effect on the length of the descriptions. For practice purposes, it is suggested that other examples in this chapter be checked using PSpice and that the exercises at the end of the chapter be investigated to develop confidence in applying the software package.

Diode Characteristics The characteristics of the D1N4148 diode used in the above analysis will now be obtained using a few maneuvers somewhat more sophisticated than those employed in the first example. The process begins by first building the network of Fig. 2.149 using the procedures just described. Note in particular that the source is labeled **E** and set at **0V** (its initial value). Next the **New Simulation Profile** icon is selected from the toolbar to obtain the **New Simulation** dialog box. For the **Name**, Fig. 2-150 is entered since it is the location of the graph to be obtained. **Create** is then selected and the **Simulation Settings** dialog box will appear. Under **Analysis Type**, **DC Sweep** is chosen because we want to sweep through a range of values for the source voltage. When **DC Sweep** is selected a list of options will simultaneously appear in the right-hand region of the dialog box, requiring that some choices be made. Since we plan to sweep through a range of voltages, the **Sweep variable** is a **Voltage source**. Its name must be entered as **E** as appearing in Fig. 2.149. The sweep will be **Linear** (equal space between data points) with a **Start value** of 0 V, **End Value** of 10 V, and an **Increment** of 0.01 V. After making all the entries, click **OK** and the



```
****    CIRCUIT DESCRIPTION

******************************************************************************

*Analysis directives:
.TRAN  0 1000ns 0
.PROBE V(alias(*)) I(alias(*))
 W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"

**** INCLUDING SCHEMATIC1.net ****
* source ORCAD2-2
V_E1        N00103 0 10Vdc
V_E2        0 N00099 5Vdc
R_R1        N00103 N00204  4.7k TC=0,0
R_R2        N00099 N00185  2.2k TC=0,0
D_D1        N00204 N00185 D1N4148

****    Diode MODEL PARAMETERS
******************************************************************************

           D1N4148
       IS    2.000000E-15

****    INITIAL TRANSIENT SOLUTION      TEMPERATURE =   27.000 DEG C

******************************************************************************
NODE      VOLTAGE
(N00099)  -5.0000
(N00103)  10.0000
(N00185)  -.4455
(N00204)  .2700


VOLTAGE SOURCE CURRENTS

 NAME        CURRENT
  V_E1       -2.070E-03
  V_E2       -2.070E-03

TOTAL POWER DISSIPATION  3.11E–02  WATTS
```

FIG. 2.148

Output file for PSpice Windows analysis of the circuit of Fig. 2.147.

RUN PSpice option can be selected. The analysis will be performed with the source voltage changing from 0 V to 10 V in 1000 steps (as resulting from the division of 10 V/0.01 V). The result, however, is simply a graph with a horizontal scale from 0 V to 10 V.

Since the plot we want is of I_D versus V_D, we must change the horizontal (x-axis) to V_D. This is accomplished by selecting **Plot** and then **Axis Settings**. An **Axis Settings** dialog box will appear, in which choices have to be made. If **Axis Variables** is selected, an **X-Axis**

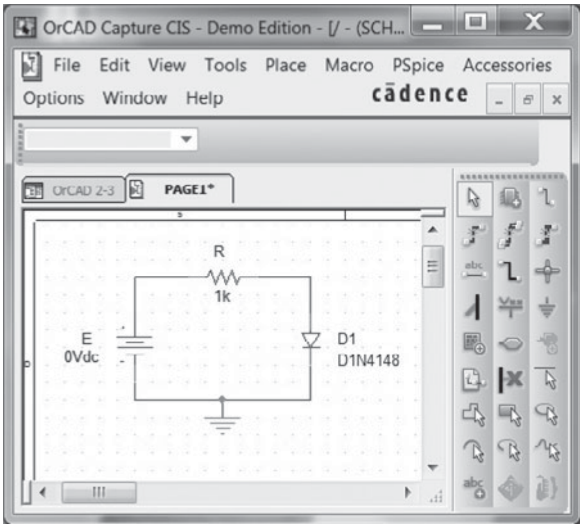

OrCAD Capture CIS - Demo Edition - [/ - (SCH...
File
Edit
View
Tools
Place
Macro
PSpice
Accessories
Options
Window
Help
cādence
OrCAD 2-3
PAGE1*
R
1k
E
0Vdc
D1
D1N4148

FIG. 2.149

Network for obtaining the characteristics of the D1N4148 diode.

Variable dialog box will appear with a list of variables that can be chosen for the *x*-axis. **V1(D1)** will be selected since it represents the voltage across the diode. If we then select **OK**, the **Axis Settings** dialog box will return, where **User Defined** is selected under the **Data Range** heading. **User Defined** is chosen because it will allow us to limit the graph to a range of 0 V to 1 V since the "on" voltage of the diode should be around 0.7 V. After entering the 0–1 V range, selecting **OK** will result in a graph with **V1(D1)** as the *x* variable with a range of 0 V to 1 V. The horizontal axis now seems to be set for the desired plot.

We must now turn our attention to the vertical axis, which should be the diode current. Choosing **Trace** followed by **Add Trace** will result in an **Add Trace** dialog box in which **I(D1)** will appear as one of the possibilities. Selecting **I(D1)** will also cause it to appear as the **Trace Expression** at the bottom of the dialog box. Selecting **OK** will then result in the diode characteristics of Fig. 2.150, clearly showing a steep rise around 0.7 V.

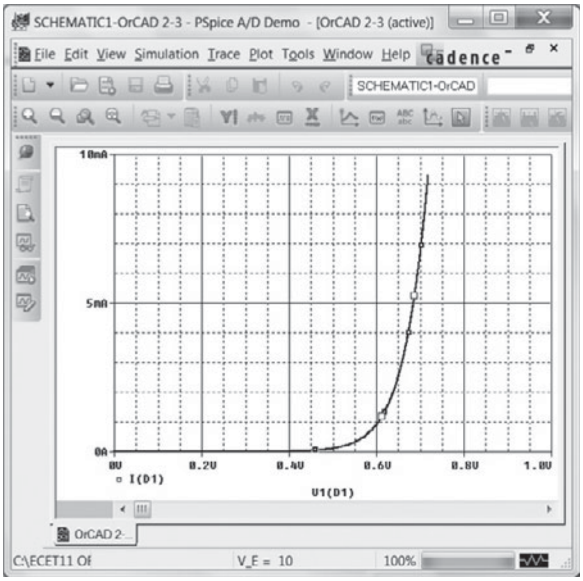

SCHEMATIC1-OrCAD 2-3 - PSpice A/D Demo - [OrCAD 2-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cadence
SCHEMATIC1-OrCAD
10mA
5mA
0A
0V
0.2V
0.4V
0.6V
0.8V
1.0V
I(D1)
V1(D1)
OrCAD 2-
C:\ECET11 Of
V_E = 10
100%

FIG. 2.150

Characteristics of the D1N4148 diode.

If we turn back to the **PSpice Model Editor** for the diode and change I_s to 3.5E-15A as in the previous example, the curve will shift to the right. Similar procedures will be used to obtain the characteristic curves for a variety of elements to be introduced in later chapters.

Multisim

Fortunately, there are a number of similarities between Cadence OrCAD and Multisim. Then again, there are a number of differences also, but the saving point is that once you become proficient in the use of one software package, the other will be much easier to learn. For those users familiar with the earlier versions of Multisim, you will find that the new version has a minimum of changes, permitting an easy transition to the new procedures.

Once the Multisim icon is chosen, a screen will appear with a vast array of toolbars. The content of each and the name of each can be found through the sequence **View-toolbars**. The result is a long vertical list of available toolbars. The content and location of each can be found by simply selecting or deleting a toolbar and noting the effect on the full screen. For our purposes the **Standard, View, Main, Components, Simulation Switch, Simulation and Instruments** will be used.

When using Multisim you have a choice between using "virtual" or "real" components. Virtual components are those that can be given any value when you build the network. The term *real* comes from the fact that the resulting list is a list of standard component values that can be purchased from a supplier. Finding a component is initiated by first selecting the second keypad (from the left) on the component toolbar that looks like a resistor. As you approach the key, the label **Place Basic** will appear. Once it is chosen, the **Select a**

Component dialog box will appear that contains a subset titled **Family**. Third down on that list is a **RATED_VIRTUAL** option with a resistor symbol. When this is selected a list of components including **RESISTOR_RATED, CAPACITOR_RATED, INDUCTOR_RATED**, and a variety of others will appear. If **RESISTOR-RATED** is selected, a resistor symbol will appear under the Symbol heading. Note that the resistor does not have a specific value. If we now select **OK** and place it on the screen in much the same way we did for the OrCAD introduction, you will find that the value was automatically labeled **R1** with a value of 1 kΩ. In order to place another resistor the same sequence must be followed, but this time the resistor will automatically be called **R2** but with the same value of 1 kΩ. This labeling process will continue in the same manner with the same 1-kΩ value for as many resistors as you place. As was done with OrCAD, the resistor labels and values can be changed quite easily. Of course, if the chosen resistor is a standard value then it can be found directly under the **RESISTOR** listing of "real" components.

We are now ready to build the diode network of Example 2.13 so we can compare results. The diodes chosen will be commercially available under the "real" listing. In this case two **1N4009** diodes were found by first selecting the keypad **Place Diode** to the right of the **Place Basic** keypad to obtain the **Select a Component** dialog box. Then the sequence **Family-DIODE-1N4009–OK** will result in a diode on the screen labeled **D1** with **1N4009** below the symbol, as shown in Fig. 2.151. Next we can place the resistors on the screen by going to the **RESISTOR** option and typing in the value of one of the resistors, in this case, the 3.3-kΩ resistor in the area provided at the top of the resistor listing. This certainly removes the need to scroll through the list looking for a particular resistor. Once found and placed, it will appear as **R1** with a value of 3.3 kΩ. The same procedure will result in a second resistor called **R2** with a value of 5.6 kΩ. In each case the elements are initially placed closest to where they will end up. The dc voltage source is found by going to the **Place Source** keypad, which is the first keypad in the **Component** toolbar. Under Family, **POWER SOURCES** is selected, followed by **DC_POWER**. Click **OK** and a voltage source will appear on the screen with the label **V1** at a level of **12 V**. The last circuit element to be set on the screen is the ground, which is accomplished by going back to the **Place Source** option and, after selecting **POWER SOURCES**, choosing "ground" under the **Component** listing. Click **OK** and the ground can be placed anywhere on the screen.

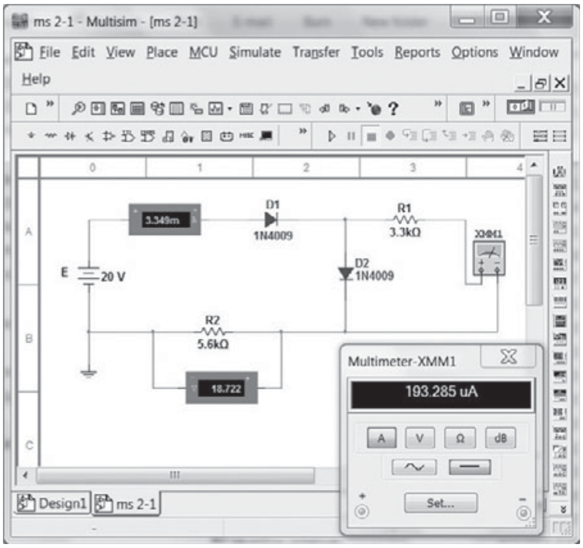


FIG. 2.151
Verifying the results of Example 2.13 using Multisim.

Now that all the components are on the screen, they must be placed and labeled properly. For each component, simply selecting the device will create a blue dashed box around it to indicate it is in the active mode. When clicked to establish this condition, it can be moved to any location on the screen. To rotate an element, establish the active mode and apply **Crtl-R** to rotate it 90 degrees. Each application of this process will rotate it an additional 90 degrees. Changing a label simply requires double-clicking the label of interest to create a small blue box around it and produce a dialog box for the change. For the source, a dialog box labeled **DC_POWER** will result, in which the heading **Label** is selected and the **refDEs** retyped as **E**. Click **OK** and the label **E** will appear. The same procedure can change the value to 20 V, although in this case the **Value** heading is chosen and the units are chosen using the scroll at the right of the entered value.

The next step is to determine what quantities are to be measured and how to measure them. For this network a multimeter will be used to measure the current through the resistor **R1**. The multimeter is found at the top of the **Instrument** toolbar. After selection it can be placed on the screen in the same manner as the other elements. Double-clicking the meter will then result in the **Multimeter-XXM1** dialog box, in which **A** is selected to set the multimeter as an ammeter. In addition, the **DC** box (a straight line) must be selected because we are dealing with dc voltages. The current through the diode **D1** and the voltage across the resistor **R2** will be found using **Indicators**, which are found as the tenth option to the right on the **Component** toolbar. The software symbol looks like an LED with a red dashed figure eight inside. Click on this option and a **Select a Component** dialog box will appear. Under **Family**, select **AMMETER** and then take note of the **Component** listing and the four options for the orientation of the indicator. For our analysis the **AMMETER_H** will be chosen since the plus sign or entering point for the current is on the left for the diode **D1**. Click **OK** and the indicator can be placed to the left of the diode **D1**. For the voltage across the resistor **R2**, the option **VOLTMETER_HR** is chosen so the polarity matches that across the resistor.

Finally, all the components and meters must be connected. This is accomplished by simply placing the cursor at the end of an element until a small circle and a set of crosshairs appear to designate the starting point. Once these are in place, click the location and an **x** will appear at the terminal. Then move to the end of the other element and left-click the mouse again—a red connecting wire will automatically appear with the most direct route between the two elements. The process is called **Automatic Wiring**.

Now that all the components are in place it is time to initiate the analysis of the circuit, an operation that can be performed in one of three ways. One option is to select **Simulate** at the head of the screen followed by **Run**. The next is the green arrow in the **Simulation** toolbar. The last is to simply toggle the switch at the head of the screen to the **1** position. In each case a solution appears in the indicators after a few seconds that seems to flicker over time. This flickering simply indicates the software package is repeating the analysis over time. To accept the solution and stop the continuing simulation, either toggle the switch to the **0** position or select the lightning bolt keypad again.

The current through the diode is 3.349 mA, which compares well with the 3.32 mA in Example 2.13. The voltage across the resistor R_2 is 18.722 V, which is close to the 18.6 V of the same example. After the simulation, the multimeter can be displayed as shown in Fig. 2.151 by double-clicking on the meter symbol. By clicking anywhere on the meter, the top portion is dark blue, and the meter can be moved to any location by simply clicking on the blue region and dragging it to the desired location. The current of 193.285 μA is very close to the 212 μA of Example 2.13. The differences are primarily due to the fact that each diode voltage is assumed to be 0.7 V, whereas in fact it is different for each diode of Fig. 2.151 since the current through each is different. In all, however, the Multisim solution is a very close match with the approximate solution of Example 2.13.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

2.2 Load-Line Analysis

1. a. Using the characteristics of Fig. 2.152b, determine I_D, V_D, and V_R for the circuit of Fig. 2.152a.
b. Repeat part (a) using the approximate model for the diode, and compare results.
c. Repeat part (a) using the ideal model for the diode, and compare results.

2. a. Using the characteristics of Fig. 2.152b, determine I_D and V_D for the circuit of Fig. 2.153.
b. Repeat part (a) with $R = 0.47\ \text{k}\Omega$.
c. Repeat part (a) with $R = 0.68\ \text{k}\Omega$.
d. Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.

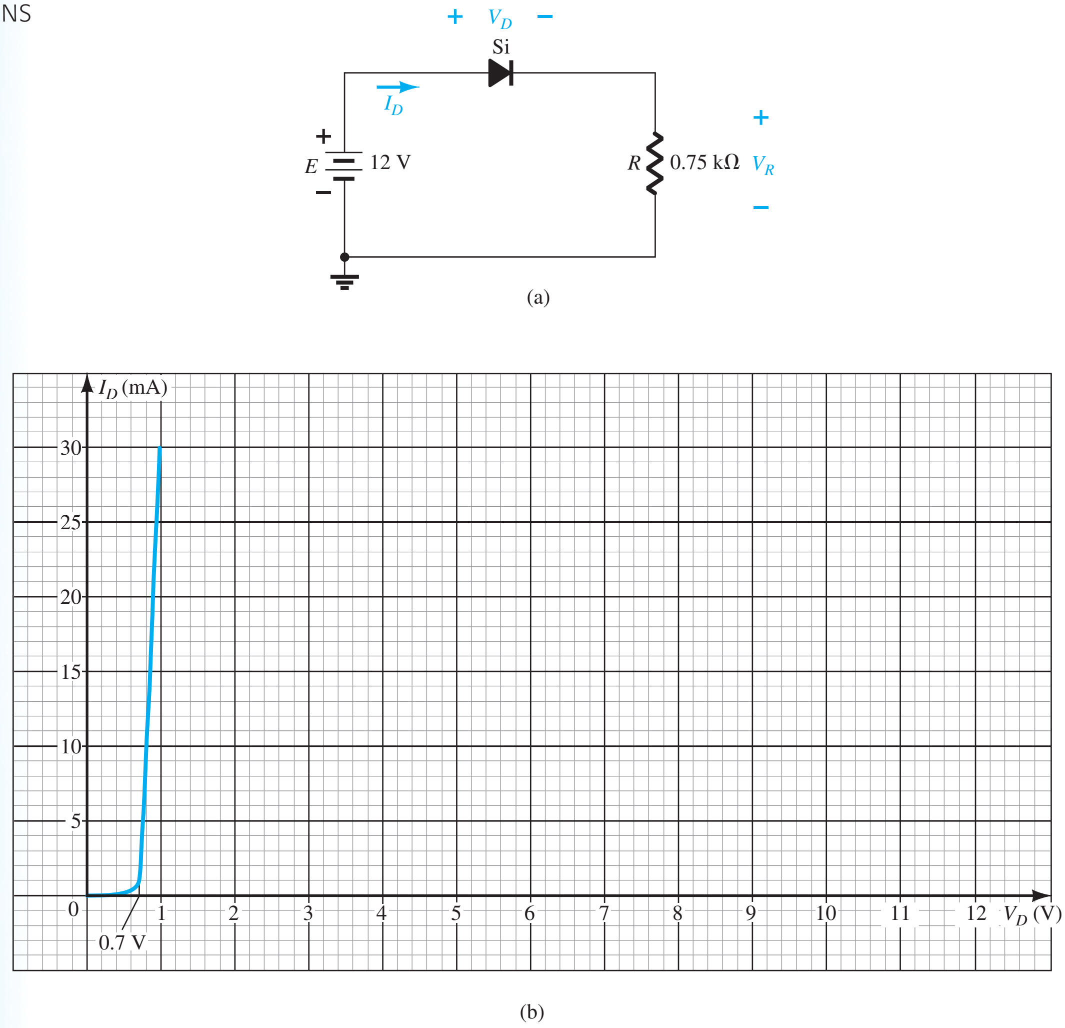

+ V_D −
Si
I_D
+
E
−
12 V
R
0.75 kΩ
+
V_R
−
(a)
I_D (mA)
30
25
20
15
10
5
0
1
2
3
4
5
6
7
8
9
10
11
12
V_D (V)
0.7 V
(b)

FIG. 2.152
Problems 1 and 2.

3. Determine the value of R for the circuit of Fig. 2.153 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.152b for the diode.

4. **a.** Using the approximate characteristics for the Si diode, determine V_D, I_D, and V_R for the circuit of Fig. 2.154.
   b. Perform the same analysis as part (a) using the ideal model for the diode.
   c. Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

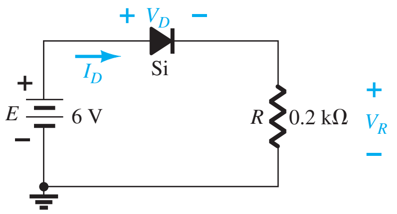

+ V_D −
I_D
Si
+
E
−
6 V
R
0.2 kΩ
+
V_R
−

FIG. 2.153
Problems 2 and 3.

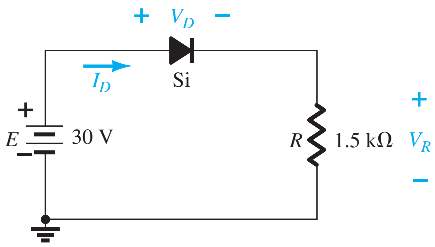
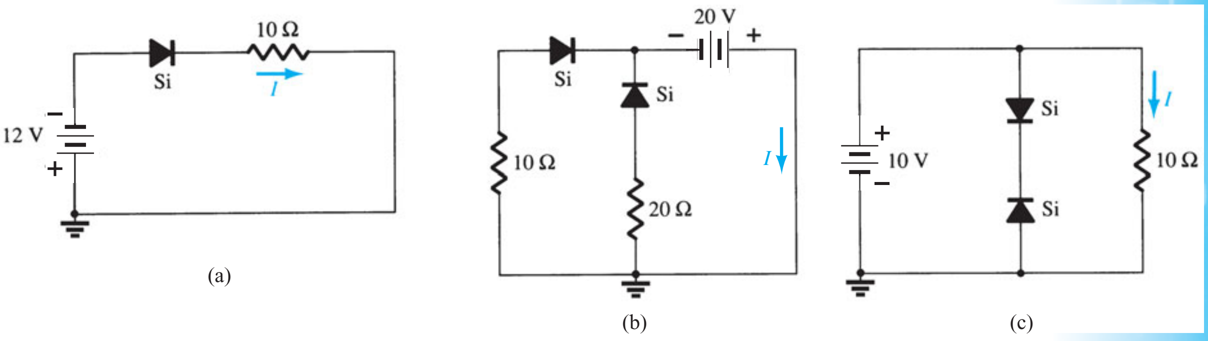

+ V_D −
I_D
Si
+
E
−
30 V
R
1.5 kΩ
+
V_R
−

FIG. 2.154
Problem 4.

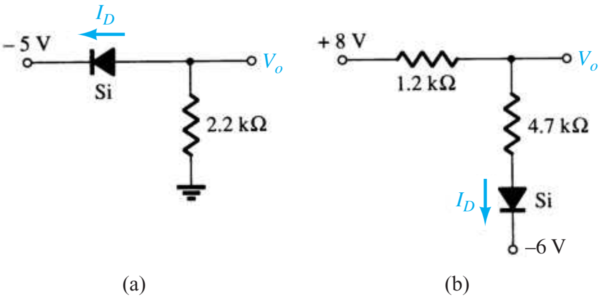
5. Determine the current I for each of the configurations of Fig. 2.155 using the approximate equivalent model for the diode.


10 Ω
Si
I
12 V
−
+
20 V
−
+
Si
Si
10 Ω
20 Ω
I
+
10 V
−
Si
Si
I
10 Ω

(a) (b) (c)

FIG. 2.155
Problem 5.

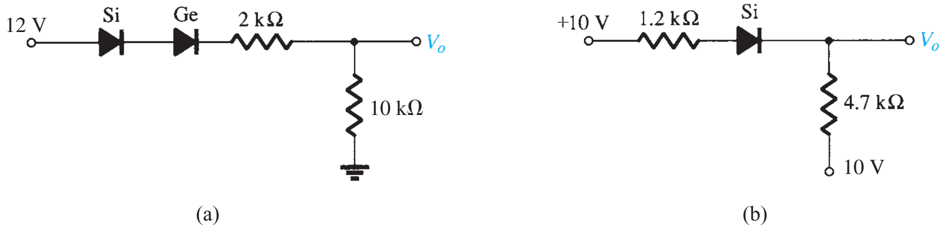
6. Determine V_o and I_D for the networks of Fig. 2.156.


I_D
−5 V
Si
V_o
2.2 kΩ
+8 V
1.2 kΩ
V_o
4.7 kΩ
I_D
Si
−6 V

(a) (b)

FIG. 2.156
Problems 6 and 49.

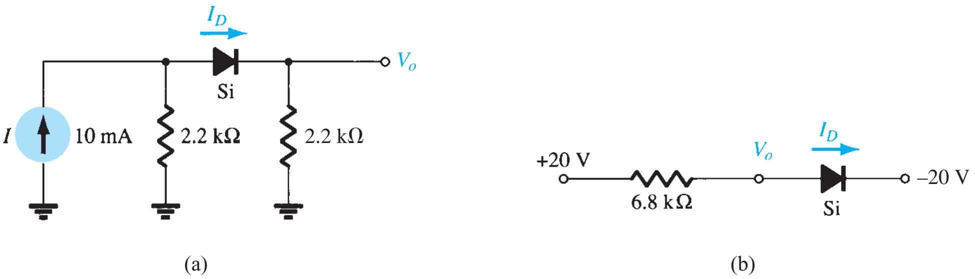
*7. Determine the level of V_o for each network of Fig. 2.157.


12 V
Si
Ge
2 kΩ
V_o
10 kΩ
+10 V
1.2 kΩ
Si
V_o
4.7 kΩ
10 V

(a) (b)

FIG. 2.157
Problem 7.

*8. Determine V_o and I_D for the networks of Fig. 2.158.


I_D
V_o
Si
I
10 mA
2.2 kΩ
2.2 kΩ
+20 V
V_o
I_D
−20 V
6.8 kΩ
Si

(a) (b)

FIG. 2.158
Problem 8.

***9.** Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.159.

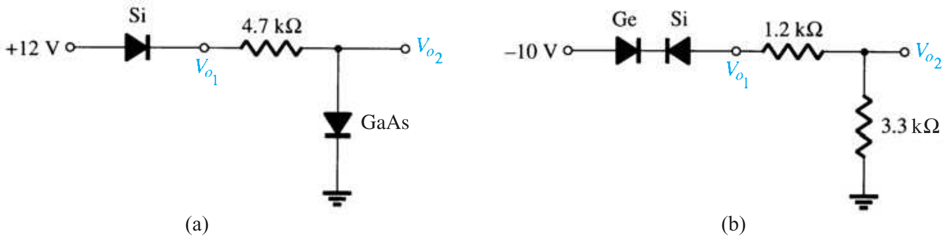

Si
4.7 kΩ
+12 V
V_{o_1}
V_{o_2}
GaAs
(a)
Ge
Si
1.2 kΩ
–10 V
V_{o_1}
V_{o_2}
3.3 kΩ
(b)

FIG. 2.159
Problem 9.

2.4 Parallel and Series-Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.160.

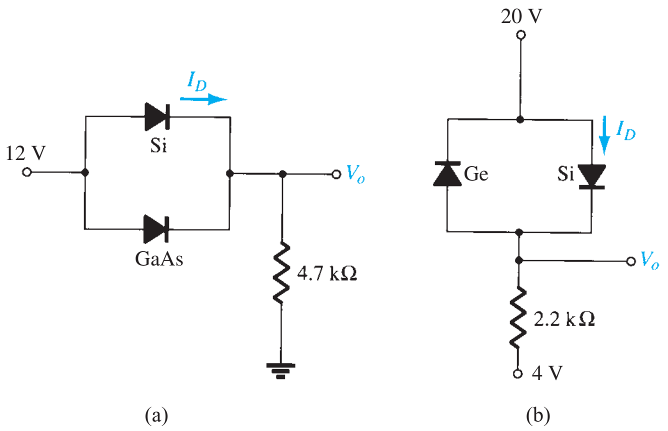

I_D
12 V
Si
GaAs
V_o
4.7 kΩ
(a)
20 V
I_D
Ge
Si
V_o
2.2 kΩ
4 V
(b)

FIG. 2.160
Problems 10 and 50.

***11.** Determine V_o and I for the networks of Fig. 2.161.

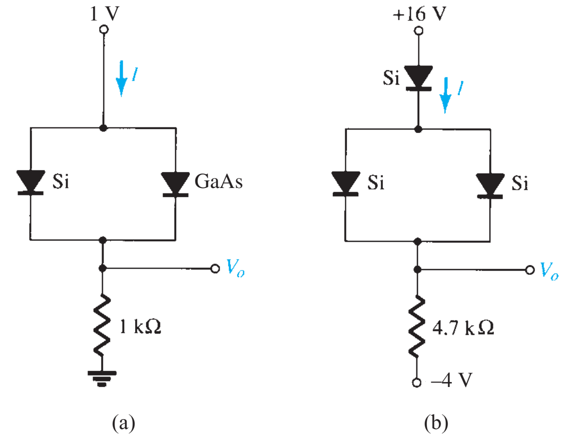

1 V
I
Si
GaAs
V_o
1 kΩ
(a)
+16 V
Si
I
Si
Si
V_o
4.7 kΩ
–4 V
(b)

FIG. 2.161
Problem 11.

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.162.

***13.** Determine V_o and I_D for the network of Fig. 2.163.

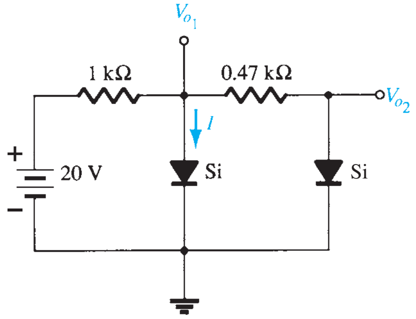

V_{o_1}
1 kΩ
0.47 kΩ
V_{o_2}
I
+
20 V
–
Si
Si

FIG. 2.162
Problem 12.

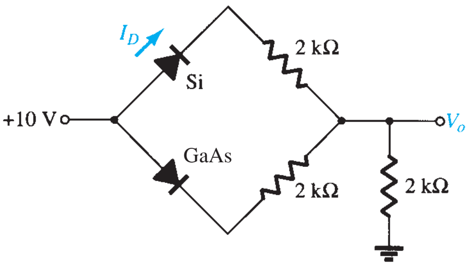

I_D
Si
2 kΩ
+10 V
V_o
GaAs
2 kΩ
2 kΩ

FIG. 2.163
Problems 13 and 51.

2.5 AND/OR Gates

14. Determine V_o for the network of Fig. 2.39 with 0 V on both inputs.

15. Determine V_o for the network of Fig. 2.39 with 10 V on both inputs.

16. Determine V_o for the network of Fig. 2.42 with 0 V on both inputs.

17. Determine V_o for the network of Fig. 2.42 with 10 V on both inputs.

18. Determine V_o for the negative logic OR gate of Fig. 2.164.

19. Determine V_o for the negative logic AND gate of Fig. 2.165.

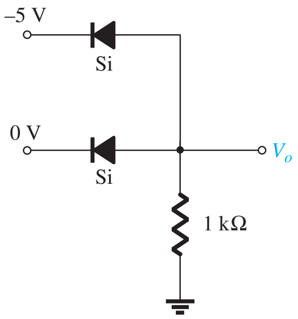

–5 V
Si
0 V
Si
V_o
1 kΩ

FIG. 2.164
Problem 18.

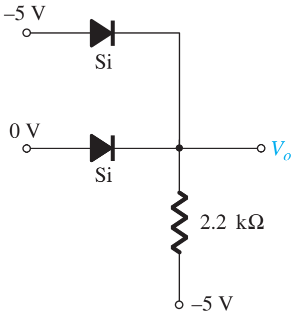

–5 V
Si
0 V
Si
V_o
2.2 kΩ
–5 V

FIG. 2.165
Problem 19.

20. Determine the level of V_o for the gate of Fig. 2.166.

21. Determine V_o for the configuration of Fig. 2.167.

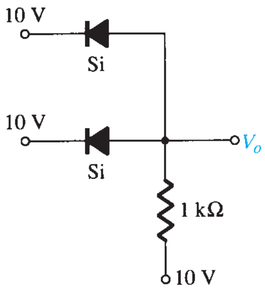

10 V
Si
10 V
Si
V_o
1 kΩ
10 V

FIG. 2.166
Problem 20.

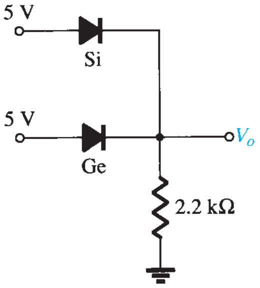

5 V
Si
5 V
Ge
V_o
2.2 kΩ

FIG. 2.167
Problem 21.

2.6 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.168. The input is a sinusoidal waveform with a frequency of 60 Hz. Determine the profit value of v_i from the given dc level.

23. Repeat Problem 22 with a silicon diode ($V_K = 0.7$ V).

24. Repeat Problem 22 with a 10 kΩ load applied as shown in Fig. 2.169. Sketch v_L and i_L.

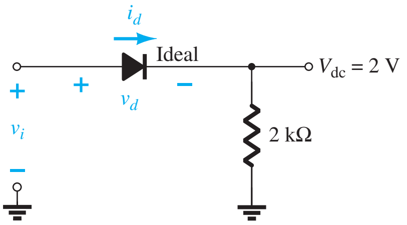

i_d
Ideal
V_{dc} = 2 V
+
+
v_d
−
v_i
−
2 kΩ

FIG. 2.168
Problems 22 through 24.

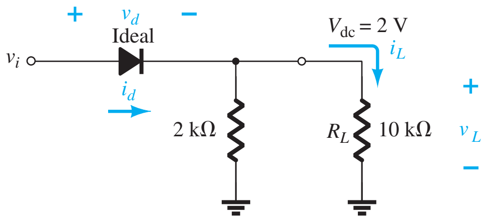

+
v_d
−
Ideal
V_{dc} = 2 V
i_L
v_i
i_d
2 kΩ
R_L
10 kΩ
+
v_L
−

FIG. 2.169
Problem 24.

25. For the network of Fig. 2.170, sketch v_o and determine V_{dc}.

***26.** For the network of Fig. 2.171, sketch v_o and i_R.

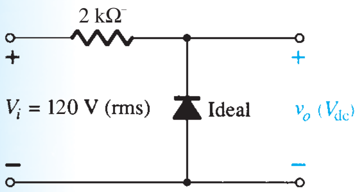

2 kΩ
+
V_i = 120 V (rms)
Ideal
+
v_o (V_{dc})
−
−

FIG. 2.170
Problem 25.

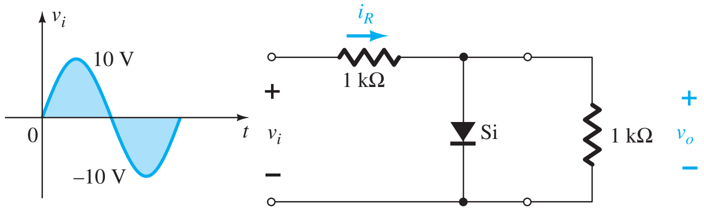

v_i
10 V
0
t
−10 V
i_R
1 kΩ
+
v_i
−
Si
1 kΩ
+
v_o
−

FIG. 2.171
Problem 26.

***27.** **a.** Given $P_{\max} = 14$ mW for each diode at Fig. 2.172, determine the maximum current rating of each diode (using the approximate equivalent model).

b. Determine $I_{\max}$ for the parallel diodes.

c. Determine the current through each diode at $V_{i_{\max}}$ using the results of part (b).

d. If only one diode were present, which would be the expected result?

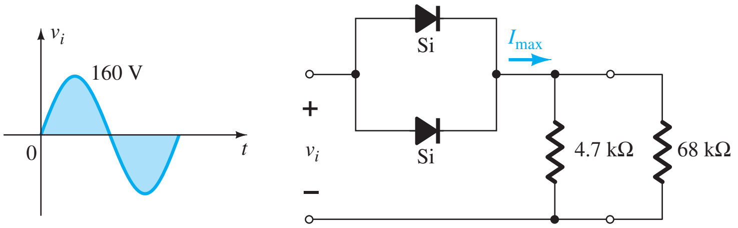

v_i
160 V
0
t
Si
$I_{\max}$
+
v_i
−
Si
4.7 kΩ
68 kΩ

FIG. 2.172
Problem 27.

2.7 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.

a. If silicon diodes are employed, what is the dc voltage available at the load?

b. Determine the required PIV rating of each diode.

c. Find the maximum current through each diode during conduction.

d. What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.173. In addition, determine the maximum current through each diode.

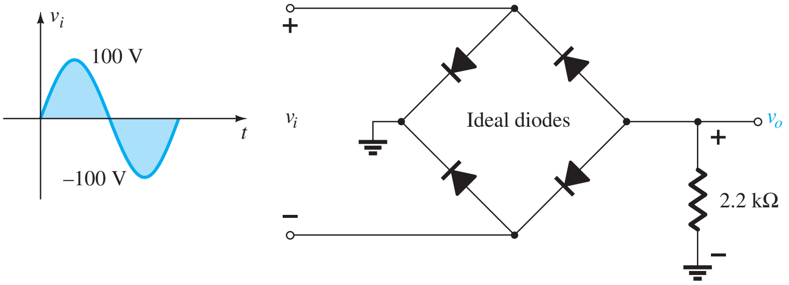

v_i
100 V
t
−100 V
+
v_i
−
Ideal diodes
v_o
+
2.2 kΩ
−

FIG. 2.173
Problem 29.

***30.** Sketch v_o for the network of Fig. 2.174 and determine the dc voltage available.

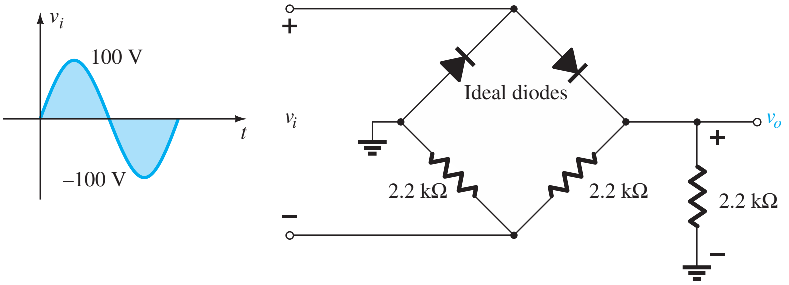

v_i
100 V
t
–100 V
+
v_i
–
Ideal diodes
2.2 kΩ
2.2 kΩ
v_o
+
2.2 kΩ
–

FIG. 2.174
Problem 30.

***31.** Sketch v_o for the network of Fig. 2.175 and determine the dc voltage available.

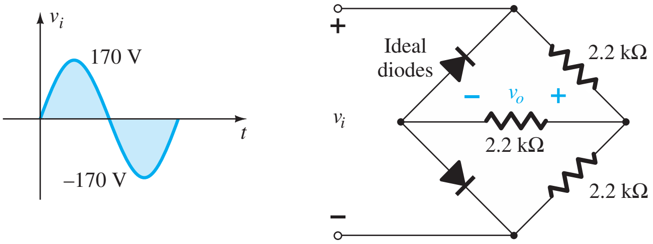

v_i
170 V
t
–170 V
+
v_i
–
Ideal diodes
2.2 kΩ
– v_o +
2.2 kΩ
2.2 kΩ

FIG. 2.175
Problem 31.

2.8 Clippers

32. Determine v_o for each network of Fig. 2.176 for the input shown.

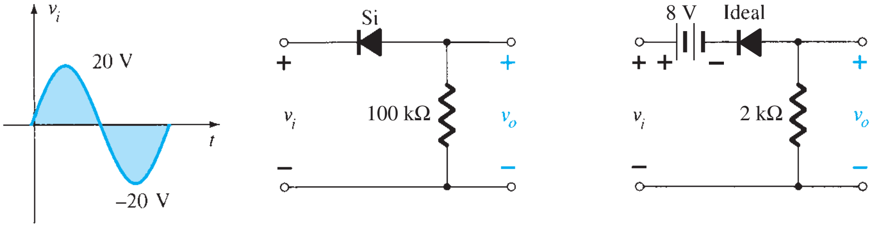
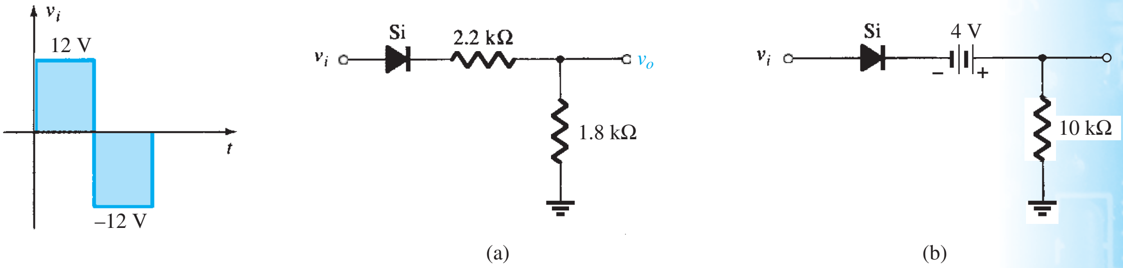

v_i
20 V
t
–20 V
Si
+
v_i
–
100 kΩ
+
v_o
–
8 V
Ideal
+ +
–
v_i
–
2 kΩ
+
v_o
–

FIG. 2.176
Problem 32.

33. Determine v_o for each network of Fig. 2.177 for the input shown.

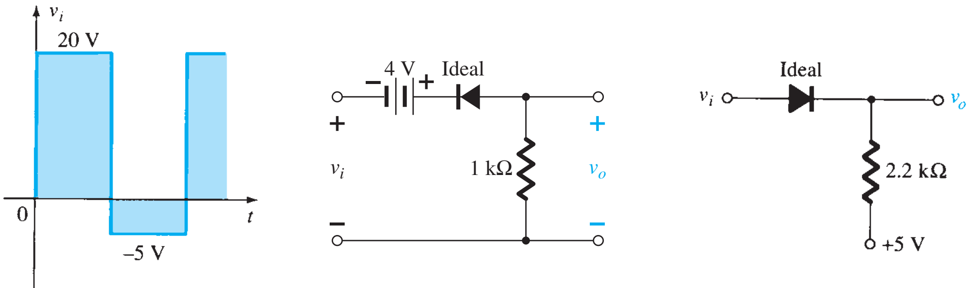

v_i
12 V
t
–12 V
v_i
Si
2.2 kΩ
v_o
1.8 kΩ
v_i
Si
4 V
–
+
v_o
10 kΩ

(a)

(b)

FIG. 2.177
Problem 33.

***34.** Determine v_o for each network of Fig. 2.178 for the input shown.

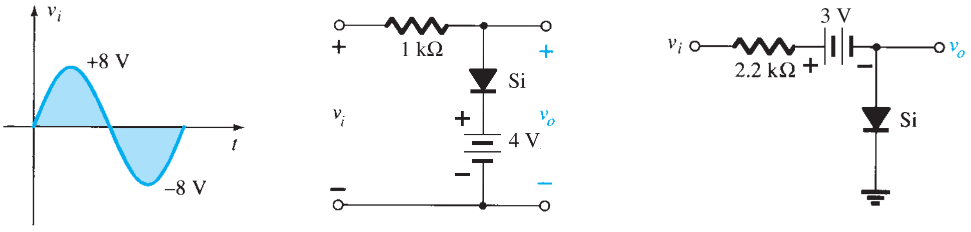


v_i
20 V
0
t
–5 V
4 V
Ideal
+
–
v_i
1 kΩ
v_o
Ideal
v_i
v_o
2.2 kΩ
+5 V

(a) (b)

FIG. 2.178
Problem 34.

***35.** Determine v_o for each network of Fig. 2.179 for the input shown.

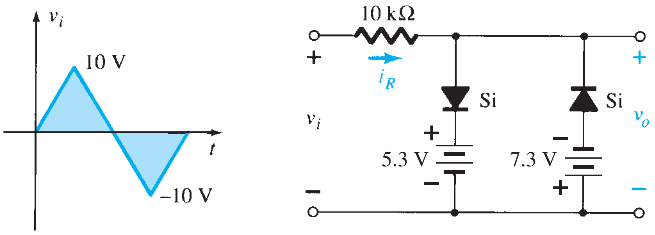


v_i
+8 V
t
–8 V
1 kΩ
Si
v_i
v_o
4 V
+
–
v_i
3 V
2.2 kΩ
v_o
Si

(a) (b)

FIG. 2.179
Problem 35.

36. Sketch i_R and v_o for the network of Fig. 2.180 for the input shown.

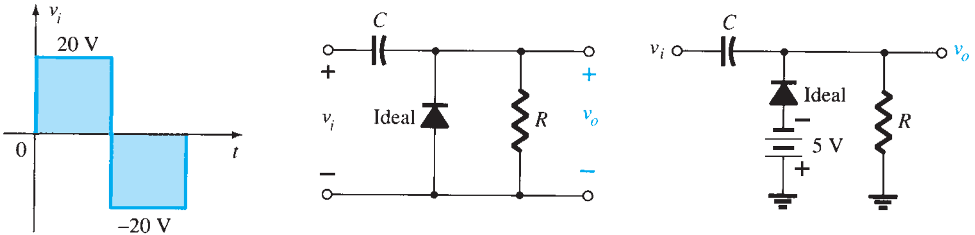


v_i
10 V
t
–10 V
10 kΩ
i_R
Si
Si
v_i
v_o
5.3 V
7.3 V
+
–

FIG. 2.180
Problem 36.

2.9 Clampers

37. Sketch v_o for each network of Fig. 2.181 for the input shown.



v_i
20 V
0
t
–20 V
C
Ideal
R
v_i
v_o
+
–
C
v_i
v_o
Ideal
5 V
R

(a) (b)

FIG. 2.181
Problem 37.

38. Sketch v_o for each network of Fig. 2.182 for the input shown.

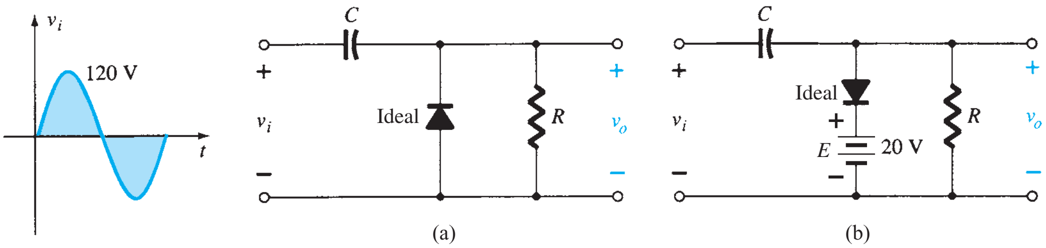

v_i
120 V
t
C
+
v_i
–
Ideal
R
+
v_o
–
C
Ideal
+
E
–
20 V
R
(a)
(b)

FIG. 2.182
Problem 38.

***39.** For the network of Fig. 2.183:

a. Calculate 5τ.
b. Compare 5τ to half the period of the applied signal.
c. Sketch v_o.

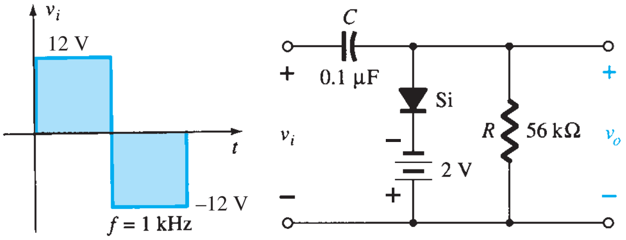

v_i
12 V
t
–12 V
f = 1 kHz
C
0.1 μF
+
v_i
–
Si
–
+
2 V
R
56 kΩ
+
v_o
–

FIG. 2.183
Problem 39.

***40.** Design a clamper to perform the function indicated in Fig. 2.184.

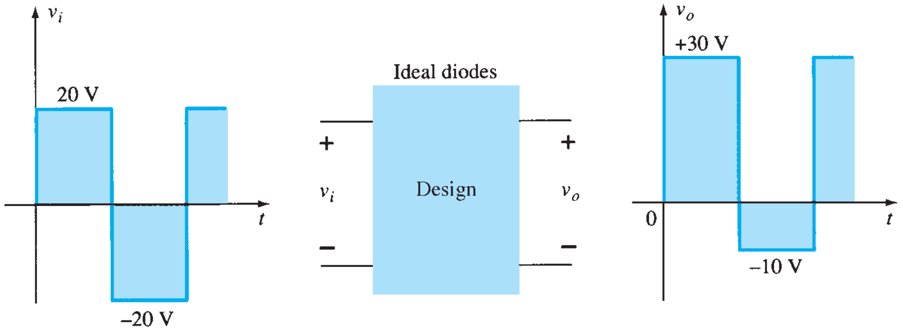

v_i
20 V
–20 V
t
Ideal diodes
+
v_i
–
Design
+
v_o
–
v_o
+30 V
0
t
–10 V

FIG. 2.184
Problem 40.

***41.** Design a clamper to perform the function indicated in Fig. 2.185.

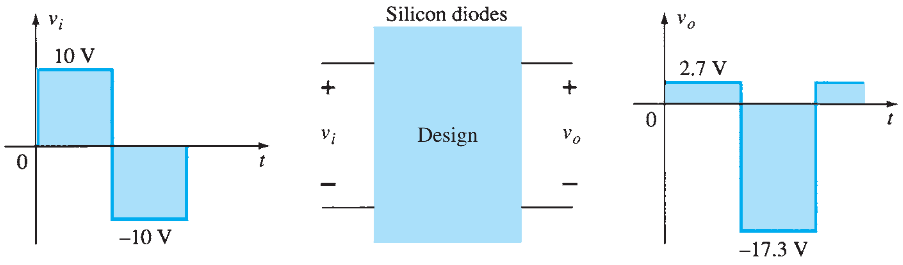

v_i
10 V
0
t
–10 V
Silicon diodes
+
v_i
–
Design
+
v_o
–
v_o
2.7 V
0
t
–17.3 V

FIG. 2.185
Problem 41.

2.10 Zener Diodes

***42.** **a.** Determine V_L, I_L, I_Z, and I_R for the network of Fig. 2.186 if $R_L = 180\ \Omega$.

b. Repeat part (a) if $R_L = 470\ \Omega$.

c. Determine the value of R_L that will establish maximum power conditions for the Zener diode.

d. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

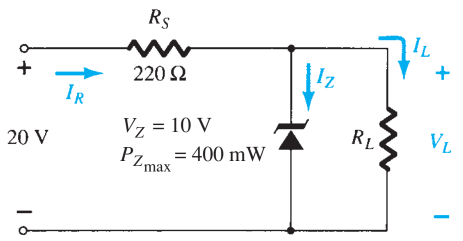


FIG. 2.186
Problem 42.

***43.** **a.** Design the network of Fig. 2.187 to maintain V_L at 12 V for a load variation (I_L) from 0 mA to 200 mA. That is, determine R_S and V_Z.

b. Determine $P_{Z\,max}$ for the Zener diode of part (a).

***44.** For the network of Fig. 2.188, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

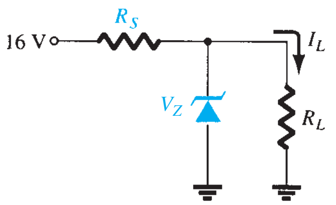


FIG. 2.187
Problem 43.

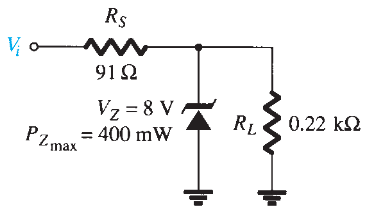


FIG. 2.188
Problems 44 and 52.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 V and 50 V. That is, determine the proper value of R_S and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.145 if the input is a 50-V square wave. Repeat for a 5-V square wave.

2.11 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.123 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.123 in terms of the peak secondary voltage V_m.

2.14 Computer Analysis

49. Perform an analysis of the network of Fig. 2.156b using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.161b using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.162 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.188 using PSpice Windows.

53. Repeat Problem 49 using Multisim.

54. Repeat Problem 50 using Multisim.

55. Repeat Problem 51 using Multisim.

56. Repeat Problem 52 using Multisim.

3

Bipolar Junction Transistors

CHAPTER OBJECTIVES

- Become familiar with the basic construction and operation of the Bipolar Junction Transistor.
- Be able to apply the proper biasing to insure operation in the active region.
- Recognize and be able to explain the characteristics of an *npn* or *pnp* transistor.
- Become familiar with the important parameters that define the response of a transistor.
- Be able to test a transistor and identify the three terminals.

3.1 INTRODUCTION

During the period 1904 to1947, the vacuum tube was the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the *control grid*, to the vacuum diode, resulting in the first amplifier, the *triode*. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and the five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance, and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Dr. S. William Shockley, Walter H. Brattain, and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories as shown in Fig. 3.1. The original transistor (a point-contact transistor) is shown in Fig. 3.2. The advantages of this three-terminal solid-state device over the tube were immediately obvious: It was smaller and lightweight; it had no heater requirement or heater loss; it had a rugged construction; it was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) have at least three terminals, with one controlling the flow or potential between the other two.

Dr. William Shockley (seated); Dr. John Bardeen (left); Dr. Walter H. Brattain. (Courtesy of AT&T Archives and History Center.)

Dr. Shockley	Born: London, England, 1910 PhD Harvard, 1936
Dr. Bardeen	Born: Madison, Wisconsin, 1908 PhD Princeton, 1936
Dr. Brattain	Born: Amoy, China, 1902 PhD University of Minnesota, 1928

All shared the Nobel Prize in 1956 for this contribution.

FIG. 3.1
Coinventors of the first transistor at Bell Laboratories.

3.2 TRANSISTOR CONSTRUCTION

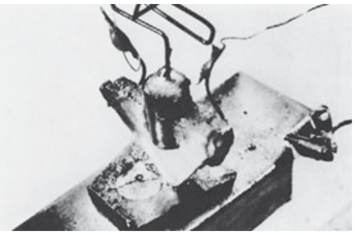
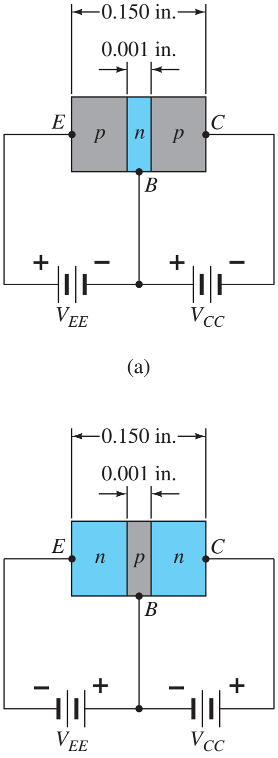


FIG. 3.2

The first transistor. (Courtesy of AT&T Archives and History Center.)

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor*, and the latter is called a *pnp transistor*. Both are shown in Fig. 3.3 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, with the base and collector only lightly doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is $0.150/0.001 = 150:1$. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 1:10 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of “free” carriers.

For the biasing shown in Fig. 3.3 the terminals have been indicated by the capital letters *E* for *emitter*, *C* for *collector*, and *B* for *base*. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from *bipolar junction transistor*, is often applied to this three-terminal device. The term *bipolar* reflects the fact that holes *and* electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a *unipolar* device. The Schottky diode of Chapter 16 is such a device.



(a)

(b)

FIG. 3.3

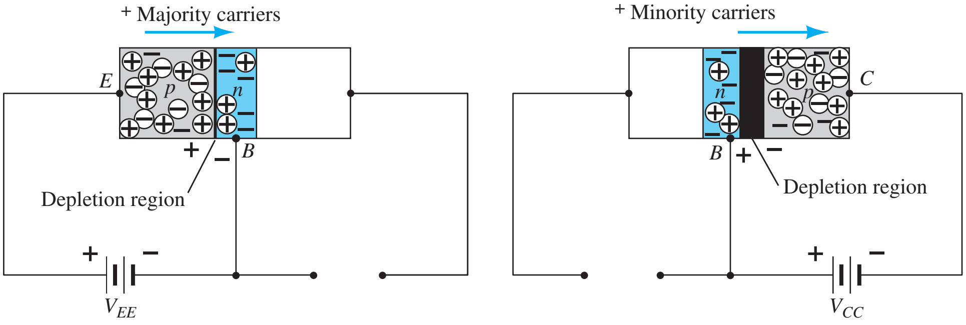
Types of transistors: (a) pnp; (b) npn.

3.3 TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor of Fig. 3.3a. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.4a the *pnp* transistor has been redrawn without the base-to-collector bias. Note the similarities between this situation and that of the *forward-biased* diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

Let us now remove the base-to-emitter bias of the *pnp* transistor of Fig. 3.3a as shown in Fig. 3.4b. Consider the similarities between this situation and that of the *reverse-biased* diode of Section 1.6. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.4b. In summary, therefore:

One p–n junction of a transistor is reverse-biased, whereas the other is forward-biased.



(a)

(b)

FIG. 3.4

Biasing a transistor: (a) forward-bias; (b) reverse-bias.

In Fig. 3.5 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority- and minority-carrier flows indicated. Note in Fig. 3.5 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.5, a large number of majority carriers will diffuse across the forward-biased *p–n* junction into the *n*-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the *p*-type material. Since the sandwiched *n*-type material is very thin and has a low conductivity, a very small number of

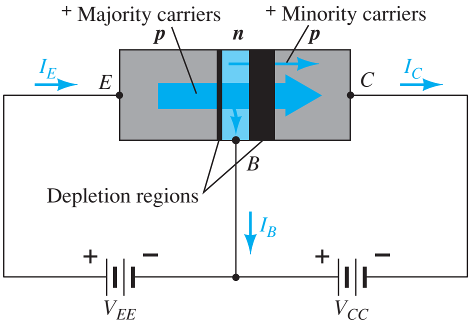


FIG. 3.5
Majority and minority carrier flow of a pnp transistor.

these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes, as compared to milliamperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Fig. 3.5. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.5.

Applying Kirchhoff's current law to the transistor of Fig. 3.5 as if it were a single node, we obtain

$$\boxed{I_E = I_C + I_B} \tag{3.1}$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, comprises two components—the majority and the minority carriers as indicated in Fig. 3.5. The minority-current component is called the *leakage current* and is given the symbol I_{CO} (I_C current with emitter terminal *O*pen). The collector current, therefore, is determined in total by

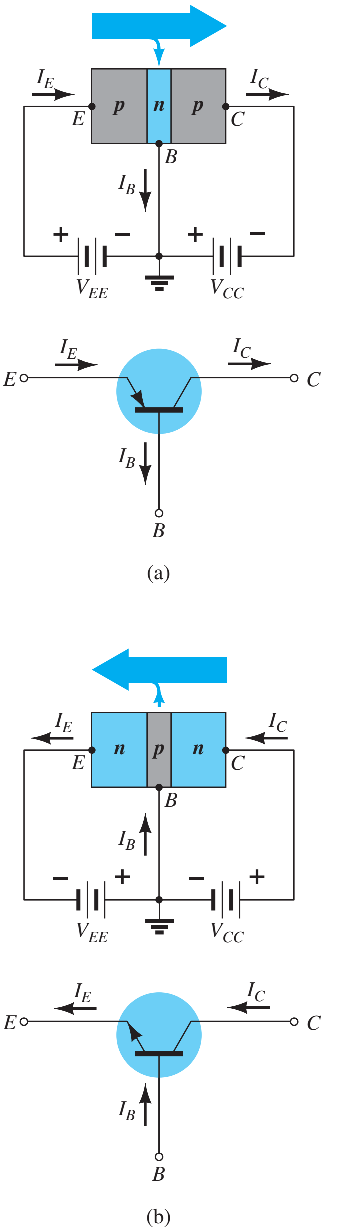
$$\boxed{I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}} \tag{3.2}$$

For general-purpose transistors, I_C is measured in milliamperes and I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

3.4 COMMON-BASE CONFIGURATION

The notation and symbols used in conjunction with the transistor in the majority of texts and manuals published today are indicated in Fig. 3.6 for the common-base configuration with *pnp* and *npn* transistors. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this text all current directions will refer to conventional (hole) flow rather than electron flow. The result is that the arrows in all electronic symbols have a direction defined by this convention. Recall that the arrow in the diode symbol defined the direction of conduction for conventional current. For the transistor:

The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.



(a)

(b)

FIG. 3.6
Notation and symbols used with the common-base configuration: (a) pnp transistor; (b) npn transistor.

All the current directions appearing in Fig. 3.6 are the actual directions as defined by the choice of conventional flow. Note in each case that $I_E = I_C + I_B$. Note also that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch. That is, compare the direction of I_E to the polarity of V_{EE} for each configuration and the direction of I_C to the polarity of V_{CC}.

To fully describe the behavior of a three-terminal device such as the common-base amplifiers of Fig. 3.6 requires two sets of characteristics—one for the *driving point* or *input* parameters and the other for the *output* side. The input set for the common-base amplifier as shown in Fig. 3.7 relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

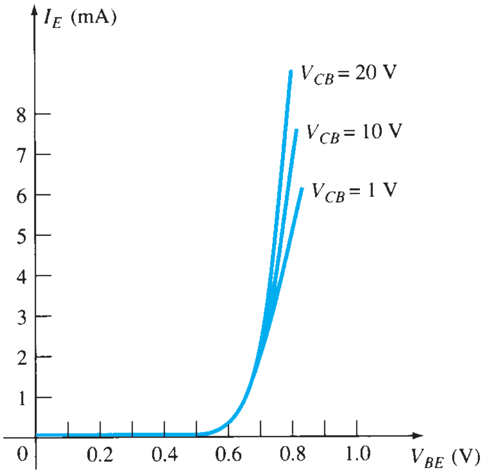


FIG. 3.7

Input or driving point characteristics for a common-base silicon transistor amplifier.

The output set relates an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E) as shown in Fig. 3.8. The output or *collector* set of characteristics has three basic regions of interest, as indicated in Fig. 3.8: the *active*, *cutoff*, and *saturation*

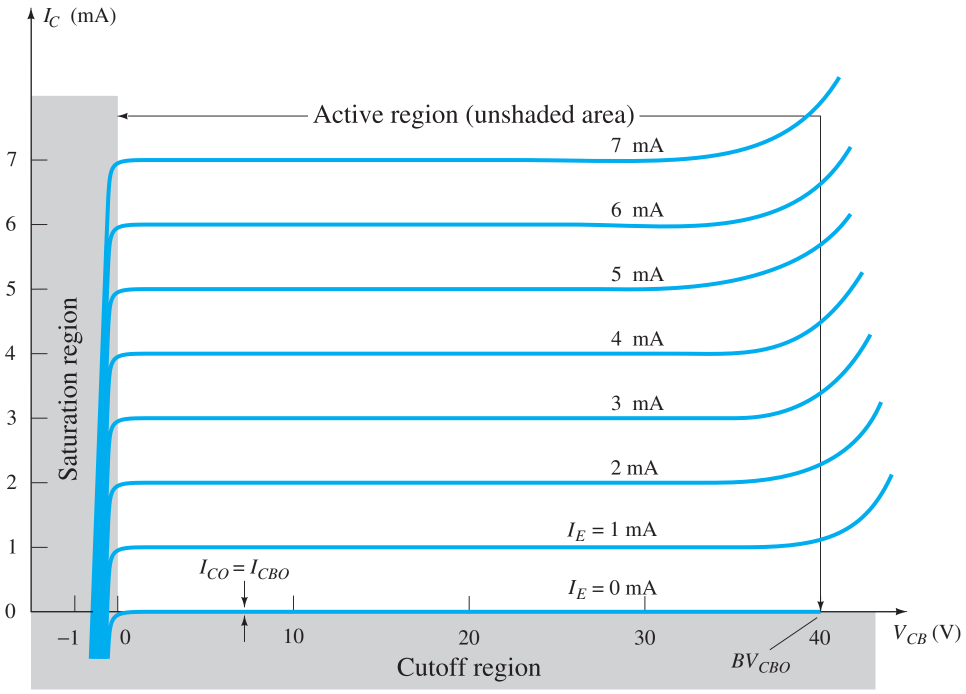


FIG. 3.8

Output or collector characteristics for a common-base transistor amplifier.

regions. The active region is the region normally employed for linear (undistorted) amplifiers. In particular:

In the active region the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

The active region is defined by the biasing arrangements of Fig. 3.6. At the lower end of the active region the emitter current (I_E) is zero, and the collector current is simply that due to the reverse saturation current I_{CO}, as indicated in Fig. 3.9. The current I_{CO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig. 3.9. The notation most frequently used for I_{CO} on data and specification sheets is, as indicated in Fig. 3.9, I_{CBO} (the collector-to-base current with the emitter leg open). Because of improved construction techniques, the level of I_{CBO} for general-purpose transistors in the low- and mid-power ranges is usually so low that its effect can be ignored. However, for higher power units I_{CBO} will still appear in the microampere range. In addition, keep in mind that I_{CBO}, like I_s, for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature.

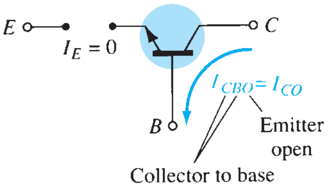


FIG. 3.9

Reverse saturation current.

Note in Fig. 3.8 that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$\boxed{I_C \cong I_E} \tag{3.3}$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 3.8. In addition:

In the cutoff region the base–emitter and collector–base junctions of a transistor are both reverse-biased.

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0 V.

In the saturation region the base–emitter and collector–base junctions are forward-biased.

The input characteristics of Fig. 3.7 reveal that for fixed values of collector voltage (V_{CB}), as the base-to-emitter voltage increases, the emitter current increases in a manner that closely resembles the diode characteristics. In fact, increasing levels of V_{CB} have such a small effect on the characteristics that as a first approximation the change due to changes in V_{CB} can be ignored and the characteristics drawn as shown in Fig. 3.10a. If we then apply the piecewise-linear approach, the characteristics of Fig. 3.10b result. Taking it a step further and ignoring the slope of the curve and therefore the resistance associated with the forward-biased junction results in the characteristics of Fig. 3.10c. For the analysis to follow in this book the equivalent model of Fig. 3.10c will be employed for all dc analysis of transistor networks. That is, once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following:

$$\boxed{V_{BE} \cong 0.7\text{ V}} \tag{3.4}$$

In other words, the effect of variations due to V_{CB} and the slope of the input characteristics will be ignored as we strive to analyze transistor networks in a manner that will provide a good approximation to the actual response without getting too involved with parameter variations of less importance.

It is important to fully appreciate the statement made by the characteristics of Fig. 3.10c. They specify that with the transistor in the "on" or active state the voltage from base to emitter will be 0.7 V at *any* level of emitter current as controlled by the external network. In fact, at the first encounter of any transistor configuration in the dc mode, one can now immediately specify that the voltage from base to emitter is 0.7 V if the device is in the active region—a very important conclusion for the dc analysis to follow.

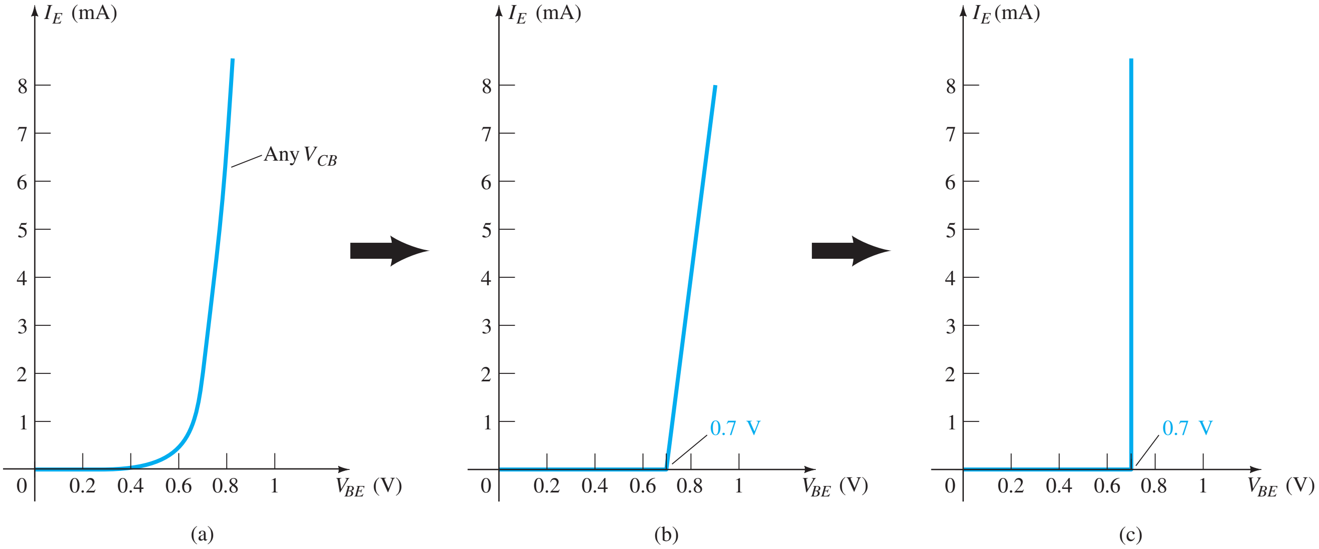


FIG. 3.10

Developing the equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

EXAMPLE 3.1

a. Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
b. Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
c. Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
d. Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution:

a. The characteristics clearly indicate that $I_C \cong I_E =$ **3 mA.**
b. The effect of changing V_{CB} is negligible and I_C continues to be **3 mA**.
c. From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V**.
d. Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c, V_{BE} is **0.7 V** for any level of emitter current.

Alpha (α)

DC Mode In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\boxed{\alpha_{dc} = \frac{I_C}{I_E}} \tag{3.5}$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that $\alpha = 1$, for practical devices alpha typically extends from 0.90 to 0.998, with most values approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes

$$\boxed{I_C = \alpha I_E + I_{CBO}} \tag{3.6}$$

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, I_C also appears to be 0 mA for the range of V_{CB} values.

AC Mode For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\boxed{\alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}} \tag{3.7}$$

The ac alpha is formally called the *common-base*, *short-circuit*, *amplification factor*, for reasons that will be more obvious when we examine transistor equivalent circuits in Chapter 5. For the moment, recognize that Eq. (3.7) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other. The use of an equation such as (3.7) will be demonstrated in Section 3.6.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $I_C \cong I_E$ and assuming for the moment that $I_B \cong 0\ \mu$A. The result is the configuration of Fig. 3.11 for the *pnp* transistor. The arrow of the symbol defines the direction of conventional flow for $I_E \cong I_C$. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the *npn* transistor the polarities will be reversed.

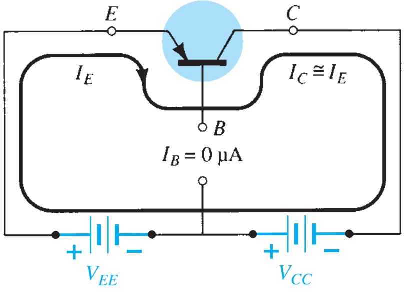


FIG. 3.11
Establishing the proper biasing management for a common-base pnp transistor in the active region.

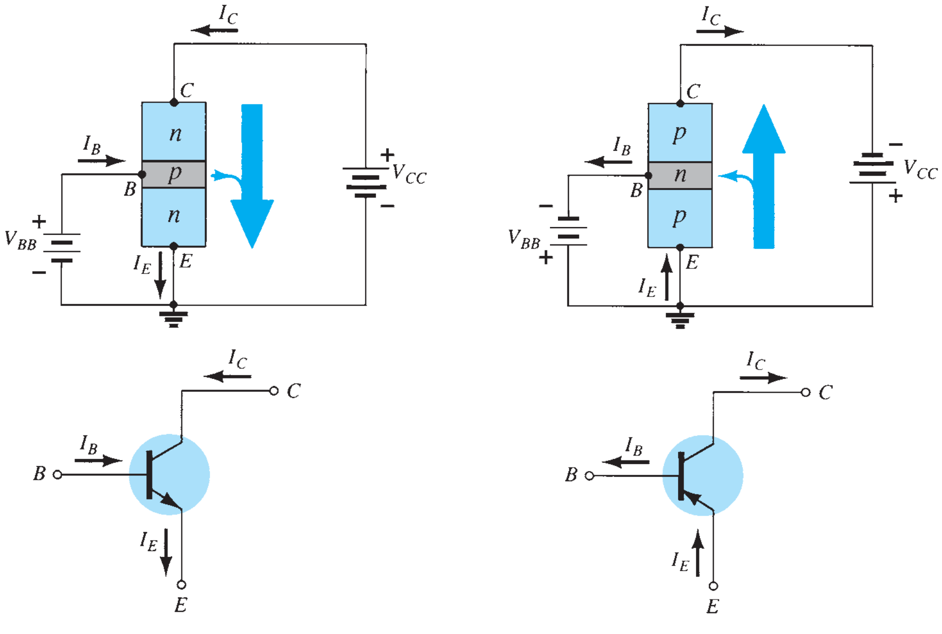
Some students feel that they can remember whether the arrow of the device symbol is pointing in or out by matching the letters of the transistor type with the appropriate letters of the phrases "pointing in" or "not pointing in." For instance, there is a match between the letters *npn* and the italic letters of *n*ot *p*ointing i*n* and the letters *pnp* with *p*ointing i*n*.

Breakdown Region

As the applied voltage V_{CB} increases there is a point where the curves take a dramatic upswing in Fig. 3.8. This is due primarily to an avalanche effect similar to that described for the diode in Chapter 1 when the reverse-bias voltage reached the breakdown region. As stated earlier the base-to-collector junction is reversed biased in the active region, but there is a point where too large a reverse-bias voltage will lead to the avalanche effect. The result is a large increase in current for small increases in the base-to-collector voltage. The largest permissible base-to-collector voltage is labeled BV_{CBO} as shown in Fig. 3.8. It is also referred to as $V_{(BR)CBO}$ as shown on the characteristics of Fig. 3.23 to be discussed later. Note in each of the above notations the use of the uppercase letter O to represent that the emitter leg is in the open state (not connected). It is important to remember when taking note of this data point that this limitation is only for the common-base configuration. You will find in the common-emitter configuration that this limiting voltage is quite a bit less.

3.5 COMMON-EMITTER CONFIGURATION

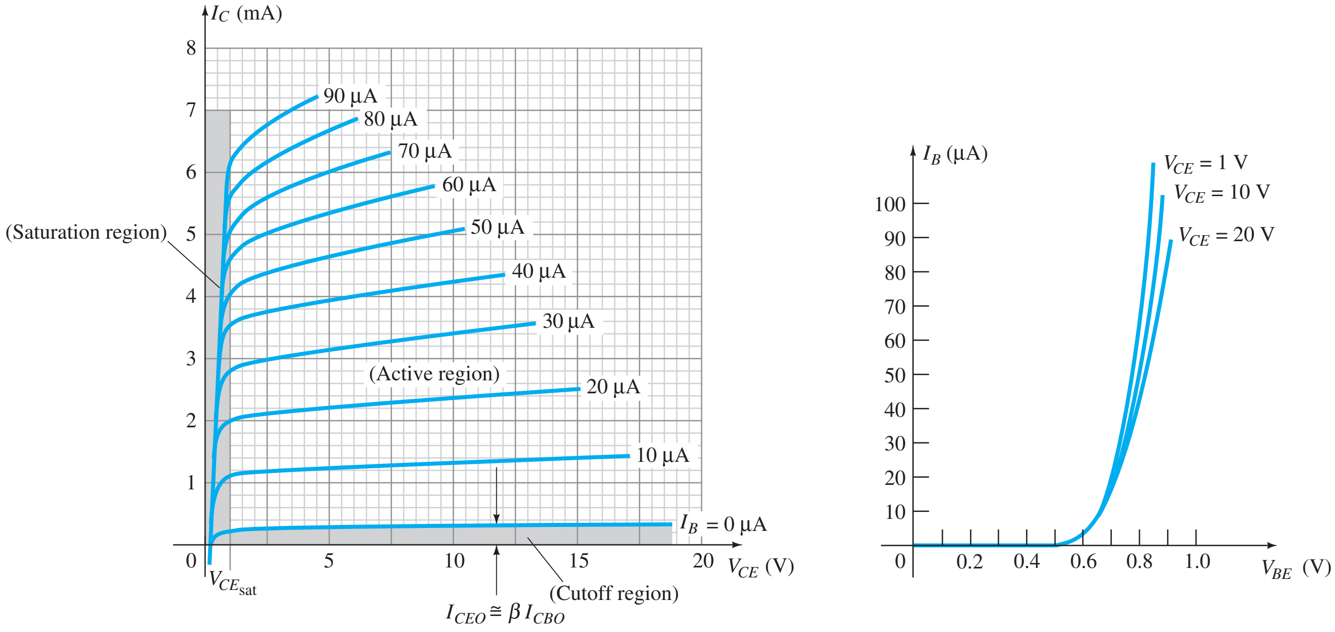
The most frequently encountered transistor configuration appears in Fig. 3.12 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base–emitter* circuit and one for the *output* or *collector–emitter* circuit. Both are shown in Fig. 3.13.



(a) (b)

FIG. 3.12

Notation and symbols used with the common-emitter configuration: (a) npn transistor; (b) pnp transistor.



(a) (b)

FIG. 3.13

Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is, $I_E = I_C + I_B$ and $I_C = \alpha I_E$.

For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Note that on the characteristics of Fig. 3.14 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line at $V_{CE_{\text{sat}}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE_{\text{sat}}}$ is called the saturation region.

In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that I_C is not equal to zero when I_B is zero. For the common-base configuration, when the input current I_E was equal to zero, the collector current was equal only to the reverse saturation current I_{CO}, so that the curve $I_E = 0$ and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

Eq. (3.6): $I_C = \alpha I_E + I_{CBO}$

Substitution gives Eq. (3.3): $I_C = \alpha(I_C + I_B) + I_{CBO}$

Rearranging yields
$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha} \tag{3.8}$$

If we consider the case discussed above, where $I_B = 0$ A, and substitute a typical value of α such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0\text{ A})}{1-\alpha} + \frac{I_{CBO}}{1-0.996}$$
$$= \frac{I_{CBO}}{0.004} = 250 I_{CBO}$$

If I_{CBO} were 1 μA, the resulting collector current with $I_B = 0$ A would be 250(1 μA) = 0.25 mA, as reflected in the characteristics of Fig. 3.14.

For future reference, the collector current defined by the condition $I_B = 0\ \mu$A will be assigned the notation indicated by the following equation:

$$\boxed{I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\ \mu\text{A}}} \tag{3.9}$$

In Fig. 3.13 the conditions surrounding this newly defined current are demonstrated with its assigned reference direction.

For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.

In other words, the region below $I_B = 0\ \mu$A is to be avoided if an undistorted output signal is required.

When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region. The

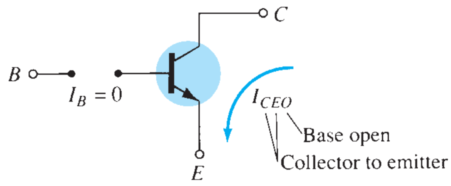


FIG. 3.14

Circuit conditions related to I_{CEO}.

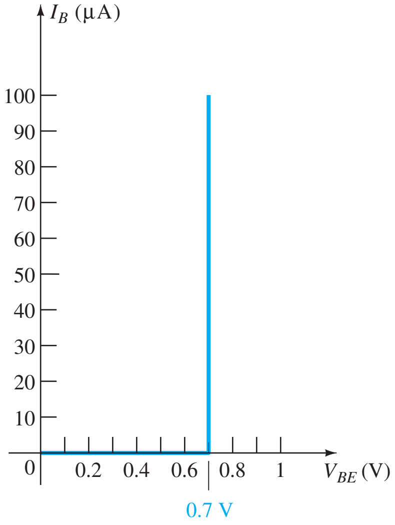


FIG. 3.15

Piecewise-linear equivalent for the diode characteristics of Fig. 3.13b.

cutoff condition should ideally be $I_C = 0$ mA for the chosen V_{CE} voltage. Since I_{CEO} is typically low in magnitude for silicon materials, *cutoff will exist for switching purposes when $I_B = 0\ \mu A$ or $I_C = I_{CEO}$ for silicon transistors only. For germanium transistors, however, cutoff for switching purposes will be defined as those conditions that exist when $I_C = I_{CBO}$.* This condition can normally be obtained for germanium transistors by reverse-biasing the base-to-emitter junction a few tenths of a volt.

Recall for the common-base configuration that the input set of characteristics was approximated by a straight-line equivalent that resulted in $V_{BE} = 0.7$ V for any level of I_E greater than 0 mA. For the common-emitter configuration the same approach can be taken, resulting in the approximate equivalent of Fig. 3.15. The result supports our earlier conclusion that for a transistor in the "on" or active region the base-to-emitter voltage is 0.7 V. In this case the voltage is fixed for any level of base current.

EXAMPLE 3.2

a. Using the characteristics of Fig. 3.13, determine I_C at $I_B = 30\ \mu A$ and $V_{CE} = 10$ V.
b. Using the characteristics of Fig. 3.13, determine I_C at $V_{BE} = 0.7$ V and $V_{CE} = 15$ V.

Solution:

a. At the intersection of $I_B = 30\ \mu A$ and $V_{CE} = 10$ V, $I_C =$ **3.4 mA**.
b. Using Fig. 3.13b, we obtain $I_B = 20\ \mu A$ at the intersection of $V_{BE} = 0.7$ V and $V_{CE} = 15$ V (between $V_{CE} = 10$ V and 20 V). From Fig. 3.13a we find that $I_C =$ **2.5 mA** at the intersection of $I_B = 20\ \mu A$ and $V_{CE} = 15$ V.

Beta (β)

DC Mode In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\boxed{\beta_{dc} = \frac{I_C}{I_B}} \tag{3.10}$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, the parameter β reveals the relative magnitude of one current with respect to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

On specification sheets β_{dc} is usually included as h_{FE} with the italic letter *h* derived from an ac *h*ybrid equivalent circuit to be introduced in Chapter 5. The subscript *FE* is derived from *f*orward-current amplification and common-*e*mitter configuration, respectively.

AC Mode For ac situations an ac beta is defined as follows:

$$\boxed{\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}} \qquad \textbf{(3.11)}$$

The formal name for β_{ac} is *common-emitter, forward-current, amplification factor*. Since the collector current is usually the output current for a common-emitter configuration and the base current is the input current, the term *amplification* is included in the nomenclature above.

Equation (3.11) is similar in format to the equation for α_{ac} in Section 3.4. The procedure for obtaining α_{ac} from the characteristic curves was not described because of the difficulty of actually measuring changes of I_C and I_E on the characteristics. Equation (3.11), however, can be described with some clarity, and, in fact, the result can be used to find α_{ac} using an equation to be derived shortly.

On specification sheets β_{ac} is normally referred to as h_{fe}. Note that the only difference between the notation used for the dc beta, specifically, $\beta_{dc} = h_{FE}$, is the type of lettering for each subscript quantity.

The use of Eq. (3.11) is best described by a numerical example using an actual set of characteristics such as appearing in Fig. 3.13a and repeated in Fig. 3.17. Let us determine β_{ac} for a region of the characteristics defined by an operating point of $I_B = 25\ \mu\text{A}$ and $V_{CE} = 7.5$ V as indicated on Fig. 3.16. The restriction of V_{CE} = constant requires that a vertical line be drawn through the operating point at $V_{CE} = 7.5$ V. At any location on this vertical line the voltage V_{CE} is 7.5 V, a constant. The change in $I_B(\Delta I_B)$ as appearing in Eq. (3.11) is then defined by choosing two points on either side of the *Q*-point along the vertical axis of about equal distances to either side of the *Q*-point. For this situation the $I_B = 20\ \mu\text{A}$ and $30\ \mu\text{A}$ curves meet the requirement without extending too far from the *Q*-point. They also

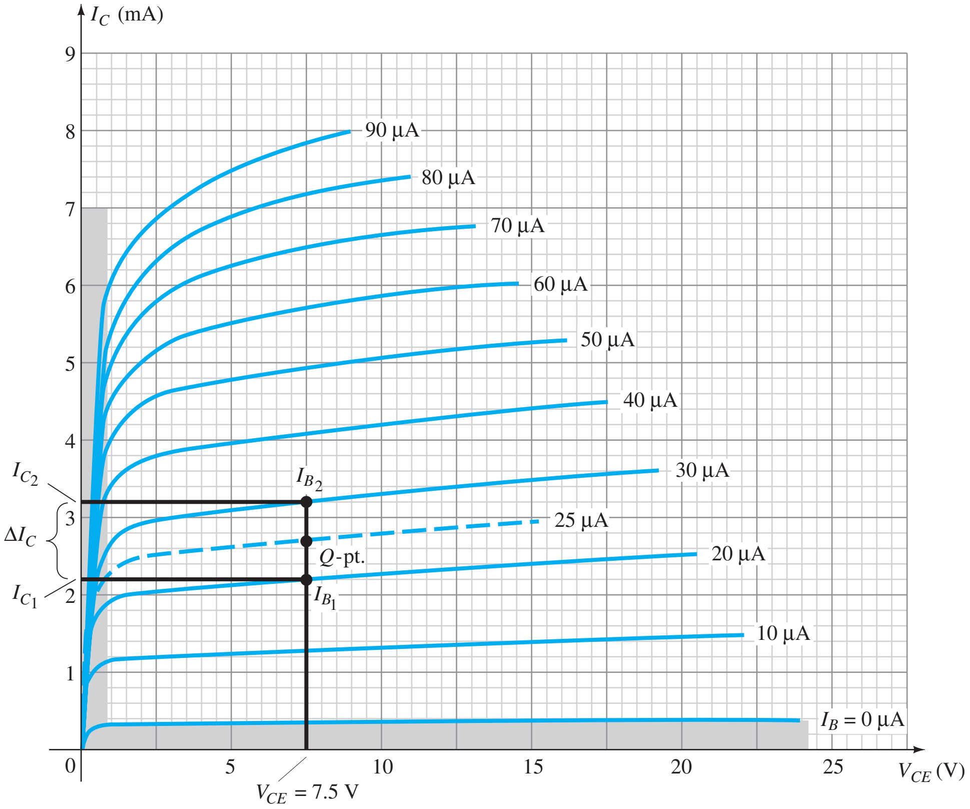


FIG. 3.16

Determining β_{ac} and β_{dc} from the collector characteristics.

define levels of I_B that are easily defined rather than require interpolation of the level of I_B between the curves. It should be mentioned that the best determination is usually made by keeping the chosen ΔI_B as small as possible. At the two intersections of I_B and the vertical axis, the two levels of I_C can be determined by drawing a horizontal line over to the vertical axis and reading the resulting values of I_C. The resulting β_{ac} for the region can then be determined by

$$\begin{aligned}\beta_{ac} &= \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}\\ &= \frac{3.2\text{ mA} - 2.2\text{ mA}}{30\ \mu\text{A} - 20\ \mu\text{A}} = \frac{1\text{ mA}}{10\ \mu\text{A}}\\ &= \mathbf{100}\end{aligned}$$

The solution above reveals that for an ac input at the base, the collector current will be about 100 times the magnitude of the base current.

If we determine the dc beta at the Q-point, we obtain

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\text{ mA}}{25\ \mu\text{A}} = \mathbf{108}$$

Although not exactly equal, the levels of β_{ac} and β_{dc} are usually reasonably close and are often used interchangeably. That is, if β_{ac} is known, it is assumed to be about the same magnitude as β_{dc}, and vice versa. Keep in mind that in the same lot (large number of transistors manufactured at the same time), the value of β_{ac} will vary somewhat from one transistor to the next even though each transistor has the same number code. The variation may not be significant, but for the majority of applications, it is certainly sufficient to validate the approximate approach above. Generally, the smaller the level of I_{CEO}, the closer are the magnitudes of the two betas. Since the trend is toward lower and lower levels of I_{CEO}, the validity of the foregoing approximation is further substantiated.

If the characteristics of a transistor are approximated by those appearing in Fig. 3.17, the level of β_{ac} would be the same in every region of the characteristics. Note that the step in I_B is fixed at 10 μA and the vertical spacing between curves is the same at every point in the characteristics—namely, 2 mA. Calculating the β_{ac} at the Q-point indicated results in

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{9\text{ mA} - 7\text{ mA}}{45\ \mu\text{A} - 35\ \mu\text{A}} = \frac{2\text{ mA}}{10\ \mu\text{A}} = \mathbf{200}$$

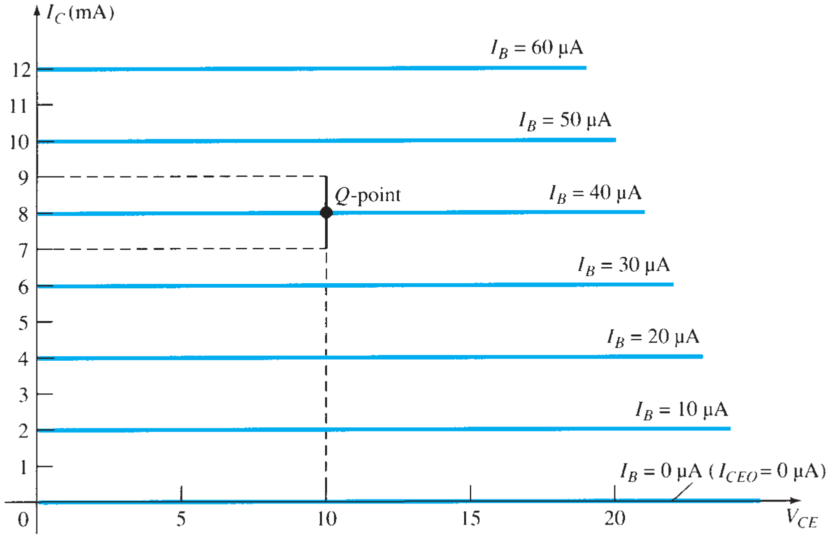


FIG. 3.17

Characteristics in which β_{ac} *is the same everywhere and* $\beta_{ac} = \beta_{dc}$.

Determining the dc beta at the same Q-point results in

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{8\text{ mA}}{40\ \mu\text{A}} = \mathbf{200}$$

revealing that if the characteristics have the appearance of Fig. 3.17, the magnitudes of β_{ac} and β_{dc} *will be the same* at every point on the characteristics. In particular, note that $I_{CEO} = 0\ \mu$A.

Although a true set of transistor characteristics will never have the exact appearance of Fig. 3.17, it does provide a set of characteristics for comparison with those obtained from a curve tracer (to be described shortly).

For the analysis to follow, the subscript dc or ac will not be included with β to avoid cluttering the expressions with unnecessary labels. For dc situations it will simply be recognized as β_{dc} and for any ac analysis as β_{ac}. If a value of β is specified for a particular transistor configuration, it will normally be used for both the dc and ac calculations.

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$, we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C results in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \tag{3.12}$$

or

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} \tag{3.13}$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \tag{3.14}$$

as indicated on Fig. 3.13a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$\boxed{I_C = \beta I_B} \tag{3.15}$$

and since

$$\begin{aligned} I_E &= I_C + I_B \\ &= \beta I_B + I_B \end{aligned}$$

we have

$$\boxed{I_E = (\beta + 1)I_B} \tag{3.16}$$

Both of the equations above play a major role in the analysis in Chapter 4.

Biasing

The proper biasing of a common-emitter amplifier can be determined in a manner similar to that introduced for the common-base configuration. Let us assume that we are presented with an *npn* transistor such as shown in Fig. 3.18a and asked to apply the proper biasing to place the device in the active region.

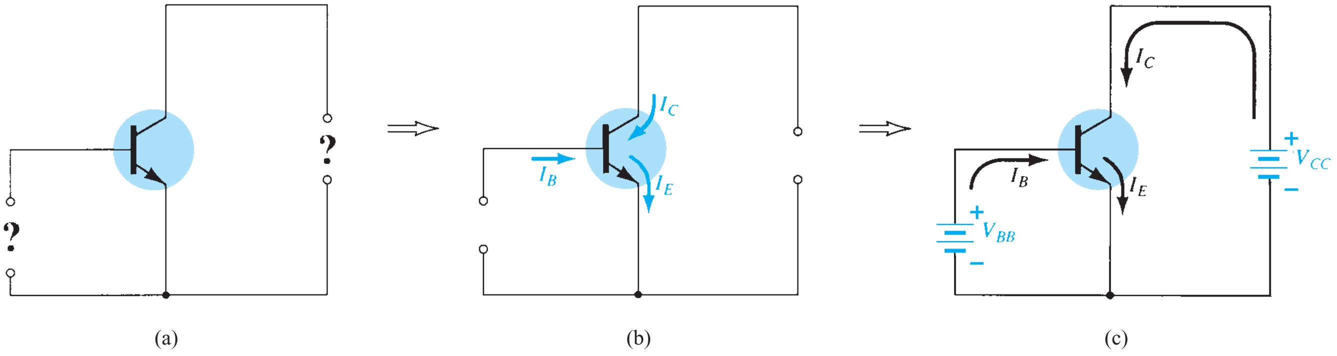


FIG. 3.18

Determining the proper biasing arrangement for a common-emitter npn transistor configuration.

The first step is to indicate the direction of I_E as established by the arrow in the transistor symbol as shown in Fig. 3.18b. Next, the other currents are introduced as shown, keeping in mind Kirchhoff's current law relationship: $I_C + I_B = I_E$. That is, I_E is the sum of I_C and I_B and both I_C and I_B must enter the transistor structure. Finally, the supplies are introduced with polarities that will support the resulting directions of I_B and I_C as shown in Fig. 3.18c to complete the picture. The same approach can be applied to *pnp* transistors. If the transistor of Fig. 3.18 was a *pnp* transistor, all the currents and polarities of Fig. 3.18c would be reversed.

Breakdown Region

As with the common-base configuration, there is a maximum collector-emitter voltage that can be applied and still remain in the active stable region of operation. In Fig. 3.19 the characteristics of Fig. 3.8 have been extended to demonstrate the impact on the characteristics at high levels of V_{CE}. At high levels of base current the currents almost climb vertically, whereas at lower levels a region develops that seems to back up on itself. This region is particularly noteworthy because an increase in current is resulting in a drop in voltage—totally different from that of any resistive element where an increase in current results in an increase in potential drop across the resistor. Regions of this nature are said to have a

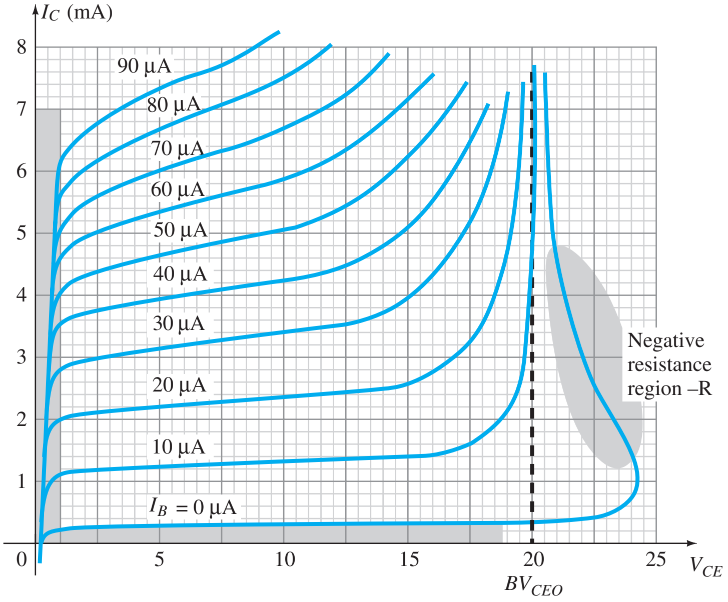


FIG. 3.19

Examining the breakdown region of a transistor in the common-emitter configuration.

negative-resistance characteristic. Although the concept of a negative resistance may seem strange at this point, this text will introduce devices and systems that rely on this type of characteristic to perform their desired task.

The recommended maximum value for a transistor under normal operating conditions is labeled BV_{CEO} as shown in Fig. 3.19 or $V_{(BR)CEO}$ as shown in Fig. 3.23. It is less than BV_{CBO} and in fact, is often half the value of BV_{CBO}. For this breakdown region there are two reasons for the dramatic change in the curves. One is the **avalanche breakdown** mentioned for the common-base configuration, whereas the other, called **punch-through**, is due to the **Early Effect**, to be introduced in Chapter 5. In total the avalanche effect is dominant because any increase in base current due to the breakdown phenomena will be increase the resulting collector current by a factor beta. This increase in collector current will then contribute to the ionization (generation of free carriers) process during breakdown, which will cause a further increase in base current and even higher levels of collector current.

3.6 COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration*, shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

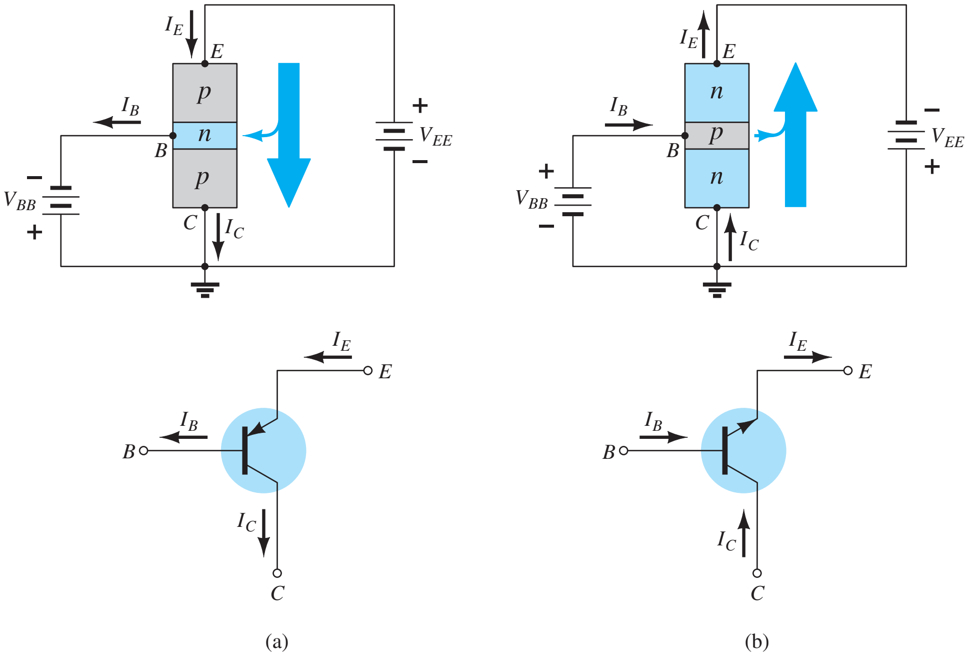


FIG. 3.20
Notation and symbols used with the common-collector configuration: (a) pnp transistor; (b) npn transistor.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.5. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{CE} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable

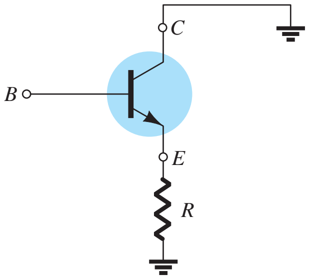


FIG. 3.21
Common-collector configuration used for impedance-matching purposes.

change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

3.7 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.8.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as *continuous* collector current) and maximum collector-to-emitter voltage (often abbreviated as BV_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{C_{\max}}$ was specified as 50 mA and BV_{CEO} as 20 V. The vertical line on the characteristics defined as $V_{CE_{\text{sat}}}$ specifies the minimum V_{CE} that can be applied without falling into the nonlinear region labeled the *saturation* region. The level of $V_{CE_{\text{sat}}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.

The maximum dissipation level is defined by the following equation:

$$\boxed{P_{C_{\max}} = V_{CE}I_C} \tag{3.17}$$

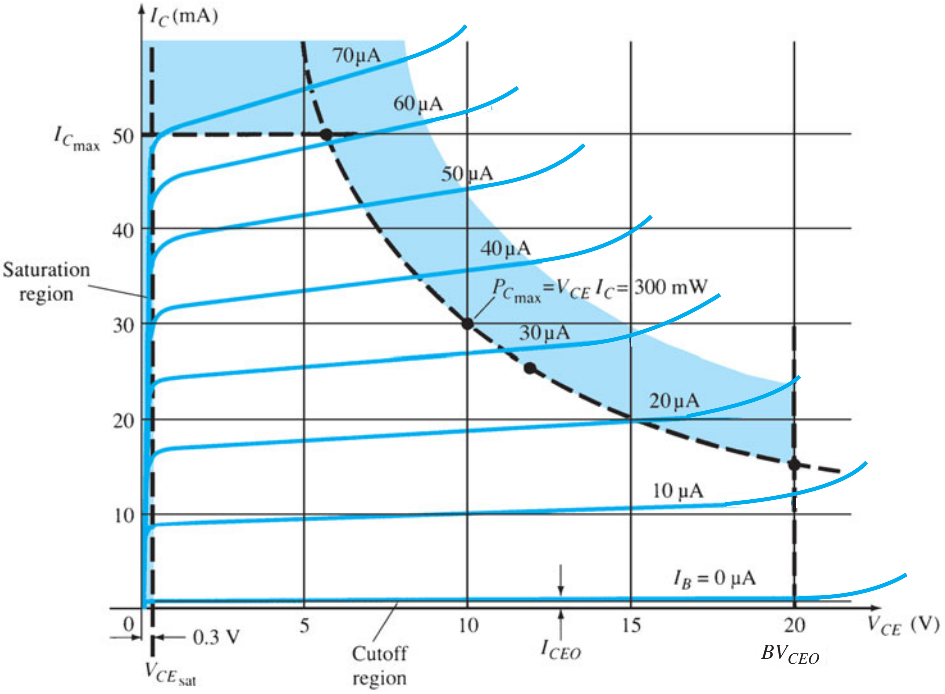


FIG. 3.22

Defining the linear (undistorted) region of operation for a transistor.

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{\max}} = V_{CE}I_C = 300 \text{ mW}$$

or

$$V_{CE}I_C = 300 \text{ mW}$$

At $I_{C_{\max}}$ At any point on the characteristics the product of V_{CE} and I_C must be equal to 300 mW. If we choose I_C to be the maximum value of 50 mA and substitute into the relationship above, we obtain

$$V_{CE}I_C = 300\text{ mW}$$
$$V_{CE}(50\text{ mA}) = 300\text{ mW}$$
$$V_{CE} = \frac{300\text{ mW}}{50\text{ mA}} = \mathbf{6\ V}$$

At $V_{CE_{\max}}$ As a result we find that if $I_C = 50$ mA, then $V_{CE} = 6$ V on the power dissipation curve as indicated in Fig. 3.22. If we now choose V_{CE} to be its maximum value of 20 V, the level of I_C is the following:

$$(20\text{ V})I_C = 300\text{ mW}$$
$$I_C = \frac{300\text{ mW}}{20\text{ V}} = \mathbf{15\ mA}$$

defining a second point on the power curve.

At $I_C = \frac{1}{2}I_{C_{\max}}$ If we now choose a level of I_C in the midrange such as 25 mA and solve for the resulting level of V_{CE}, we obtain

$$V_{CE}(25\text{ mA}) = 300\text{ mW}$$

and

$$V_{CE} = \frac{300\text{ mW}}{25\text{ mA}} = \mathbf{12\ V}$$

as also indicated in Fig. 3.22.

A rough estimate of the actual curve can usually be drawn using the three points defined above. Of course, the more points one has, the more accurate is the curve, but a rough estimate is normally all that is required.

The *cutoff* region is defined as that region below $I_C = I_{CEO}$. This region must also be avoided if the output signal is to have minimum distortion. On some specification sheets only I_{CBO} is provided. One must then use the equation $I_{CEO} = \beta I_{CBO}$ to establish some idea of the cutoff level if the characteristic curves are unavailable. Operation in the resulting region of Fig. 3.22 will ensure minimum distortion of the output signal and current and voltage levels that will not damage the device.

If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE}I_C$ fall into the following range:

$$\boxed{\begin{aligned} I_{CEO} &\leqq \boldsymbol{I_C} \leqq I_{C_{\max}} \\ V_{CE_{\text{sat}}} &\leqq \boldsymbol{V_{CE}} \leqq V_{CE_{\max}} \\ &\boldsymbol{V_{CE}I_C} \leqq P_{C_{\max}} \end{aligned}} \qquad \mathbf{(3.18)}$$

For the common-base characteristics the maximum power curve is defined by the following product of output quantities:

$$\boxed{P_{C_{\max}} = V_{CB}I_C} \qquad \mathbf{(3.19)}$$

3.8 TRANSISTOR SPECIFICATION SHEET

Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood. Although all the parameters have not been introduced, a broad number will now be familiar. The remaining parameters will be introduced in the chapters that follow. Reference will then be made to this specification sheet to review the manner in which the parameter is presented.

The information provided as Fig. 3.23 is provided by the Fairchild Semiconductor Corporation. The 2N4123 is a general-purpose *npn* transistor with the casing and terminal identification appearing in the top-right corner of Fig. 3.23a. Most specification sheets are broken down into *maximum ratings*, *thermal characteristics*, and *electrical characteristics*. The electrical characteristics are further broken down into “on,” “off,” and small-signal characteristics. The “on” and “off” characteristics refer to dc limits, whereas the small-signal characteristics include the parameters of importance to ac operation.

Note in the maximum rating list that $V_{CE_{\max}} = V_{CEO} = 30\text{ V}$ with $I_{C_{\max}} = 200\text{ mA}$. The maximum collector dissipation $P_{C_{\max}} = P_D = 625\text{ mW}$. The derating factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1° rise in temperature above 25°C. In the “off” characteristics I_{CBO} is specified as 50 nA

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25˚C Derate above 25˚C	P_D	625 5.0	mW mW˚C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	–55 to +150	˚C

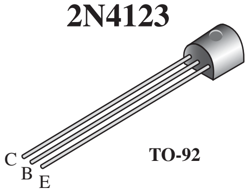
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	˚C W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	˚C W

FAIRCHILD

SEMICONDUCTOR ™

2N4123



General Purpose
Transistor
NPN Silicon

ELECTRICAL CHARACTERISTICS (T_A = 25˚C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250		MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 MHz)	C_{obo}	–	4.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ibo}	–	8.0	pF
Collector-Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 100 kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	200	–
Current Gain – High Frequency (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	NF	–	6.0	dB

(1) Pulse Test: Pulse Width = 300 μs. Duty Cycle = 2.0%

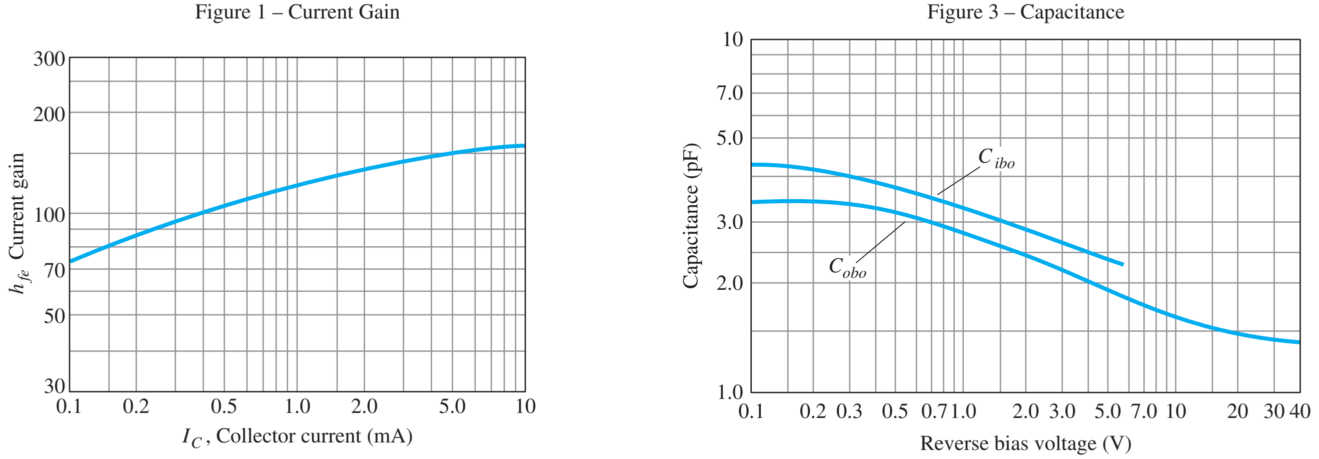
(a)

FIG. 3.23

Transistor specification sheet.

h PARAMETERS

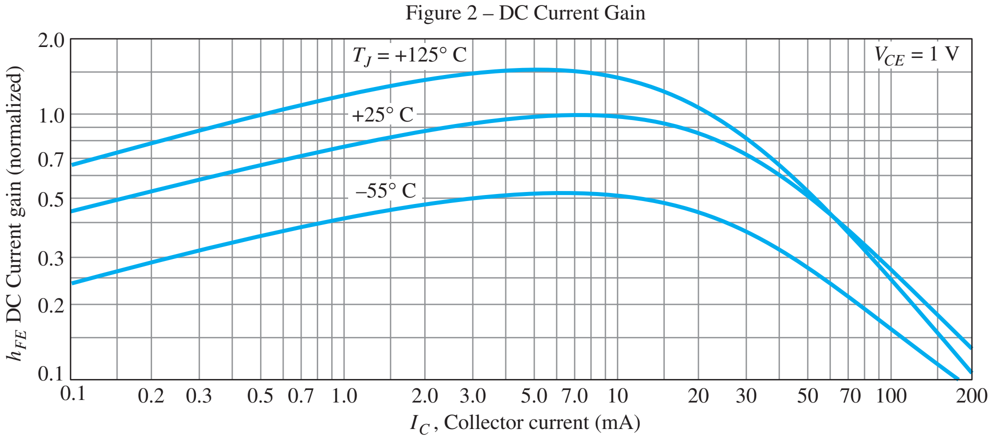
$V_{CE} = 10$ V, $f = 1$ kHz, $T_A = 25$°C



(b)

(d)

STATIC CHARACTERISTICS

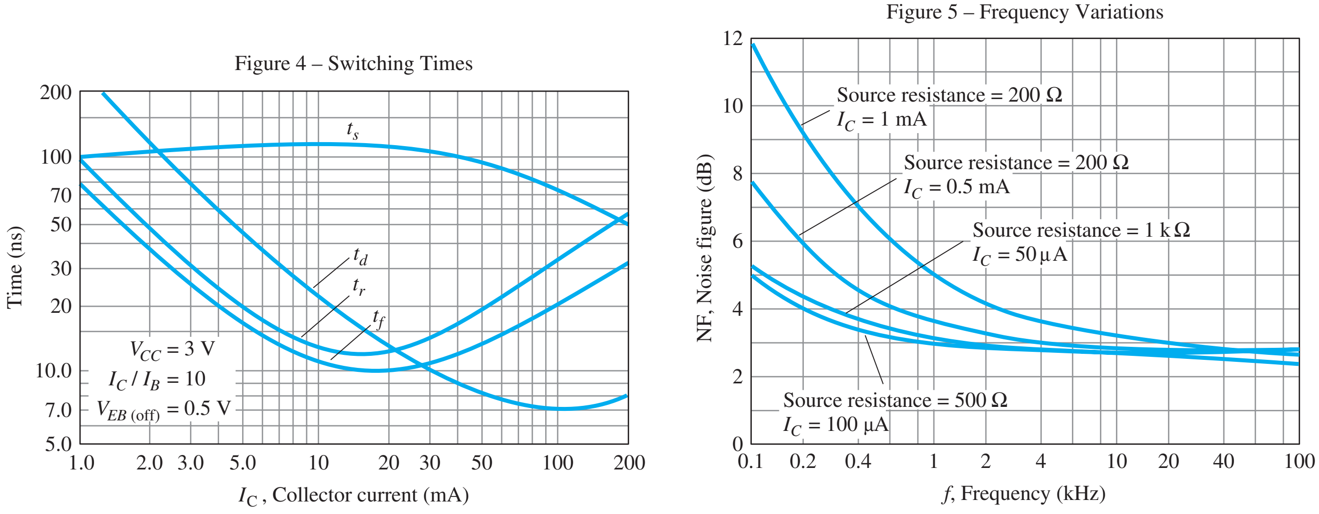


(c)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

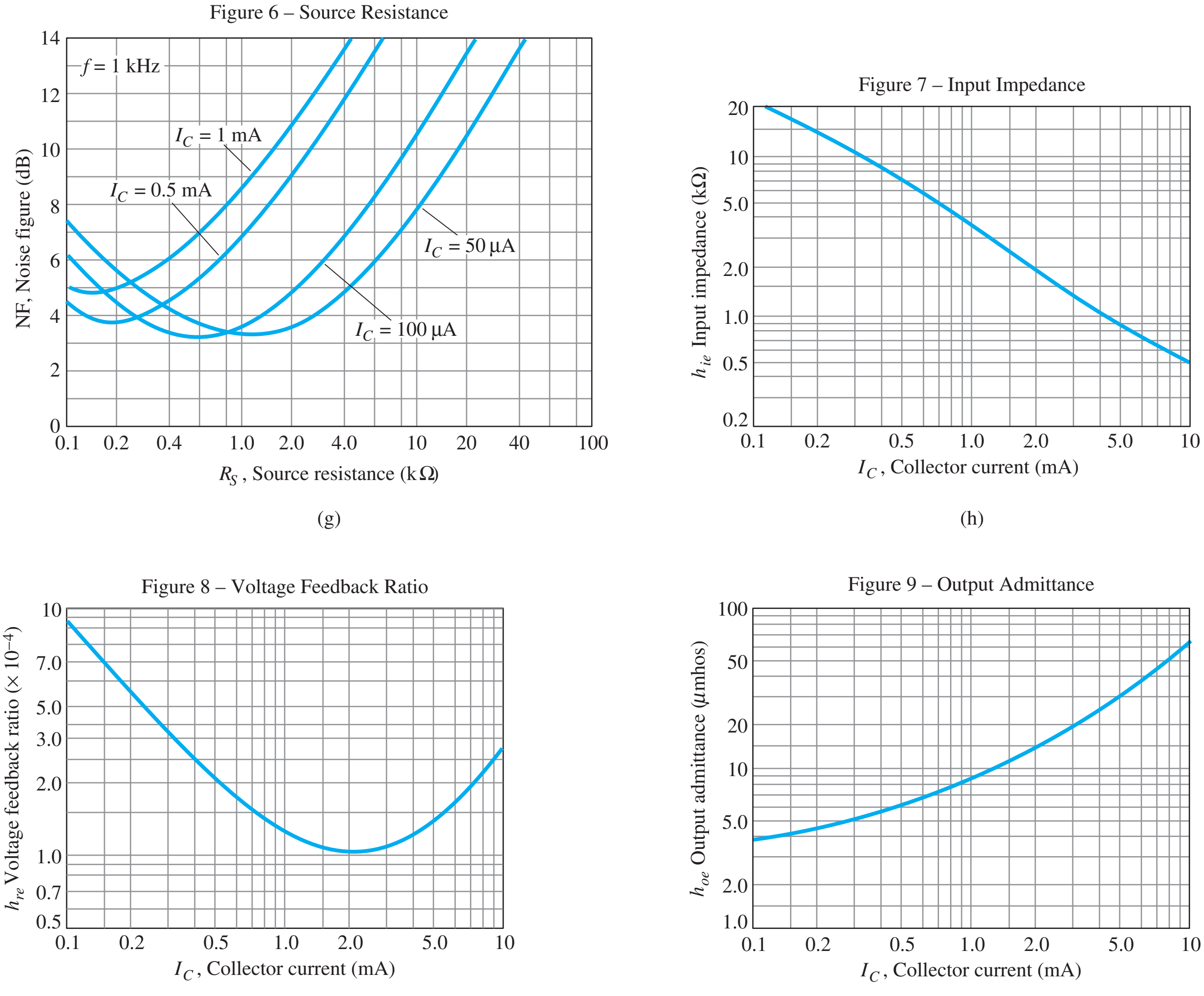
($V_{CE} = 5$ Vdc, $T_A = 25$°C)
Bandwidth = 1.0 Hz



(e)

(f)

FIG. 3.23
Continued.



(g) (h)

(i) (j)

FIG. 3.23

Continued.

and in the "on" characteristics $V_{CE_{sat}} = 0.3$ V. The level of h_{FE} has a range of 50 to 150 at $I_C = 2$ mA and $V_{CE} = 1$ V and a minimum value of 25 at a higher current of 50 mA at the same voltage.

The limits of operation have now been defined for the device and are repeated below in the format of Eq. (3.18) using $h_{FE} = 150$ (the upper limit) and $I_{CEO} \cong \beta I_{CBO} = (150)(50\text{ nA}) = 7.5\ \mu\text{A}$. Certainly, for many applications the $7.5\ \mu\text{A} = 0.0075$ mA can be considered to be 0 mA on an approximate basis.

Limits of Operation

$$7.5\ \mu\text{A} \leqq \boldsymbol{I_C} \leqq 200\text{ mA}$$
$$0.3\text{ V} \leqq \boldsymbol{V_{CE}} \leqq 30\text{ V}$$
$$\boldsymbol{V_{CE}I_C} \leqq 650\text{ mW}$$

β Variation

In the small-signal characteristics the level of h_{fe} (β_{ac}) is provided along with a plot of how it varies with collector current in Fig. 3.23b. In Fig. 3.23c the effect of temperature and collector current on the level of h_{FE} (β_{dc}) is demonstrated. At room temperature (25°C), note that h_{FE} (β_{dc}) is a maximum value of 1 in the neighborhood of about 8 mA. As I_C increases beyond this level, h_{FE} drops off to one-half the value with I_C equal to 50 mA. It also drops to this level if I_C decreases to the low level of 0.15 mA. Since this is a *normalized* curve, if we have a transistor with $\beta_{dc} = h_{FE} = 120$ at room temperature (25°C), the maximum value at 8 mA is 120. At $I_C = 50$ mA it has dropped to about 0.52 and $h_{fe} = (0.52)120 = 62.4$. In other words, normalizing reveals that the actual level of h_{FE} at any level of I_C has been divided by the maximum value of h_{FE} at that temperature and $I_C = 8$ mA. Note also that the horizontal scale of Fig. 3.23(c) is a log scale. Log scales are examined in depth in Chapter 9. You may want to look back at the plots of this section when you find time to review the first few sections of Chapter 9.

Capacitance Variation The capacitance C_{ibo} and C_{obo} of Fig. 3.23(d) are the input and output capacitance levels, respectively, for the transistor in the common-base configuration. Their level is such that their impact can be ignored except for relatively high frequencies. Otherwise, they can be approximated by open circuits in any dc or ac analysis.

Switching Times Figure 3.23(e) includes the important parameters that define the response of a transistor to an input that switches from the "off" to "on" state or vice versa. Each parameter will be discussed in detail in Section 4.15.

Noise Figures Versus Frequency and Source Resistance The noise figure is a measure of the additional disturbance that is added to the desired signal response of an amplifier. In Fig. 3.23(f) the dB level of the noise figure is displayed for a wide frequency response at particular levels of source resistance. The lowest levels occur at the highest frequencies for the variety of collector currents and source resistance. As the frequency drops the noise figure increases with a strong sensitivity to the collector current.

In Fig. 3.23(g) the noise figure is plotted for various levels of source resistance and collector current. For each current level the higher the source resistance, the higher the noise figure.

Hybrid Parameters Figures 3.23(b), (h), (i), and (j) provide the components of a hybrid equivalent model for the transistor that will be discussed in detail in Chapter 5. In each case, note that the variation is plotted against the collector current—a defining level for the equivalent network. For most applications the most important parameters are h_{fe} and h_{ie}. The higher the collector current, the higher the magnitude of h_{fe} and the lower the level of h_{ie}. As indicated above, all the parameters will be discussed in detail in Sections 5.19–5.21.

Before leaving this description of the characteristics, note that the actual collector characteristics are not provided. In fact, most specification sheets provided by manufacturers fail to provide the full characteristics. It is expected that the data provided are sufficient to use the device effectively in the design process.

3.9 TRANSISTOR TESTING

As with diodes, there are three routes one can take to check a transistor: use of a *curve tracer*, a *digital meter*, and an *ohmmeter.*

Curve Tracer

The curve tracer of Fig. 1.43 will provide the display of Fig. 3.24 once all the controls have been properly set. The smaller displays to the right reveal the scaling to be applied to the characteristics. The vertical sensitivity is 2 mA/div, resulting in the scale shown to the left of the monitor's display. The horizontal sensitivity is 1 V/div, resulting in the scale shown below the characteristics. The step function reveals that the curves are separated by a difference of 10 μA, starting at 0 μA for the bottom curve. The last scale factor provided can be used to quickly determine the β_{ac} for any region of the characteristics. Simply multiply the displayed factor by the number of divisions between I_B curves in the region of interest. For instance, let us determine β_{ac} at a Q-point of $I_C = 7$ mA and $V_{CE} = 5$ V. In this region of the display, the distance between I_B curves is $\frac{9}{10}$ of a division, as indicated on Fig. 3.25. Using the factor specified, we find that

$$\beta_{ac} = \frac{9}{10}\,\cancel{\text{div}}\left(\frac{200}{\cancel{\text{div}}}\right) = \mathbf{180}$$

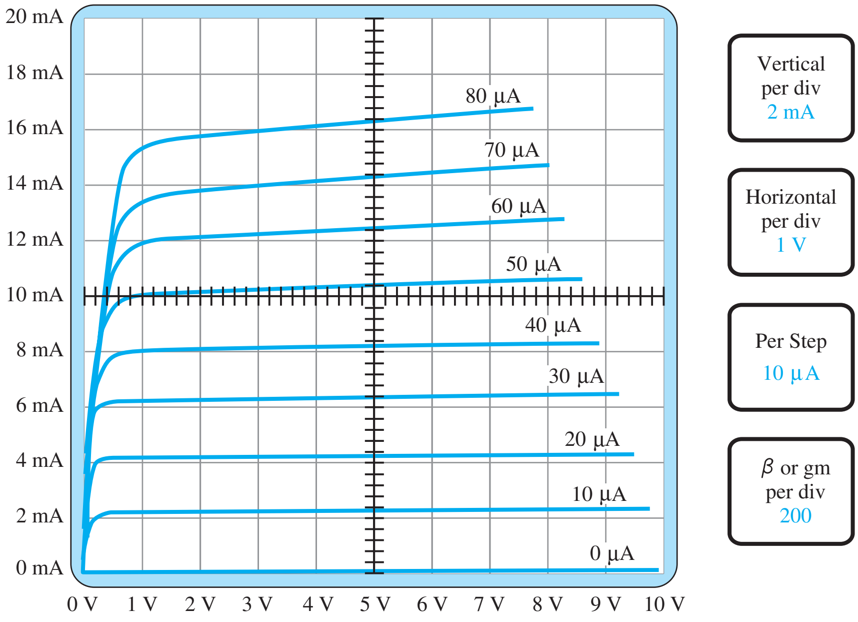


FIG. 3.24

Curve tracer response to 2N3904 npn transistor.

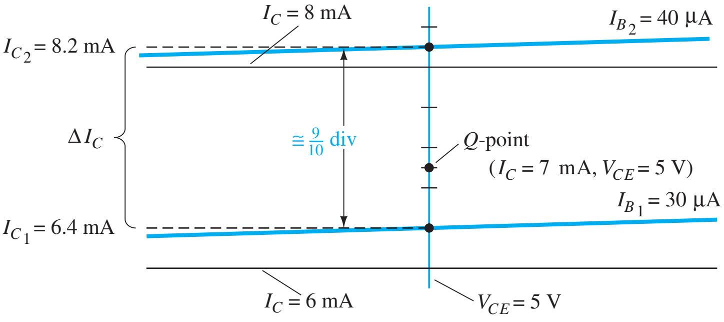

$I_C = 8$ mA
$I_{C_2} = 8.2$ mA
$I_{B_2} = 40$ μA
ΔI_C
$\cong \frac{9}{10}$ div
Q-point
($I_C = 7$ mA, $V_{CE} = 5$ V)
$I_{B_1} = 30$ μA
$I_{C_1} = 6.4$ mA
$I_C = 6$ mA
$V_{CE} = 5$ V

FIG. 3.25

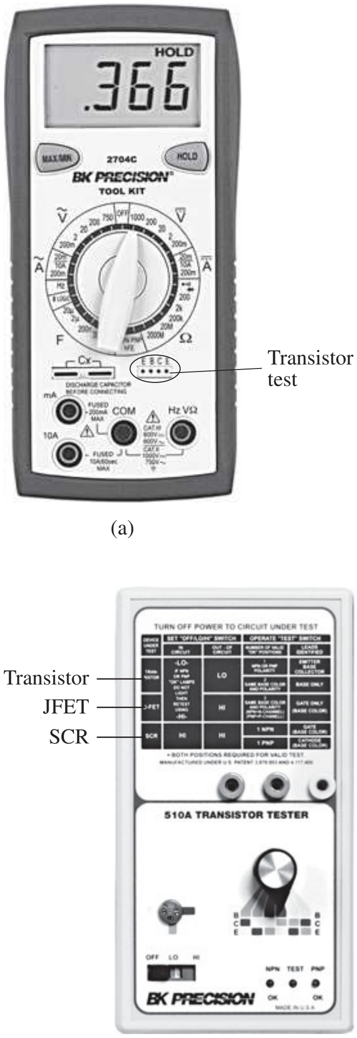
Determining β_{ac} for the transistor characteristics of Fig. 3.24 at $I_C = 7$ mA and $V_{CE} = 5$ V.

Using Eq. (3.11) gives

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{8.2\text{ mA} - 6.4\text{ mA}}{40\ \mu\text{A} - 30\ \mu\text{A}}$$

$$= \frac{1.8\text{ mA}}{10\ \mu\text{A}} = \mathbf{180}$$

verifying the determination above.


HOLD
.366
2704C
BK PRECISION
TOOL KIT
Transistor test
Transistor
JFET
SCR
510A TRANSISTOR TESTER
BK PRECISION

(a)

(b)

FIG. 3.26

Transistor testers: (a) digital meter; (b) dedicated tester. (Courtesy of B+K Precision Corporation.)

Transistor Testers

There is a variety of transistor testers available. Some are simply part of a digital meter as shown in Fig. 3.26a that can measure a variety of levels in a network. Others, such as that in Fig. 3.26, are dedicated to testing a limited number of elements. The meter of Fig. 3.26b can be used to test transistors, JFETs (Chapter 6), and SCRs (Chapter 17) in and out of the circuit. In all cases the power must first be turned off to the circuit in which the element appears to ensure that the internal battery of the tester is not damaged and to provide a correct reading. Once a transistor is connected, the switch can be moved through all the possible combinations until the test light comes on and identifies the terminals of the transistor. The tester will also indicate an OK if the *npn* or *pnp* transistor is operating properly.

Any meter with a diode-checking capability can also be used to check the status of a transistor. With the collector open the base-to-emitter junction should result in a low voltage of about 0.7 V with the red (positive) lead connected to the base and the black (negative) lead connected to the emitter. A reversal of the leads should result in an OL indication to represent the reverse-biased junction. Similarly, with the emitter open, the forward- and reverse-bias states of the base-to-collector junction can be checked.

Ohmmeter

An ohmmeter or the resistance scales of a *d*igital *m*ulti*m*eter (DMM) can be used to check the state of a transistor. Recall that for a transistor in the active region the base-to-emitter junction is forward-biased and the base-to-collector junction is reverse-biased. Essentially, therefore, the forward-biased junction should register a relatively low resistance, whereas the reverse-biased junction shows a much higher resistance. For an *npn* transistor, the forward-biased junction (biased by the internal supply in the resistance mode) from base to emitter should be checked as shown in Fig. 3.27 and result in a reading that will typically fall in the range of 100 Ω to a few kilohms. The reverse-biased base-to-collector junction (again reverse-biased by the internal supply) should be checked as shown in Fig. 3.28 with a reading typically exceeding 100 kΩ. For a *pnp* transistor the leads are reversed for each junction. Obviously, a large or small resistance in both directions (reversing the leads) for either junction of an *npn* or *pnp* transistor indicates a faulty device.

If both junctions of a transistor result in the expected readings, the type of transistor can also be determined by simply noting the polarity of the leads as applied to the base-emitter junction. If the positive (+) lead is connected to the base and the negative lead (−) to the emitter, a low resistance reading would indicate an *npn* transistor. A high resistance reading would indicate a *pnp* transistor. Although an ohmmeter can also be used to determine the leads (base, collector, and emitter) of a transistor, it is assumed that this determination can be made by simply looking at the orientation of the leads on the casing.

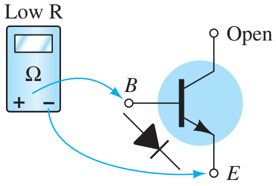


FIG. 3.27
Checking the forward-biased base-to-emitter junction of an npn transistor.

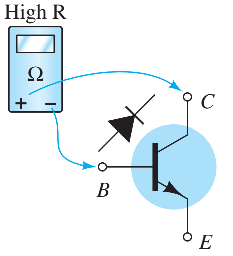


FIG. 3.28
Checking the reverse-biased base-to-collector junction of an npn transistor.

3.10 TRANSISTOR CASING AND TERMINAL IDENTIFICATION

After the transistor has been manufactured using one of the techniques described in Appendix A, leads of, typically, gold, aluminum, or nickel are then attached and the entire structure is encapsulated in a container such as that shown in Fig. 3.29. Those with the heavy-duty construction are high-power devices, whereas those with the small can (top hat) or plastic body are low- to medium-power devices.

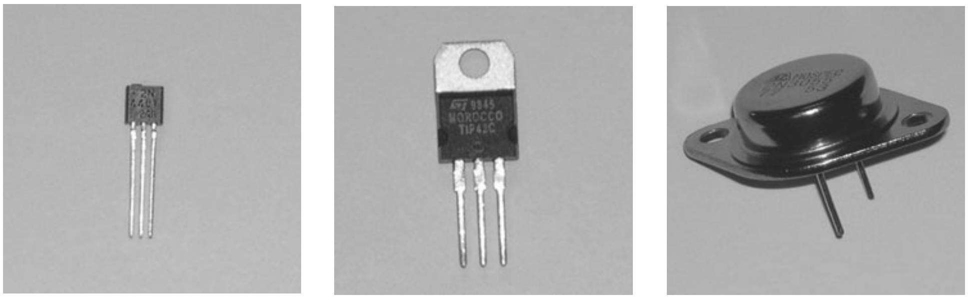

(a) (b) (c)

FIG. 3.29
Various types of general-purpose or switching transistors: (a) low power; (b) medium power; (c) medium to high power.

Whenever possible, the transistor casing will have some marking to indicate which leads are connected to the emitter, collector, or base of a transistor. A few of the methods commonly used are indicated in Fig. 3.30.

The internal construction of a TO-92 package in the Fairchild line appears in Fig. 3.31. Note the very small size of the actual semiconductor device. There are gold bond wires, a copper frame, and an epoxy encapsulation.

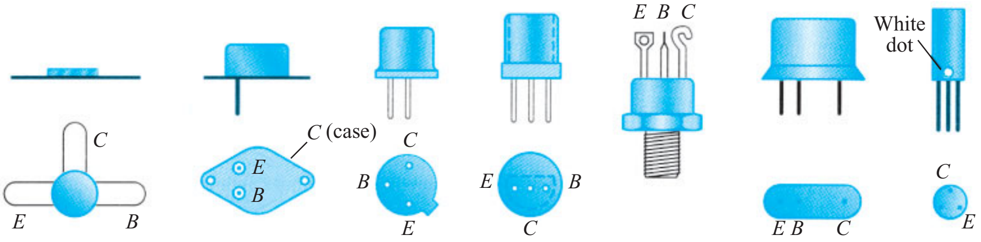
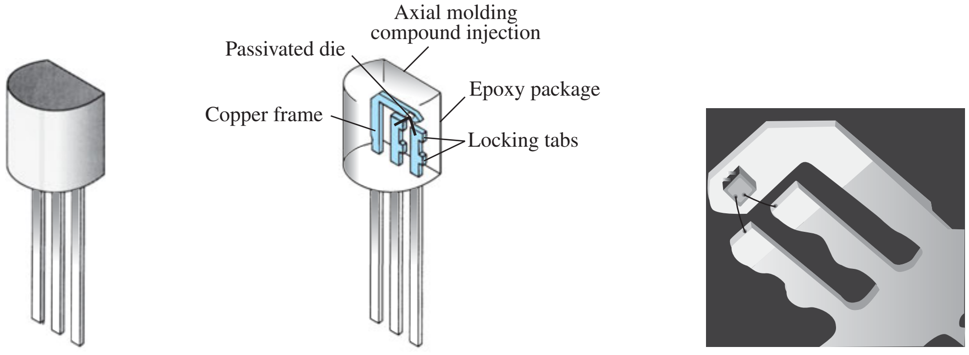

C
E
B
C (case)
E
B
C
B
E
E
B
C
E B C
White dot
E B
C
C
E

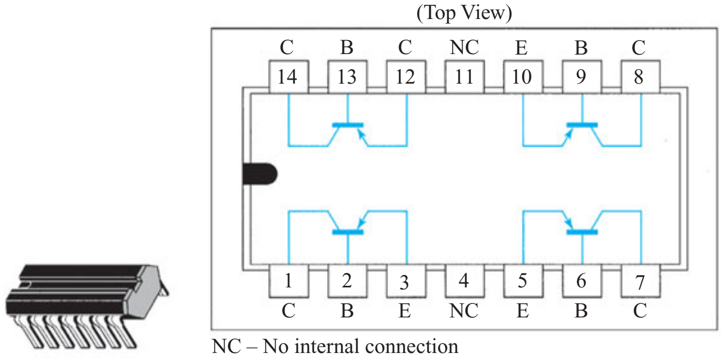
FIG. 3.30
Transistor terminal identification.


Axial molding compound injection
Passivated die
Epoxy package
Copper frame
Locking tabs

(a) (b) (c)

FIG. 3.31
Internal construction of a Fairchild transistor in a TO-92 package.

Four (quad) individual *pnp* silicon transistors can be housed in the 14-pin plastic dual-in-line package appearing in Fig. 3.32a. The internal pin connections appear in Fig. 3.32b. As with the diode IC package, the indentation in the top surface reveals the number 1 and 14 pins.


(Top View)
C B C NC E B C
14 13 12 11 10 9 8
1 2 3 4 5 6 7
C B E NC E B C

NC – No internal connection

(a) (b)

FIG. 3.32
Type Q2T2905 Texas Instruments quad pnp silicon transistor:
(a) appearance; (b) pin connections.

3.11 TRANSISTOR DEVELOPMENT

As mentioned in Section 1.1, Moore's law predicts that the transistor count of an integrated circuit will double every 2 years. First presented in a paper by Gordon E. Moore in 1965, the prediction has had an amazing accuracy level. A plot of the transistor count versus years appearing in Fig. 3.33 is almost linear through the years. The amazing number of two billion transistors in a single integrated circuit using 45 nm lines is really beyond comprehension. A 1 in. line contains more than 564,000 of the 45 nm lines of construction used in ICs today. Try to draw 100 lines in a 1 in. width using a pencil—almost impossible. The relative dimensions of drawing 45 nm lines in a 1 in. width would be like drawing a line

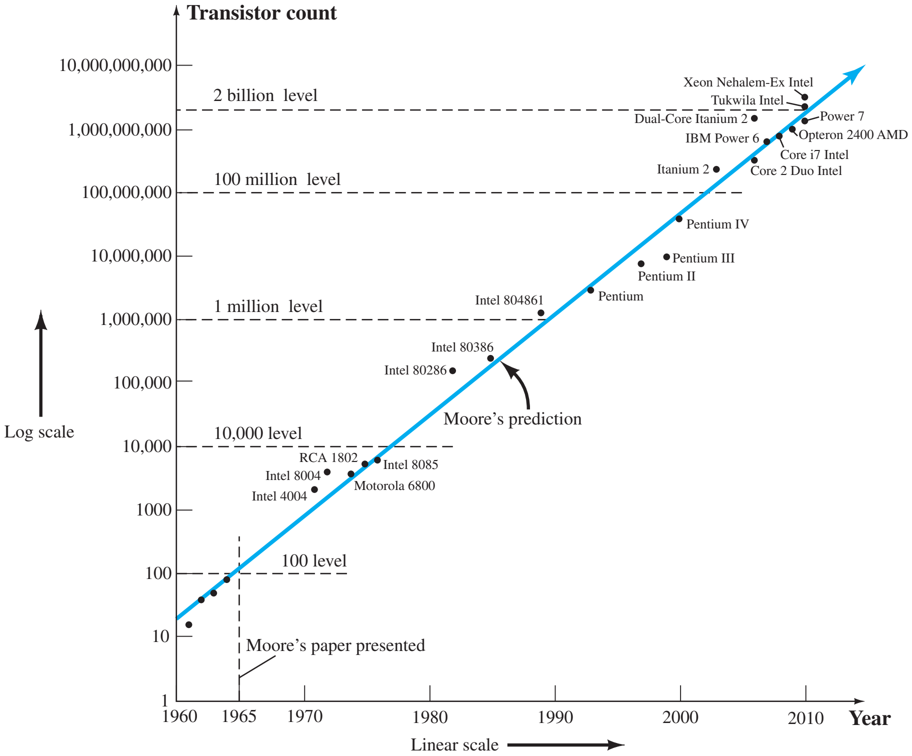


FIG. 3.33

Transistor IC count versus time for the period 1960 to the present.

with a width of 1 in. across a highway that is almost 9 miles long.* Although there is continuing talk that Moore's law will eventually suffer from density, performance, reliability, and budget corners, the general consensus of the industrial community is that Moore's law will continue to be applicable for the next decade or two. Although silicon continues to be the leading fabrication material, there is a family of semiconductors referred to as III V **compound semiconductors** (the three and five referring to the number of valence electrons in each element) that are making important inroads into future development. One in particular is indium gallium arsenide, or **InGaAs**, which has improved transport characteristics. Others include **GaAlAs, AlGaN, and AllnN**, which are all being developed for increased speed, reliability, stability, reduced size, and improved fabrication techniques.

Currently the **Intel® Core™ i7 Quad Core** processor has over 730 million transistors with a clock speed of 3.33 GHz in a package slightly larger than a 1.6″ square. Recent developments by Intel include their **Tukwila** processor that will house over two billion transistors. Interestingly enough, Intel continues to employ silicon in its research development of transistors that will be 30% smaller and 25% faster than today's fastest transistors using 20 nm technology. IBM, in concert with the Georgia Institute of Technology, has developed a silicon-germanium transistor that can operate at frequencies exceeding 500 GHz—an enormous increase over current standards.

Innovation continues to be the backbone of this ever-developing field, with one Swedish team introducing a **junctionless** transistor primarily to simplify the manufacturing process. Another has introduced **carbon nanotubes** (a carbon molecule in the form of a hollow cylinder that has a diameter about 1/50,000 the width of a human hair) as a path toward faster, smaller, and cheaper transistors. Hewlett Packard is developing a **Crossbar Latch** transistor that employs a grid of parallel conducting and signal wires to create junctions that act as switches.

The question was often asked many years ago: Where can the field go from here? Obviously, based on what we see today, there seems to be no limit to the innovative spirit of individuals in the field as they search for new directions of investigation.

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*In metric units, it would be like drawing more than 220,000 lines in a 1-cm length or a 1-cm width line across a highway over 2.2 km long.

3.12 SUMMARY

Important Conclusions and Concepts

1. Semiconductor devices have the following advantages over vacuum tubes: They are (1) of **smaller size**, (2) more **lightweight**, (3) more **rugged**, and (4) more **efficient**. In addition, they have (1) **no warm-up period**, (2) **no heater requirement**, and (3) **lower operating voltages**.
2. Transistors are **three-terminal devices** of three semiconductor layers having a base or center layer a great deal **thinner** than the other two layers. The outer two layers are both of either *n*- or *p*-type materials, with the sandwiched layer the opposite type.
3. One *p–n* junction of a transistor is **forward-biased**, whereas the other is **reverse-biased**.
4. The dc emitter current is always the **largest current** of a transistor, whereas the base current is always the **smallest**. The emitter current is always the **sum** of the other two.
5. The collector current is made up of **two components**: the **majority component** and the **minority current** (also called the ***leakage*** **current**).
6. The arrow in the transistor symbol defines the direction of **conventional current flow for the emitter current** and thereby defines the direction for the other currents of the device.
7. A three-terminal device needs **two sets of characteristics** to completely define its characteristics.
8. In the active region of a transistor, the base–emitter junction is **forward-biased**, whereas the collector–base junction is **reverse-biased**.
9. In the cutoff region the base–emitter and collector–base junctions of a transistor are **both reverse-biased**.
10. In the saturation region the base–emitter and collector–base junctions are **forward-biased**.
11. On an average basis, as a first approximation, the base-to-emitter voltage of an operating transistor can be assumed to be **0.7 V**.
12. The quantity alpha (α) relates the collector and emitter currents and is always close to **one**.
13. The impedance between terminals of a forward-biased junction is always relatively **small**, whereas the impedance between terminals of a reverse-biased junction is usually **quite large**.
14. The arrow in the symbol of an *npn* transistor points out of the device (**n**ot **p**ointing **in**), whereas the arrow points in to the center of the symbol for a *pnp* transistor (**p**ointing **in**).
15. For linear amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.
16. The quantity beta (β) provides an important relationship between the base and collector currents, and is usually between **50 and 400**.
17. The dc beta is defined by a simple **ratio of dc currents at an operating point**, whereas the ac beta is **sensitive to the characteristics** in the region of interest. For most applications, however, the two are considered equivalent as a first approximation.
18. To ensure that a transistor is operating within its maximum power level rating, simply find the **product of the collector-to-emitter voltage and the collector current**, and compare it to the rated value.

Equations

$$I_E = I_C + I_B, \qquad I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}, \qquad V_{BE} \cong 0.7\ \text{V}$$

$$\alpha_{\text{dc}} = \frac{I_C}{I_E}, \qquad \alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}, \qquad I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\ \mu\text{A}}$$

$$\beta_{\text{dc}} = \frac{I_C}{I_B}, \qquad \beta_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}, \qquad \alpha = \frac{\beta}{\beta + 1}$$

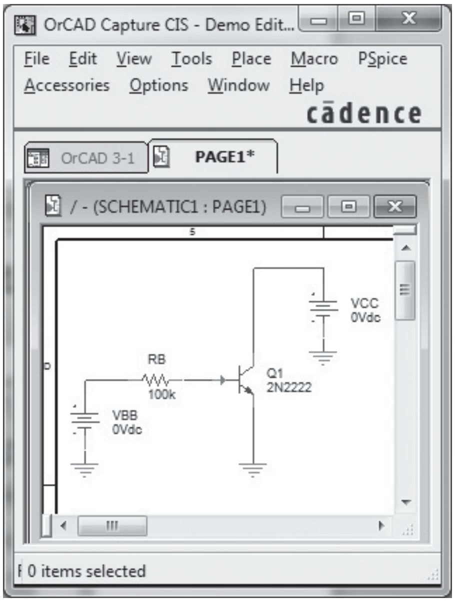
$$I_C = \beta I_B, \qquad I_E = (\beta + 1)I_B, \qquad P_{C_{\max}} = V_{CE} I_C$$

3.13 COMPUTER ANALYSIS

Cadence OrCAD

Since the transistor characteristics were introduced in this chapter, it seems appropriate that a procedure for obtaining those characteristics using PSpice Windows should be examined. The transistors are listed in the **EVAL** library and start with the letter **Q**. The library includes two *npn* transistors, two *pnp* transistors, and two Darlington configurations. The fact that there is a series of curves defined by the levels of I_B will require that a sweep of I_B values (a *nested sweep*) occur within a sweep of collector-to-emitter voltages. This is unnecessary for the diode, however, since only one curve would result.

First, the network in Fig. 3.34 is established using the same procedure as defined in Chapter 2. The voltage V_{CC} will establish our main sweep, whereas the voltage V_{BB} will determine the nested sweep. For future reference, note the panel at the top right of the menu bar with the scroll control when building networks. This option allows you to retrieve elements that have been used in the past. For instance, if you placed a resistor a few elements ago, simply return to the scroll bar and scroll until the resistor **R** appears. Click the location once, and the resistor will appear on the screen.


OrCAD Capture CIS - Demo Edit...
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OrCAD 3-1
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
VCC
0Vdc
RB
100k
Q1
2N2222
VBB
0Vdc
0 items selected

FIG. 3.34

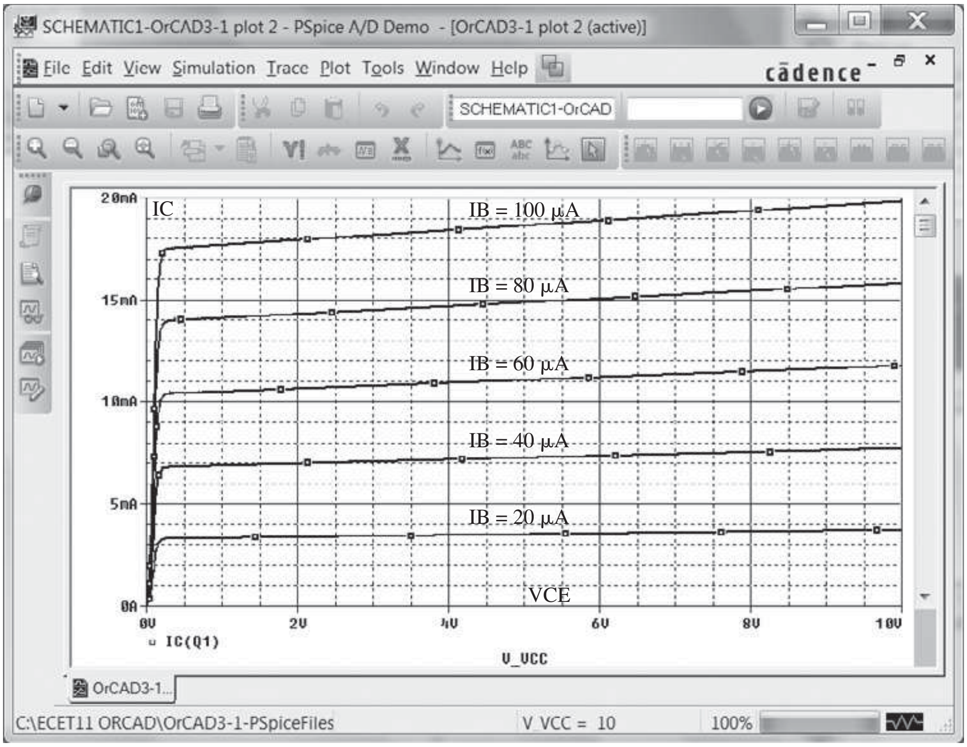
Network employed to obtain the collector characteristics of the Q2N2222 transistor.

Once the network is established as appearing in Fig. 3.34, select the **New Simulation Profile** key and insert **OrCAD 3-1** as the **Name**. Then select **Create** to obtain the **Simulation Settings** dialog box. The **Analysis type** will be **DC Sweep**, with the **Sweep variable** being a **Voltage Source**. Insert VCC as the name for the swept voltage source and select **Linear** for the sweep. The **Start value** is 0 V, the **End value** 10 V, and the **Increment** 0.01 V.

It is important not to select x in the top right corner of the box to leave the settings control. We must first enter the nested sweep variable by selecting **Secondary Sweep** and inserting VBB as the voltage source to be swept. Again, it will be a **Linear** sweep, but now the starting value will be 2.7 V to correspond with an initial current of 20 μA as determined by

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{2.7\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = 20\ \mu\text{A}$$

The **End value** is 10.7 V to correspond with a current of 100 μA. The **Increment** is set at 2 V, corresponding to a change in base current of 20 μA. Both sweeps are now set, but before leaving the dialog box **be sure both sweeps are enabled by a check in the box next to each sweep**. Often after entering the second sweep, the user fails to establish the second sweep before leaving the dialog box. Once both are selected, leave the dialog box and select **Run PSpice**. The result will be a graph with a voltage **VCC** varying from 0 V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File Edit View Simulation Trace Plot Tools Window Help
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SCHEMATIC1-OrCAD
20mA
15mA
10mA
5mA
0A
IC
IB = 100 μA
IB = 80 μA
IB = 60 μA
IB = 40 μA
IB = 20 μA
VCE
0V
2V
4V
6V
8V
10V
IC(Q1)
V_VCC
OrCAD3-1...
C:\ECET11 ORCAD\OrCAD3-1-PSpiceFiles
V_VCC = 10
100%

FIG. 3.35

Collector characteristics for the transistor of Fig. 3.34.

to 10 V. To establish the various *I* curves, apply the sequence **Trace-Add Trace** to obtain the **Add Trace** dialog box. Select **IC(Q1)**, the collector current of the transistor for the vertical axis. An **OK**, and the characteristics will appear. Unfortunately, however, they extend from −10 mA to +20 mA on the vertical axis. This can be corrected by the sequence **Plot-Axis Settings**, which again will result in the **Axis Settings** dialog box. Select **Y-Axis** and under **Data Range** choose **User Defined** and set the range as 0–20 mA. An **OK**, and the plot of Fig. 3.35 will appear. Labels on the plot can be added using the production version of OrCAD.

The first curve at the bottom of Fig. 3.35 represents $I_B = 20\ \mu\text{A}$. The curve above is $I_B = 40\ \mu\text{A}$, the next 60 μA, and so on. If we choose a point in the middle of the characteristics defined by $V_{CE} = 4$ V and $I_B = 60\ \mu\text{A}$ as shown in Fig. 3.35 β can be determined from

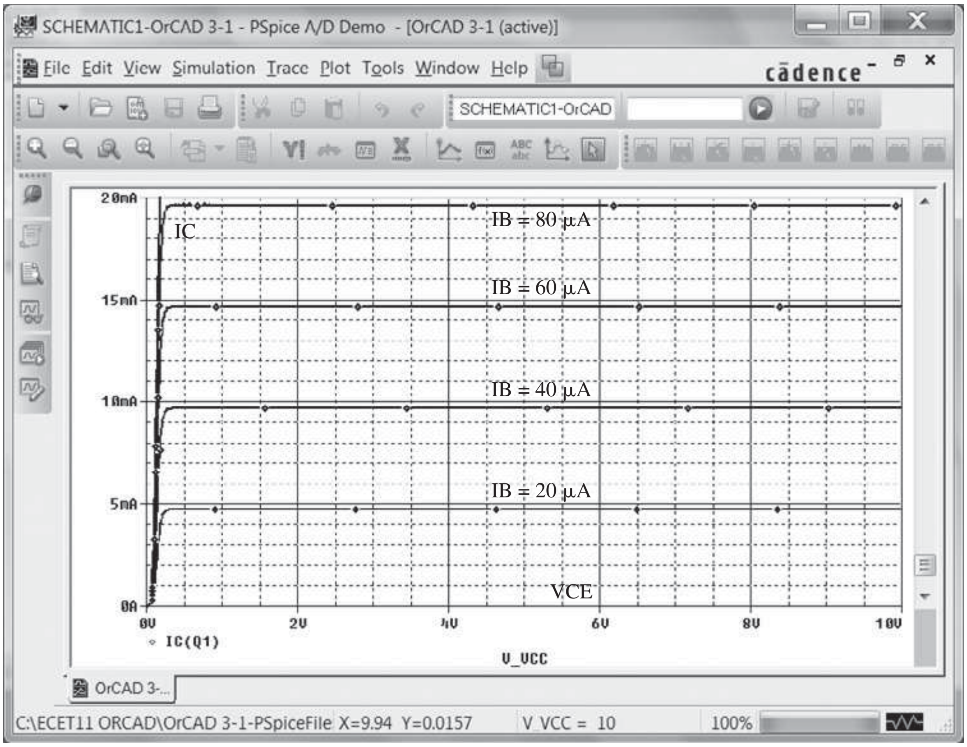
$$\beta = \frac{I_C}{I_B} = \frac{11\ \text{mA}}{60\ \mu\text{A}} = 183.3$$

Like the diode, the other parameters of the device will have a noticeable effect on the operating conditions. If we return to the transistor specifications using **Edit-PSpice Model** to obtain the **PSpice Model Editor Demo** dialog box, we can delete all the parameters except the Bf value. Be sure to leave the parentheses surrounding the value of Bf during the deletion process. When you exit the box the **Model Editor/16.3** dialog box will appear asking you to save changes. It was saved as **OrCAD 3-1** and the circuit was simulated again to obtain the characteristics of Fig. 3.36 following another adjustment of the range of the vertical axis.

Note first that the curves are all horizontal, meaning the element is void of any resistive characteristics. In addition, the equal spacing of the curves throughout reveals that beta is the same everywhere. At the intersection of $V_{CE} = 4$ V and $I_B = 60\ \mu\text{A}$, the new value of β is

$$\beta = \frac{I_C}{I_B} = \frac{14.6\ \text{mA}}{60\ \mu\text{A}} = 243.3$$

The real value of the above analysis is to recognize that even though beta may be provided, the actual performance of the device will be very dependent on its other parameters. Assume an ideal device is always a good starting point, but an actual network provides a different set of results.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File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
20mA
15mA
10mA
5mA
0A
IC
IB = 80 μA
IB = 60 μA
IB = 40 μA
IB = 20 μA
VCE
0V
2V
4V
6V
8V
10V
IC(Q1)
V_VCC
OrCAD 3-...
C:\ECET11 ORCAD\OrCAD 3-1-PSpiceFile X=9.94 Y=0.0157
V_VCC = 10
100%

FIG. 3.36

Ideal collector characteristics for the transistor of Fig. 3.34.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

3.2 Transistor Construction

1. What names are applied to the two types of BJT transistors? Sketch the basic construction of each and label the various minority and majority carriers in each. Draw the graphic symbol next to each. Is any of this information altered by changing from a silicon to a germanium base?
2. What is the major difference between a bipolar and a unipolar device?

3.3 Transistor Operation

3. How must the two transistor junctions be biased for proper transistor amplifier operation?
4. What is the source of the leakage current in a transistor?
5. Sketch a figure similar to Fig. 3.4a for the forward-biased junction of an *npn* transistor. Describe the resulting carrier motion.
6. Sketch a figure similar to Fig. 3.4b for the reverse-biased junction of an *npn* transistor. Describe the resulting carrier motion.
7. Sketch a figure similar to Fig. 3.5 for the majority- and minority-carrier flow of an *npn* transistor. Describe the resulting carrier motion.
8. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
9. If the emitter current of a transistor is 8 mA and I_B is $1/100$ of I_C, determine the levels of I_C and I_B.

3.4 Common-Base Configuration

10. From memory, sketch the transistor symbol for a *pnp* and an *npn* transistor, and then insert the conventional flow direction for each current.
11. Using the characteristics of Fig. 3.7, determine V_{BE} at $I_E = 5$ mA for $V_{CB} = 1$, 10, and 20 V. Is it reasonable to assume on an approximate basis that V_{CB} has only a slight effect on the relationship between V_{BE} and I_E?

12. **a.** Determine the average ac resistance for the characteristics of Fig. 3.10b.
b. For networks in which the magnitude of the resistive elements is typically in kilohms, is the approximation of Fig. 3.10c a valid one [based on the results of part (a)]?

13. **a.** Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3.5$ mA and $V_{CB} = 10$ V.
b. Repeat part (a) for $I_E = 3.5$ mA and $V_{CB} = 20$ V.
c. How have the changes in V_{CB} affected the resulting level of I_C?
d. On an approximate basis, how are I_E and I_C related based on the results above?

14. **a.** Using the characteristics of Figs. 3.7 and 3.8, determine I_C if $V_{CB} = 5$ V and $V_{BE} = 0.7$ V.
b. Determine V_{BE} if $I_C = 5$ mA and $V_{CB} = 15$ V.
c. Repeat part (b) using the characteristics of Fig. 3.10b.
d. Repeat part (b) using the characteristics of Fig. 3.10c.
e. Compare the solutions for V_{BE} for parts (b) through (d). Can the difference be ignored if voltage levels greater than a few volts are typically encountered?

15. **a.** Given an α_{dc} of 0.998, determine I_C if $I_E = 4$ mA.
b. Determine α_{dc} if $I_E = 2.8$ mA, $I_C = 2.75$ mA and $I_{CBO} = 0.1\ \mu$A.

16. From memory only, sketch the common-base BJT transistor configuration (for *npn* and *pnp*) and indicate the polarity of the applied bias and resulting current directions.

3.5 Common-Emitter Configuration

17. Define I_{CBO} and I_{CEO}. How are they different? How are they related? Are they typically close in magnitude?

18. Using the characteristics of Fig. 3.13:
a. Find the value of I_C corresponding to $V_{BE} = +750$ mV and $V_{CE} = +4$ V.
b. Find the value of V_{CE} and V_{BE} corresponding to $I_C = 3.5$ mA and $I_B = 30\ \mu$A.

***19.** **a.** For the common-emitter characteristics of Fig. 3.13, find the dc beta at an operating point of $V_{CE} = 6$ V and $I_C = 2$ mA.
b. Find the value of α corresponding to this operating point.
c. At $V_{CE} = +6$ V, find the corresponding value of I_{CEO}.
d. Calculate the approximate value of I_{CBO} using the dc beta value obtained in part (a).

***20.** **a.** Using the characteristics of Fig. 3.13a, determine I_{CEO} at $V_{CE} = 10$ V.
b. Determine β_{dc} at $I_B = 10\ \mu$A and $V_{CE} = 10$ V.
c. Using the β_{dc} determined in part (b), calculate I_{CBO}.

21. **a.** Using the characteristics of Fig. 3.13a, determine β_{dc} at $I_B = 60\ \mu$A and $V_{CE} = 4$ V.
b. Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 7$ V.
c. Repeat part (a) at $I_B = 10\ \mu$A and $V_{CE} = 10$ V.
d. Reviewing the results of parts (a) through (c), does the value of β_{dc} change from point to point on the characteristics? Where were the higher values found? Can you develop any general conclusions about the value of β_{dc} on a set of characteristics such as those provided in Fig. 3.13a?

***22.** **a.** Using the characteristics of Fig. 3.13a, determine β_{ac} at $I_B = 60\ \mu$A and $V_{CE} = 4$ V.
b. Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 7$ V.
c. Repeat part (a) at $I_B = 10\ \mu$A and $V_{CE} = 10$ V.
d. Reviewing the results of parts (a) through (c), does the value of β_{ac} change from point to point on the characteristics? Where are the high values located? Can you develop any general conclusions about the value of β_{ac} on a set of collector characteristics?
e. The chosen points in this exercise are the same as those employed in Problem 21. If Problem 21 was performed, compare the levels of β_{dc} and β_{ac} for each point and comment on the trend in magnitude for each quantity.

23. Using the characteristics of Fig. 3.13a, determine β_{dc} at $I_B = 25\ \mu$A and $V_{CE} = 10$ V. Then calculate α_{dc} and the resulting level of I_E. (Use the level of I_C determined by $I_C = \beta_{dc} I_B$.)

24. **a.** Given that $\alpha_{dc} = 0.980$, determine the corresponding value of β_{dc}.
b. Given $\beta_{dc} = 120$, determine the corresponding value of α.
c. Given that $\beta_{dc} = 120$ and $I_C = 2.0$ mA, find I_E and I_B.

25. From memory only, sketch the common-emitter configuration (for *npn* and *pnp*) and insert the proper biasing arrangement with the resulting current directions for I_B, I_C, and I_E.

3.6 Common-Collector Configuration

26. An input voltage of 2 V rms (measured from base to ground) is applied to the circuit of Fig. 3.21. Assuming that the emitter voltage follows the base voltage exactly and that V_{be} (rms) $= 0.1$ V, calculate the circuit voltage amplification ($A_v = V_o/V_i$) and emitter current for $R_E = 1\ \text{k}\Omega$.

27. For a transistor having the characteristics of Fig. 3.13, sketch the input and output characteristics of the common-collector configuration.

3.7 Limits of Operation

28. Determine the region of operation for a transistor having the characteristics of Fig. 3.13 if $I_{C_{\max}} = 6$ mA, $BV_{CEO} = 15$ V, and $P_{C_{\max}} = 35$ mW.

29. Determine the region of operation for a transistor having the characteristics of Fig. 3.8 if $I_{C_{\max}} = 7$ mA, $BV_{CBO} = 20$ V, and $P_{C_{\max}} = 42$ mW.

3.8 Transistor Specification Sheet

30. Referring to Fig. 3.23, determine the temperature range for the device in degrees Fahrenheit.

31. Using the information provided in Fig. 3.23 regarding $P_{D_{\max}}$, $V_{CE_{\max}}$, $I_{C_{\max}}$ and $V_{CE_{\text{sat}}}$, sketch the boundaries of operation for the device.

32. Based on the data of Fig. 3.23, what is the expected value of I_{CEO} using the average value of β_{dc}?

33. How does the range of h_{FE} (Fig. 3.23c, normalized from $h_{FE} = 100$) compare with the range of h_{fe} (Fig. 3.23b) for the range of I_C from 0.1 to 10 mA?

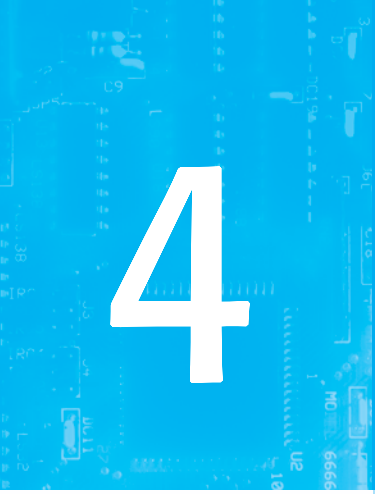
34. Using the characteristics of Fig. 3.23d, determine whether the input capacitance in the common-base configuration increases or decreases with increasing levels of reverse-bias potential. Can you explain why?

***35.** Using the characteristics of Fig. 3.23b, determine how much the level of h_{fe} has changed from its value at 1 mA to its value at 10 mA. Note that the vertical scale is a log scale that may require reference to Section 11.2. Is the change one that should be considered in a design situation?

***36.** Using the characteristics of Fig. 3.23c, determine the level of β_{dc} at $I_C = 10$ mA at the three levels of temperature appearing in the figure. Is the change significant for the specified temperature range? Is it an element to be concerned about in the design process?

3.9 Transistor Testing

37. **a.** Using the characteristics of Fig. 3.24, determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
b. Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
c. Determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
d. Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
e. How does the level of β_{ac} and β_{dc} compare in each region?
f. Is the approximation $\beta_{\text{dc}} \cong \beta_{\text{ac}}$ a valid one for this set of characteristics?



4

DC Biasing—BJTs

CHAPTER OBJECTIVES

- Be able to determine the dc levels for the variety of important BJT configurations.
- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.
- Be able to perform a load-line analysis of the most common BJT configurations.
- Become acquainted with the design process for BJT amplifiers.
- Understand the basic operation of transistor switching networks.
- Begin to understand the troubleshooting process as applied to BJT configurations.
- Develop a sense for the stability factors of a BJT configuration and how they affect its operation due to changes in specific characteristics and environmental changes.

4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion. Fortunately, the superposition theorem is applicable, and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the bipolar junction transistor (BJT) amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity in the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$\boxed{V_{BE} \cong 0.7\text{ V}} \tag{4.1}$$

$$\boxed{I_E = (\beta + 1)I_B \cong I_C} \tag{4.2}$$

$$\boxed{I_C = \beta I_B} \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The

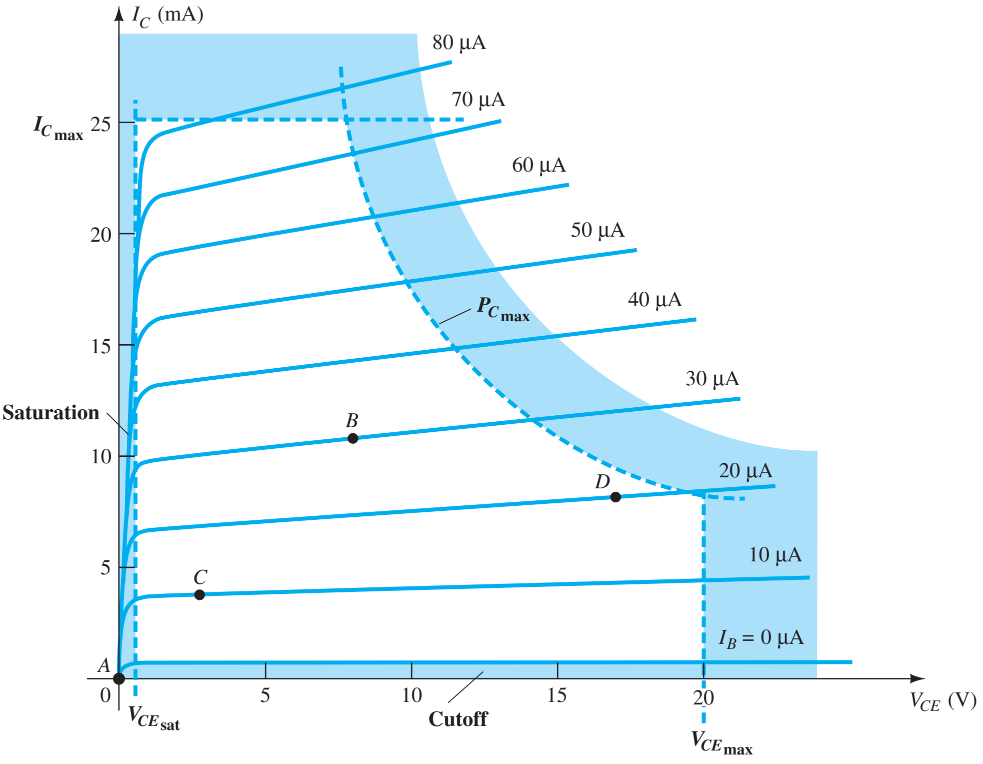


FIG. 4.1

Various operating points within the limits of operation of a transistor.

biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{\max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{\max}}$. The maximum power constraint is defined by the curve $P_{C_{\max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\ \mu\text{A}$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{\text{sat}}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, we can select many different operating areas or points. The chosen Q-point often depends on the intended use of the circuit. Still, we can consider some differences among the various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a Q-point at A—namely, zero current through the device (and zero voltage across it). Because it is necessary to bias a device so that it can respond to the entire range of an input signal, point A would not be suitable. For point B, if a signal is applied to the circuit, the device will vary in current and voltage from the operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary, but not enough to drive the device into *cutoff* or *saturation.* Point C would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0$ V and $I_C = 0$ mA. Operating at point C also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point B is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point D sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point B therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 5) but not the case necessarily for power amplifiers, which will be considered in Chapter 12. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, we must also take the effect of temperature into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor S,* which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. ***The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.***
2. ***The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.***

[Note that for forward bias the voltage across the *p–n* junction is *p*-positive, whereas for reverse bias it is opposite (reverse) with *n*-positive.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction reverse-biased

2. *Cutoff-region operation:*
   Base–emitter junction reverse-biased
   Base–collector junction reverse-biased
3. *Saturation-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the *actual* current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency. For dc, $f = 0$ Hz, and $X_C = 1/2\pi fC = 1/2\pi(0)C = \infty\,\Omega$. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

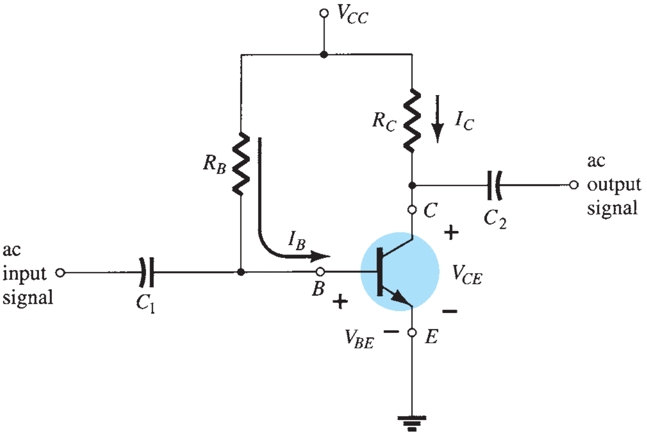


FIG. 4.2
Fixed-bias circuit.

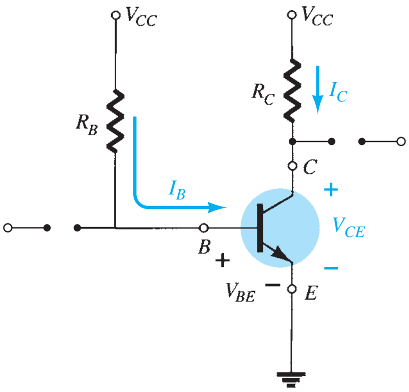


FIG. 4.3
DC equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B results in the following:

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \qquad \textbf{(4.4)}$$

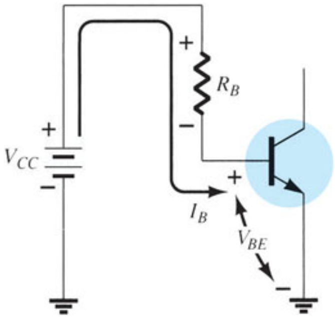


FIG. 4.4
Base–emitter loop.

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}). In addition, because the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

Collector–Emitter Loop

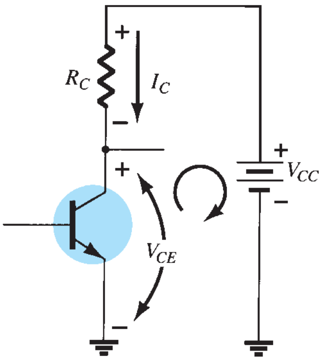


FIG. 4.5
Collector–emitter loop.

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$\boxed{I_C = \beta I_B} \tag{4.5}$$

It is interesting to note that because the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{4.6}$$

which states that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$\boxed{V_{CE} = V_C - V_E} \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case,* since $V_E = 0$ V, we have

$$\boxed{V_{CE} = V_C} \tag{4.8}$$

In addition, because

$$\boxed{V_{BE} = V_B - V_E} \tag{4.9}$$

and $V_E = 0$ V, then

$$\boxed{V_{BE} = V_B} \tag{4.10}$$

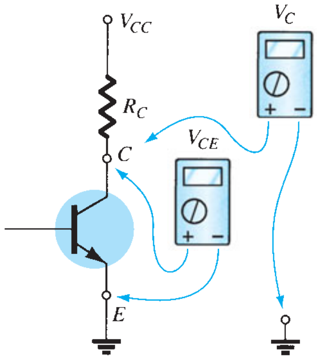


FIG. 4.6
Measuring V_{CE} and V_C.

Keep in mind that voltage levels such as V_{CE} are determined by placing the positive lead (normally red) of the voltmeter at the collector terminal with the negative lead (normally black) at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

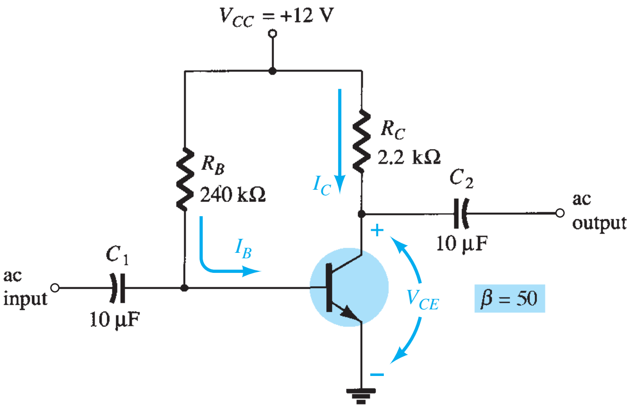


FIG. 4.7

DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6):
$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_CR_C \\ &= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega) \\ &= \mathbf{6.83\ V} \end{aligned}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

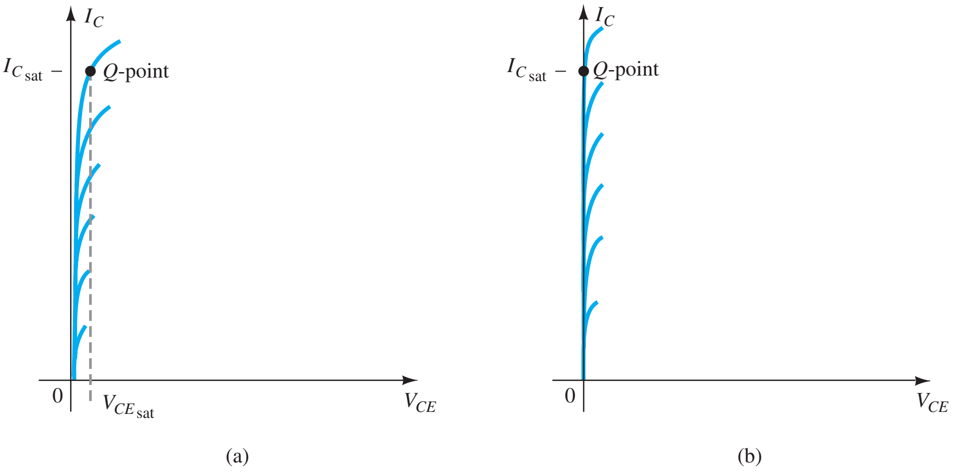
d. Using double-subscript notation yields
$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7\text{ V} - 6.83\text{ V} \\ &= \mathbf{-6.13\ V} \end{aligned}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of water. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.



(a) (b)

FIG. 4.8

Saturation regions: (a) actual; (b) approximate.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high, and the voltage V_{CE} is assumed to be 0 V. Applying Ohm's law, we can determine the resistance between collector and emitter terminals as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{\text{sat}}}} = 0\ \Omega$$

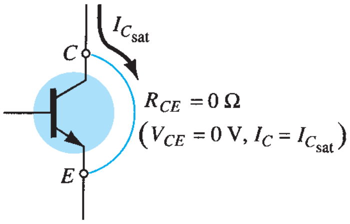


FIG. 4.9
Determining $I_{C_{\text{sat}}}$.

Applying the results to the network schematic results in the configuration of Fig. 4.9.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

$$\boxed{I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}} \qquad (4.11)$$

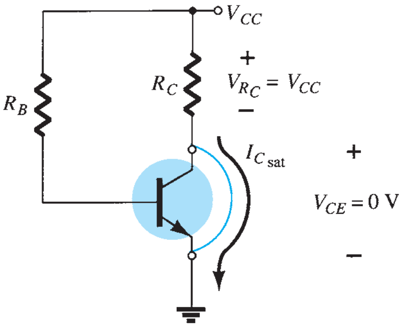


FIG. 4.10
Determining $I_{C_{\text{sat}}}$ for the fixed-bias configuration.

Once $I_{C_{\text{sat}}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\ mA}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

Recall that the load-line solution for a diode network was found by superimposing the actual diode characteristics of the diode on a plot of the network equation involving the same network variables. The intersection of the two plots defined the actual operating conditions for the network. It is referred to as load-line analysis because the load (network resistors) of the network defined the slope of the straight line connecting the points defined by the network parameters.

The same approach can be applied to BJT networks. The characteristics of the BJT are superimposed on a plot of the network equation defined by the same axis parameters. The load resistor R_C for the fixed-bias configuration will define the slope of the network equation and the resulting intersection between the two plots. The smaller the load resistance, the

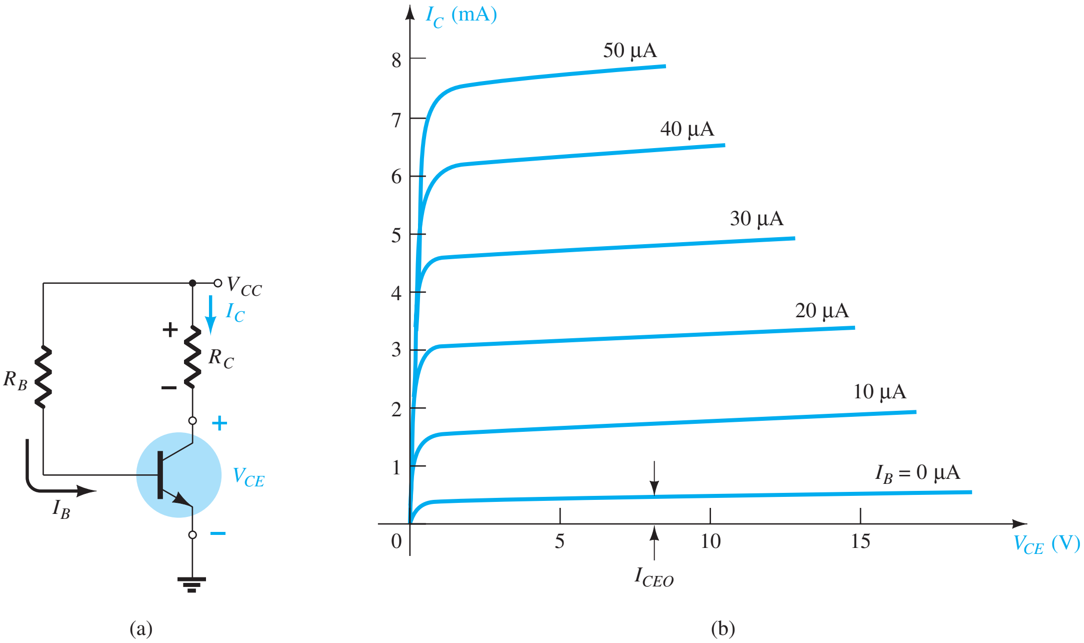


FIG. 4.11

Load-line analysis: (a) the network; (b) the device characteristics.

steeper the slope of the network load line. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$\boxed{V_{CE} = V_{CC}\big|_{I_C = 0\text{ mA}}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

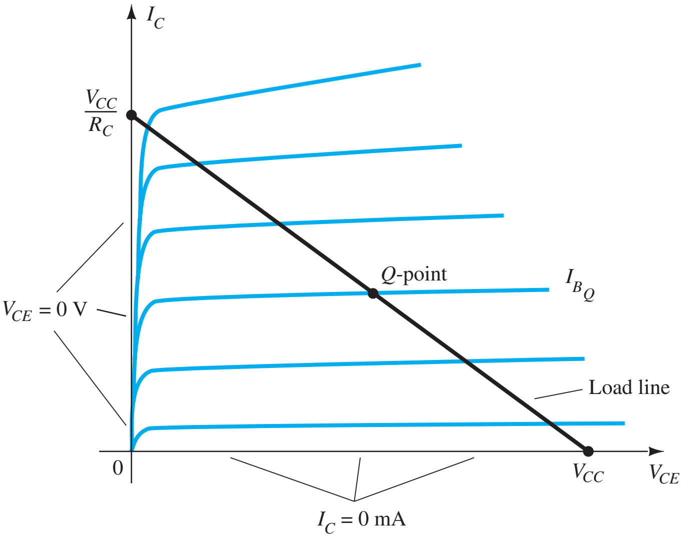


FIG. 4.12

Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\text{ V}}} \qquad \textbf{(4.14)}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), we can draw the straight line established by Eq. (4.12). The resulting line on the graph of Fig. 4.12 is called the *load line* because it is defined by the load resistor R_C. By solving for the resulting level of I_B, we can establish the actual Q-point as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B, the Q-point moves up or down the load line as shown in Fig. 4.13 for increasing values of I_B. If V_{CC} is held fixed and R_C increased, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} decreased, the load line shifts as shown in Fig. 4.15.

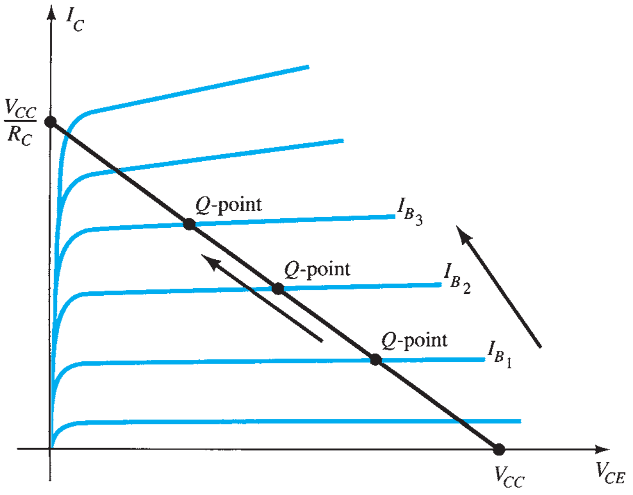


FIG. 4.13
Movement of the Q-point with increasing level of I_B.

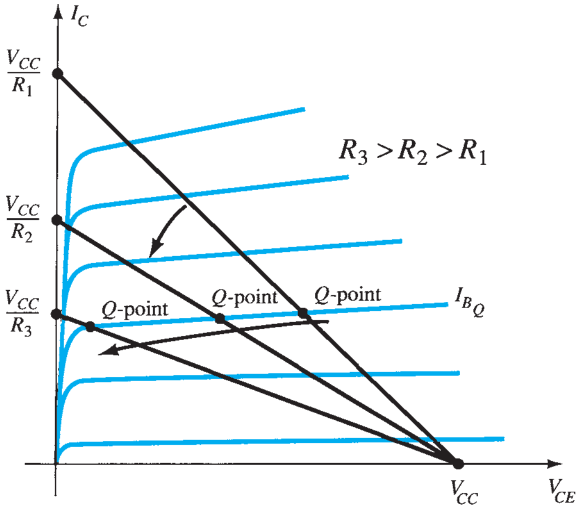


FIG. 4.14
Effect of an increasing level of R_C on the load line and the Q-point.

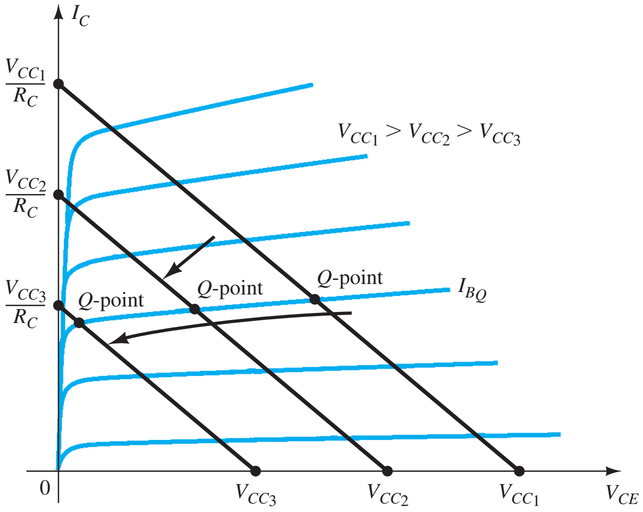


FIG. 4.15
Effect of lower values of V_{CC} on the load line and the Q-point.

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

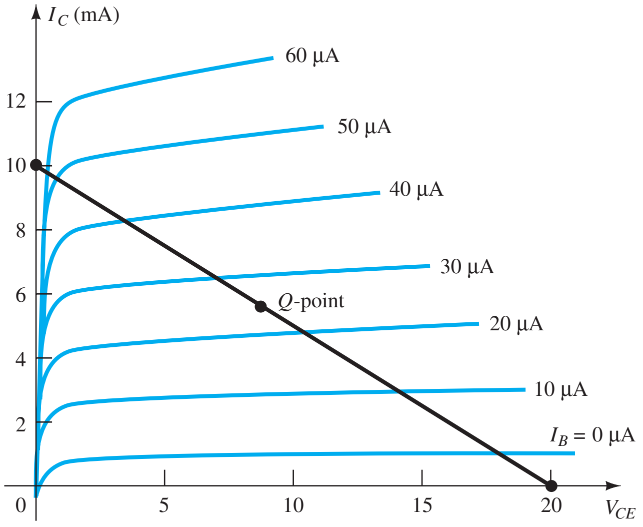


FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-BIAS CONFIGURATION

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The more stable a configuration, the less its response will change due to undesireable changes in temperature and parameter

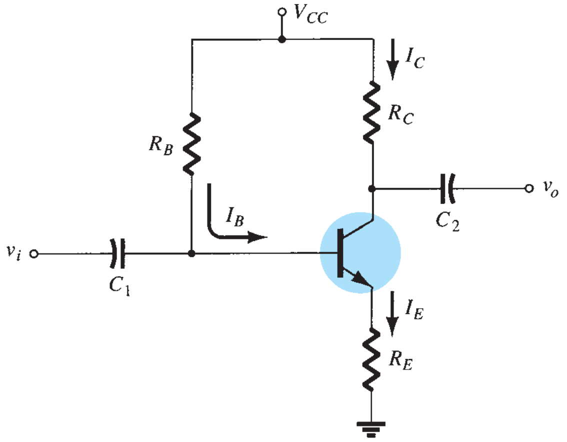


FIG. 4.17
BJT bias circuit with emitter resistor.

variations. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop. The dc equivalent of Fig. 4.17 appears in Fig 4.18 with a separation of the source to create an input and output section.

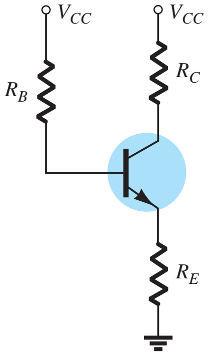


FIG. 4.18
DC equivalent of Fig. 4.17.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.18 can be redrawn as shown in Fig. 4.19. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_BR_B - V_{BE} - I_ER_E = 0 \tag{4.15}$$

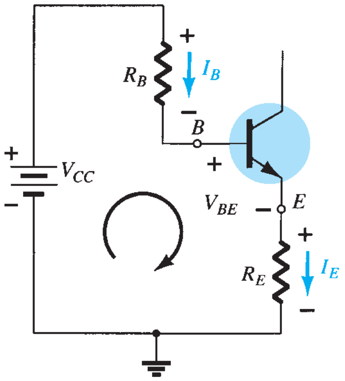


FIG. 4.19
Base–emitter loop.

Recall from Chapter 3 that

$$I_E = (\beta + 1)I_B \tag{4.16}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_BR_B - V_{BE} - (\beta + I)I_BR_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (−1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{4.17}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of Fig. 4.20. Solving for the current I_B results in the same equation as obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base–emitter loop. Because β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.21,

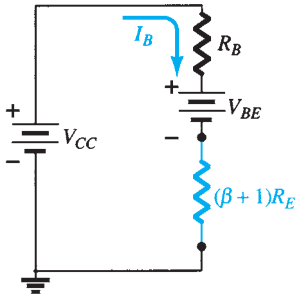


FIG. 4.20
Network derived from Eq. (4.17).

$$\boxed{R_i = (\beta + 1)R_E} \tag{4.18}$$

Equation (4.18) will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base–emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

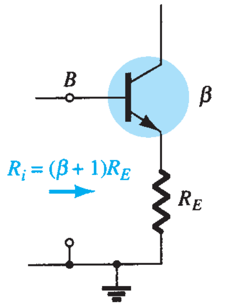


FIG. 4.21
Reflected impedance level of R_E.

Collector–Emitter Loop

The collector–emitter loop appears in Fig. 4.22. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_ER_E + V_{CE} + I_CR_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.19}$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$\boxed{V_E = I_E R_E} \tag{4.20}$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$\boxed{V_C = V_{CE} + V_E} \tag{4.21}$$

or

$$\boxed{V_C = V_{CC} - I_C R_C} \tag{4.22}$$

The voltage at the base with respect to ground can be determined using Fig. 4.18

$$\boxed{V_B = V_{CC} - I_B R_B} \tag{4.23}$$

or

$$\boxed{V_B = V_{BE} + V_E} \tag{4.24}$$

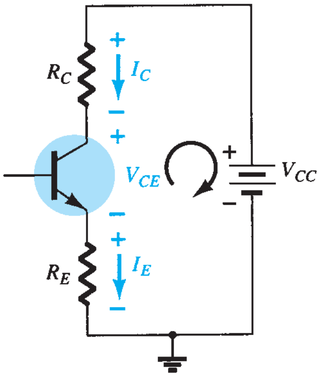


FIG. 4.22
Collector–emitter loop.

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

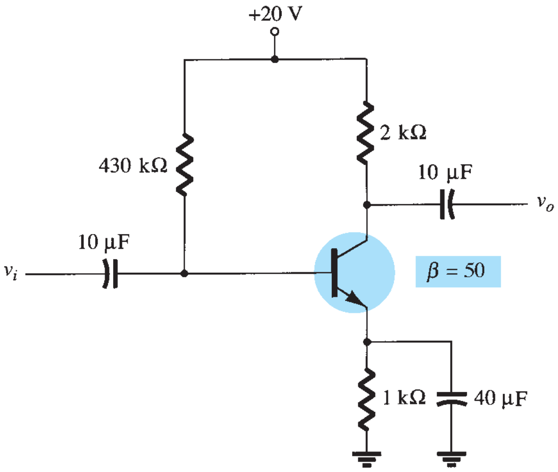


FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17):
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b.
$$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

c. Eq. (4.19):
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\text{ V}}$$

d.
$$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\text{ V}}$$

e.
$$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\text{ V}}$$

or
$$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\text{ V}}$$

f.
$$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\text{ V}}$$

g.
$$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\text{ V}}\text{ (reverse-biased as required)}$$

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change. Although a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5 Prepare a table and compare the bias voltage and currents of the circuits of Fig. 4.7 and Fig. 4.23 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution: Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

Effect of β variation on the response of the fixed-bias configuration of Fig. 4.7.

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. The value of I_B is the same, and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

Effect of β variation on the response of the emitter-bias configuration of Fig. 4.23.

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C—or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.23 is therefore more stable than that of Fig. 4.7 for the same change in β.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.24 and calculate the resulting collector current. For Fig. 4.24

$$\boxed{I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E}} \tag{4.25}$$

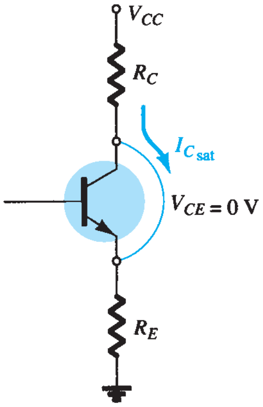


FIG. 4.24

Determining $I_{C_{\text{sat}}}$ for the emitter-stabilized bias circuit.

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

EXAMPLE 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$\begin{aligned} I_{C_{\text{sat}}} &= \frac{V_{CC}}{R_C + R_E} \\ &= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega} \\ &= \mathbf{6.67\ mA} \end{aligned}$$

which is about three times the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.25 (denoted I_{B_Q}).

The collector–emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

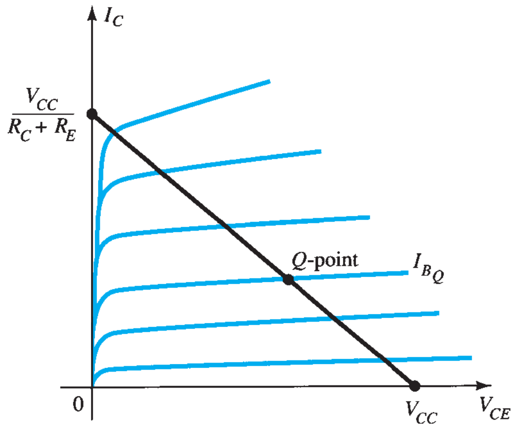


FIG. 4.25

Load line for the emitter-bias configuration.

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C = 0\text{ mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\text{ V}}} \tag{4.27}$$

as shown in Fig. 4.25. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.

EXAMPLE 4.7

a. Draw the load line for the network of Fig. 4.26a on the characteristics for the transistor appearing in Fig. 4.26b.
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

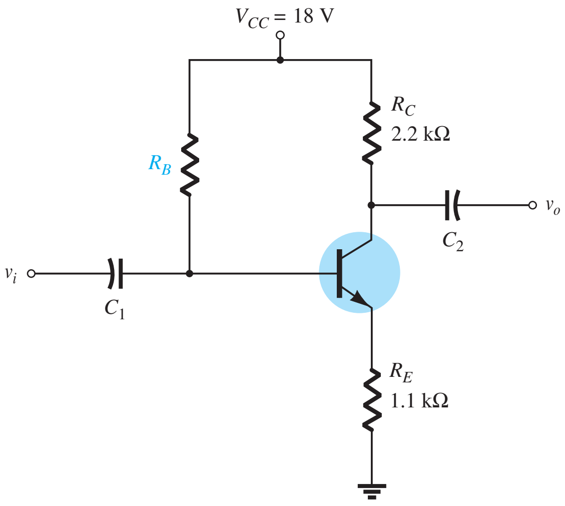


FIG. 4.26a
Network for Example 4.7.

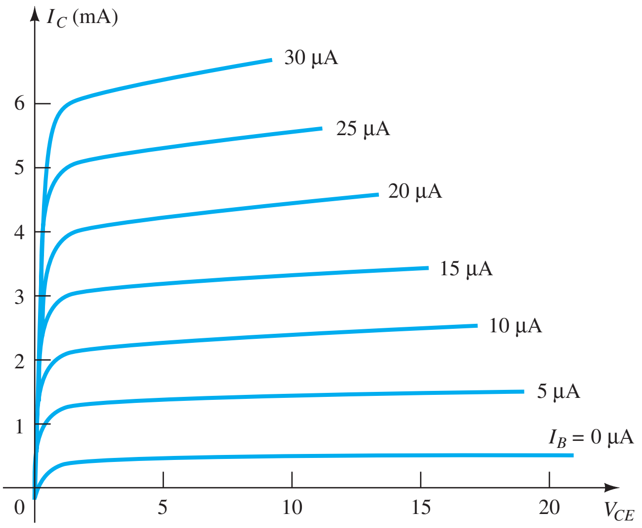


FIG. 4.26b
Example 4.7.

Solution:

a. Two points on the characteristics are required to draw the load line.

At $V_{CE} = 0$ V: $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{18\text{ V}}{2.2\text{ k}\Omega + 1.1\text{ k}\Omega} = \dfrac{18\text{ V}}{3.3\text{ k}\Omega} = 5.45\text{ mA}$

At $I_C = 0$ mA: $V_{CE} = V_{CC} = 18$ V

The resulting load line appears in Fig. 4.27.

b. From the characteristics of Fig. 4.27 we find

$V_{CE_Q} \cong \mathbf{7.5\ V}, I_{C_Q} \cong \mathbf{3.3\ mA}$

c. The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3\text{ mA}}{15\ \mu\text{A}} = \mathbf{220}$$

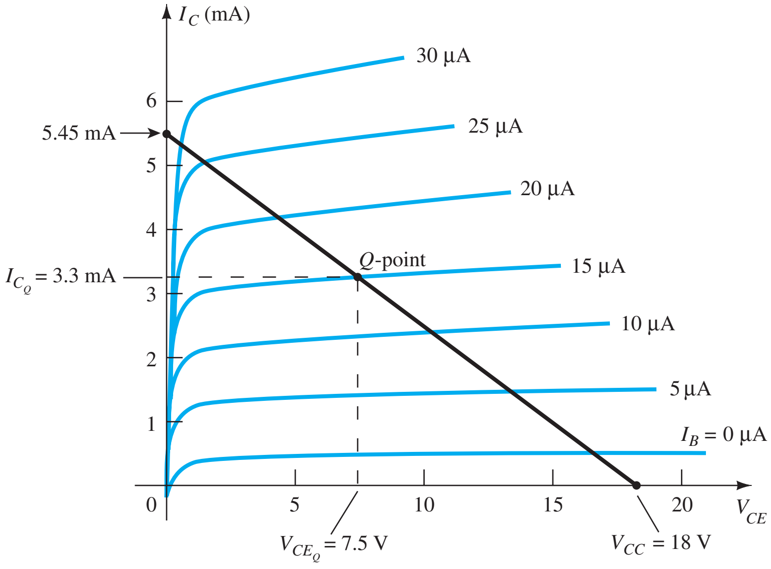


FIG. 4.27

Example 4.7.

d. Applying Eq. 4.17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18\text{ V} - 0.7\text{ V}}{R_B + (220 + 1)(1.1\text{ k}\Omega)}$$

$$\text{and } 15\ \mu\text{A} = \frac{17.3\text{ V}}{R_B + (221)(1.1\text{ k}\Omega)} = \frac{17.3\text{ V}}{R_B + 243.1\text{ k}\Omega}$$

$$\text{so that } (15\ \mu\text{A})(R_B) + (15\ \mu\text{A})(243.1\text{ k}\Omega) = 17.3\text{ V}$$

$$\text{and } (15\ \mu\text{A})(R_B) = 17.3\text{ V} - 3.65\text{ V} = 13.65\text{ V}$$

$$\text{resulting in } R_B + \frac{13.65\text{ V}}{15\ \mu\text{A}} = \mathbf{910\text{ k}\Omega}$$

4.5 VOLTAGE-DIVIDER BIAS CONFIGURATION

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.28 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.29. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted earlier, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

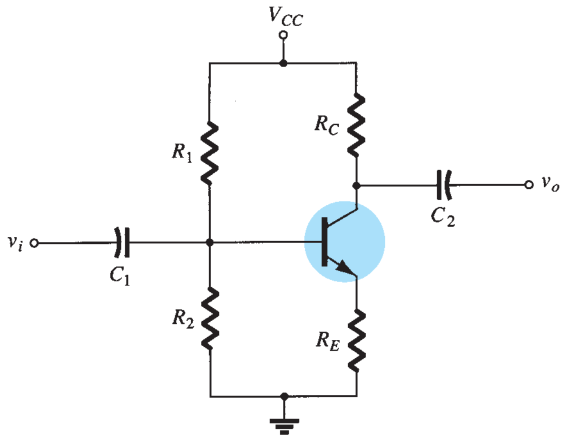


FIG. 4.28
Voltage-divider bias configuration.

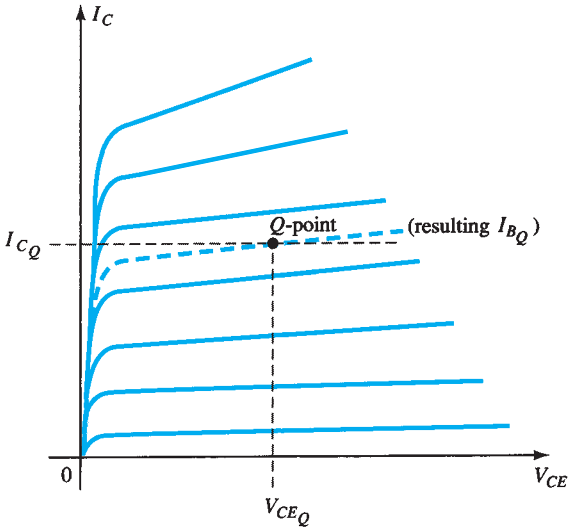


FIG. 4.29
Defining the Q-point for the voltage-divider bias configuration.

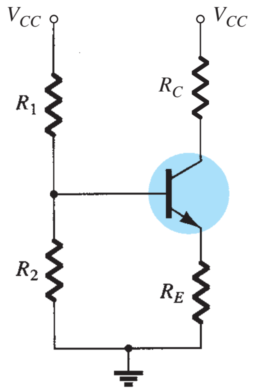


FIG. 4.30
DC components of the voltage-divider configuration.

Exact Analysis

For the dc analysis the network of Fig. 4.28 can be redrawn as shown in Fig. 4.30. The input side of the network can then be redrawn as shown in Fig. 4.31 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

R_{Th} The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.32:

$$\boxed{R_{Th} = R_1 \| R_2} \tag{4.28}$$

E_{Th} The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.33 determined as follows:

Applying the voltage-divider rule gives

$$\boxed{E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}} \tag{4.29}$$

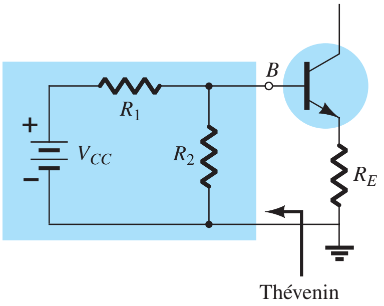


FIG. 4.31
Redrawing the input side of the network of Fig. 4.28.

The Thévenin network is then redrawn as shown in Fig. 4.34, and I_{B_Q} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$\boxed{I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}} \tag{4.30}$$

Although Eq. (4.30) initially appears to be different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.31}$$

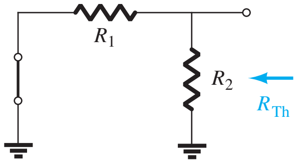


FIG. 4.32
Determining R_{Th}.

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

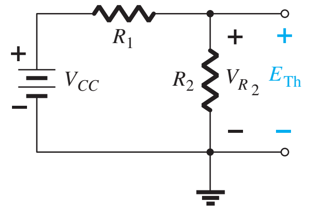


FIG. 4.33
Determining E_{Th}.

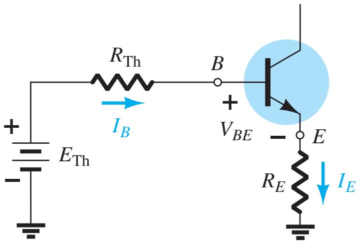


FIG. 4.34
Inserting the Thévenin equivalent circuit.

EXAMPLE 4.8 Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.35.

Solution: Eq. (4.28): $R_{Th} = R_1 \| R_2$

$$= \frac{(39\text{ k}\Omega)(3.9\text{ k}\Omega)}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 3.55\text{ k}\Omega$$

Eq. (4.29): $$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\text{ k}\Omega)(22\text{ V})}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 2\text{ V}$$

Eq. (4.30): $$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (101)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 151.5\text{ k}\Omega}$$

$$= 8.38\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (100)(8.38\ \mu\text{A})$$

$$= \mathbf{0.84\ mA}$$

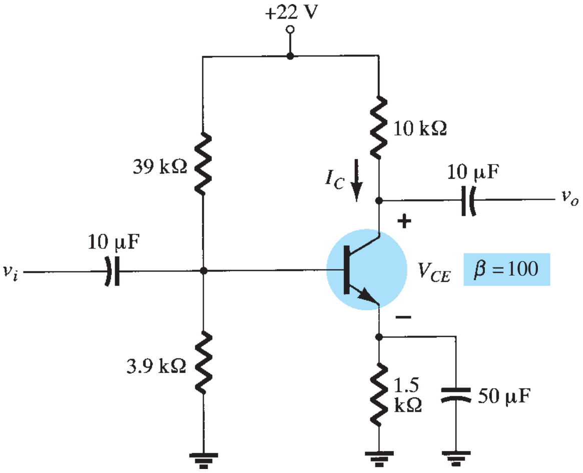


FIG. 4.35
Beta-stabilized circuit for Example 4.8.

Eq. (4.31): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\text{ V} - (0.84\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega)$$

$$= 22\text{ V} - 9.66\text{ V}$$

$$= \mathbf{12.34\ V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.36. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially 0 A compared to I_1 or I_2, then $I_1 = I_2$, and R_1 and R_2 can be considered series elements. The voltage across R_2, which is actually the base voltage, can be

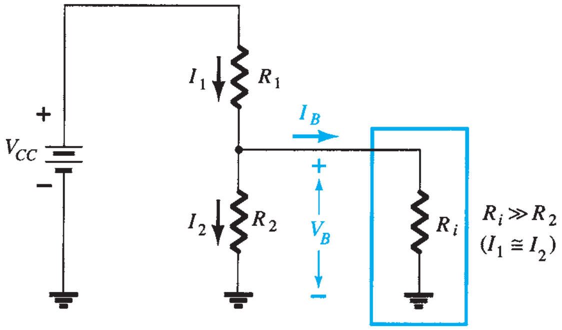


FIG. 4.36

Partial-bias circuit for calculating the approximate base voltage V_B.

determined using the voltage-divider rule (hence the name for the configuration). That is,

$$\boxed{V_B = \frac{R_2 V_{CC}}{R_1 + R_2}} \tag{4.32}$$

Because $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied is

$$\boxed{\beta R_E \geq 10R_2} \tag{4.33}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$\boxed{V_E = V_B - V_{BE}} \tag{4.34}$$

and the emitter current can be determined from

$$\boxed{I_E = \frac{V_E}{R_E}} \tag{4.35}$$

and

$$\boxed{I_{C_Q} \cong I_E} \tag{4.36}$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because $I_E \cong I_C$,

$$\boxed{V_{CE_Q} = V_{CC} - I_C(R_C + R_E)} \tag{4.37}$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The *Q*-point (as determined by I_{C_Q} and V_{CE_Q}) is therefore independent of the value of β.

EXAMPLE 4.9 Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: Testing:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\text{ k}\Omega) \geq 10(3.9\text{ k}\Omega)$$
$$150\text{ k}\Omega \geq 39\text{ k}\Omega\ (\textit{satisfied})$$

$$\text{Eq. (4.32):}\quad V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\text{ k}\Omega)(22\text{ V})}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 2\text{ V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\text{Eq. (4.34):}\quad V_E = V_B - V_{BE} = 2\text{ V} - 0.7\text{ V} = 1.3\text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.5\text{ k}\Omega} = \mathbf{0.867\text{ mA}}$$

compared to 0.84 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\text{ V} - (0.867\text{ mA})(10\text{ kV} + 1.5\text{ k}\Omega) = 22\text{ V} - 9.97\text{ V} = \mathbf{12.03\text{ V}}$$

versus 12.34 V obtained in Example 4.8.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer is the approximate to the exact solution. Example 4.11 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.10 Repeat the exact analysis of Example 4.8 if β is reduced to 50, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: This example is not a comparison of exact versus approximate methods, but a testing of how much the Q-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{\mathrm{Th}} = 3.55\text{ k}\Omega, \qquad E_{\mathrm{Th}} = 2\text{ V}$$

$$I_B = \frac{E_{\mathrm{Th}} - V_{BE}}{R_{\mathrm{Th}} + (\beta + 1)R_E} = \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (51)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 76.5\text{ k}\Omega} = 16.24\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(16.24\ \mu\text{A}) = \mathbf{0.81\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\text{ V} - (0.81\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega) = \mathbf{12.69\text{ V}}$$

Tabulating the results, we have:

Effect of β variation on the response of the voltage-divider configuration of Fig. 4.35.

β	I_{C_Q} (mA)	V_{CE_Q} (V)
100	0.84 mA	12.34 V
50	0.81 mA	12.69 V

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 100 to 50, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.

Important Note: Looking back on the results for the fixed-bias configuration, we find the current decreased from 4.71 mA to 2.35 mA when beta dropped from 100 to 50. For the voltage-divider configuration, the same change in beta only resulted in a change in current from 0.84 mA to 0.81 mA. Even more noticeable is the change in V_{CE_Q} for the fixed-bias configuration. Dropping beta from 100 to 50 resulted in an increase in voltage from 1.64 to 6.83 V (a change of over 300%). For the voltage-divider configuration, the increase in voltage was only from 12.34 V to 12.69 V, which is a change of less than 3%. In summary, therefore, changing beta by 50% resulted in a change in an important network parameter of over 300% for the fixed-bias configuration and less than 3% for the voltage-divider configuration—a significant difference.

EXAMPLE 4.11 Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) *will not be satisfied* and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

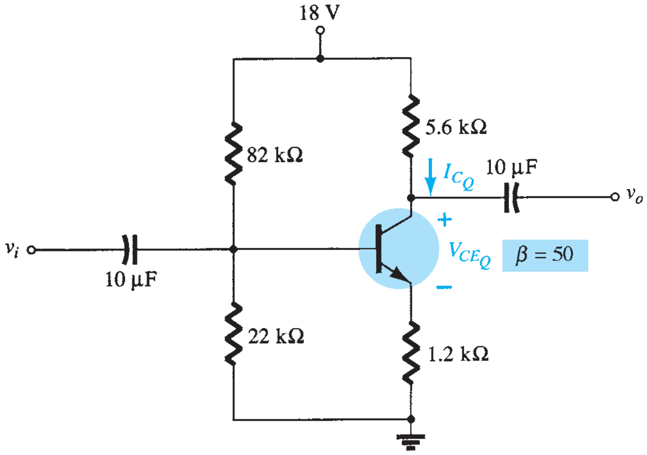


FIG. 4.37
Voltage-divider configuration for Example 4.11.

Solution: Exact analysis:

Eq. (4.33):

$$\beta R_E \geq 10R_2$$
$$(50)(1.2\text{ k}\Omega) \geq 10(22\text{ k}\Omega)$$
$$60\text{ k}\Omega \ngeq 220\text{ k}\Omega\ (\textit{not satisfied})$$
$$R_{\text{Th}} = R_1 \| R_2 = 82\text{ k}\Omega \| 22\text{ k}\Omega = 17.35\text{ k}\Omega$$
$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\text{ k}\Omega(18\text{ V})}{82\text{ k}\Omega + 22\text{ k}\Omega} = 3.81\text{ V}$$
$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\text{ V} - 0.7\text{ V}}{17.35\text{ k}\Omega + (51)(1.2\text{ k}\Omega)} = \frac{3.11\text{ V}}{78.55\text{ k}\Omega} = 39.6\ \mu\text{A}$$
$$I_{C_Q} = \beta I_B = (50)(39.6\ \mu\text{A}) = \mathbf{1.98\ mA}$$
$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 18\text{ V} - (1.98\text{ mA})(5.6\text{ k}\Omega + 1.2\text{ k}\Omega) \\ &= \mathbf{4.54\ V} \end{aligned}$$

Approximate analysis:

$$V_B = E_{\text{Th}} = 3.81\text{ V}$$
$$V_E = V_B - V_{BE} = 3.81\text{ V} - 0.7\text{ V} = 3.11\text{ V}$$
$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.59\ mA}$$
$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 18\text{ V} - (2.59\text{ mA})(5.6\text{ k}\Omega + 1.2\text{ k}\Omega) \\ &= \mathbf{3.88\ V} \end{aligned}$$

Tabulating the results, we have:

Comparing the exact and approximate approaches.

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, whereas V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$\boxed{I_{C_{\text{sat}}} = I_{C_{\max}} = \frac{V_{CC}}{R_C + R_E}} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.25, with

$$\boxed{I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\text{ V}}} \tag{4.39}$$

and

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0\text{ mA}}} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 COLLECTOR FEEDBACK CONFIGURATION

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.38. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop, with the results then applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.39 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

It is important to note that the current through R_C is not I_C, but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B, and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

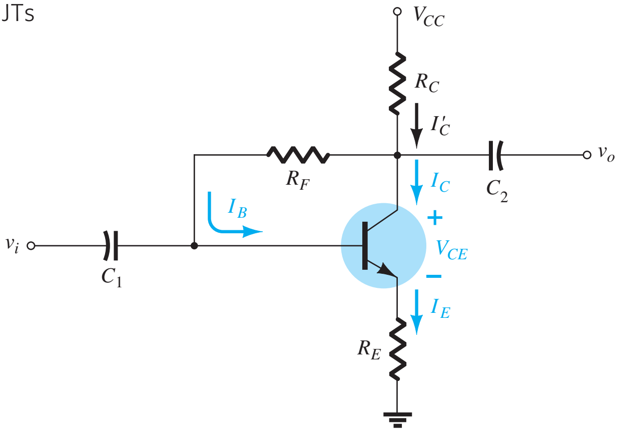


FIG. 4.38
DC bias circuit with voltage feedback.

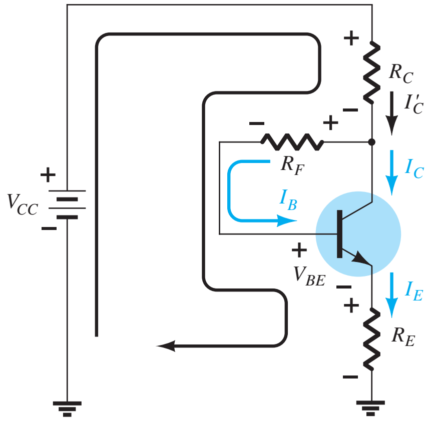


FIG. 4.39
Base–emitter loop for the network of Fig. 4.38.

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

and solving for I_B yields

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}} \tag{4.41}$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, whereas the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has the following format, which can be compared with the result for the fixed-bias and emitter-bias configurations.

$$I_B = \frac{V'}{R_F + \beta R'}$$

For the fixed-bias configuration $\beta R'$ does not exist. For the emitter-bias setup (with $\beta + 1 \cong \beta$), $R' = R_E$.

Because $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\dfrac{R_F}{\beta} + R'}$$

In general, the larger R' is compared with $\dfrac{R_F}{\beta}$, the more accurate the approximation that

$$I_{C_Q} \cong \frac{V'}{R'}$$

The result is an equation absent of β, which would be very stable for variations in β. Because R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is 0 Ω for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

Collector–Emitter Loop

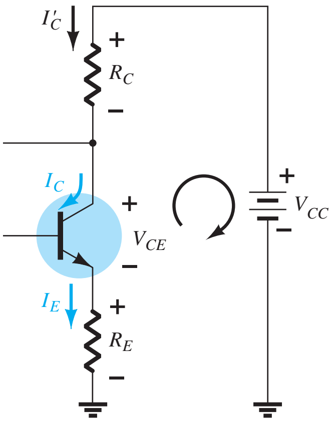


FIG. 4.40
Collector–emitter loop for the network of Fig. 4.38.

The collector–emitter loop for the network of Fig. 4.38 is provided in Fig. 4.40. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Because $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.42}$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

EXAMPLE 4.12 Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.41.

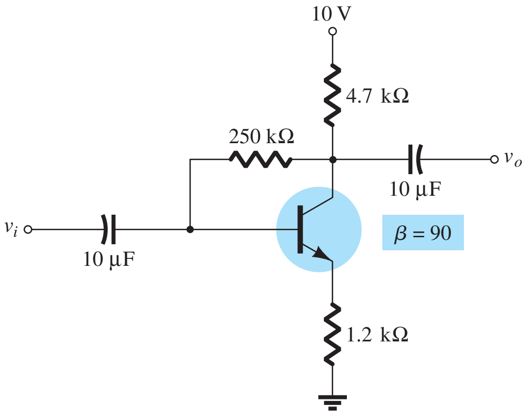


FIG. 4.41

Network for Example 4.12.

Solution: Eq. (4.41):

$$\begin{aligned}
I_B &= \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} \\
&= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)} \\
&= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega} \\
&= 11.91\ \mu\text{A} \\
I_{C_Q} &= \beta I_B = (90)(11.91\ \mu\text{A}) \\
&= \mathbf{1.07\ mA} \\
V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\
&= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega) \\
&= 10\text{ V} - 6.31\text{ V} \\
&= \mathbf{3.69\ V}
\end{aligned}$$

EXAMPLE 4.13 Repeat Example 4.12 using a beta of 135 (50% greater than in Example 4.12).

Solution: It is important to note in the solution for I_B in Example 4.12 that the second term in the denominator of the equation is much larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less is the sensitivity to changes in beta. In this example, the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (135)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 796.5\text{ k}\Omega} = \frac{9.3\text{ V}}{1046.5\text{ k}\Omega}$$
$$= 8.89\ \mu\text{A}$$

and
$$I_{C_Q} = \beta I_B$$
$$= (135)(8.89\ \mu\text{A})$$
$$= \mathbf{1.2\ mA}$$

and
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.2\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 10\text{ V} - 7.08\text{ V}$$
$$= \mathbf{2.92\ V}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1%, whereas the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q-point.

EXAMPLE 4.14 Determine the dc level of I_B and V_C for the network of Fig. 4.42.

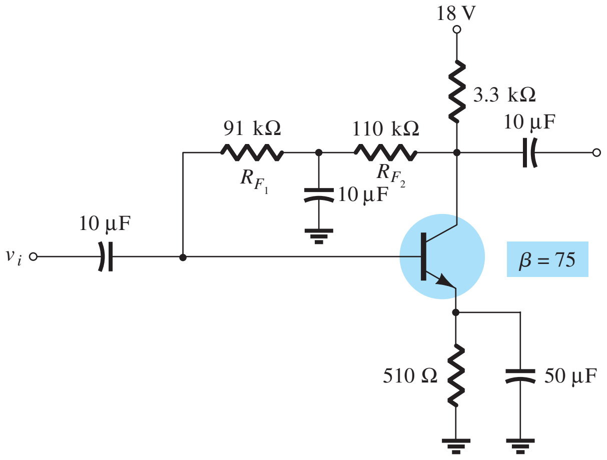


FIG. 4.42

Network for Example 4.14.

Solution: In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and $R_B = R_{F_1} + R_{F_2}$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\text{ k}\Omega + 110\text{ k}\Omega) + (75)(3.3\text{ k}\Omega + 0.51\text{ k}\Omega)}$$
$$= \frac{17.3\text{ V}}{201\text{ k}\Omega + 285.75\text{ k}\Omega} = \frac{17.3\text{ V}}{486.75\text{ k}\Omega}$$
$$= \mathbf{35.5\ \mu A}$$

$$\begin{aligned} I_C &= \beta I_B \\ &= (75)(35.5\ \mu\text{A}) \\ &= 2.66\text{ mA} \\ V_C &= V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C \\ &= 18\text{ V} - (2.66\text{ mA})(3.3\text{ k}\Omega) \\ &= 18\text{ V} - 8.78\text{ V} \\ &= \mathbf{9.22\ V} \end{aligned}$$

Saturation Conditions

Using the approximation $I'_C = I_C$, we find that the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$\boxed{I_{C_{\text{sat}}} = I_{C_{\max}} = \frac{V_{CC}}{R_C + R_E}} \qquad \textbf{(4.43)}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ results in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} is defined by the chosen bias configuration.

EXAMPLE 4.15 Given the network of Fig. 4.43 and the BJT characteristics of Fig. 4.44.

a. Draw the load line for the network on the characteristics.
b. Determine the dc beta in the center region of the characteristics. Define the chosen point as the Q-point.
c. Using the dc beta calculated in part b, find the dc value of I_B.
d. Find I_{C_Q} and I_{CE_Q}.

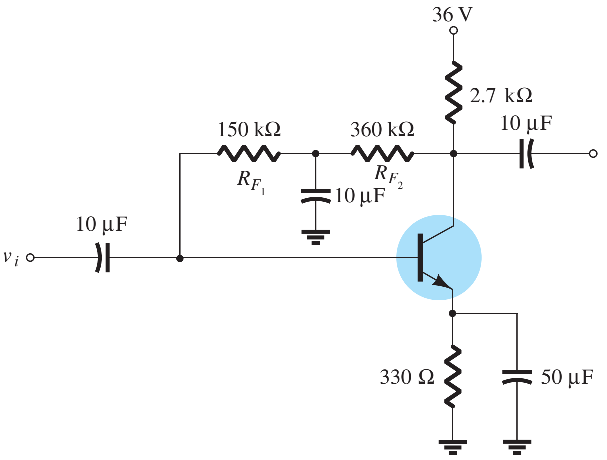


FIG. 4.43
Network for Example 4.15.

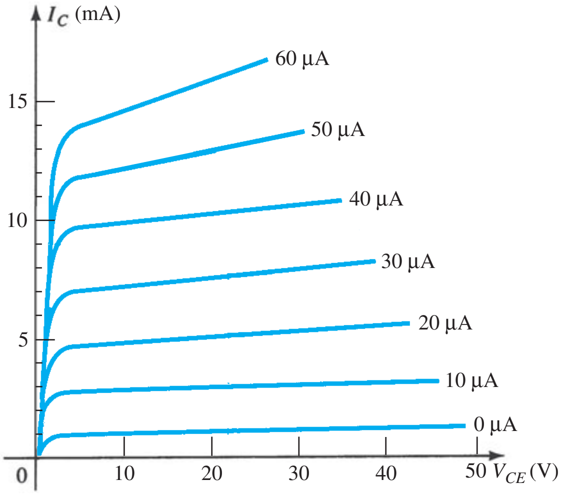


FIG. 4.44
BJT characteristics.

Solution:

a. The load line is drawn on Fig. 4.45 as determined by the following intersections:

$$V_{CE} = 0\text{ V}: I_C = \frac{V_{CC}}{R_C + R_E} = \frac{36\text{ V}}{2.7\text{ k}\Omega + 330\ \Omega} = \mathbf{11.88\ mA}$$

$$I_C = 0\text{ mA}: V_{CE} = V_{CC} = \mathbf{36\ V}$$

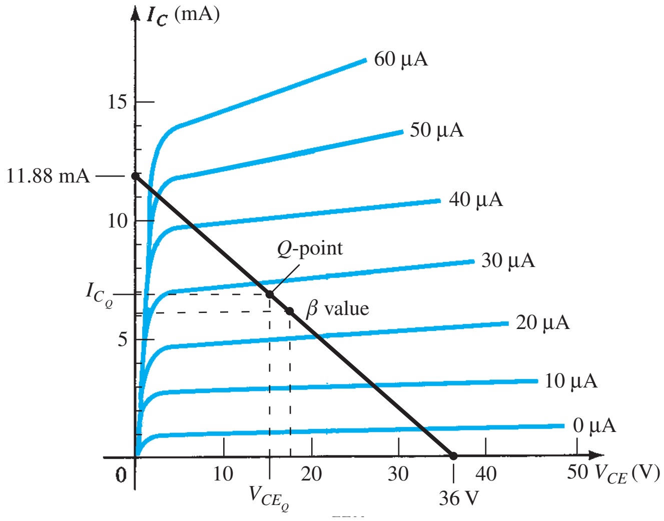


FIG. 4.45

Defining the Q-point for the voltage-divider bias configuration of Fig. 4.43.

b. The dc beta was determined using $I_B = 25\ \mu\text{A}$ and V_{CE} about 17 V.

$$\beta \cong \frac{I_{C_Q}}{I_{B_Q}} = \frac{6.2\text{ mA}}{25\ \mu\text{A}} = \mathbf{248}$$

c. Using Eq. 4.41:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{36\text{ V} - 0.7\text{ V}}{510\text{ k}\Omega + 248(2.7\text{ k}\Omega + 330\ \Omega)}$$

$$= \frac{35.3\text{ V}}{510\text{ k}\Omega + 751.44\text{ k}\Omega}$$

and $I_B = \dfrac{35.3\text{ V}}{1.261\text{ M}\Omega} = \mathbf{28\ \mu A}$

d. From Fig. 4.45 the quiescent values are

$I_{C_Q} \cong$ **6.9 mA** and $V_{CE_Q} \cong$ **15 V**

4.7 EMITTER-FOLLOWER CONFIGURATION

The previous sections introduced configurations in which the output voltage is typically taken off the collector terminal of the BJT. This section will examine a configuration where the output is taken off the emitter terminal as shown in Fig. 4.46. The configuration of Fig. 4.46 is not the only one where the output can be taken off the emitter terminal. In fact, any of the configurations just described can be used so long as there is a resistor in the emitter leg.

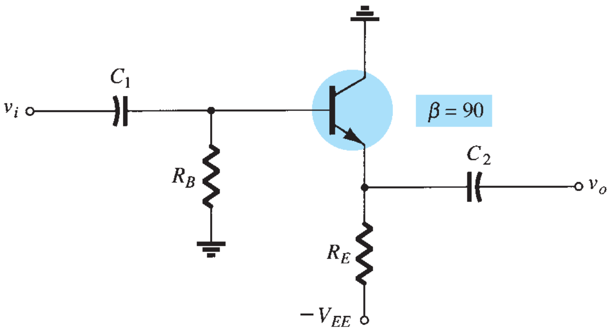


FIG. 4.46

Common-collecter (emitter-follower) configuration.

The dc equivalent of the network of Fig. 4.46 appears in Fig. 4.47

Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_BR_B - V_{BE} - I_ER_E + V_{EE} = 0$$

and using $I_E = (\beta + 1)I_B$

$$I_BR_B + (\beta + 1)I_BR_E = V_{EE} - V_{BE}$$

so that

$$\boxed{I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{4.44}$$

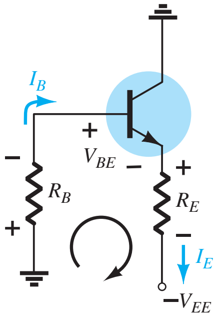


FIG. 4.47
dc equivalent of Fig. 4.46.

For the output network, an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_ER_E + V_{EE} = 0$$

and

$$\boxed{V_{CE} = V_{EE} - I_ER_E} \tag{4.45}$$

EXAMPLE 4.16 Determine V_{CE_Q} and I_{E_Q} for the network of Fig. 4.48.

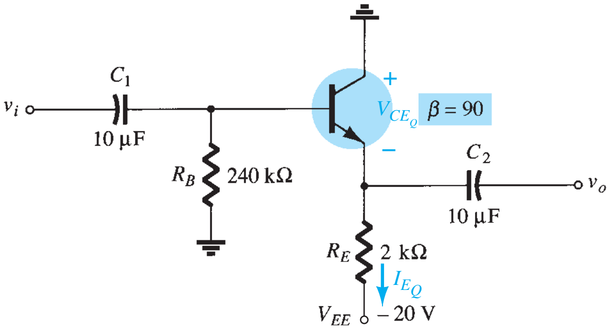


FIG. 4.48
Example 4.16.

Solution:

Eq. 4.44:

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega + (90 + 1)2\text{ k}\Omega} = \frac{19.3\text{ V}}{240\text{ k}\Omega + 182\text{ k}\Omega}$$
$$= \frac{19.3\text{ V}}{422\text{ k}\Omega} = 45.73\ \mu\text{A}$$

and Eq. 4.45:

$$V_{CE_Q} = V_{EE} - I_ER_E$$
$$= V_{EE} - (\beta + 1)I_BR_E$$
$$= 20\text{ V} - (90 + 1)(45.73\ \mu\text{A})(2\text{ k}\Omega)$$
$$= 20\text{ V} - 8.32\text{ V}$$
$$= \mathbf{11.68\ V}$$
$$I_{E_Q} = (\beta + 1)I_B = (91)(45.73\ \mu\text{A})$$
$$= 4.16\text{ mA}$$

4.8 COMMON-BASE CONFIGURATION

The common-base configuration is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential. It is a fairly popular configuration because in the ac domain it has a very low input impedance, high output impedance, and good gain.

A typical common-base configuration appears in Fig. 4.49. Note that two supplies are used in this configuration and the base is the common terminal between the input emitter terminal and output collector terminal.

The dc equivalent of the input side of Fig. 4.49 appears in Fig. 4.50.

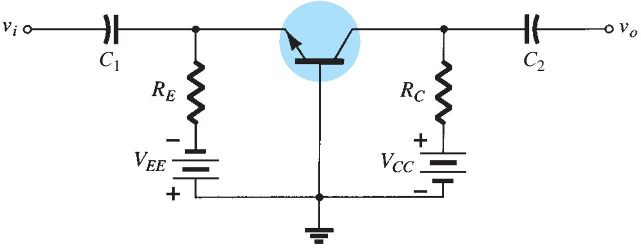


FIG. 4.49
Common-base configuration.

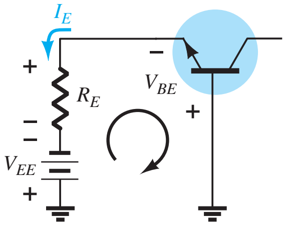


FIG. 4.50
Input dc equivalent of Fig. 4.49.

Applying Kirchhoff's voltage law will result in

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{R_E}} \tag{4.46}$$

Applying Kirchhoff's voltage law to the entire outside perimeter of the network of Fig. 4.51 will result in

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

and solving for V_{CE}:
$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

Because
$$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)} \tag{4.47}$$

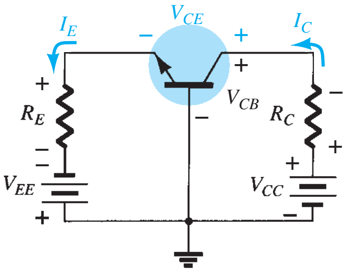


FIG. 4.51
Determining V_{CE} and V_{CB}.

The voltage V_{CB} of Fig. 4.51 can be found by applying Kirchhoff's voltage law to the output loop of Fig 4.51 to obtain:

$$V_{CB} + I_C R_C - V_{CC} = 0$$

or
$$V_{CB} = V_{CC} - I_C R_C$$

Using
$$I_C \cong I_E$$

we have
$$\boxed{V_{CB} = V_{CC} - I_C R_C} \tag{4.48}$$

EXAMPLE 4.17 Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of Fig. 4.52.

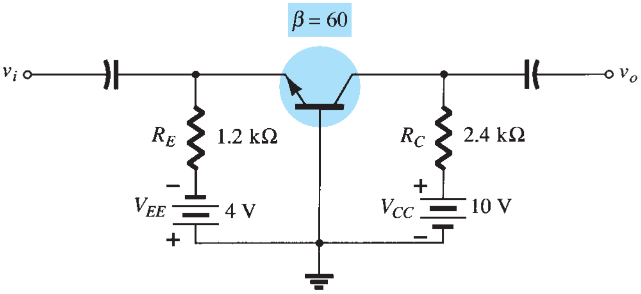


FIG. 4.52
Example 4.17.

Solution: Eq. 4.46:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.75\text{ mA}}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{ mA}}{60 + 1} = \frac{2.75\text{ mA}}{61} = \mathbf{45.08\ \mu A}$$

Eq. 4.47:

$$\begin{aligned} V_{CE} &= V_{EE} + V_{CC} - I_E(R_C + R_E) \\ &= 4\text{ V} + 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega + 1.2\text{ k}\Omega) \\ &= 14\text{ V} - (2.75\text{ mA})(3.6\text{ k}\Omega) \\ &= 14\text{ V} - 9.9\text{ V} \\ &= \mathbf{4.1\text{ V}} \end{aligned}$$

Eq. 4.48:

$$\begin{aligned} V_{CB} &= V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C \\ &= 10\text{ V} - (60)(45.08\ \mu\text{A})(24\text{ k}\Omega) \\ &= 10\text{ V} - 6.49\text{ V} \\ &= \mathbf{3.51\text{ V}} \end{aligned}$$

4.9 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a single publication. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite directly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.38. The analysis is quite similar, but does require dropping R_E from the applied equation.

EXAMPLE 4.18 For the network of Fig. 4.53:

a. Determine I_{C_Q} and V_{CE_Q}.
b. Find V_B, V_C, V_E, and V_{BC}.

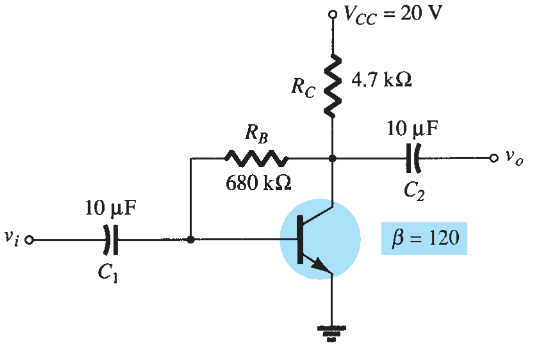


FIG. 4.53
Collector feedback with $R_E = 0\ \Omega$.

Solution:

a. The absence of R_E reduces the reflection of resistive levels to simply that of R_C, and the equation for I_B reduces to

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \\ &= \frac{20\text{ V} - 0.7\text{ V}}{680\text{ k}\Omega + (120)(4.7\text{ k}\Omega)} = \frac{19.3\text{ V}}{1.244\text{ M}\Omega} \\ &= \mathbf{15.51\ \mu A} \\ I_{C_Q} &= \beta I_B = (120)(15.51\ \mu\text{A}) \\ &= \mathbf{1.86\ mA} \\ V_{CE_Q} &= V_{CC} - I_C R_C \\ &= 20\text{ V} - (1.86\text{ mA})(4.7\text{ k}\Omega) \\ &= \mathbf{11.26\ V} \end{aligned}$$

b.

$$\begin{aligned} V_B &= V_{BE} = \mathbf{0.7\ V} \\ V_C &= V_{CE} = \mathbf{11.26\ V} \\ V_E &= \mathbf{0\ V} \\ V_{BC} &= V_B - V_C = 0.7\text{ V} - 11.26\text{ V} \\ &= \mathbf{-10.56\ V} \end{aligned}$$

In the next example, the applied voltage is connected to the emitter leg and R_C is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.

EXAMPLE 4.19 Determine V_C and V_B for the network of Fig. 4.54.

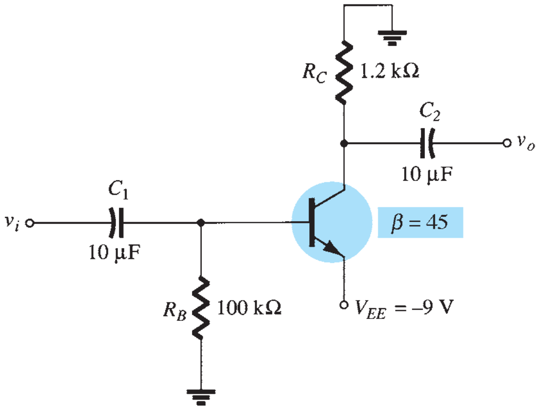


FIG. 4.54

Example 4.19.

Solution: Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

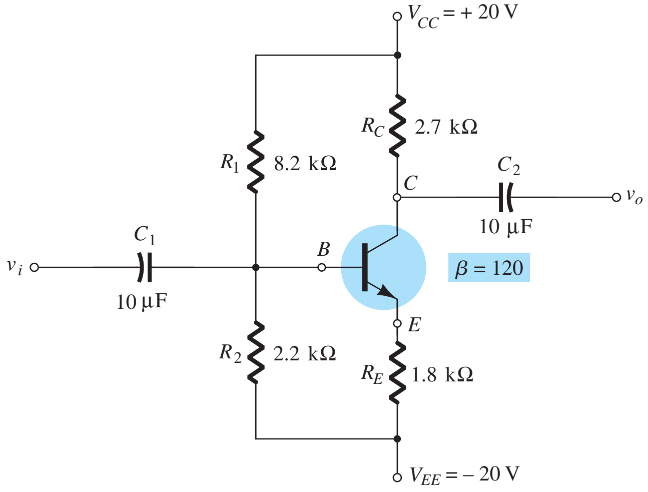
Substitution yields

$$\begin{aligned} I_B &= \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} \\ &= \frac{8.3\text{ V}}{100\text{ k}\Omega} \\ &= 83\ \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_C &= \beta I_B \\ &= (45)(83\ \mu\text{A}) \\ &= 3.735\ \text{mA} \\ V_C &= -I_C R_C \\ &= -(3.735\ \text{mA})(1.2\ \text{k}\Omega) \\ &= \mathbf{-4.48\ V} \\ V_B &= -I_B R_B \\ &= -(83\ \mu\text{A})(100\ \text{k}\Omega) \\ &= \mathbf{-8.3\ V} \end{aligned}$$

Example 4.20 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

EXAMPLE 4.20 Determine V_C and V_B for the network of Fig. 4.55.



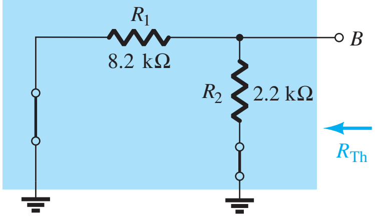
$V_{CC} = +20$ V
R_C 2.7 kΩ
R_1 8.2 kΩ
C_2
C
v_o
10 µF
C_1
B
v_i
$\beta = 120$
10 µF
E
R_2 2.2 kΩ
R_E 1.8 kΩ
$V_{EE} = -20$ V

FIG. 4.55
Example 4.20.

Solution: The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.56 and 4.57.

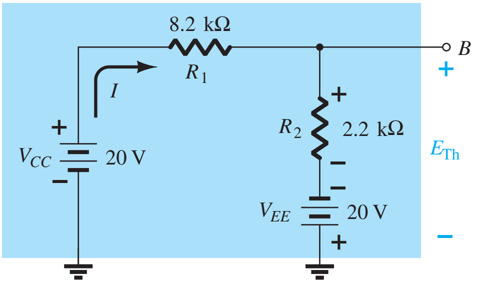
R_{Th}

$$R_{Th} = 8.2\ \text{k}\Omega \,\|\, 2.2\ \text{k}\Omega = 1.73\ \text{k}\Omega$$



R_1
8.2 kΩ
B
R_2 2.2 kΩ
R_{Th}

FIG. 4.56
Determining R_{Th}.



8.2 kΩ
R_1
B
+
I
+
R_2 2.2 kΩ
+
V_{CC} 20 V
–
E_{Th}
–
–
V_{EE} 20 V
+
–

FIG. 4.57
Determining E_{Th}.

E_{Th}

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\ \mathrm{V} + 20\ \mathrm{V}}{8.2\ \mathrm{k\Omega} + 2.2\ \mathrm{k\Omega}} = \frac{40\ \mathrm{V}}{10.4\ \mathrm{k\Omega}}$$
$$= 3.85\ \mathrm{mA}$$
$$E_{\mathrm{Th}} = IR_2 - V_{EE}$$
$$= (3.85\ \mathrm{mA})(2.2\ \mathrm{k\Omega}) - 20\ \mathrm{V}$$
$$= -11.53\ \mathrm{V}$$

The network can then be redrawn as shown in Fig. 4.58, where the application of Kirchhoff's voltage law results in

$$-E_{\mathrm{Th}} - I_B R_{\mathrm{Th}} - V_{BE} - I_E R_E + V_{EE} = 0$$

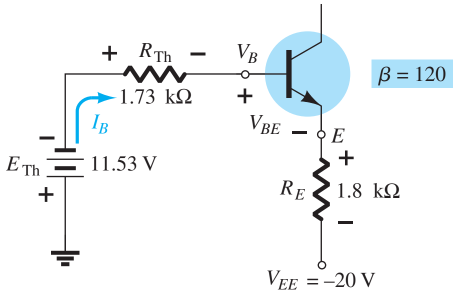


FIG. 4.58

Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{\mathrm{Th}} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{\mathrm{Th}} = 0$$

and

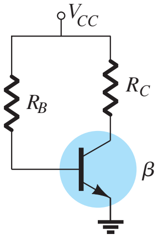
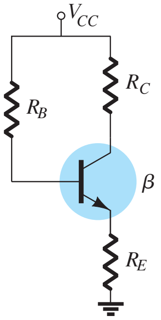
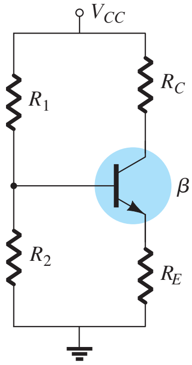
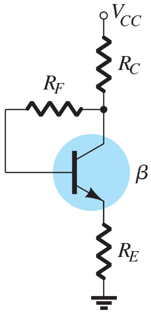
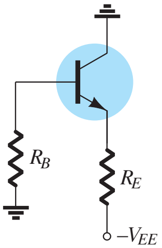
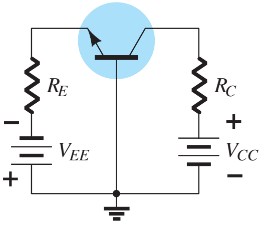
$$I_B = \frac{V_{EE} - E_{\mathrm{Th}} - V_{BE}}{R_{\mathrm{Th}} + (\beta + 1)R_E}$$
$$= \frac{20\ \mathrm{V} - 11.53\ V - 0.7\ \mathrm{V}}{1.73\ \mathrm{k\Omega} + (121)(1.8\ \mathrm{k\Omega})}$$
$$= \frac{7.77\ \mathrm{V}}{219.53\ \mathrm{k\Omega}}$$
$$= 35.39\ \mu\mathrm{A}$$
$$I_C = \beta I_B$$
$$= (120)(35.39\ \mu\mathrm{A})$$
$$= 4.25\ \mathrm{mA}$$
$$V_C = V_{CC} - I_C R_C$$
$$= 20\ \mathrm{V} - (4.25\ \mathrm{mA})(2.7\ \mathrm{k\Omega})$$
$$= \mathbf{8.53\ V}$$
$$V_B = -E_{\mathrm{Th}} - I_B R_{\mathrm{Th}}$$
$$= -(11.53\ \mathrm{V}) - (35.39\ \mu\mathrm{A})(1.73\ \mathrm{k\Omega})$$
$$= \mathbf{-11.59\ V}$$

4.10 SUMMARY TABLE

Table 4.1 is a review of the most common single-stage BJT configurations with their respective equations. Note the similarities that exist between the equations for the various configurations.

TABLE 4.1

BJT Bias Configurations

Type	Configuration	Pertinent Equations
Fixed-bias	 V_{CC} R_B R_C β	$I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias	 V_{CC} R_B R_C β R_E	$I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Voltage-divider bias	 V_{CC} R_1 R_C β R_2 R_E	EXACT: $R_{\text{Th}} = R_1 \| R_2, E_{\text{Th}} = \dfrac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \dfrac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \dfrac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \dfrac{V_E}{R_E}, I_B = \dfrac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Collector-feedback	 V_{CC} R_C R_F β R_E	$I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Emitter-follower		$I_B = \dfrac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
Common-base	 R_E R_C − V_{EE} + + V_{CC} −	$I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$ $I_B = \dfrac{I_E}{\beta + 1}, I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$

4.11 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

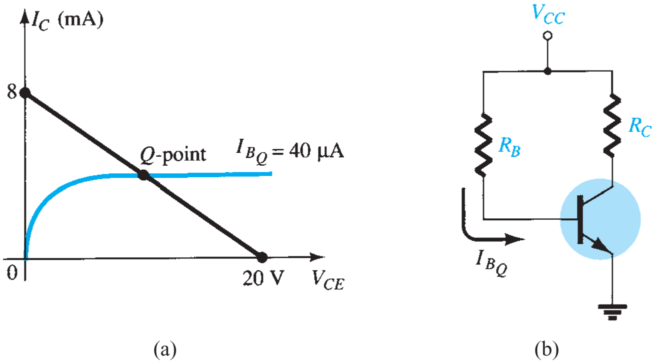
The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$\boxed{R_{\text{unknown}} = \frac{V_R}{I_R}} \qquad \textbf{(4.49)}$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.49) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from the design specifications. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b.



(a) (b)

FIG. 4.59
Example 4.21.

Solution: From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ \text{V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{40\ \mu\text{A}} = \frac{19.3\text{ V}}{40\ \mu\text{A}}$$
$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values are
$$R_C = 2.4\text{ k}\Omega$$
$$R_B = 470\text{ k}\Omega$$

Using standard resistor values gives
$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

EXAMPLE 4.22 Given that $I_{C_Q} = 2$ mA and $V_{CE_Q} = 10$ V, determine R_1 and R_C for the network of Fig. 4.60.

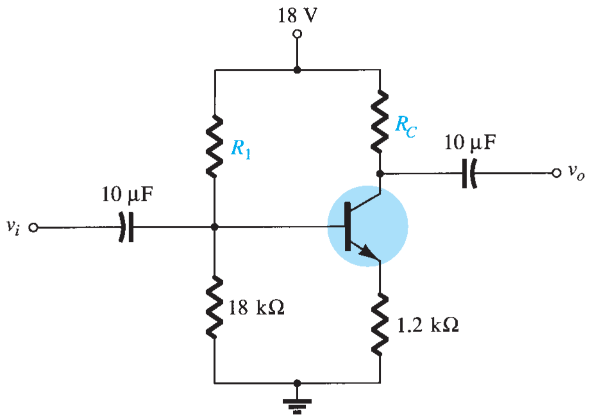


FIG. 4.60
Example 4.22.

Solution:

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\text{ mA})(1.2\text{ k}\Omega) = 2.4\text{ V}$$
$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\text{ V}$$

and
$$\frac{(18\text{ k}\Omega)(18\text{ V})}{R_1 + 18\text{ k}\Omega} = 3.1\text{ V}$$
$$324\text{ k}\Omega = 3.1R_1 + 55.8\text{ k}\Omega$$
$$3.1R_1 = 268.2\text{ k}\Omega$$
$$R_1 = \frac{268.2\text{ k}\Omega}{3.1} = \mathbf{86.52\ k\Omega}$$
$$\text{Eq. (4.49):}\quad R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

with
$$V_C = V_{CE} + V_E = 10\text{ V} + 2.4\text{ V} = 12.4\text{ V}$$

and
$$R_C = \frac{18\text{ V} - 12.4\text{ V}}{2\text{ mA}}$$
$$= \mathbf{2.8\ k\Omega}$$

The nearest standard commercial values to R_1 are 82 kΩ and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 4.7 kΩ = 86.7 kΩ would result in a value very close to the design level.

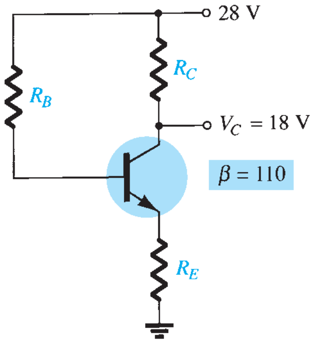


FIG. 4.61
Example 4.23.

EXAMPLE 4.23 The emitter-bias configuration of Fig. 4.61 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{\text{sat}}$, $I_{C_{\text{sat}}} = 8\text{ mA}$, $V_C = 18\text{ V}$, and $\beta = 110$. Determine R_C, R_E, and R_B.

Solution:

$$I_{C_Q} = \tfrac{1}{2}I_{C_{\text{sat}}} = 4\text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28\text{ V} - 18\text{ V}}{4\text{ mA}} = \mathbf{2.5\text{ k}\boldsymbol{\Omega}}$$

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E}$$

and
$$R_C + R_E = \frac{V_{CC}}{I_{C_{\text{sat}}}} = \frac{28\text{ V}}{8\text{ mA}} = 3.5\text{ k}\Omega$$

$$R_E = 3.5\text{ k}\Omega - R_C$$

$$= 3.5\text{ k}\Omega - 2.5\text{ k}\Omega$$

$$= \mathbf{1\text{ k}\boldsymbol{\Omega}}$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4\text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and
$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

with
$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28\text{ V} - 0.7\text{ V}}{36.36\ \mu\text{A}} - (111)(1\text{ k}\Omega)$$

$$= \frac{27.3\text{ V}}{36.36\ \mu\text{A}} - 111\text{ k}\Omega$$

$$= \mathbf{639.8\text{ k}\boldsymbol{\Omega}}$$

For standard values,

$$R_C = 2.4\text{ k}\Omega$$

$$R_E = 1\text{ k}\Omega$$

$$R_B = 620\text{ k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we concentrate on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.62. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector–emitter loop has two unknown quantities present—the resistors R_C and R_E. At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.62 using the criteria just introduced for the emitter voltage.

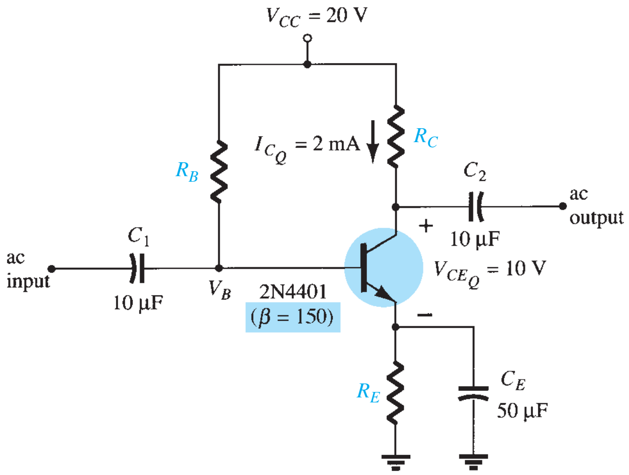


FIG. 4.62

Emitter-stabilized bias circuit for design consideration.

EXAMPLE 4.24 Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\ k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$
$$= \mathbf{4\ k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$
$$\cong \mathbf{1.3\ M\Omega}$$

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.63 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage V_E, as in the previous design consideration, leads to a direct, straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

EXAMPLE 4.25 Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.63 for the operating point indicated.

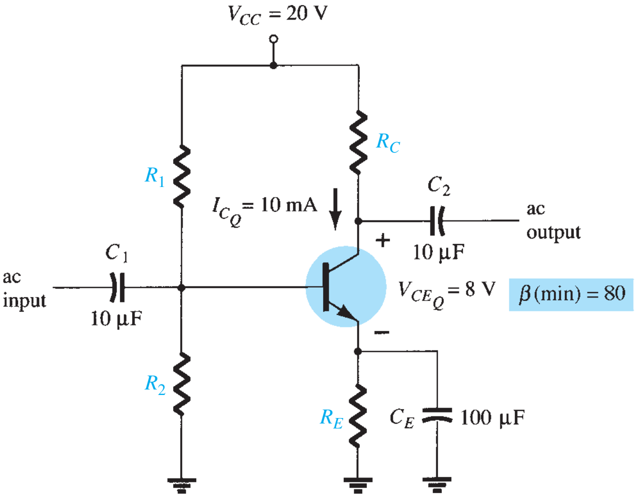


FIG. 4.63
Current-gain-stabilized circuit for design considerations.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$
$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

The equations for the calculation of the base resistors R_1 and R_2 will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, R_1 and R_2. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through R_1 and R_2 should be approximately equal to and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

Substitution yields

$$R_2 \leq \tfrac{1}{10}(80)(0.2\text{ k}\Omega)$$
$$= \mathbf{1.6\ k\Omega}$$

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

and
$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$
$$2.7R_1 = 27.68\text{ k}\Omega$$
$$R_1 = \mathbf{10.25\text{ k}\Omega} \quad (\text{use } 10\text{ k}\Omega)$$

4.12 MULTIPLE BJT NETWORKS

The BJT networks introduced thus far have only been single-stage configurations. This section will cover some of the most popular networks using multiple transistors. It will demonstrate how the methods introduced thus far in this chapter can be applied to networks with any number of components.

The **R–C coupling** of Fig. 4.64 is probably the most common. The collector output of one stage is fed directly into the base of the next stage using a coupling capacitor C_C. The capacitor is chosen to ensure that it will block dc between the stages and act like a short circuit to any ac signal. The network of Fig. 4.64 has two voltage-divider stages, but the same coupling can be used between any combination of networks such as the fixed-bias or emitter-follower configurations. Substituting an open-circuit equivalent for C_C and the other capacitors of the network will result in the two bias arrangements shown in Fig. 4.65. The methods of analysis introduced in this chapter can then be applied to each stage separately since one stage will not affect the other. Of course, the 20 V dc supply must be applied to each isolated component.

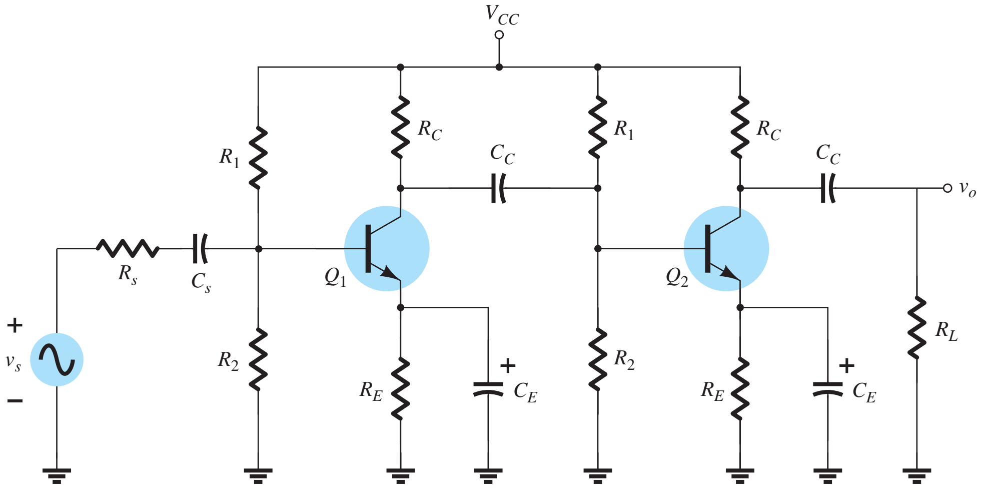


FIG. 4.64
R–C coupled BJT amplifiers.

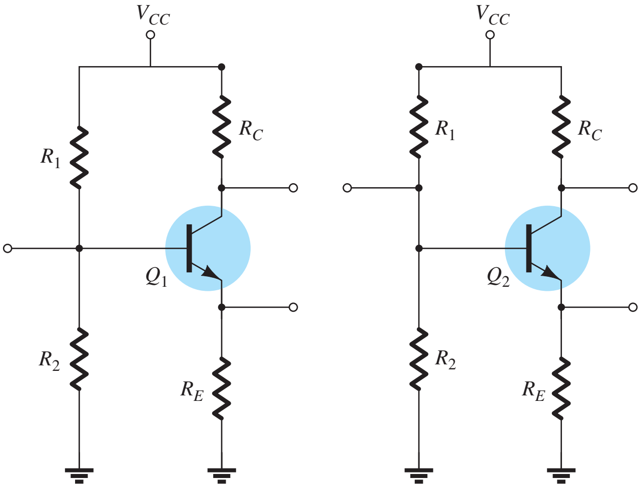


FIG. 4.65
DC equivalent of Fig. 4.64.

The **Darlington** configuration of Fig. 4.66 feeds the output of one stage directly into the input of the succeeding stage. Since the output of Fig. 4.66 is taken directly off the emitter terminal, you will find in the next chapter that the ac gain is very close to 1 but the input impedance is very high, making it attractive for use in amplifiers operating off sources that have a relatively high internal resistance. If a load resistor were added to the collector leg and the output taken off the collector terminal, the configuration would provide a very high gain.

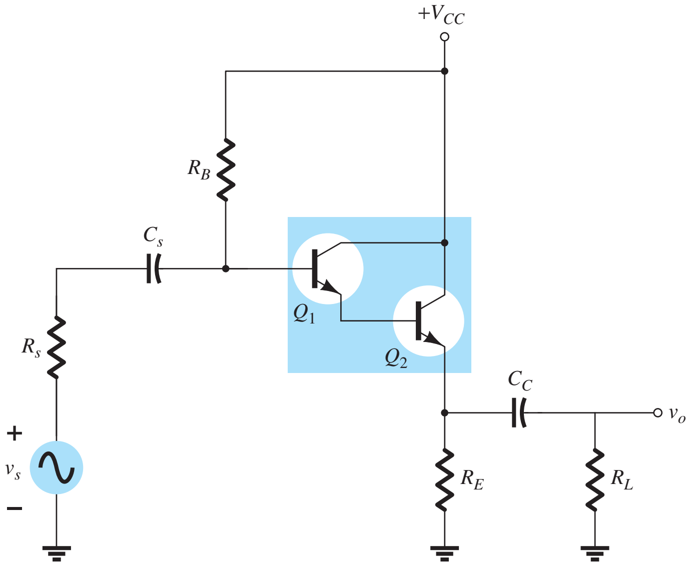


FIG. 4.66

Darlington amplifier.

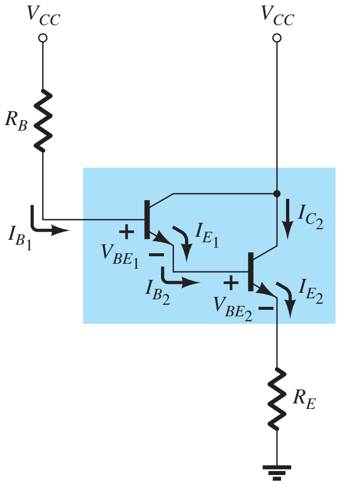


FIG. 4.67

DC equivalent of Fig. 4.66.

For the dc analysis of Fig. 4.67 assuming a beta β_1 for the first transistor and β_2 for the second, the base current for the second transistor is

$$I_{B_2} = I_{E_1} = (\beta_1 + 1)I_{B_1}$$

and the emitter current for the second transistor is

$$I_{E_2} = (\beta_2 + 1)I_{B_2} = (\beta_2 + 1)(\beta_1 + 1)I_{B_1}$$

Assuming $\beta \gg 1$ for each transistor, we find the net beta for the configuration is

$$\boxed{\beta_D = \beta_1\beta_2} \tag{4.50}$$

which compares directly with a single-stage amplifier having a gain of β_D.

Applying an analysis similar to that of Section 4.4 will result in the following equation for the base current:

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

Defining

$$\boxed{V_{BE_D} = V_{BE_1} + V_{BE_2}} \tag{4.51}$$

we have

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E}} \tag{4.52}$$

The currents

$$\boxed{I_{C_2} \cong I_{E_2} = \beta_D I_{B_1}} \tag{4.53}$$

and the dc voltage at the emitter terminal is

$$\boxed{V_{E_2} = I_{E_2}R_E} \tag{4.54}$$

The collector voltage for this configuration is obviously equal to that of the source V.

$$\boxed{V_{C_2} = V_{CC}} \tag{4.55}$$

and the voltage across the output of the transistor is

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

and

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \tag{4.56}$$

The **Cascode** configuration of Fig. 4.68 ties the collector of one transistor to the emitter of the other. In essence it is a voltage-divider network with a common-base configuration at the collector. The result is a network with a high gain and a reduced Miller capacitance—a topic to be examined in Section 9.9.

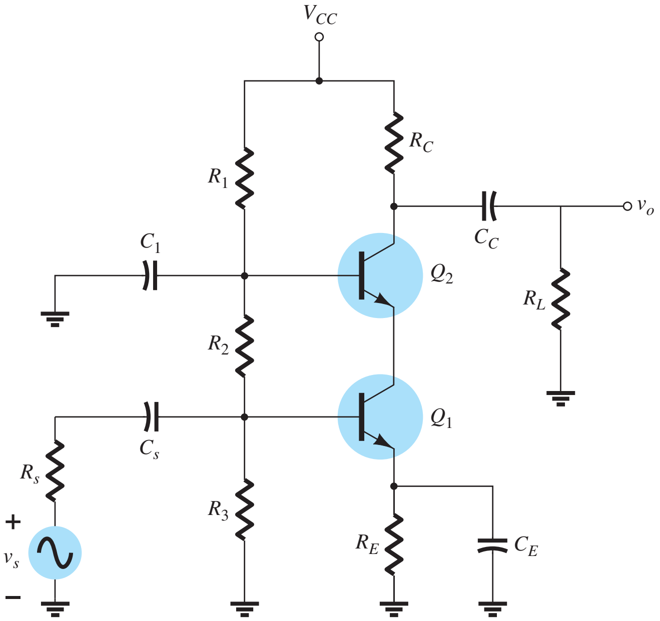


FIG. 4.68
Cascode amplifier.

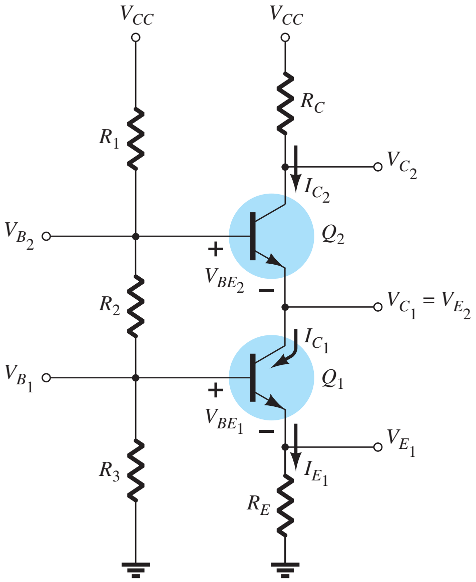


FIG. 4.69
DC equivalent of Fig. 4.68.

The dc analysis is initiated by assuming the current through the bias resistors R_1, R_2, and R_3 of Fig. 4.69 is much larger than the base current of each transistor. That is,

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} \gg I_{B_1} \text{ or } I_{B_2}$$

The result is that the voltage at the base of the transistor Q_1 is simply determined by an application of the voltage-divider rule:

$$\boxed{V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3}V_{CC}} \tag{4.57}$$

The voltage at the base of the transistor Q_2 is found in the same manner:

$$\boxed{V_{B_2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3}V_{CC}} \tag{4.58}$$

The emitter voltages are then determined by

$$\boxed{V_{E_1} = V_{B_1} - V_{BE_1}} \tag{4.59}$$

and

$$\boxed{V_{E_2} = V_{B_2} - V_{BE_2}} \tag{4.60}$$

with the emitter and collector currents determined by:

$$\boxed{I_{C_2} \cong I_{E_2} \cong I_{C_1} \cong I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_{E_1} + R_{E_2}}} \tag{4.61}$$

The collector voltage V_{C_1}:

$$\boxed{V_{C_1} = V_{B_2} - V_{BE_2}} \tag{4.62}$$

and the collector voltage V_{C_2}:

$$\boxed{V_{C_2} = V_{CC} - I_{C_2}R_C} \tag{4.63}$$

The current through the biasing resistors is

$$\boxed{I_{R_1} \cong I_{R_2} \cong I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3}} \tag{4.64}$$

and each base current is determined by

$$\boxed{I_{B_1} = \frac{I_{C_1}}{\beta_1}} \tag{4.65}$$

with

$$\boxed{I_{B_2} = \frac{I_{C_2}}{\beta_2}} \tag{4.66}$$

The next multistage configuration to be introduced is the **Feedback Pair** of Fig. 4.70, which employs both an *npn* and *pnp* transistor. The result is a configuration that provides high gain with increased stability.

The dc version with all the currents labeled appears in Fig. 4.71.

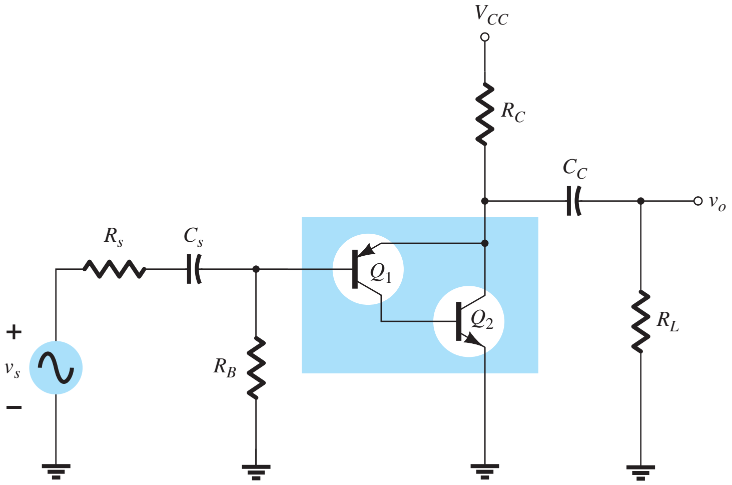


FIG. 4.70
Feedback Pair amplifier.

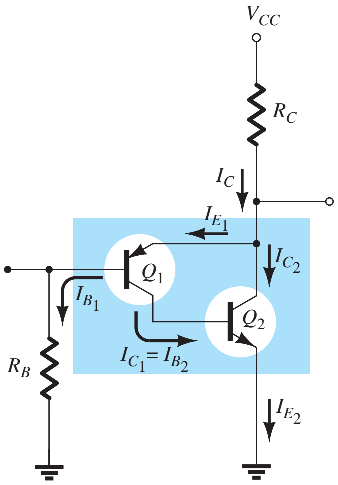


FIG. 4.71
DC equivalent of Fig. 4.70.

The base current

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1}$$

and

$$I_{C_2} = \beta_2 I_{B_2}$$

so that

$$\boxed{I_{C_2} \cong I_{E_2} = \beta_1\beta_2 I_{B_1}} \tag{4.67}$$

The collector current

$$\begin{aligned} I_C &= I_{E_1} + I_{E_2} \\ &\cong \beta_1 I_{B_1} + \beta_1\beta_2 I_{B_1} \\ &= \beta_1(1 + \beta_2)I_{B_1} \end{aligned}$$

so that

$$\boxed{I_C \cong \beta_1\beta_2 I_{B_1}} \tag{4.68}$$

Applying Kirchhoff's voltage law down from the source to ground will result in

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

or

$$V_{CC} - V_{EB_1} - \beta_1\beta_2 I_{B_1} R_C - I_{B_1} R_B = 0$$

and

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1\beta_2 R_C}} \tag{4.69}$$

The base voltage V_{B_1} is

$$\boxed{V_{B_1} = I_{B_1} R_B} \tag{4.70}$$

and

$$\boxed{V_{B_2} = V_{BE_2}} \tag{4.71}$$

The collector voltage $V_{C_2} = V_{E_1}$ is

$$\boxed{V_{C_2} = V_{CC} - I_C R_C} \tag{4.72}$$

and

$$\boxed{V_{C_1} = V_{BE_2}} \tag{4.73}$$

In this case

$$\boxed{V_{CE_2} = V_{C_2}} \tag{4.74}$$

and

$$V_{EC_1} = V_{E_1} - V_{C_1}$$

so that

$$\boxed{V_{EC_1} = V_{C_2} - V_{BE_2}} \tag{4.75}$$

The last multistage configuration to be introduced is the **Direct Coupled** amplifier such as appearing in Example 4.26. Note the absence of a coupling capacitor to isolate the dc levels of each stage. The dc levels in one stage will directly affect the dc levels in succeeding stages. The benefit is that the coupling capacitor typically limits the low-frequency response of the amplifier. Without coupling capacitors, the amplifier can amplify signals of very low frequency—in fact down to dc. The disadvantage is that any variation in dc levels due to a variety of reasons in one stage can affect the dc levels in the succeeding stages of the amplifier.

EXAMPLE 4.26 Determine the dc levels for the currents and voltages of the direct-coupled amplifier of Fig. 4.72. Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases wherein the input impedance of the next stage is quite low. The common-collector amplifier is acting like a **buffer** between stages.

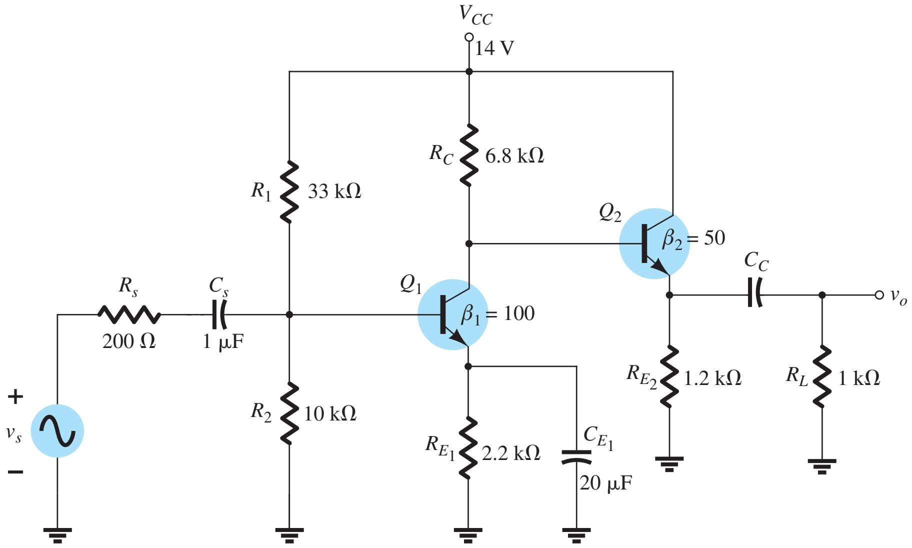

V_{CC}
14 V
R_C
6.8 kΩ
R_1
33 kΩ
Q_2
$\beta_2 = 50$
C_C
R_s
C_s
Q_1
200 Ω
1 μF
$\beta_1 = 100$
v_o
R_{E_2}
1.2 kΩ
R_L
1 kΩ
+
v_s
−
R_2
10 kΩ
R_{E_1}
2.2 kΩ
C_{E_1}
20 μF

FIG. 4.72
Direct-coupled amplifier.

Solution: The dc equivalent of Fig. 4.72 appears as Fig. 4.73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 4.5.

$$I_{B_1} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_{E_1}}$$

with
$$R_{\text{Th}} = R_1 \| R_2$$

and
$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

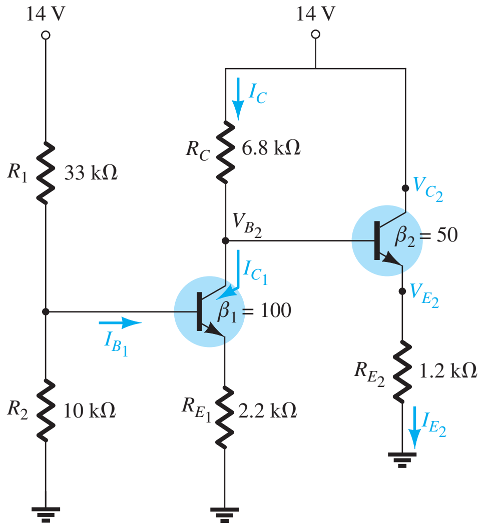

14 V
14 V
I_C
R_C
6.8 kΩ
R_1
33 kΩ
V_{C_2}
V_{B_2}
$\beta_2 = 50$
I_{C_1}
$\beta_1 = 100$
V_{E_2}
I_{B_1}
R_{E_2}
1.2 kΩ
R_2
10 kΩ
R_{E_1}
2.2 kΩ
I_{E_2}

FIG. 4.73
DC equivalent of Fig. 4.72.

In this case,

$$R_{\text{Th}} = 33\text{ k}\Omega \| 10\text{ k}\Omega = 7.67\text{ k}\Omega$$

and
$$E_{\text{Th}} = \frac{10\text{ k}\Omega(14\text{ V})}{10\text{ k}\Omega + 33\text{ k}\Omega} = 3.26\text{ V}$$

so that
$$I_{B_1} = \frac{3.26\text{ V} - 0.7\text{ V}}{7.67\text{ k}\Omega + (100 + 1)\,2.2\text{ k}\Omega} = \frac{2.56\text{ V}}{229.2\text{ k}\Omega} = \mathbf{11.17\ \mu A}$$

with
$$I_{C_1} = \beta I_{B_1} = 100\,(11.17\ \mu\text{A}) = \mathbf{1.12\ mA}$$

In Fig. 4.73 we find that

$$\boxed{V_{B_2} = V_{CC} - I_C R_C} \tag{4.76}$$

$$= 14\text{ V} - (1.12\text{ mA})(6.8\text{ k}\Omega) = 14\text{ V} - 7.62\text{ V} = \mathbf{6.38\ V}$$

and
$$V_{E_2} = V_{B_2} - V_{BE_2} = 6.38\text{ V} - 0.7\text{ V} = \mathbf{5.68\ V}$$

resulting in

$$\boxed{I_{E_2} = \frac{V_{E_2}}{R_{E_2}}} \tag{4.77}$$

$$= \frac{5.68\text{ V}}{1.2\text{ k}\Omega} = \mathbf{4.73\ mA}$$

Obviously,

$$\boxed{V_{C_2} = V_{CC}} \tag{4.78}$$

$$= 14\text{ V}$$

and
$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \tag{4.79}$$

$$= 14\text{ V} - 5.68\text{ V} = \mathbf{8.32\ V}$$

4.13 CURRENT MIRRORS

The **current mirror** is a dc network in which the current through a load is controlled by a current at another point in the network. That is, if the controlling current is raised or lowered the current through the load will change to the same level. The discussion to follow will demonstrate that the effectiveness of the design is dependent on the fact that the two transistors employed have identical characteristics. The basic configuration appears in Fig. 4.74. Note that the two transistors are back to back and the collector of one is connected to the base of the two transistors.

Assume identical transistors will result in $V_{BE_1} = V_{BE_2}$ and $I_{B_1} = I_{B_2}$ as defined by the base-to-emitter characteristics of Fig. 4.75. Raise the base to emitter voltage, and the current of each will rise to the same value.

Since the base to emitter voltages of the two transistors in Fig. 4.74 are in parallel, they must have the same voltage. The result is that $I_{B_1} = I_{B_2}$ at every set base to emitter voltage.

It is clear from Fig. 4.74 that
$$I_B = I_{B_1} + I_{B_2}$$

and if
$$I_{B_1} = I_{B_2}$$

then
$$I_B = I_{B_1} + I_{B_1} = 2I_{B_1}$$

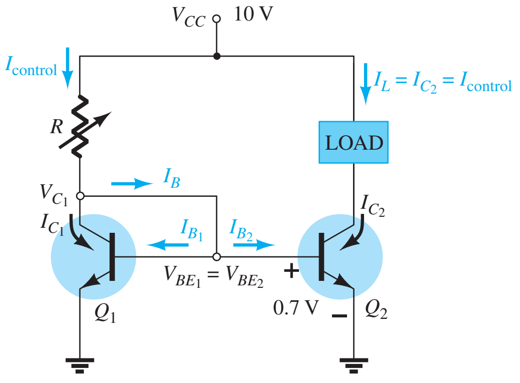


FIG. 4.74
Current mirror using back-to-back BJTs.

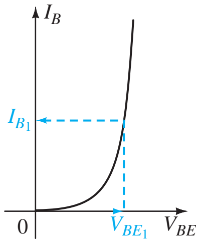


FIG. 4.75
Base characteristics for transistor Q_1 (and Q_2).

In addition,
$$I_{\text{control}} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1}$$
but
$$I_{C_1} = \beta_1 I_{B_1}$$
so
$$I_{\text{control}} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1}$$
and since β_1 is typically $\gg 2$,
$$I_{\text{control}} \cong \beta_1 I_{B_1}$$
or
$$\boxed{I_{B_1} = \frac{I_{\text{control}}}{\beta_1}} \qquad \textbf{(4.80)}$$

If the control current is raised, the resulting I_{B_1} will increase as determined by Eq. 4.80. If I_{B_1} increases, the voltage V_{BE_1} must increase as dictated by the response curve of Fig. 4.75. If V_{BE_1} increases, then V_{BE_2} must increase by the same amount and I_{B_2} will also increase. The result is that $I_L = I_{C_2} = \beta I_{B_2}$ will also increase to the level established by the control current.

Referring to Fig. 4.74 we find the control current is determined by

$$\boxed{I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R}} \qquad \textbf{(4.81)}$$

revealing that for a fixed V_{CC}, the resistor R can be used to set the control current.

The network also has a measure of built-in control that will try to ensure that any variation in load current will be corrected by the configuration itself. For instance, if I_L should try to increase for whatever reason, the base current of Q_2 will also increase due to the relationship $I_{B2} = I_{C2}/\beta_2 = I_L/\beta_2$. Returning to Fig. 4.101, we find that an increase in I_{B2} will cause voltage V_{BE_2} to increase also. Because the base of Q_2 is connected directly to the collector of Q_1, the voltage V_{CE_1} will increase also. This action causes the voltage across the control resistor R to decrease, causing I_R to drop. But if I_R drops, the base current I_B will drop, causing both I_{B_1} and I_{B_2} to drop also. A drop in I_{B_2} will cause the collector current and therefore the load current to drop also. The result, therefore, is a sensitivity to unwanted changes that the network will make every effort to correct.

The entire sequence of events just described can be presented on a single line as shown below. Note that at one end the load current is trying to increase, and at the end of the sequence the load current is forced to return to its original level.

$$I_L\uparrow I_{C_2}\uparrow I_{B_2}\uparrow V_{BE_2}\uparrow V_{CE_1}\downarrow, I_R\downarrow, I_B\downarrow, I_{B_2}\downarrow I_{C_2}\downarrow I_L\downarrow$$

Note

EXAMPLE 4.27 Calculate the mirrored current I in the circuit of Fig. 4.76.

Solution: Eq. (4.75):

$$I = I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{12\text{ V} - 0.7\text{ V}}{1.1\text{ k}\Omega} = \mathbf{10.27\text{ mA}}$$

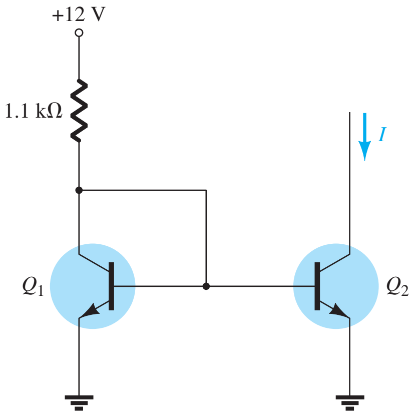


FIG. 4.76
Current mirror circuit for Example 4.27.

EXAMPLE 4.28 Calculate the current I through each of the transistor Q_2 and Q_3 in the circuit of Fig. 4.77.

Solution: Since $V_{BE_1} = V_{BE_2} = V_{BE_3}$ then $I_{B_1} = I_{B_2} = I_{B_3}$

Substituting $I_{B_1} = \dfrac{I_{\text{control}}}{\beta}$ and $I_{B_2} = \dfrac{I}{\beta}$ with $I_{B_3} = \dfrac{I}{\beta}$

we have $\dfrac{I_{\text{control}}}{\beta} = \dfrac{I}{\beta} = \dfrac{I}{\beta}$

so I must equal I_{control}

and $I_{\text{control}} = \dfrac{V_{CC} - V_{BE}}{R} = \dfrac{6\text{ V} - 0.7\text{ V}}{1.3\text{ k}\Omega} = \mathbf{4.08\ mA}$

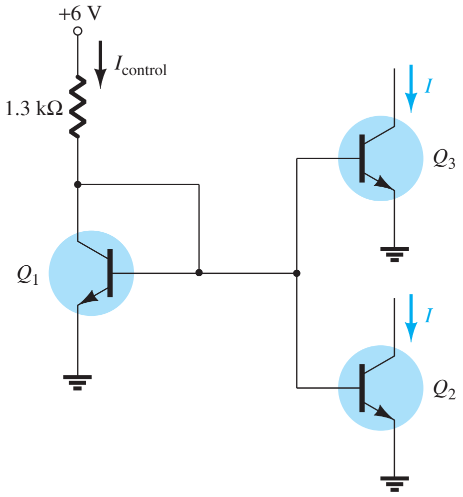


FIG. 4.77
Current mirror circuit for Example 4.28.

Figure 4.78 shows another form of current mirror to provide higher output impedance than that of Fig. 4.74. The control current through R is

$$I_{\text{control}} = \frac{V_{CC} - 2V_{BE}}{R} \approx I_C + \frac{I_C}{\beta} = \frac{\beta + 1}{\beta} I_C \approx I_C$$

Assuming that Q_1 and Q_2 are well matched, we find that the output current I is held constant at

$$I \approx I_C = I_{\text{control}}$$

Again we see that the output current I is a mirrored value of the current set by the fixed current through R.

Figure 4.79 shows still another form of current mirror. The junction field effect transistor (see Chapter 6) provides a constant current set at the value of I_{DSS}. This current is mirrored, resulting in a current through Q_2 of the same value:

$$I = I_{DSS}$$

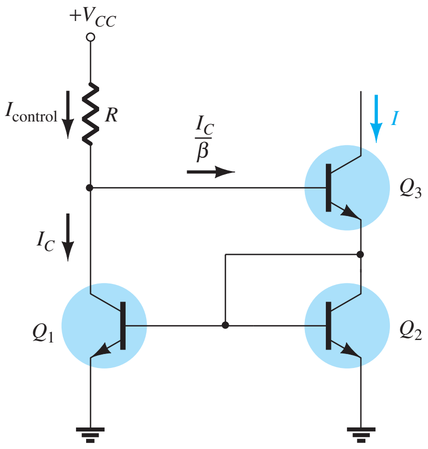


FIG. 4.78
Current mirror circuit with higher output impedance.

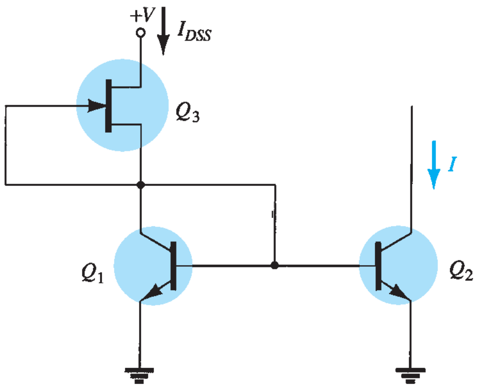
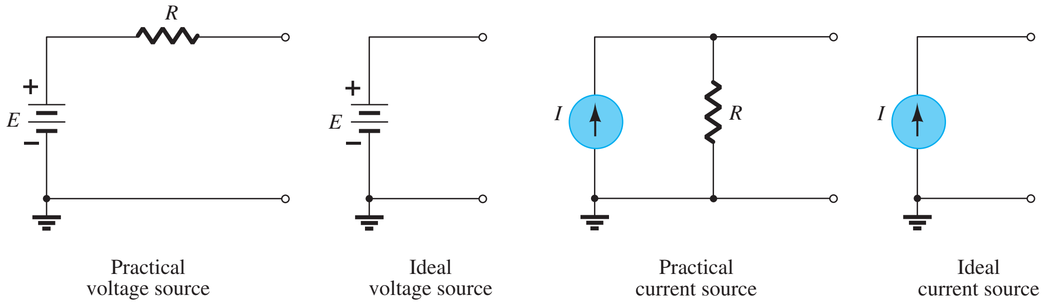


FIG. 4.79
Current mirror connection.

4.14 CURRENT SOURCE CIRCUITS

The concept of a power supply provides the starting point in our consideration of current source circuits. A practical voltage source (Fig. 4.80a) is a voltage supply in series with a resistance. An ideal voltage source has $R = 0$, whereas a practical source includes some small resistance. A practical current source (Fig. 4.80b) is a current supply in parallel with a resistance. An ideal current source has $R = \infty\,\Omega$, whereas a practical current source includes some very large resistance.



(a)

(b)

FIG. 4.80
Voltage and current sources.

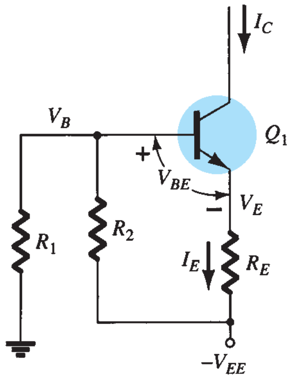


FIG. 4.81
Discrete constant-current source.

An ideal current source provides a constant current regardless of the load connected to it. There are many uses in electronics for a circuit providing a constant current at a very high impedance. Constant-current circuits can be built using bipolar devices, FET devices, and a combination of these components. There are circuits used in discrete form and others more suitable for operation in integrated circuits.

Bipolar Transistor Constant-Current Source

Bipolar transistors can be connected in a circuit that acts as a constant-current source in a number of ways. Figure 4.81 shows a circuit using a few resistors and an *npn* transistor for operation as a constant-current circuit. The current through I_E can be determined as follows. Assuming that the base input impedance is much larger than R_1 or R_2, we have

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE})$$

and

$$V_E = V_B - 0.7\text{ V}$$

with

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C \tag{4.82}$$

where I_C is the constant current provided by the circuit of Fig. 4.81.

EXAMPLE 4.29 Calculate the constant current I in the circuit of Fig. 4.82.

Solution:

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE}) = \frac{5.1\text{ k}\Omega}{5.1\text{ k}\Omega + 5.1\text{ k}\Omega}(-20\text{ V}) = -10\text{ V}$$

$$V_E = V_B - 0.7\text{ V} = 10\text{ V} - 0.7\text{ V} = -10.7\text{ V}$$

$$I = I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-10.7\text{ V} - (-20\text{ V})}{2\text{ k}\Omega}$$

$$= \frac{9.3\text{ V}}{2\text{ k}\Omega} = \mathbf{4.65\text{ mA}}$$

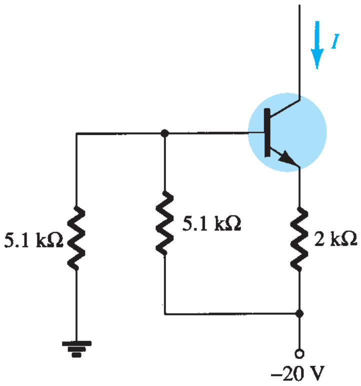


FIG. 4.82
Constant-current source for Example 4.29.

Transistor/Zener Constant-Current Source

Replacing resistor R_2 with a Zener diode, as shown in Fig. 4.83, provides an improved constant-current source over that of Fig. 4.81. The Zener diode results in a constant current calculated using the base-emitter KVL (Kirchhoff voltage loop) equation. The value of I can be calculated using

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E} \tag{4.83}$$

A major point to consider is that the constant current depends on the Zener diode voltage, which remains quite constant, and the emitter resistor R_E. The voltage supply V_{EE} has no effect on the value of I.

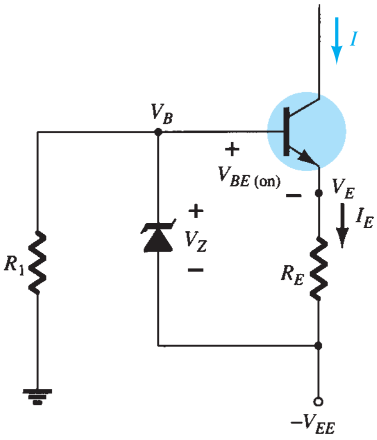


FIG. 4.83
Constant-current circuit using Zener diode.

EXAMPLE 4.30 Calculate the constant current I in the circuit of Fig. 4.84.

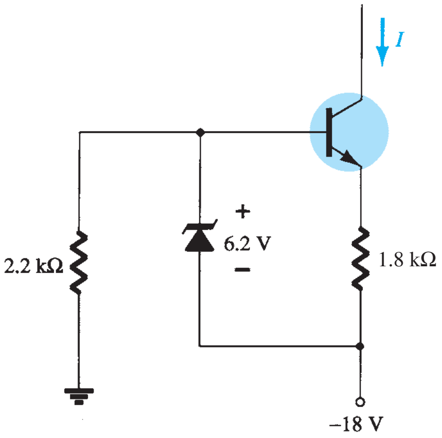


FIG. 4.84
Constant-current circuit for Example 4.30.

Solution:

$$\text{Eq. (4.83):}\quad I = \frac{V_Z - V_{BE}}{R_E} = \frac{6.2\text{ V} - 0.7\text{ V}}{1.8\text{ k}\Omega} = 3.06\text{ mA} \approx \mathbf{3\text{ mA}}$$

4.15 *pnp* TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of I_B is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

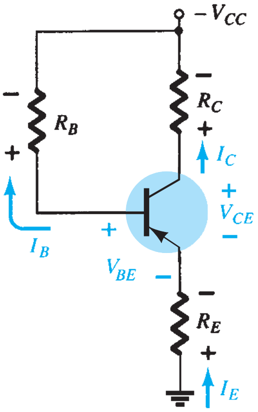


FIG. 4.85

pnp transistor in an emitter-stabilized configuration.

As noted in Fig. 4.85, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.85, both V_{BE} and V_{CE} will be negative quantities.

Applying Kirchhoff's voltage law to the base–emitter loop results in the following equation for the network of Fig. 4.85:

$$-I_ER_E + V_{BE} - I_BR_B + V_{CC} = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$\boxed{I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E}} \qquad \textbf{(4.84)}$$

The resulting equation is the same as Eq. (4.17) except for the sign for V_{BE}. However, in this case $V_{BE} = -0.7$ V and the substitution of values results in the same sign for each term of Eq. (4.84) as Eq. (4.17). Keep in mind that the direction of I_B is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.85.

For V_{CE} Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

$$-I_ER_E + V_{CE} - I_CR_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ gives

$$\boxed{V_{CE} = -V_{CC} + I_C(R_C + R_E)} \qquad \textbf{(4.85)}$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Because V_{CC} will be larger than the magnitude of the succeeding term, the voltage V_{CE} will have a negative sign, as noted in an earlier paragraph.

EXAMPLE 4.31 Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.86.

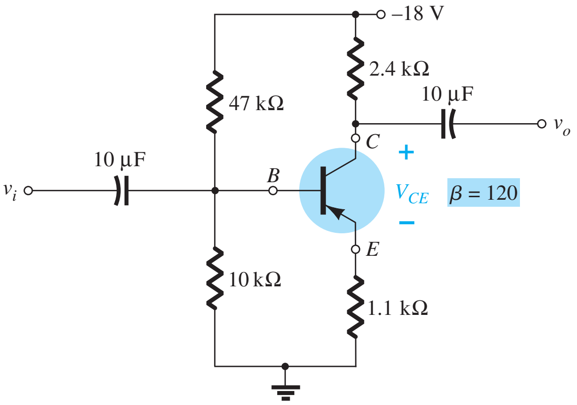


FIG. 4.86

pnp transistor in a voltage-divider bias configuration.

Solution: Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$\begin{aligned}(120)(1.1\text{ k}\Omega) &\geq 10(10\text{ k}\Omega)\\ 132\text{ k}\Omega &\geq 100\text{ k}\Omega \quad (\textit{satisfied})\end{aligned}$$

Solving for V_B, we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10\text{ k}\Omega)(-18\text{ V})}{47\text{ k}\Omega + 10\text{ k}\Omega} = -3.16\text{ V}$$

Note the similarity in format of the equation with the resulting negative voltage for V_B.

Applying Kirchhoff's voltage law around the base–emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$\begin{aligned}V_E &= -3.16\text{ V} - (-0.7\text{ V})\\ &= -3.16\text{ V} + 0.7\text{ V}\\ &= -2.46\text{ V}\end{aligned}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation $V_E = V_B - V_{BE}$ would be exactly the same. The only difference surfaces when the values are substituted.

The current is

$$I_E = \frac{V_E}{R_E} = \frac{2.46\text{ V}}{1.1\text{ k}\Omega} = 2.24\text{ mA}$$

For the collector–emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

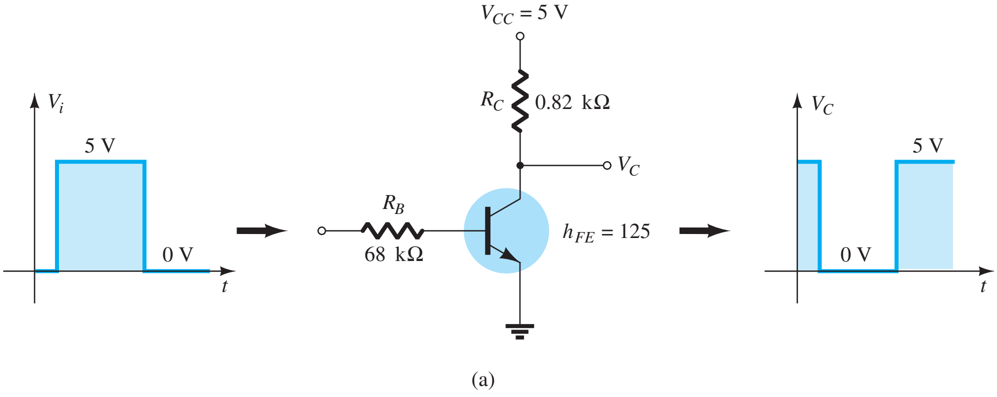
$$\begin{aligned}V_{CE} &= -18\text{ V} + (2.24\text{ mA})(2.4\text{ k}\Omega + 1.1\text{ k}\Omega)\\ &= -18\text{ V} + 7.84\text{ V}\\ &= \mathbf{-10.16\text{ V}}\end{aligned}$$

4.16 TRANSISTOR SWITCHING NETWORKS

The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can be used as switches for computer and control applications. The network of Fig. 4.87a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V. The resistor R_B will ensure that the full applied voltage of 5 V will not appear across the base-to-emitter junction. It will also set the I_B level for the "on" condition.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.87b. For our purposes we will assume that $I_C = I_{CEO} \cong 0$ mA when $I_B = 0\ \mu$A (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.87b. In addition, we will assume that $V_{CE} = V_{CE_{\text{sat}}} \cong 0$ V rather than the typical 0.1-V to 0.3-V level.

When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing



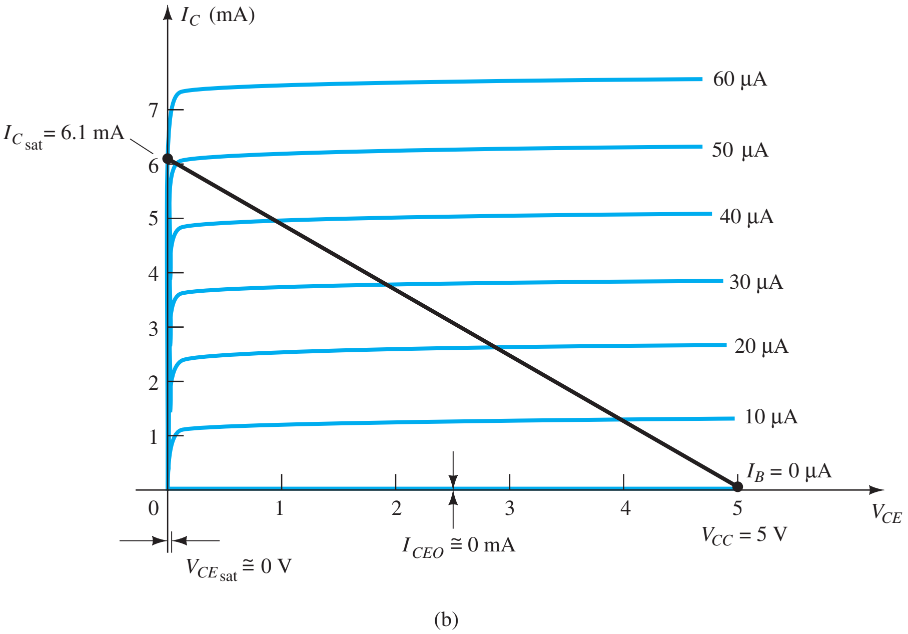


FIG. 4.87

Transistor inverter.

near the saturation level. In Fig. 4.87b, this requires that $I_B > 50\ \mu A$. The saturation level for the collector current for the circuit of Fig. 4.87a is defined by

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}} \tag{4.86}$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$\boxed{I_B > \frac{I_{C_{sat}}}{\beta_{dc}}} \tag{4.87}$$

For the network of Fig. 4.87b, when $V_i = 5$ V, the resulting level of I_B is

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and
$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (4.87) gives

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

which is satisfied. Certainly, any level of I_B greater than 60 μA will pass through a Q-point on the load line that is very close to the vertical axis.

For $V_i = 0$ V, $I_B = 0\ \mu$A, and because we are assuming that $I_C = I_{CEO} = 0$ mA, the voltage drop across R_C as determined by $V_{RC} = I_C R_C = 0$ V, resulting in $V_C = +5$ V for the response indicated in Fig. 4.87a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current I_C is quite high and the voltage V_{CE} very low. The result is a resistance level between the two terminals determined by

$$R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}$$

and is depicted in Fig. 4.88.

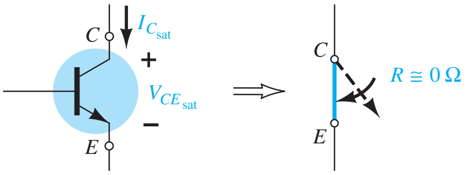


FIG. 4.88
Saturation conditions and the resulting terminal resistance.

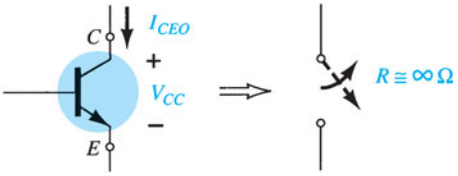


FIG. 4.89
Cutoff conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{\text{sat}}}$ such as 0.15 V gives

$$R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\ \Omega$$

which is a relatively low value and can be considered as approximately 0 Ω when placed in series with resistors in the kilohm range.

For $V_i = 0$ V, as shown in Fig. 4.89, the cutoff condition results in a resistance level of the following magnitude:

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \boldsymbol{\infty\ \Omega}$$

resulting in the open-circuit equivalence. For a typical value of $I_{CEO} = 10\ \mu$A, the magnitude of the cutoff resistance is

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\ \mu\text{A}} = \mathbf{500\ k\Omega}$$

which certainly approaches an open-circuit equivalence for many situations.

EXAMPLE 4.32 Determine R_B and R_C for the transistor inverter of Fig. 4.90 if $I_{C_{\text{sat}}} = 10$ mA.

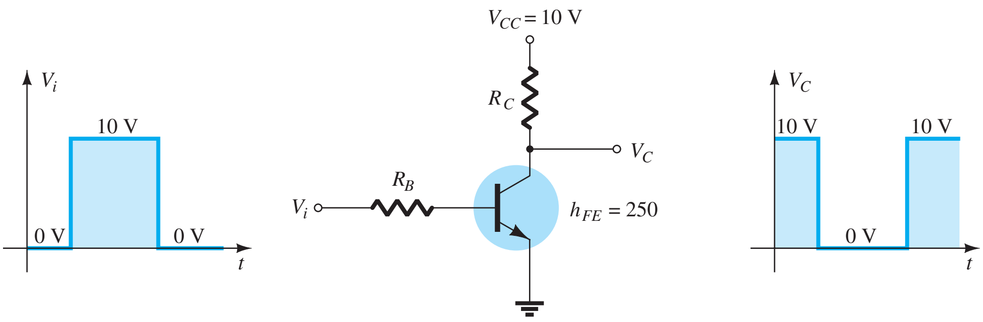


FIG. 4.90
Inverter for Example 4.32.

Solution: At saturation,

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation,

$$I_B \cong \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{10\text{ mA}}{250} = 40\ \mu\text{A}$$

Choosing $I_B = 60\ \mu\text{A}$ to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain

$$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\ \mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\text{ k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\ \mu\text{A}$$

and

$$I_B = 62\ \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = 40\ \mu\text{A}$$

Therefore, use $R_B = \mathbf{150\text{ k}\Omega}$ and $R_C = \mathbf{1\text{ k}\Omega}$.

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.91. The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and is defined by

$$\boxed{t_{\text{on}} = t_r + t_d} \tag{4.88}$$

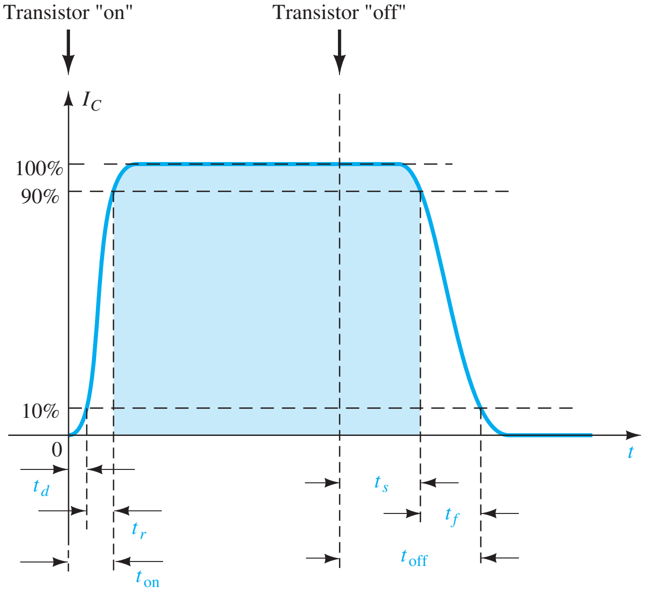


FIG. 4.91
Defining the time intervals of a pulse waveform.

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$\boxed{t_{\text{off}} = t_s + t_f} \tag{4.89}$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at $I_C = 10$ mA, we find that

$$t_s = 120 \text{ ns}$$
$$t_d = 25 \text{ ns}$$
$$t_r = 13 \text{ ns}$$

and $$t_f = 12 \text{ ns}$$

so that $$t_{\text{on}} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = \mathbf{38\ ns}$$

and $$t_{\text{off}} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = \mathbf{132\ ns}$$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises:

$$t_{\text{on}} = \mathbf{12\ ns} \text{ and } t_{\text{off}} = \mathbf{18\ ns}$$

4.17 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

For an "on" transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.

The proper connections for measuring V_{BE} appear in Fig. 4.92. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V or a negative value, would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used, but a negative reading should be expected.

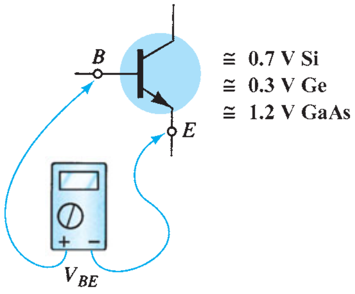


FIG. 4.92
Checking the dc level of V_{BE}.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of V_{CE} in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless it is being employed in a switching mode. However:

For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

For $V_{CC} = 20$ V, a reading of V_{CE} of 1 V to 2 V or from 18 V to 20 V as measured in Fig. 4.93 is certainly an uncommon result, and unless the device was knowingly designed for this response, the design and operation should be investigated. If $V_{CE} = 20$ V (with $V_{CC} = 20$ V) at least two possibilities exist—either the device (BJT) is damaged and has the characteristics

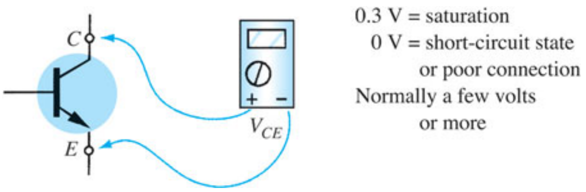


FIG. 4.93
Checking the dc level of V_{CE}.

of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.94, establishing I_C at 0 mA and $V_{R_C} = 0$ V. In Fig. 4.94, the black lead of the voltmeter is connected to the common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a consequent zero voltage drop across R_C will result in a reading of 20 V. If the meter is connected between the collector terminal and ground of the BJT, the reading will be 0 V because V_{CC} is blocked from the active device by the open circuit. One of the most common errors in the laboratory is the use of the wrong resistance value for a given design. Imagine the impact of using a 680-Ω resistor for R_B rather than the design value of 680 kΩ. For $V_{CC} = 20$ V and a fixed-bias configuration, the resulting base current would be

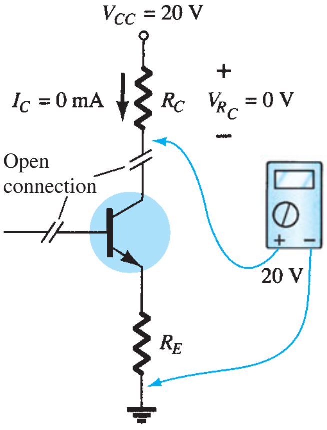


FIG. 4.94

Effect of a poor connection or damaged device.

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\ \Omega} = 28.4\text{ mA}$$

rather than the desired 28.4 μA—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Because actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is measurements closer to theoretical levels and some insurance that the correct resistance value is being employed.

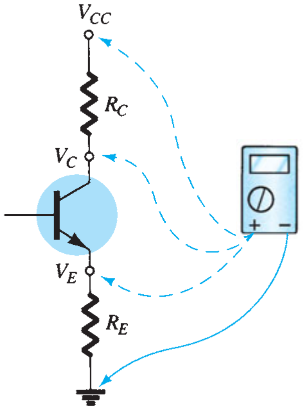


FIG. 4.95

Checking voltage levels with respect to ground.

There are times when frustration will develop. You check the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection of a lead is faulty? How often has simply touching a lead at the proper point created a "make or break" situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader is the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and "touching" the important terminals with the red (positive) lead. In Fig. 4.95, if the red lead is connected directly to V_{CC}, it should read V_{CC} volts because the network has one common ground for the supply and network parameters. At V_C the reading should be less, as determined by the drop across R_C, and V_E should be less than V_C by the collector–emitter voltage V_{CE}. The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If V_{R_C} and V_{R_E} are reasonable values but V_{CE} is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if V_{CE} registers a level of about 0.3 V as defined by $V_{CE} = V_C - V_E$ (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than "breaking" the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.

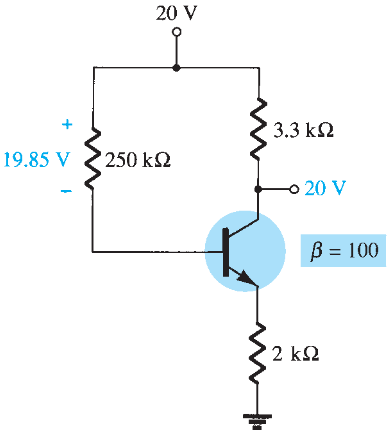


FIG. 4.96

Network for Example 4.33.

EXAMPLE 4.33 Based on the readings provided in Fig. 4.96, determine whether the network is operating properly and, if not, the probable cause.

Solution: The 20 V at the collector immediately reveals that $I_C = 0$ mA, due to an open circuit or a nonoperating transistor. The level of $V_{R_B} = 19.85$ V also reveals that the transistor is "off" because the difference of $V_{CC} - V_{R_B} = 0.15$ V is less than that required to turn "on" the transistor and provide some voltage for V_E. In fact, if we assume a short-circuit condition from base to emitter, we obtain the following current through R_B:

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20\text{ V}}{252\text{ k}\Omega} = 79.4\ \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85\text{ V}}{250\text{ k}\Omega} = 79.4\ \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (101)(2\text{ k}\Omega)} = \frac{19.3\text{ V}}{452\text{ k}\Omega} = 42.7\ \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

EXAMPLE 4.34 Based on the readings appearing in Fig. 4.97, determine whether the transistor is "on" and the network is operating properly.

Solution: Based on the resistor values of R_1 and R_2 and the magnitude of V_{CC}, the voltage $V_B = 4$ V seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an "on" transistor. However, the 20 V at the collector reveals that $I_C = 0$ mA, although the connection to the supply must be "solid" or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between R_C and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohm-meter, and if it is okay, check the transistor using one of the methods described in Chapter 3.

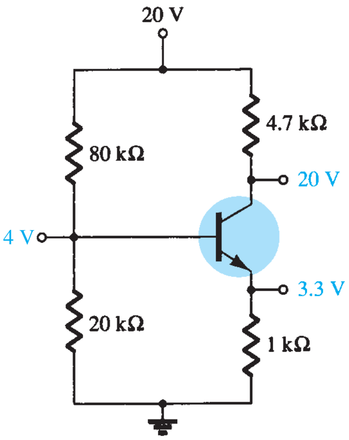


FIG. 4.97
Network for Example 4.34.

4.18 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 2.5 mV per degree Celsius (°C) increase in temperature

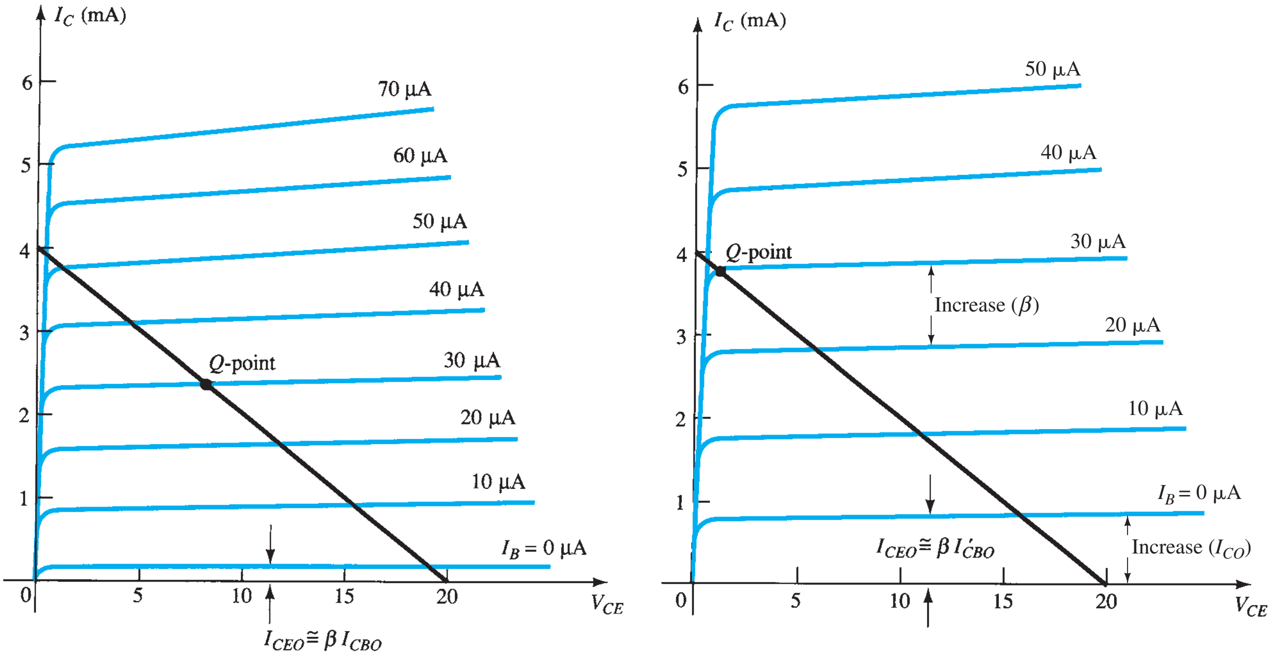
I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.2 reveals how the levels of I_{CO} and V_{BE} change with increase in temperature for a particular transistor. At room temperature (about 25°C) $I_{CO} = 0.1$ nA, whereas at 100°C (boiling point of water) I_{CO} is about 200 times larger, at 20 nA. For the same temperature variation, β increases from 50 to 80 and V_{BE} drops from 0.65 V to 0.48 V. Recall that I_B is quite sensitive to the level of V_{BE}, especially for levels beyond the threshold value.

TABLE 4.2
Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE} (V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^3	120	0.3

The effect of changes in leakage current (I_{CO}) and current gain (β) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.98a and b. Figure 4.98 shows how the transistor collector characteristics change from a temperature of



(a)

(b)

FIG. 4.98

Shift in dc bias point (Q-point) due to change in temperature: (a) 25°C; (b) 100°C.

25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise, but also causes an increase in beta, as revealed by the larger spacing between curves.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.98a at $I_B = 30\ \mu\text{A}$. Because the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.98b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector–emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

Stability Factors $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor S is defined for each of the parameters affecting bias stability as follows:

$$\boxed{S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}} \tag{4.90}$$

$$\boxed{S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}} \tag{4.91}$$

$$\boxed{S(\beta) = \frac{\Delta I_C}{\Delta \beta}} \tag{4.92}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.90) through (4.92) to be sensitivity factors because:

The higher the stability factor, the more sensitive is the network to variations in that parameter.

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject. Our analysis will begin with the $S(I_{CO})$ level for each configuration.

$S(I_{CO})$

Fixed-Bias Configuration

For the fixed-bias configuration, the following equation results:

$$\boxed{S(I_{CO}) \cong \beta} \tag{4.93}$$

Emitter-Bias Configuration

For the emitter-bias configuration of Section 4.4, an analysis of the network results in

$$\boxed{S(I_{CO}) \cong \frac{\beta(1 + R_B/R_E)}{\beta + R_B/B_E}} \tag{4.94}$$

For $R_B/R_E \gg \beta$, Eq. (4.94) reduces to the following:

$$\boxed{S(I_{CO}) \cong \beta}_{R_B/R_E \gg \beta} \tag{4.95}$$

as shown on the graph of $S(I_{CO})$ versus R_B/R_E in Fig. 4.99.

For $R_B/R_E \ll 1$, Eq. (4.94) will approach the following level (as shown in Fig. 4.99):

$$\boxed{S(I_{CO}) \cong 1}_{R_B/R_E \ll 1} \tag{4.96}$$

revealing that the stability factor will approach its lowest level as R_E becomes sufficiently large. Keep in mind, however, that good bias control normally requires that R_B be greater than R_E. The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.99 that the lowest value of $S(I_{CO})$ is 1, revealing that I_C will always increase at a rate equal to or greater than I_{CO}.

For the range where R_B/R_E ranges between 1 and $(\beta + 1)$, the stability factor will be determined by

$$\boxed{S(I_{CO}) \cong \frac{R_B}{R_E}} \tag{4.97}$$

The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches β.

Note that the equation for the fixed-bias configuration matches the maximum value for the emitter-bias configuration. The result clearly reveals that the fixed-bias configuration has a poor stability factor and a high sensitivity to variations in I_{CO}.

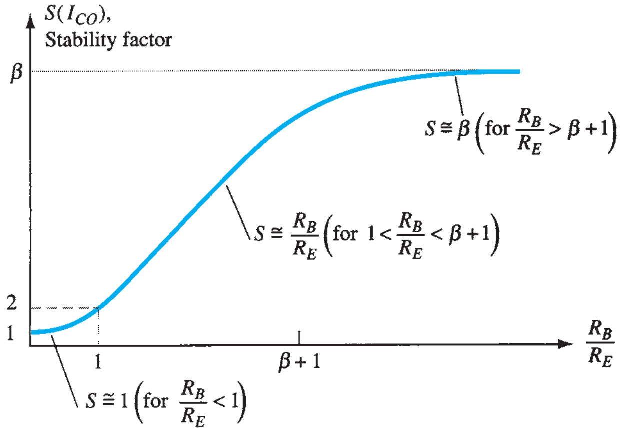


FIG. 4.99

Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the emitter-bias configuration.

Voltage-Divider Bias Configuration

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.100, for the voltage-divider bias configuration. For the network of Fig. 4.100, the equation for $S(I_{CO})$ is the following:

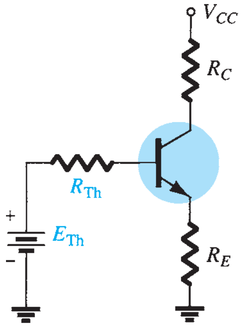


FIG. 4.100

Equivalent circuit for the voltage-divider configuration.

$$\boxed{S(I_{CO}) \cong \frac{\beta(1 + R_{Th}/R_E)}{\beta + R_{Th}/R_E}} \tag{4.98}$$

Note the similarities with Eq. (4.94), where it was determined that $S(I_{CO})$ had its lowest level and the network had its greatest stability when $R_E > R_B$. For Eq. (4.98), the corresponding condition is $R_E > R_{Th}$, or R_{Th}/R_E should be as small as possible. For the voltage-divider bias configuration, R_{Th} can be much less than the corresponding R_{Th} of the emitter-bias configuration and still have an effective design.

Feedback-Bias Configuration ($R_E = 0\ \Omega$)

In this case,

$$\boxed{S(I_{CO}) \cong \frac{\beta(1 + R_B/R_C)}{\beta + R_B/R_C}} \tag{4.99}$$

Because the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.101a, the equation for the base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$\boxed{I_C = \beta I_B + (\beta + 1)I_{CO}} \tag{4.100}$$

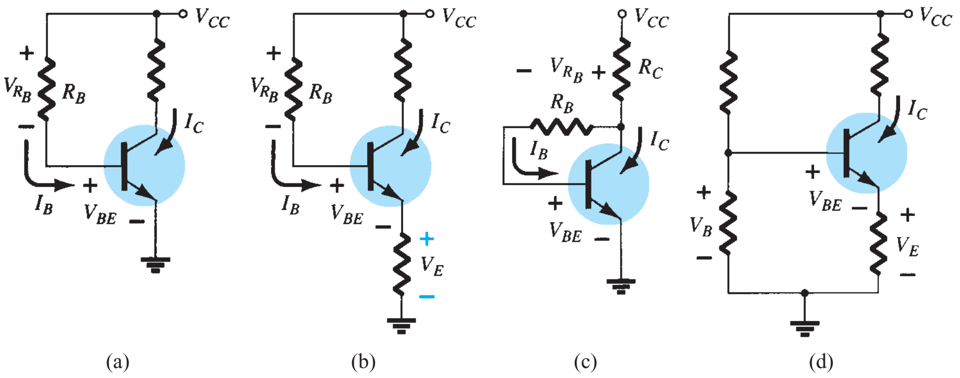


FIG. 4.101

Review of biasing managements and the stability factor $S(I_{CO})$.

If I_C as defined by Eq. (4.93) should increase due to an increase in I_{CO}, there is nothing in the equation for I_B that would attempt to offset this undesirable increase in current level (assuming V_{BE} remains constant). In other words, the level of I_C would continue to rise with temperature, with I_B maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.101b, however, an increase in I_C due to an increase in I_{CO} will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of I_B as determined by the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E\uparrow}{R_B} \tag{4.101}$$

A drop in I_B will have the effect of reducing the level of I_C through transistor action and thereby offset the tendency of I_C to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.101c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If I_C should increase due to an increase in temperature, the level of V_{R_C} will increase in the equation

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C}\uparrow}{R_B} \tag{4.102}$$

and the level of I_B will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant I_C begins to rise, the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.101d. If the condition $\beta R_E \gg 10R_2$ is satisfied, the voltage V_B will remain fairly constant for changing levels of I_C. The base-to-emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If I_C should increase, V_E will increase as described above, and for a constant V_B the voltage V_{BE} will drop. A drop in V_{BE} will establish a lower level of I_B, which will try to offset the increased level of I_C.

EXAMPLE 4.35 Calculate the stability factor and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.2 for the following emitter-bias arrangements:

a. $R_B/R_E = 250\ (R_B = 250R_E)$.
b. $R_B/R_E = 10\ (R_B = 10R_E)$.
c. $R_B/R_E = 0.01(R_E = 100R_B)$.

Solution:

a. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} = \frac{50(1 + 250)}{50 + 250} \cong \mathbf{41.83}$$

which begins to approach the level defined by $\beta = 50$.
The change in I_C is given by

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (41.83)(19.9\text{ nA}) \cong \mathbf{0.83\ \mu A}$$

b. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} = \frac{50(1 + 10)}{50 + 10} \cong \mathbf{9.17}$$

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (9.17)(19.9\text{ nA}) \cong \mathbf{0.18\ \mu A}$$

c. $$S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E} = \frac{50(1 + 0.01)}{50 + 0.01} \cong \mathbf{1.01}$$

which is certainly very close to the level of 1 forecast if $R_B/R_E \ll 1$.
We have

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = 1.01(19.9\text{ nA}) = \mathbf{20.1\ nA}$$

Example 4.35 reveals how lower and lower levels of I_{CO} for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in I_C is considerably different in a circuit having ideal stability ($S = 1$) from one having a stability factor of 41.83, the change in I_C is not that significant. For example, the amount of change in I_C from a dc bias current set at, say, 2 mA, would be from 2 mA to 2.00083 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of I_{CO} have had a very positive impact on the stability question.

$S(V_{BE})$

The stability factor $S(V_{BE})$ is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

Fixed-Bias Configuration

For the fixed-bias configuration:

$$\boxed{S(V_{BE}) \cong \frac{-\beta}{R_B}} \tag{4.103}$$

Emitter-Bias Configuration

For the emitter-bias configuration:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + R_B/R_E}} \tag{4.104}$$

Substituting the condition $\beta \gg R_B/R_E$ results in the following equation for $S(V_{BE})$:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E}} \tag{4.105}$$

which shows that the larger the resistance R_E, the lower is the stability factor and the more stable is the system.

Voltage-Divider Configuration

For the voltage-divider configuration:

$$\boxed{S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_{\mathrm{Th}}/R_E}} \tag{4.106}$$

Feedback-Bias Configuration

For the feedback-bias configuration:

$$\boxed{S(V_{BE}) = \frac{-\beta/R_C}{\beta + R_B/R_C}} \tag{4.107}$$

EXAMPLE 4.36 Determine the stability factor $S(V_{BE})$ and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.2 for the following bias arrangements.

a. Fixed-bias with $R_B = 240\text{ k}\Omega$ and $\beta = 100$.
b. Emitter-bias with $R_B = 240\text{ k}\Omega$, $R_E = 1\text{ k}\Omega$, and $\beta = 100$.
c. Emitter-bias with $R_B = 47\text{ k}\Omega$, $R_E = 4.7\text{ k}\Omega$, and $\beta = 100$.

Solution:

a. Eq. (4.103):

$$\begin{aligned} S(V_{BE}) &= -\frac{\beta}{R_B} \\ &= -\frac{100}{240\text{ k}\Omega} \\ &= \mathbf{-0.417 \times 10^{-3}} \end{aligned}$$

and

$$\begin{aligned} \Delta I_C &= [S(V_{BE})](\Delta V_{BE}) \\ &= (-0.417 \times 10^{-3})(0.48\text{ V} - 0.65\text{ V}) \\ &= (-0.417 \times 10^{-3})(-0.17\text{ V}) \\ &= \mathbf{70.9\ \mu A} \end{aligned}$$

b. In this case, $\beta = 100$ and $R_B/R_E = 240$. The condition $\beta \gg R_B/R_E$ is not satisfied, negating the use of Eq. (4.105) and requiring the use of Eq. (4.104).

Eq. (4.104):

$$\begin{aligned} S(V_{BE}) &= \frac{-\beta/R_E}{\beta + R_B/R_E} \\ &= \frac{-(100)/(1\text{ k}\Omega)}{100 + (240\text{ k}\Omega/1\text{ k}\Omega)} = \frac{-0.1}{100 + 240} \\ &= \mathbf{-0.294 \times 10^{-3}} \end{aligned}$$

which is about 30% less than the fixed-bias value due to the additional R_E term in the denominator of the $S(V_{BE})$ equation. We have

$$\begin{aligned} \Delta I_C &= [S(V_{BE})](\Delta V_{BE}) \\ &= (-0.294 \times 10^{-3})(-0.17\text{ V}) \\ &\cong \mathbf{50\ \mu A} \end{aligned}$$

c. In this case,

$$\beta = 100 \gg \frac{R_B}{R_E} = \frac{47\text{ k}\Omega}{4.7\text{ k}\Omega} = 10 \quad (\textit{satisfied})$$

Eq. (4.105):
$$S(V_{BE}) = -\frac{1}{R_E}$$
$$= -\frac{1}{4.7\ \text{k}\Omega}$$
$$= \mathbf{-0.212 \times 10^{-3}}$$

and
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$
$$= (-0.212 \times 10^{-3})(-0.17\ \text{V})$$
$$= \mathbf{36.04\ \mu A}$$

In Example 4.36, the increase of 70.9 μA will have some impact on the level of I_{C_Q}. For a situation where $I_{C_Q} = 2$ mA, the resulting collector current increases to a 3.5% increase.

$$I_{C_Q} = 2\ \text{mA} + 70.9\ \mu\text{A}$$
$$= 2.0709\ \text{mA}$$

For the voltage-divider configuration, the level of R_B will be changed to R_{Th} in Eq. (4.104) (as defined by Fig. 4.100). In Example 4.36, the use of $R_B = 47\ \text{k}\Omega$ is a questionable design. However, R_{Th} for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for $S(V_{BE})$ for the feedback network will be similar to that of Eq. (4.104) with R_E replaced by R_C.

$S(\beta)$

The last stability factor to be investigated is that of $S(\beta)$. The mathematical development is more complex than that encountered for $S(I_{CO})$ and $S(V_{BE})$, as suggested by some of the following equations.

Fixed-Bias Configuration

For the fixed-bias configuration

$$\boxed{S(\beta) = \frac{I_{C_1}}{\beta_1}} \qquad \textbf{(4.108)}$$

Emitter-Bias Configuration

For the emitter-bias configuration

$$\boxed{S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(\beta_2 + R_B/R_E)}} \qquad \textbf{(4.109)}$$

The notation I_{C_1} and β_1 is used to define their values under one set of network conditions, whereas the notation β_2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

EXAMPLE 4.37 Determine I_{C_Q} at a temperature of 100°C if $I_{C_Q} = 2$ mA at 25°C for the emitter-bias configuration. Use the transistor described by Table 4.2, where $\beta_1 = 50$ and $\beta_2 = 80$, and a resistance ratio R_B/R_E of 20.

Solution:

Eq. (4.109):
$$S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$
$$= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050}$$
$$= \mathbf{8.32 \times 10^{-6}}$$

and
$$\begin{aligned}\Delta I_C &= [S(\beta)][\Delta\beta]\\ &= (8.32 \times 10^{-6})(30)\\ &\cong \mathbf{0.25\ mA}\end{aligned}$$

In conclusion, therefore, the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

Voltage-Divider Bias Configuration

For the voltage-divider bias configuration

$$\boxed{S(\beta) = \frac{I_{C_1}(1 + R_{\text{Th}}/R_E)}{\beta_1(\beta_2 + R_{\text{Th}}/R_E)}} \qquad \textbf{(4.110)}$$

Feedback-bias Configuration

For the collector feedback-bias configuration

$$\boxed{S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + \beta_2 R_C)}} \qquad \textbf{(4.111)}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation for each configuration

$$\boxed{\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta} \qquad \textbf{(4.112)}$$

The equation may initially appear quite complex, but note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in I_C from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.78) becomes

$$\boxed{\Delta I_C = \beta\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta} \qquad \textbf{(4.113)}$$

after substituting the stability factors as derived in this section. Let us now use Table 4.2 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\Delta I_{CO} = 20\text{ nA} - 0.1\text{ nA} = 19.9\text{ nA}$$
$$\Delta V_{BE} = 0.48\text{ V} - 0.65\text{ V} = -0.17\text{ V} \quad \text{(note the sign)}$$
and
$$\Delta\beta = 80 - 50 = 30$$

Starting with a collector current of 2 mA with an R_B of 240 kΩ, we obtain the resulting change in I_C due to an increase in temperature of 75°C as follows:

$$\begin{aligned}\Delta I_C &= (50)(19.9\text{ nA}) - \frac{50}{240\text{ k}\Omega}(-0.17\text{ V}) + \frac{2\text{ mA}}{50}(30)\\ &= 1\ \mu\text{A} + 35.42\ \mu\text{A} + 1200\ \mu\text{A}\\ &= 1.236\text{ mA}\end{aligned}$$

which is a significant change due primarily to the change in β. The collector current has increased from 2 mA to 3.236 mA, but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration is employed with a ratio $R_{\text{Th}}/R_E = 2$ and $R_E = 4.7\text{ k}\Omega$, then

$$S(I_{CO}) = 2.89, \quad S(V_{BE}) = -0.2 \times 10^{-3}, \quad S(\beta) = 1.445 \times 10^{-6}$$

and
$$\begin{aligned}\Delta I_C &= (2.89)(19.9\text{ nA}) - 0.2 \times 10^{-3}(-0.17\text{ V}) + 1.445 \times 10^{-6}(30)\\ &= 57.51\text{ nA} + 34\ \mu\text{A} + 43.4\ \mu\text{A}\\ &= 0.077\text{ mA}\end{aligned}$$

The resulting collector current is 2.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case, $S(\beta)$ did not override the other two factors, and the effects of $S(V_{BE})$ and $S(I_{CO})$ were equally important. In fact, at higher temperatures, the effects of $S(I_{CO})$ and $S(V_{BE})$ will be greater than $S(\beta)$ for the device of Table 4.2. For temperatures below 25°C, I_C will decrease with increasingly negative temperature levels.

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques, which continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

General Conclusion:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

4.19 PRACTICAL APPLICATIONS

As with the diodes in Chapter 2, it would be virtually impossible to provide even a surface treatment of the broad areas of application of BJTs. However, a few applications are chosen here to demonstrate how different facets of the characteristics of BJTs are used to perform various functions.

BJT Diode Usage and Protective Capabilities

As you begin to scan complex networks you will often find transistors being used where all three terminals are not connected in the network—particularly the collector lead. In such cases it is most likely being used as a diode rather than a transistor. There are a number of reasons for such use, including the fact that it is cheaper to buy a large number of transistors rather than a smaller bundle and then pay separately for specific diodes. Also, in ICs the manufacturing process may be more direct to make additional transistors that introduce the diode construction sequence. Two examples of its use as a diode appear in Fig. 4.102. In Fig. 4.102a it is being used in a simple diode network. In Fig. 4.102b it is being used to establish a reference level.

Often times you will see a diode connected directly across a device as shown in Fig. 4.103 to simply ensure that the voltage across a device or system with the polarity shown cannot exceed the forward bias voltage of 0.7 V. In the reverse direction if the breakdown strength is sufficiently high it will simply appear as an open circuit. Again, however, only two terminals of the BJT are being employed.

The point to be made is that one should not assume that every BJT transistor in a network is being used for amplification or as a buffer between stages. The number of areas of application for BJTs beyond these areas is quite extensive.

Relay Driver

This application is in some ways a continuation of the discussion introduced for diodes about how the effects of inductive kick can be minimized through proper design. In Fig. 4.104a, a transistor is used to establish the current necessary to energize the relay in the

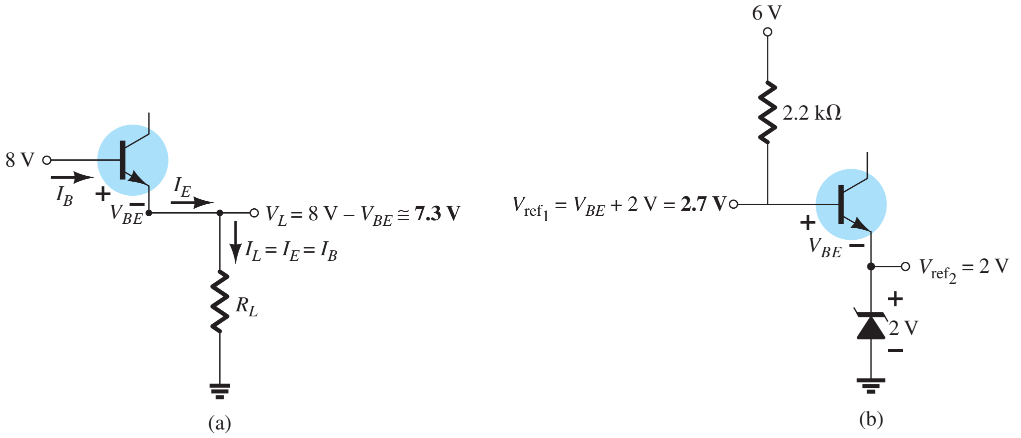

8 V
I_B
+
V_{BE}
–
I_E
$V_L = 8\text{ V} - V_{BE} \cong 7.3\text{ V}$
$I_L = I_E = I_B$
R_L
(a)
6 V
2.2 kΩ
$V_{\text{ref}_1} = V_{BE} + 2\text{ V} = 2.7\text{ V}$
+
V_{BE}
–
$V_{\text{ref}_2} = 2\text{ V}$
+
2 V
–
(b)

FIG. 4.102

BJT applications as a diode: (a) simple series diode circuit; (b) setting a reference level.

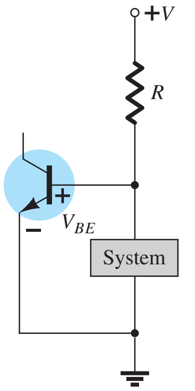


FIG. 4.103

Acting as a protective device.

collector circuit. With no input at the base of the transistor, the base current, collector current, and coil current are essentially 0 A, and the relay sits in the unenergized state (normally open, NO). However, when a positive pulse is applied to the base, the transistor turns on, establishing sufficient current through the coil of the electromagnet to close the relay. Problems can now develop when the signal is removed from the base to turn off the transistor and deenergize the relay. Ideally, the current through the coil and the transistor will quickly drop to zero, the arm of the relay will be released, and the relay will simply remain dormant until the next "on" signal. However, we know from our basic circuit courses that the current through a coil cannot change instantaneously, and, in fact, the more quickly it changes, the greater the induced voltage across the coil as defined by $v_L = L(di_L/dt)$. In this case, the rapidly changing current through the coil will develop a large voltage across the coil with the polarity shown in Fig. 4.104a, which will appear directly across the output of the transistor. The chances are likely that its magnitude will exceed the maximum ratings of the transistor, and the semiconductor device will be permanently damaged. The voltage across the coil will not remain at its highest switching level but will oscillate as shown until its level drops to zero as the system settles down.

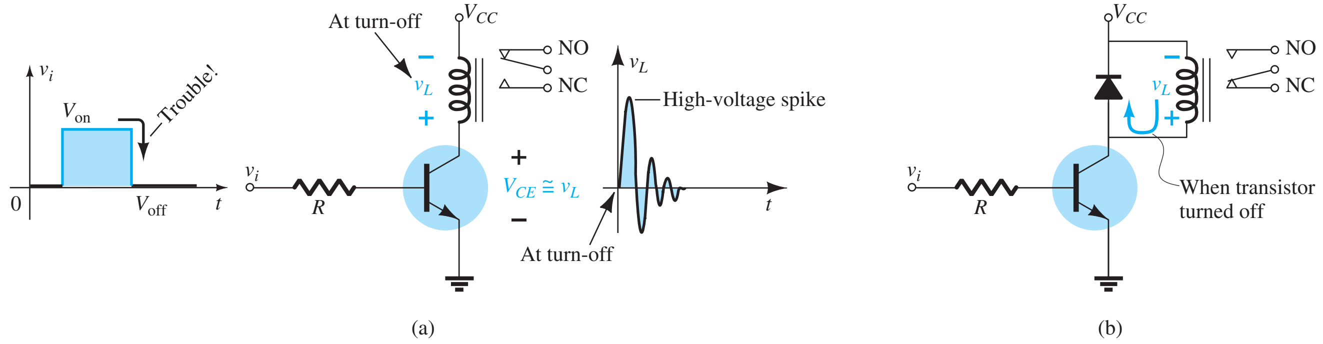


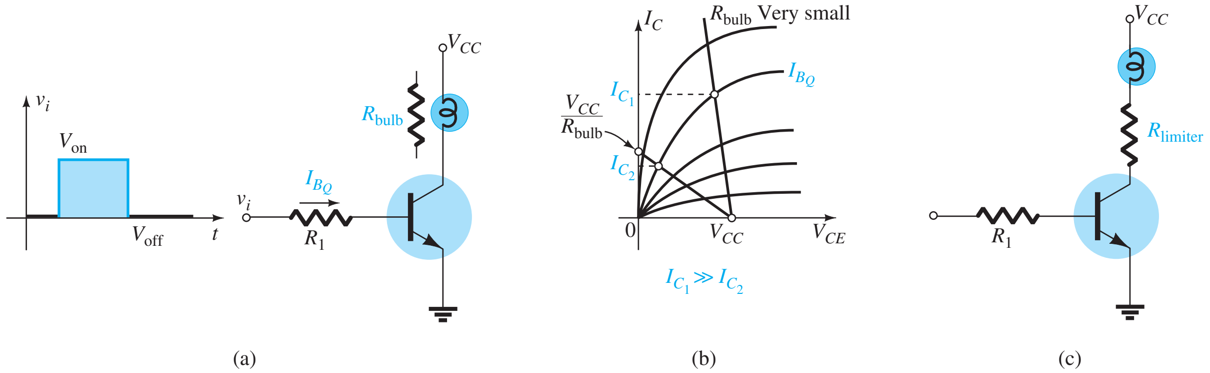
FIG. 4.104

Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.

This destructive action can be subdued by placing a diode across the coil as shown in Fig. 4.104b. During the "on" state of the transistor, the diode is back-biased; it sits like an open circuit and doesn't affect a thing. However, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its "on" state. The current through the inductor established during the "on" state of the transistor can then continue to flow through the diode, eliminating the severe change in current level. Because the inductive current is switched to the diode almost instantaneously after the "off" state is established, the diode must have a current rating to match the current through the inductor and the transistor when in the "on" state. Eventually, because of the resistive elements in the loop, including the resistance of the coil windings and the diode, the high-frequency (quickly oscillating) variation in voltage level across the coil will decay to zero, and the system will settle down.

Light Control

In Fig. 4.105a, a transistor is used as a switch to control the "on" and "off" states of the lightbulb in the collector branch of the network. When the switch is in the "on" position, we have a fixed-bias situation where the base-to-emitter voltage is at its 0.7-V level, and the base current is controlled by the resistor R_1 and the input impedance of the transistor. The current through the bulb will then be beta times the base current, and the bulb will light up. A problem can develop, however, if the bulb has not been on for a while. When a lightbulb is first turned on, its resistance is quite low, even though the resistance will increase rapidly the longer the bulb is on. This can cause a momentary high level of collector current, which could damage the bulb and the transistor over time. In Fig. 4.105b, for instance, the load line for the same network with a cold and a hot resistance for the bulb is included. Note that even though the base current is set by the base circuit, the intersection with the load line results in a higher current for the cold lightbulb. Any concern about the turn-on level can easily be corrected by inserting an additional small resistor in series with the lightbulb, as shown in Fig. 43.105c, just to ensure a limit on the initial surge in current when the bulb is first turned on.



(a) (b) (c)

FIG. 4.105

Using the transistor as a switch to control the on–off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

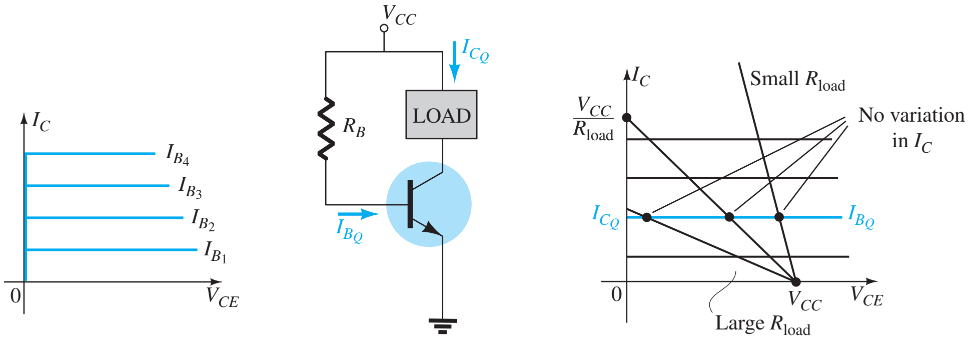
Maintaining a Fixed Load Current

If we assume that the characteristics of a transistor have the ideal appearance of Fig. 4.106a (constant beta throughout) a source, fairly independent of the applied load, can be constructed using the simple transistor configuration of Fig. 4.106b. The base current is fixed so no matter where the load line is, the load or collector current remains the same. In other words, the collector current is independent of the load in the collector circuit. However, because the actual characteristics are more like those in Fig. 4.106b, where beta will vary from point to point, and even though the base current may be fixed by the configuration, the beta will vary from point to point with the load intersection, and $I_C = I_L$ will vary—not characteristic of a good current source. Recall, however, that the voltage-divider configuration resulted in a low level of sensitivity to beta, so perhaps if that biasing arrangement is used, the current source equivalent is closer to reality. In fact, that is the case. If a biasing arrangement such as shown in Fig. 4.107 is employed, the sensitivity to changes in operating point due to varying loads is much less, and the collector current will remain fairly constant for changes in load resistance in the collector branch. In fact, the emitter voltage is determined by

$$V_E = V_B - 0.7\text{ V}$$

with the collector or load current determined by

$$I_C \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7\text{ V}}{R_E}$$


I_C
I_{B_4}
I_{B_3}
I_{B_2}
I_{B_1}
0
V_{CE}
V_{CC}
I_{CQ}
R_B
LOAD
I_{BQ}
I_C
Small R_{load}
$\frac{V_{CC}}{R_{\text{load}}}$
No variation in I_C
I_{CQ}
I_{BQ}
0
V_{CC}
V_{CE}
Large R_{load}

(a) (b) (c)

FIG. 4.106

Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why I_C remains constant.

Using Fig. 4.107, we can describe the improved stability by examining the case where I_C may be trying to rise for any number of reasons. The result is that $I_E = I_C$ will also rise and the voltage $V_{R_E} = I_E R_E$ will increase. However, if we assume V_B to be fixed (a good assumption because its level is determined by two fixed resistors and a voltage source), the base-to-emitter voltage $V_{B_E} = V_B - V_{R_E}$ will drop. A drop in V_{BE} will cause I_B and therefore $I_C (= \beta I_B)$ to drop. The result is a situation where any tendency for I_C to increase will be met with a network reaction that will work against the change to stabilize the system.

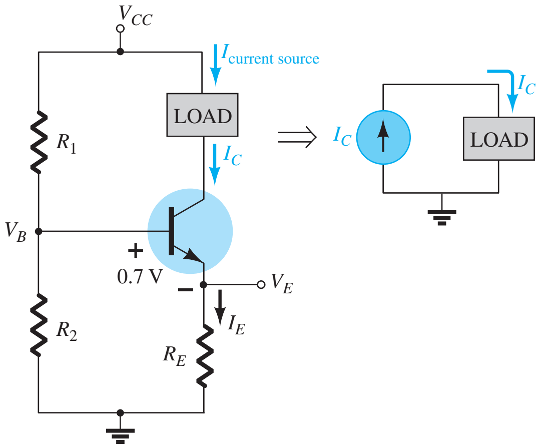

V_{CC}
$I_{\text{current source}}$
LOAD
R_1
I_C
V_B
+
0.7 V
−
V_E
R_2
I_E
R_E
I_C
I_C
LOAD

FIG. 4.107

Network establishing a fairly constant current source due to its reduced sensitivity to changes in beta.

Alarm System with a CCS

An alarm system with a constant-current source of the type just introduced appears in Fig. 4.108. Because $\beta R_E = (100)(1\text{ k}\Omega) = 100\text{ k}\Omega$ is much greater than R_1, we can use the approximate approach and find the voltage V_{R_1},

$$V_{R_1} = \frac{2\text{ k}\Omega(16\text{ V})}{2\text{ k}\Omega + 4.7\text{ k}\Omega} = 4.78\text{ V}$$

and then the voltage across R_E,

$$V_{R_E} = V_{R_1} - 0.7\text{ V} = 4.78\text{ V} - 0.7\text{ V} = 4.08\text{ V}$$

and finally the emitter and collector current,

$$I_E = \frac{V_{R_E}}{R_E} = \frac{4.08\text{ V}}{1\text{ k}\Omega} = 4.08\text{ mA} \cong 4\text{ mA} = I_C$$

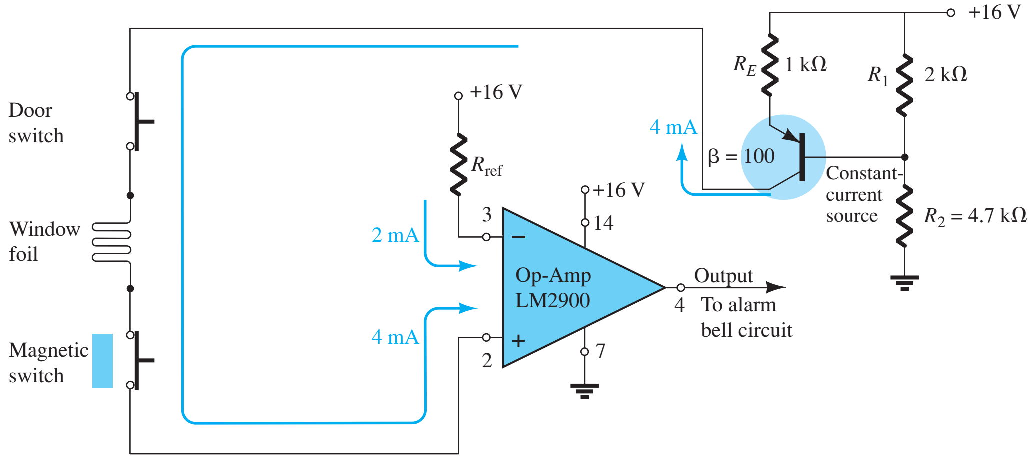
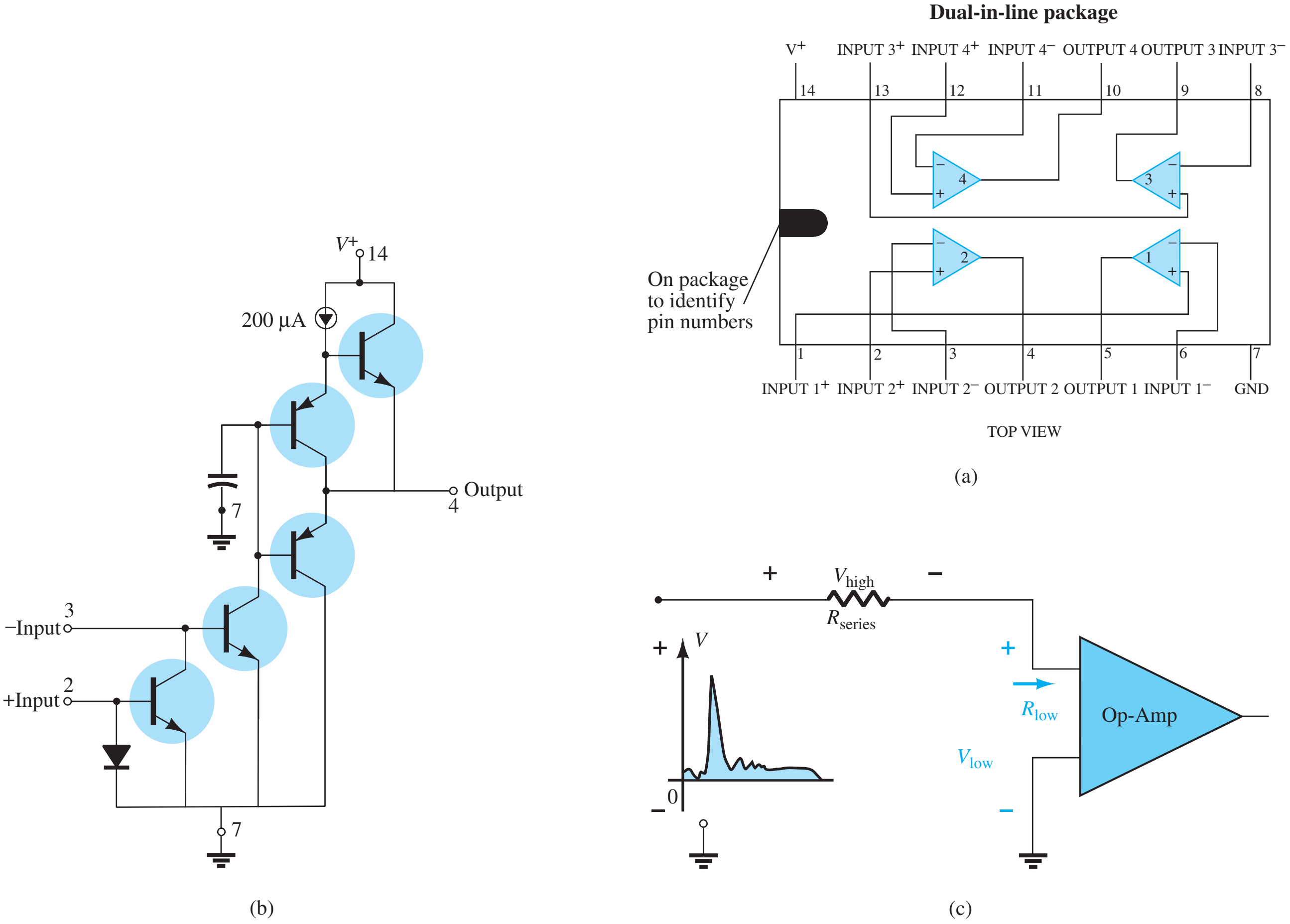

Door switch
Window foil
Magnetic switch
+16 V
R_{ref}
2 mA
4 mA
3
2
+16 V
14
7
Op-Amp LM2900
Output
4 To alarm bell circuit
+16 V
R_E 1 kΩ
R_1 2 kΩ
4 mA
β = 100
Constant-current source
R_2 = 4.7 kΩ

FIG. 4.108
An alarm system with a constant-current source and an op-amp comparator.

Because the collector current is the current through the circuit, the 4-mA current will remain fairly constant for slight variations in network loading. Note that the current passes through a series of sensor elements and finally into an op-amp designed to compare the 4-mA level with the set level of 2 mA. (Although the op-amp may be a new device to you, it will be discussed in detail in Chapter 10—you will not need to know the details of its behavior for this application.)

The LM2900 operational amplifier of Fig. 4.108 is one of four found in the dual-in-line integrated circuit package appearing in Fig. 4.109a. Pins 2, 3, 4, 7, and 14 were used


Dual-in-line package
V+
INPUT 3+
INPUT 4+
INPUT 4−
OUTPUT 4
OUTPUT 3
INPUT 3−
14
13
12
11
10
9
8
On package to identify pin numbers
1
2
3
4
5
6
7
INPUT 1+
INPUT 2+
INPUT 2−
OUTPUT 2
OUTPUT 1
INPUT 1−
GND
TOP VIEW
V+ 14
200 µA
7
−Input 3
+Input 2
Output 4
7
+
V_{high}
−
R_{series}
+
V
0
−
+
R_{low}
V_{low}
−
Op-Amp

(a)

(b)

(c)

FIG. 4.109
LM2900 operational amplifier: (a) dual-in-line package (DIP); (b) components; (c) impact of low-input impedance.

for the design of Fig. 4.108. For the sake of interest only, note in Fig. 4.109b the number of elements required to establish the desired terminal characteristics for the op-amp—as mentioned earlier, the details of its internal operation are left for another time. The 2 mA at terminal 3 of the op-amp is a *reference* current established by the 16-V source and R_{ref} at the negative side of the op-amp input. The 2-mA current level is required as a level against which the 4-mA current of the network is to be compared. As long as the 4-mA current on the positive input to the op-amp remains constant, the op-amp will provide a "high" output voltage, exceeding 13.5 V, with a typical level of 14.2 V (according to the specification sheets for the op-amp). However, if the sensor current drops from 4 mA to a level below 2 mA, the op-amp will respond with a "low" output voltage, typically about 0.1 V. The output of the op-amp will then signal the alarm circuit about the disturbance. Note from the above that it is not necessary for the sensor current to drop all the way down to 0 mA to signal the alarm circuit. Only a variation around the reference level that appears unusual is required—a good alarm feature.

One very important characteristic of this particular op-amp is the low-input impedance as shown in Fig. 4.109c. This feature is important because one does not want alarm circuits reacting to every voltage spike or turbulence that comes down the line because of some external switching action or outside forces such as lightning. In Fig. 4.109c, for instance, if a high-voltage spike should appear at the input to the series configuration, most of the voltage will appear across the series resistor rather than the op-amp—thus preventing a false output and an activation of the alarm.

Logic Gates

In this application we will expand on the coverage of transistor switching networks in Section 4.15. To review, the collector-to-emitter impedance of a transistor is quite low near or at saturation and large near or at cutoff. For instance, the load line defines *saturation* as the point where the current is quite high and the collector-to-emitter voltage quite low as shown in Fig. 4.110. The resulting resistance, defined by $R_{\text{sat}} = \dfrac{V_{CE_{\text{sat}}}(\text{low})}{I_{C_{\text{sat}}}(\text{high})}$, is quite low and is often approximated as a short circuit. At *cutoff*, the current is relatively low and the voltage near its maximum value as shown in Fig. 4.110, resulting in a very high impedance between the collector and emitter terminal, which is often approximated by an open circuit.

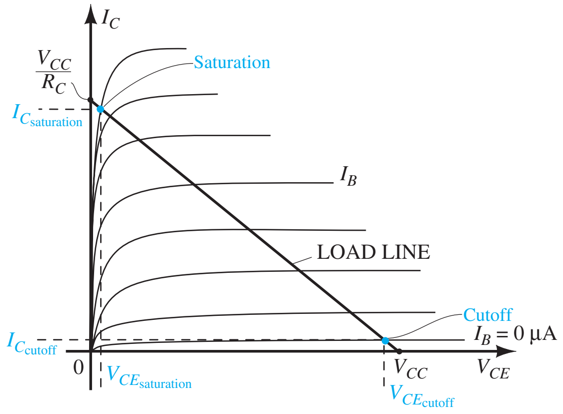
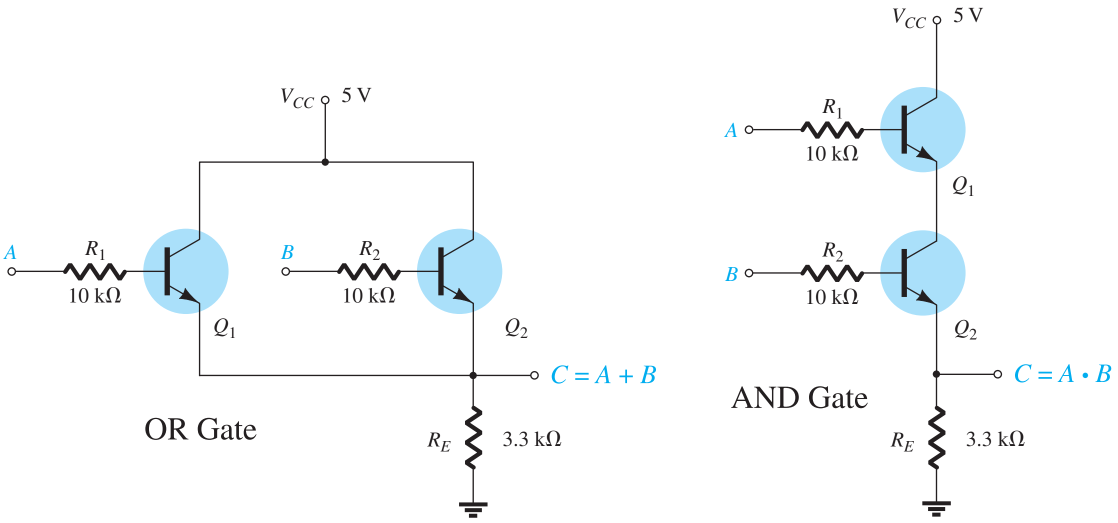


FIG. 4.110
Points of operation for a BJT logic gate.

The above impedance levels established by "on" and "off" transistors make it relatively easy to understand the operation of the logic gates of Fig. 4.111. Because there are two inputs to each gate, there are four possible combinations of voltages at the input to the transistors. A 1, or "on," state is defined by a high voltage at the base terminal to turn the transistor on. A 0, or "off," state is defined by 0 V at the base, ensuring that transistor is off. If both *A* and *B* of the OR gate of Fig. 4.111a have a low or 0-V input, both transistors are off (cutoff), and the impedance between the collector and the emitter of each transistor can be approximated by an open circuit. Mentally replacing both transistors by open circuits between the collector and the emitter will remove any connection between the applied bias of 5 V and the output. The result is zero current through each transistor and through the 3.3-kΩ resistor. The output voltage is therefore 0 V, or "low"—a 0 state. On the other hand, if transistor Q_1 is on and Q_2 is off due to a positive voltage at the base of Q_1 and 0 V at the base of Q_2, then the short-circuit equivalent between the collector and emitter for transistor Q_1 can be applied, and the voltage at the output is 5 V, or "high"—a 1 state. Finally, if both transistors are turned on by a positive voltage applied to the base of each, they will both ensure that the output voltage is 5 V, or "high"—a 1 state. The operation of the OR gate is properly defined: an output if either input terminal has applied turn-on voltage or if both are in the "on" state. A 0 state exists only if both do not have a 1 state at the input terminals.

The AND gate of Fig. 4.111b requires that the output be high only if both inputs have a turn-on voltage applied. If both are in the "on" state, a short-circuit equivalent can be used for the connection between the collector and the emitter of each transistor, providing a direct path from the applied 5-V source to the output—thereby establishing a high, or 1, state at the output terminal. If one or both transistors are off due to 0 V at the input terminal, an open circuit is placed in series with the path from the 5-V supply voltage to the output, and the output voltage is 0 V, or an "off" state.



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

1 = high
0 = low

(a)

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(b)

FIG. 4.111

BJT logic gates: (a) OR; (b) AND.

Voltage Level Indicator

The last application to be introduced in this section, the voltage level indicator, includes three of the elements introduced thus far: the transistor, the Zener diode, and the LED. The voltage level indicator is a relatively simple network using a green LED to indicate when the source voltage is close to its monitoring level of 9 V. In Fig. 4.112 the potentiometer is set to establish 5.4 V at the point indicated. The result is sufficient voltage to turn on both the 4.7-V Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED.

Once the potentiometer is set, the LED will emit its green light as long as the supply voltage is near 9 V. However, if the terminal voltage of the 9-V battery should decrease, the voltage set up by the voltage-divider network may drop to 5 V from 5.4 V. At 5 V there is insufficient voltage to turn on both the Zener and the transistor, and the transistor will be in the "off" state. The LED will immediately turn off, revealing that the supply voltage has dropped below 9 V or that the power source has been disconnected.

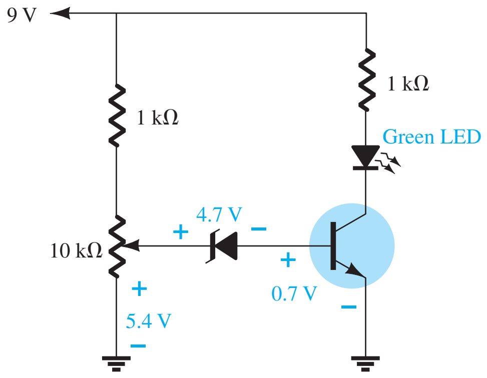


FIG. 4.112
Voltage level indicator.

4.20 SUMMARY

Important Conclusions and Concepts

1. No matter what type of configuration a transistor is used in, the basic relationships between the currents are **always the same**, and the base-to-emitter voltage is the **threshold value** if the transistor is in the "on" state.
2. The operating point defines where the transistor will operate on its characteristic curves under **dc conditions**. For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.
3. For most configurations the dc analysis begins with a determination of the **base current**.
4. For the dc analysis of a transistor network, all capacitors are replaced by an **open-circuit equivalent**.
5. The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable due its **sensitivity to beta** at the operating point.
6. Determining the saturation (maximum) collector current for any configuration can usually be done quite easily if an **imaginary short circuit** is superimposed between the collector and emitter terminals of the transistor. The resulting current through the short is then the saturation current.
7. The equation for the load line of a transistor network can be found by applying **Kirchhoff's voltage law** to the output or collector network. The Q-point is then determined by finding the **intersection** between the base current and the load line drawn on the device characteristics.
8. The emitter-stabilized biasing arrangement is less sensitive to changes in beta—providing more stability for the network. Keep in mind, however, that any resistance in the emitter leg is "seen" at the base of the transistor as a much **larger resistor**, a fact that will reduce the base current of the configuration.
9. The voltage-divider bias configuration is probably the most common of all the configurations. Its popularity is due primarily to its **low sensitivity** to changes in beta from one transistor to another of the same lot (with the same transistor label). The exact analysis can be applied to any configuration, but the approximate one can be applied only if the reflected emitter resistance as seen at the base **is much larger** than the lower resistor of the voltage-divider bias arrangement connected to the base of the transistor.

10. When analyzing the dc bias with a voltage feedback configuration, be sure to remember that ***both*** the emitter resistor and the collector resistor are reflected back to the base circuit by beta. The least sensitivity to beta is obtained when the reflected resistance is much larger than the feedback resistor between the base and the collector.
11. For the common-base configuration the **emitter current is normally determined first** due to the presence of the base-to-emitter junction in the same loop. Then the fact that the emitter and the collector currents are essentially of the same magnitude is employed.
12. A clear understanding of the procedure employed to analyze a dc transistor network will usually permit a design of the same configuration with a minimum of difficulty and confusion. Simply start with those relationships that **minimize the number of unknowns** and then proceed to make some decisions about the unknown elements of the network.
13. In a switching configuration, a transistor quickly moves between **saturation and cutoff, or vice versa**. Essentially, the impedance between collector and emitter can be approximated as a short circuit for saturation and an open circuit for cutoff.
14. When checking the operation of a dc transistor network, first check that the base-to-emitter voltage is very close to **0.7 V** and that the collector-to-emitter voltage is between **25% and 75% of the applied voltage V_{CC}**.
15. The analysis of *pnp* configurations is exactly the same as that applied to *npn* transistors with the exception that current directions will **reverse** and voltages will have the **opposite** polarities.
16. Beta is very sensitive to **temperature**, and V_{BE} **decreases** about 2.5 mV (0.0025 V) for each 1° increase in temperature on a Celsius scale. The reverse saturation current typically **doubles** for every 10° increase in Celsius temperature.
17. Keep in mind that networks that are the **most stable** and least sensitive to temperature changes have the **smallest stability factors**.

Equations

$$V_{BE} \cong 0.7\text{ V}, \qquad I_E = (\beta + 1)I_B \cong I_C, \qquad I_C = \beta I_B$$

Fixed bias:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \qquad I_C = \beta I_B$$

Emitter stabilized:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \qquad R_i = (\beta + 1)R_E$$

Voltage-divider bias:

$$\textit{Exact:}\quad R_{\text{Th}} = R_1 \| R_2, \qquad E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

$$\textit{Approximate: Test}\quad \beta R_E \geq 10R_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad V_E = V_B - V_{BE}, \qquad I_E = \frac{V_E}{R_E} \cong I_C$$

DC bias with voltage feedback:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}, \qquad I'_C \cong I_C \cong I_E$$

Common base:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}, \qquad I_C \cong I_E$$

Transistor switching networks:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}, \qquad I_B > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}}, \qquad R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}, \qquad t_{\text{on}} = t_r + t_d, \qquad t_{\text{off}} = t_s + t_f$$

Stability factors:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}, \qquad S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}, \qquad S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$S(I_{CO})$:

$$\textit{Fixed bias:} \quad S(I_{CO}) \cong \beta$$

$$\textit{Emitter bias:} \quad S(I_{CO}) = \frac{\beta(1 + R_B/R_E)^*}{\beta + R_B/R_E}$$

*Voltage-divider bias: Change R_B to R_{Th} in above equation.

*Feedback bias: Change R_E to R_C in above equation.

$S(V_{BE})$:

$$\textit{Fixed bias:} \quad S(V_{BE}) = -\frac{\beta}{R_B}$$

$$\textit{Emitter bias:} \quad S(V_{BE}) = \frac{-\beta/R_E^{\dagger}}{\beta + R_B/R_E}$$

†Voltage-divider bias: Change R_B to R_{Th} in above equation.

†Feedback bias: Change R_E to R_C in above equation.

$S(\beta)$:

$$\textit{Fixed bias:} \quad S(\beta) = \frac{I_{C_1}}{\beta_1}$$

$$\textit{Emitter bias:} \quad S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)^{\ddagger}}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

‡Voltage-divider bias: Change R_B to R_{Th} in above equation.

‡Feedback bias: Change R_E to R_C in above equation.

4.21 COMPUTER ANALYSIS

Cadence OrCAD

Voltage-Divider Configuration The results of Example 4.8 will now be verified using Cadence OrCAD. Using methods described in detail in the previous chapters, we can construct the network of Fig. 4.113. Recall from the previous chapter that the transistor is found under the **EVAL** library, the dc source under the **SOURCE** library, and the resistors under the **ANALOG** library. The capacitor has not been called up earlier but can also be found in the **ANALOG** library. For the transistor, the list of available transistors can be found in the **EVAL** library.

The value of beta is changed to 140 to match Example 4.8 by first clicking on the transistor symbol on the screen. It will then appear boxed in red to reveal it is in an active status. Then proceed with **Edit-PSpice Model**, and the **PSpice Model Editor Demo** dialog box will appear in which **Bf** can be changed to **140**. As you try to leave the dialog box the **Model Editor/16.3** dialog box will appear asking if you want to save the changes in the network library. Once they are saved, the screen will automatically return with beta set at its new value.

The analysis can then proceed by selecting the **New simulation profile** key (looks like a printout with an asterisk in the top left corner) to obtain the **New Simulation** dialog box. Insert Fig. 4.113 and select **Create**. The **Simulation Settings** dialog box will appear in which **Bias Point** is selected under the **Analysis Type** heading. An **OK**, and the system is ready for simulation.

Proceed by selecting the **Run PSpice** key (white arrow in green background) or the sequence **PSpice–Run**. The bias voltages will appear as shown in Fig. 4.113 if the **V** option selected. The collector-to-emitter voltage is 13.19 V − 1.333 V = 11.857 V versus 12.22 V of Example 4.8. The difference is primarily due to the fact that we are using an actual transistor whose parameters are very sensitive to the operating conditions. Also recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

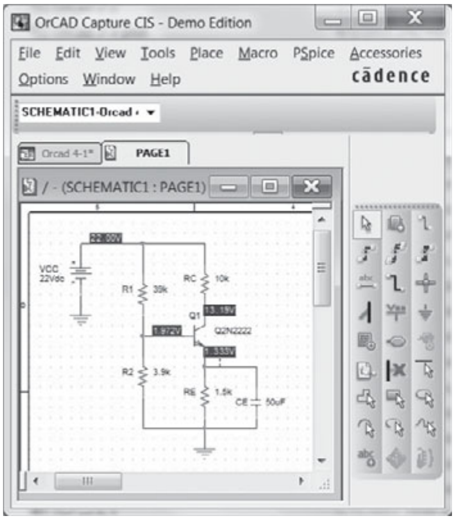

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories
Options Window Help
cādence
SCHEMATIC1-Orcad
Orcad 4-1*
PAGE1
/ - (SCHEMATIC1 : PAGE1)
22.00V
VCC
22Vdc
R1 39k
RC 10k
13.19V
Q1
1.972V
Q2N2222
1.333V
R2 3.9k
RE 1.5k
CE 50uF

FIG. 4.113

Applying PSpice Windows to the voltage-divider configuration of Example 4.8.

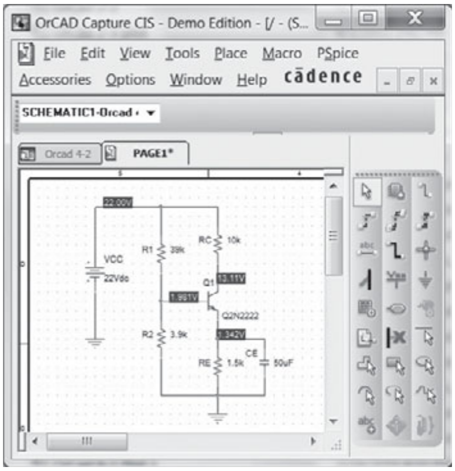

OrCAD Capture CIS - Demo Edition - [/ - (S...
File Edit View Tools Place Macro PSpice
Accessories Options Window Help
cādence
SCHEMATIC1-Orcad
Orcad 4-2
PAGE1*
22.00V
VCC
22Vdc
R1 39k
RC 10k
13.11V
Q1
1.991V
Q2N2222
1.342V
R2 3.9k
RE 1.5k
CE 50uF

FIG. 4.114

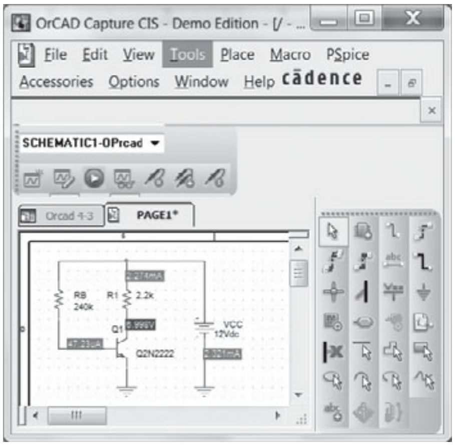
Response obtained after changing β from 140 to 255.9 for the network of Fig. 4.113.

Because the voltage-divider network has a low sensitivity to changes in beta, let us return to the transistor specifications and replace beta by the default value of 255.9 and see how the results change. The result is the printout of Fig. 4.114, with voltage levels very close to those obtained in Fig. 4.113.

Note the distinct advantage of having the network set up in memory. Any parameter can now be changed and a new solution obtained almost instantaneously—a wonderful advantage in the design process.

Fixed-Bias Configuration Although the voltage-divider bias network is relatively insensitive to changes in the beta value, the fixed-bias configuration is very sensitive to beta variations. This can be demonstrated by setting up the fixed-bias configuration of Example 4.1 using a beta of 50 for the first run. The results of Fig. 4.115 demonstrate that the design is a fairly good one. The collector or collector-to-emitter voltage is appropriate for the applied source. The resulting base and collector currents are fairly common for a good design.

However, if we now go back to the transistor specifications and change beta back to the default value of 255.9, we obtain the results of Fig. 4.116. The collector voltage is now only 0.113 V at a current of 5.4 mA—a terrible operating point. Any applied ac signal would be severely truncated due to the low collector voltage.


OrCAD Capture CIS - Demo Edition - [/ - ...
File Edit View Tools Place Macro PSpice
Accessories Options Window Help
cādence
SCHEMATIC1-OPrcad
Orcad 4-3
PAGE1*
2.274mA
RB
240k
R1 2.2k
Q1
47.23uA
Q2N2222
VCC
12Vdc
2.321mA

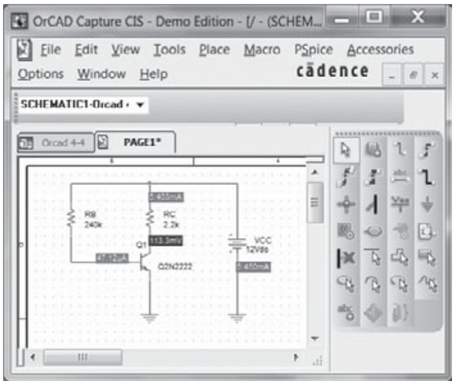

OrCAD Capture CIS - Demo Edition - [/ - (SCHEM...
File Edit View Tools Place Macro PSpice Accessories
Options Window Help
cādence
SCHEMATIC1-Orcad
Orcad 4-4
PAGE1*
RB
240k
RC
2.2k
113.3mV
Q1
Q2N2222
VCC
12Vdc

FIG. 4.115

Fixed-bias configuration with a β of 50.

FIG. 4.116

Network of Fig. 4.115 with a β of 255.9.

Clearly, therefore, from the preceding analysis, the voltage-divider configuration is the preferred design if there is any concern about beta variations.

Multisim

Multisim will now be applied to the fixed-bias network of Example 4.4 to provide an opportunity to review the transistor options internal to the software package and to compare results with the handwritten approximate solution.

All the components of Fig. 4.117 except the transistor can be entered using the procedure described in Chapter 2. Transistors are available through the **Transistor** key pad, which is the fourth option down on the **Component** toolbar. When it is selected, the **Select a Component** dialog box will appear, from which **BJT_NPN** is chosen. The result is a **Component** list, from which **2N2222A** can be selected. An **OK**, and the transistor will appear on the screen with the labels **Q1** and **2N2222A**. The label **Bf = 50** can be added by first selecting **Place** in the top toolbar followed by the **Text** option. Place the resulting marker in the area you want to place the text and click once more. The result is a blank space with a blinking marker for where the text will appear when entered. When finished, a second double-click, and the label is set. To move the label to the position shown in Fig. 4.117, simply click on the label to place the four small squares around the device. Then click it once more and drag it to the desired position. Release the clicker, and it is in place. Another click, and the four small markers will disappear.

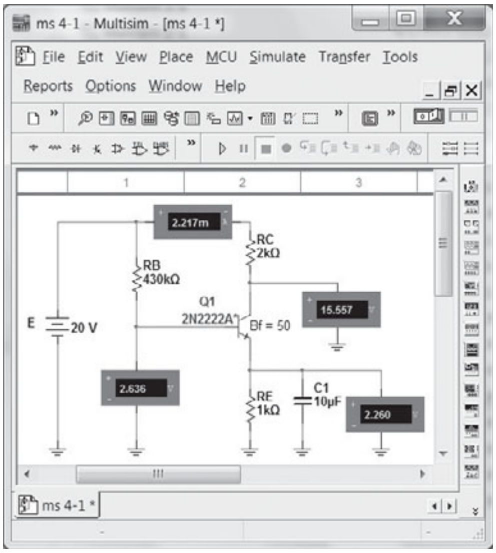

ms 4-1 - Multisim - [ms 4-1 *]
File Edit View Place MCU Simulate Transfer Tools
Reports Options Window Help
1
2
3
2.217m
RC
2kΩ
RB
430kΩ
Q1
2N2222A*
Bf = 50
15.557
E
20 V
2.636
RE
1kΩ
C1
10µF
2.260
ms 4-1 *

FIG. 4.117

Verifying the results of Example 4.4 using Multisim.

Even though the label may say **Bf = 50**, the transistor will still have the default parameters stored in memory. To change the parameters, the first step is to click on the device to establish the device boundaries. Then select **Edit**, followed by **Properties**, to obtain the **BJT_NPN** dialog box. If it is not already present, select **Value** and then **Edit Model**. The result will be the **Edit Model** dialog box in which β and I_s can be set to 50 and 1 nA, respectively. Then choose **Change Part Model** to obtain the **BJT_NPN** dialog box again and select **OK**. The transistor symbol on the screen will now have an asterisk to indicate that the default parameters have been modified. One more click to remove the four markers, and the transistor is set with its new parameters.

The indicators appearing in Fig. 4.117 were set as described in the previous chapter.

Finally, the network must be simulated using one of the methods described in Chapter 2. For this example the switch was set to the **1** position and then back to the **0** position after the Indicator values stabilized. The relatively low levels of current were partially responsible for the low level of this voltage.

The results are a close match with those of Example 4.4 with $I_C = 2.217$ mA, $V_B = 2.636$ V, $V_C = 15.557$ V, and $V_E = 2.26$ V.

The relatively few comments required here to permit the analysis of transistor networks is a clear indication that the breadth of analysis using Multisim can be expanded dramatically without having to learn a whole new set of rules—a very welcome characteristic of most technology software packages.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

4.3 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 4.118, determine:
  - **a.** I_{B_Q}.
  - **b.** I_{C_Q}.
  - **c.** V_{CE_Q}.
  - **d.** V_C.
  - **e.** V_B.
  - **f.** V_E.

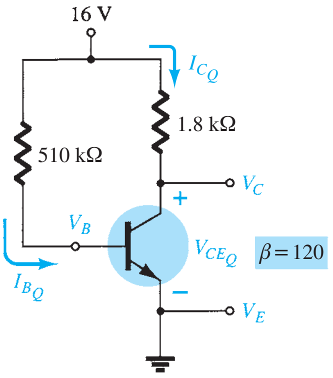

16 V
I_{C_Q}
1.8 kΩ
510 kΩ
V_C
+
V_B
V_{CE_Q}
$\beta = 120$
I_{B_Q}
–
V_E

FIG. 4.118
Problems 1, 4, 6, 7, 14, 65, 69, 71, and 75.

2. Given the information appearing in Fig. 4.119, determine:
  - **a.** I_C.
  - **b.** R_C.
  - **c.** R_B.
  - **d.** V_{CE}.

3. Given the information appearing in Fig. 4.120, determine:
  - **a.** I_C.
  - **b.** V_{CC}.
  - **c.** β.
  - **d.** R_B.

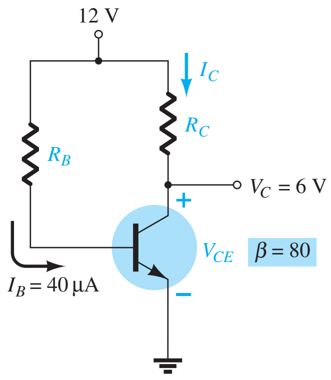

12 V
I_C
R_C
R_B
$V_C = 6$ V
+
V_{CE}
$\beta = 80$
$I_B = 40\ \mu$A
–

FIG. 4.119
Problem 2.

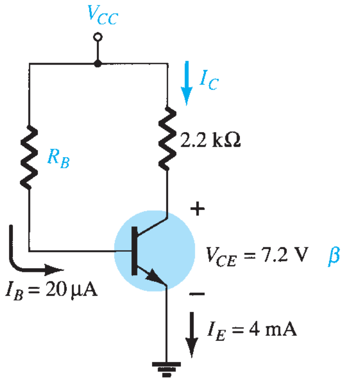

V_{CC}
I_C
2.2 kΩ
R_B
+
$V_{CE} = 7.2$ V
β
$I_B = 20\ \mu$A
–
$I_E = 4$ mA

FIG. 4.120
Problem 3.

4. Find the saturation current ($I_{C_{\text{sat}}}$) for the fixed-bias configuration of Fig. 4.118.

***5.** Given the BJT transistor characteristics of Fig. 4.121:

a. Draw a load line on the characteristics determined by $E = 21$ V and $R_C = 3$ kΩ for a fixed-bias configuration.

b. Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point.

c. What are the resulting values of I_{C_Q} and V_{CE_Q}?

d. What is the value of β at the operating point?

e. What is the value of α defined by the operating point?

f. What is the saturation current ($I_{C_{\text{sat}}}$) for the design?

g. Sketch the resulting fixed-bias configuration.

h. What is the dc power dissipated by the device at the operating point?

i. What is the power supplied by V_{CC}?

j. Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

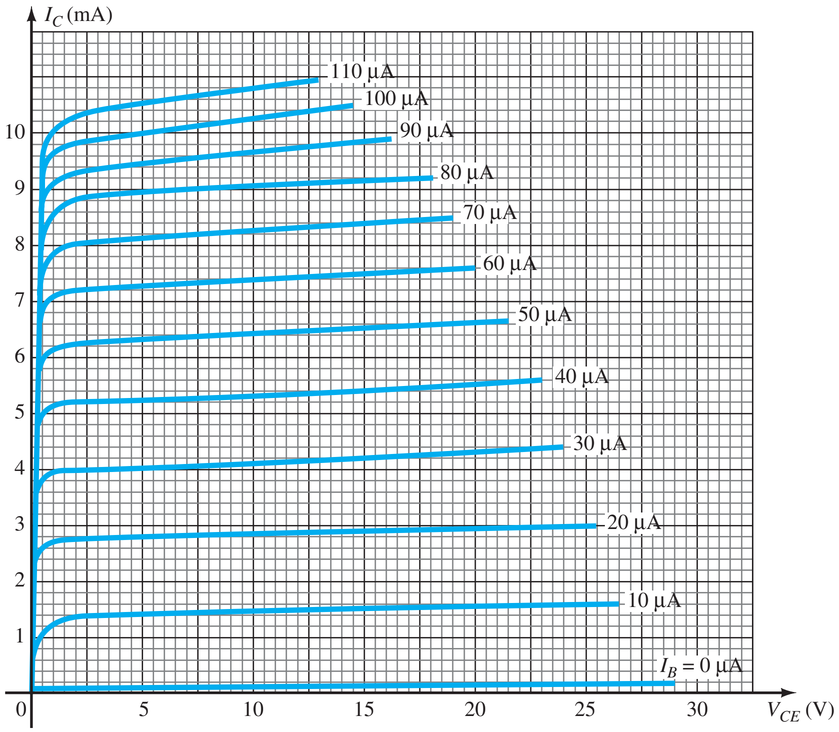


FIG. 4.121

Problems 5, 6, 9, 13, 24, 44, and 57.

6. a. Ignoring the provided value of $\beta_{(120)}$ draw the load line for the network of Fig. 4.118 on the characteristics of Fig. 4.121.

b. Find the Q-point and the resulting I_{C_Q} and V_{CE_Q}.

c. What is the beta value at this Q-point?

7. If the base resistor of Fig. 4.118 is increased to 910 kΩ, find the new Q-point and resulting values of I_{C_Q} and V_{CE_Q}.

4.4 Emitter-Bias Configuration

8. For the emitter-stabilized bias circuit of Fig. 4.122, determine:

a. I_{B_Q}.

b. I_{C_Q}.

c. V_{CE_Q}.

d. V_C.

e. V_B.

f. V_E.

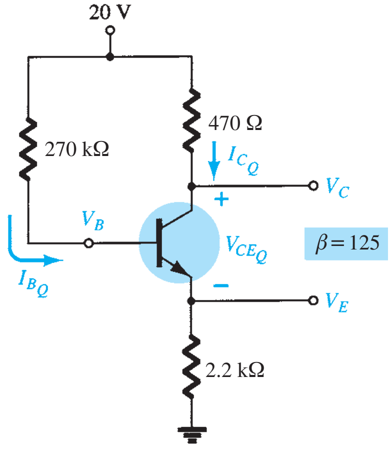

20 V
270 kΩ
470 Ω
I_{C_Q}
V_C
+
V_B
I_{B_Q}
V_{CE_Q}
$\beta = 125$
–
V_E
2.2 kΩ

FIG. 4.122
Problems 8, 9, 12, 14, 66, 69, 72, and 76.

9. **a.** Draw the load line for the network of Fig. 4.122 on the characteristics of Fig. 4.121 using β from problem 8 to find I_{B_Q}.
b. Find the Q-point and resulting values I_{C_Q} and V_{CE_Q}.
c. Find the value of β at the Q-point.
d. How does the value of part (c) compare with $\beta = 125$ in problem 8?
e. Why are the results for problem 9 different from those of problem 8?

10. Given the information provided in Fig. 4.123, determine:
a. R_C.
b. R_E.
c. R_B.
d. V_{CE}.
e. V_B.

11. Given the information provided in Fig. 4.124, determine:
a. β.
b. V_{CC}.
c. R_B.

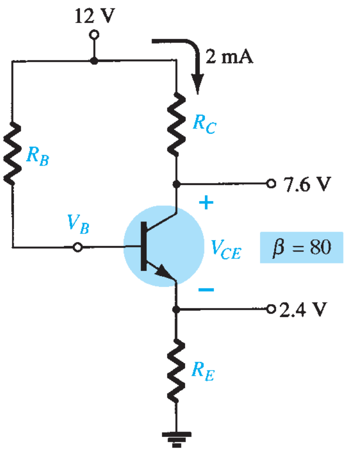

12 V
2 mA
R_C
R_B
7.6 V
+
V_B
V_{CE}
$\beta = 80$
–
2.4 V
R_E

FIG. 4.123
Problem 10.

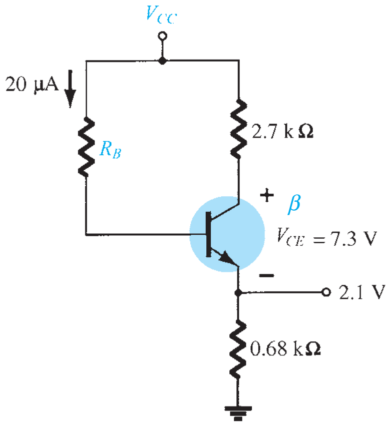

V_{CC}
20 μA
R_B
2.7 kΩ
+
β
$V_{CE} = 7.3$ V
–
2.1 V
0.68 kΩ

FIG. 4.124
Problem 11.

12. Determine the saturation current ($I_{C_{\text{sat}}}$) for the network of Fig. 4.122.

***13.** Using the characteristics of Fig. 4.121, determine the following for an emitter-bias configuration if a Q-point is defined at $I_{C_Q} = 4$ mA and $V_{CE_Q} = 10$ V.
a. R_C if $V_{CC} = 24$ V and $R_E = 1.2\ \text{k}\Omega$.
b. β at the operating point.
c. R_B.
d. Power dissipated by the transistor.
e. Power dissipated by the resistor R_C.

***14.** **a.** Determine I_C and V_{CE} for the network of Fig. 4.118.

b. Change β to 180 and determine the new value of I_C and V_{CE} for the network of Fig. 4.118.

c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}}\right| \times 100\%$$

d. Determine I_C and V_{CE} for the network of Fig. 4.122.

e. Change β to 187.5 and determine the new value of I_C and V_{CE} for the network of Fig. 4.122.

f. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part c})} - I_{C(\text{part d})}}{I_{C(\text{part d})}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part c})} - V_{CE(\text{part d})}}{V_{CE(\text{part d})}}\right| \times 100\%$$

g. In each of the above, the magnitude of β was increased 50%. Compare the percentage change in I_C and V_{CE} for each configuration, and comment on which seems to be less sensitive to changes in β.

4.5 Voltage-Divider Bias Configuration

15. For the voltage-divider bias configuration of Fig. 4.125, determine:

a. I_{B_Q}.

b. I_{C_Q}.

c. V_{CE_Q}.

d. V_C.

e. V_E.

f. V_B.

16. **a.** Repeat problem 15 for $\beta = 140$ using the general approach (not the approximate).

b. What levels are affected the most? Why?

17. Given the information provided in Fig. 4.126, determine:

a. I_C.

b. V_E.

c. V_B.

d. R_1.

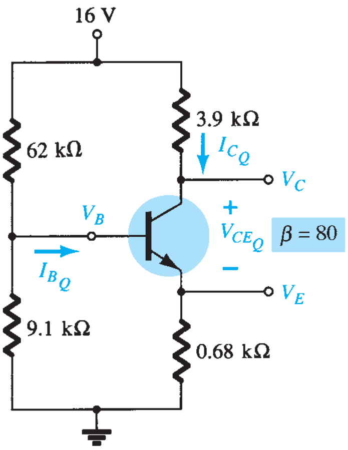


FIG. 4.125
Problems 15, 16, 20, 23, 25, 67, 69, 70, 73, and 77.

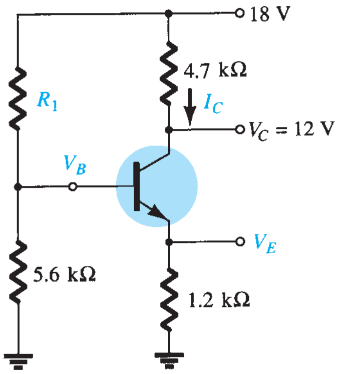


FIG. 4.126
Problems 17 and 19.

18. Given the information appearing in Fig. 4.127, determine:

a. I_C.

b. V_E.

c. V_{CC}.

d. V_{CE}.

e. V_B.

f. R_1.

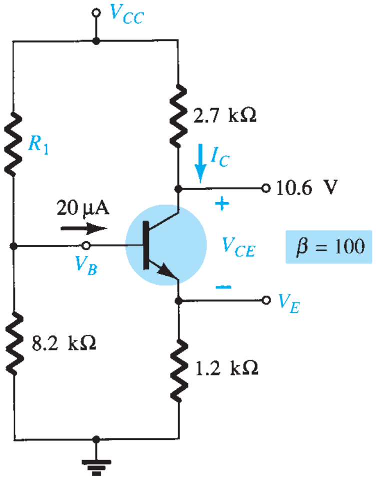


FIG. 4.127
Problem 18.

19. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.125.

20. **a.** Repeat problem 16 with $\beta = 140$ using the approximate approach and compare results.
b. Is the approximate approach valid?

***21.** Determine the following for the voltage-divider configuration of Fig. 4.128 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
a. I_C.
b. V_{CE}.
c. I_B.
d. V_E.
e. V_B.

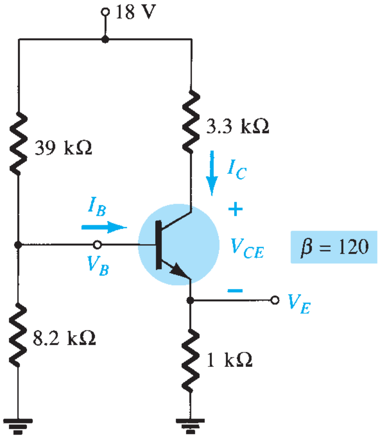


FIG. 4.128
Problems 21, 22, and 26.

***22.** Repeat Problem 21 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?

23. **a.** Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} for the network of Problem 15 (Fig. 4.125) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.
b. Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} using the exact approach.
c. Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.

***24.** **a.** Using the characteristics of Fig. 4.121, determine R_C and R_E for a voltage-divider network having a Q-point of $I_{C_Q} = 5$ mA and $V_{CE_Q} = 8$ V. Use $V_{CC} = 24$ V and $R_C = 3R_E$.
b. Find V_E.
c. Determine V_B.
d. Find R_2 if $R_1 = 24$ kΩ assuming that $\beta R_E > 10R_2$.
e. Calculate β at the Q-point.
f. Test Eq. (4.33), and note whether the assumption of part (d) is correct.

***25. a.** Determine I_C and V_{CE} for the network of Fig. 4.125.

b. Change β to 120 (50% increase), and determine the new values of I_C and V_{CE} for the network of Fig. 4.125.

c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}}\right| \times 100\%, \quad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}}\right| \times 100\%$$

d. Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 14.

e. Based on the results of part (d), which configuration is least sensitive to variations in β?

***26. a.** Repeat parts (a) through (e) of Problem 25 for the network of Fig. 4.128. Change β to 180 in part (b).

b. What general conclusions can be made about networks in which the condition $\beta R_E > 10R_2$ is satisfied and the quantities I_C and V_{CE} are to be determined in response to a change in β?

4.6 Collector-Feedback Configuration

27. For the collector-feedback configuration of Fig. 4.129, determine:

a. I_B.

b. I_C.

c. V_C.

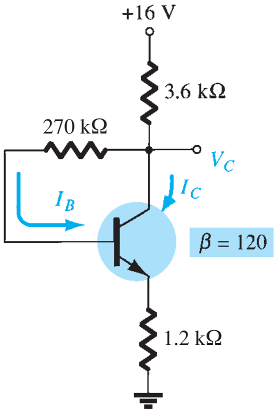


FIG. 4.129

Problems 27, 28, 74, and 78.

28. For the network of problem 27

a. Determine I_{C_Q} using the equation $I_{C_Q} \cong \dfrac{V'}{R'} = \dfrac{V_{CC} - V_{BE}}{R_C + R_E}$

b. Compare with the results of problem 27 for I_{C_Q}.

c. Compare R' to $R_{F/\beta}$.

d. Is the statement valid that the larger R′ is compared with $R_{F/\beta}$, the more accurate the equation $I_{C_Q} \cong \dfrac{V'}{R'}$? Prove using a short derivation for the exact current I_{C_Q}.

e. Repeat parts (a) and (b) for $\beta = 240$ and comment on the new level of I_{C_Q}.

29. For the voltage feedback network of Fig. 4.130, determine:

a. I_C.

b. V_C.

c. V_E.

d. V_{CE}.

30. a. Compare levels of $R' = R_C + R_E$ to $R_{F/\beta}$ for the network of Fig. 4.131.

b. Is the approximation $I_{C_Q} \cong V'/R'$ valid?

***31. a.** Determine the levels of I_C and V_{CE} for the network of Fig. 4.131.

b. Change β to 135 (50% increase), and calculate the new levels of I_C and V_{CE}.

c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}}\right| \times 100\%, \quad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}}\right| \times 100\%$$

d. Compare the results of part (c) with those of Problems 14(c), 14(f), and 25(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in β?

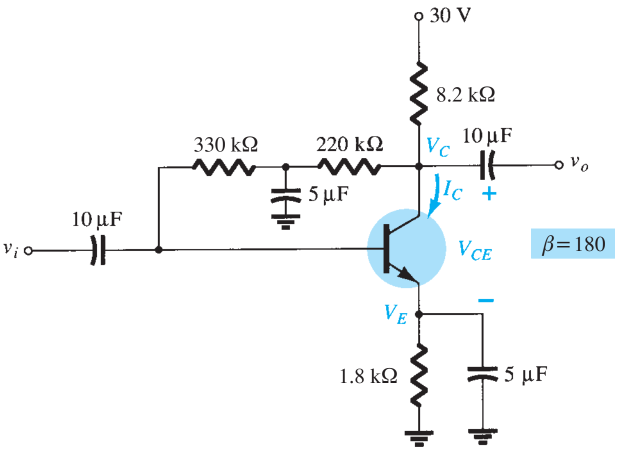

30 V
8.2 kΩ
330 kΩ
220 kΩ
V_C
10 μF
v_o
5 μF
I_C
+
10 μF
v_i
V_{CE}
β = 180
V_E
−
1.8 kΩ
5 μF

FIG. 4.130
Problems 29 and 30.

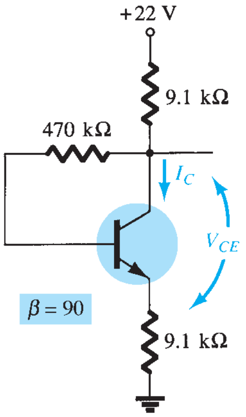

+22 V
9.1 kΩ
470 kΩ
I_C
V_{CE}
β = 90
9.1 kΩ

FIG. 4.131
Problems 30 and 31.

32. Determine the range of possible values for V_C for the network of Fig. 4.132 using the 1-MΩ potentiometer.

***33.** Given $V_B = 4$ V for the network of Fig. 4.133, determine:
- **a.** V_E.
- **b.** I_C.
- **c.** V_C.
- **d.** V_{CE}.
- **e.** I_B.
- **f.** β.

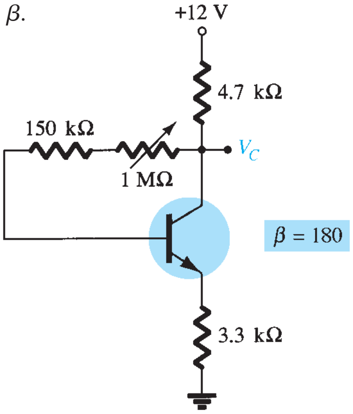

+12 V
4.7 kΩ
150 kΩ
1 MΩ
V_C
β = 180
3.3 kΩ

FIG. 4.132
Problem 32.

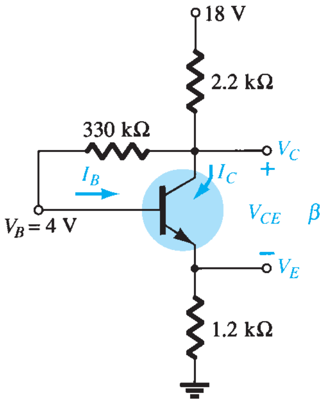

18 V
2.2 kΩ
330 kΩ
V_C
I_B
I_C
+
V_B = 4 V
V_{CE}
β
−
V_E
1.2 kΩ

FIG. 4.133
Problem 33.

4.7 Emitter-Follower Configuration

***34.** Determine the level of V_E and I_E for the network of Fig. 4.134.

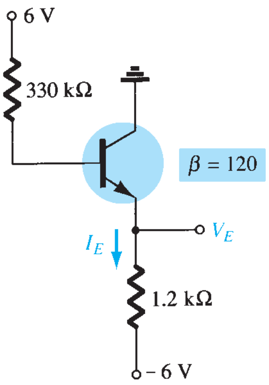

6 V
330 kΩ
β = 120
V_E
I_E
1.2 kΩ
−6 V

FIG. 4.134
Problem 34.

35. For the emitter follower network of Fig. 4.135
- **a.** Find I_B, I_C, and I_E.
- **b.** Determine V_B, V_C, and V_E.
- **c.** Calculate V_{BC} and V_{CE}.

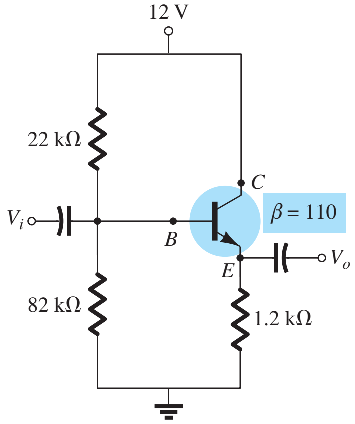

12 V
22 kΩ
C
V_i
β = 110
B
V_o
E
82 kΩ
1.2 kΩ

FIG. 4.135
Problem 35.

4.8 Common-Base Configuration

***36.** For the network of Fig. 4.136, determine:
- **a.** I_B.
- **b.** I_C.
- **c.** V_{CE}.
- **d.** V_C.

***37.** For the network of Fig. 4.137, determine:
- **a.** I_E.
- **b.** V_C.
- **c.** V_{CE}.

38. For the common-base network of Fig. 4.138
- **a.** Using the information provided determine the value of R_C.
- **b.** Find the currents I_B and I_E.
- **c.** Determine the voltages V_{BC} and V_{CE}.

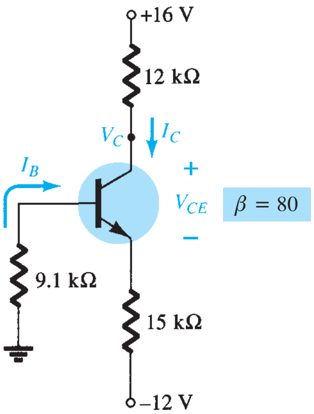

+16 V
12 kΩ
V_C
I_C
I_B
+
V_{CE}
β = 80
−
9.1 kΩ
15 kΩ
−12 V

FIG. 4.136
Problem 36.

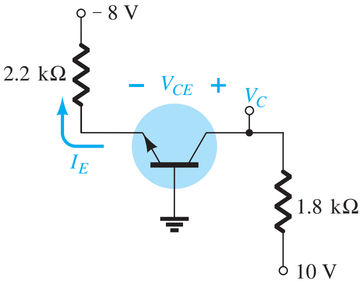

− 8 V
2.2 kΩ
− V_{CE} +
V_C
I_E
1.8 kΩ
10 V

FIG. 4.137
Problem 37.

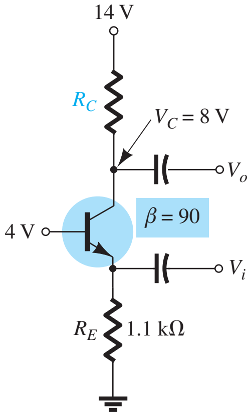

14 V
R_C
V_C = 8 V
V_o
4 V
β = 90
V_i
R_E
1.1 kΩ

FIG. 4.138
Problem 38.

4.9 Miscellaneous Bias Configurations

***39.** For the network of Fig. 4.139, determine:
- **a.** I_B.
- **b.** I_C.
- **c.** V_E.
- **d.** V_{CE}.

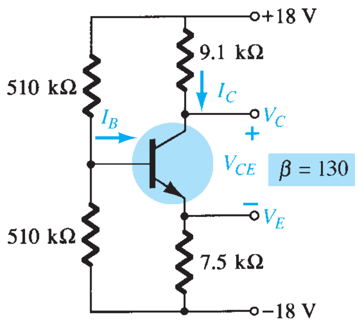

+18 V
9.1 kΩ
510 kΩ
I_C
V_C
I_B
+
V_{CE}
β = 130
–
V_E
510 kΩ
7.5 kΩ
–18 V

FIG. 4.139
Problem 39.

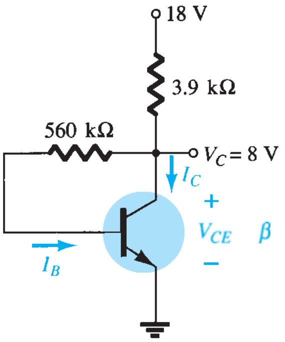

18 V
3.9 kΩ
560 kΩ
V_C = 8 V
I_C
+
V_{CE}
β
–
I_B

FIG. 4.140
Problems 40 and 68.

40. Given $V_C = 8$ V for the network of Fig. 4.140, determine:
- **a.** I_B.
- **b.** I_C.
- **c.** β.
- **d.** V_{CE}.

4.11 Design Operations

41. Determine R_C and R_B for a fixed-bias configuration if $V_{CC} = 12$ V, $\beta = 80$, and $I_{C_Q} = 2.5$ mA with $V_{CE_Q} = 6$ V. Use standard values.

42. Design an emitter-stabilized network at $I_{C_Q} = \frac{1}{2}I_{C_{\text{sat}}}$ and $V_{CE_Q} = \frac{1}{2}V_{CC}$. Use $V_{CC} = 20$ V, $I_{C_{\text{sat}}} = 10$ mA, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

43. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of $I_{C_Q} = 4$ mA and $V_{CE_Q} = 8$ V. Choose $V_E = \frac{1}{8}V_{CC}$. Use standard values.

***44.** Using the characteristics of Fig. 4.121, design a voltage-divider configuration to have a saturation level of 10 mA and a *Q*-point one-half the distance between cutoff and saturation. The available supply is 28 V, and V_E is to be one-fifth of V_{CC}. The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

4.12 Multiple BJT Networks

45. For the *R–C*-coupled amplifier of Fig. 4.141 determine
- **a.** the voltages V_B, V_C, and V_E for each transistor.
- **b.** the currents I_B, I_C, and I_E for each transistor

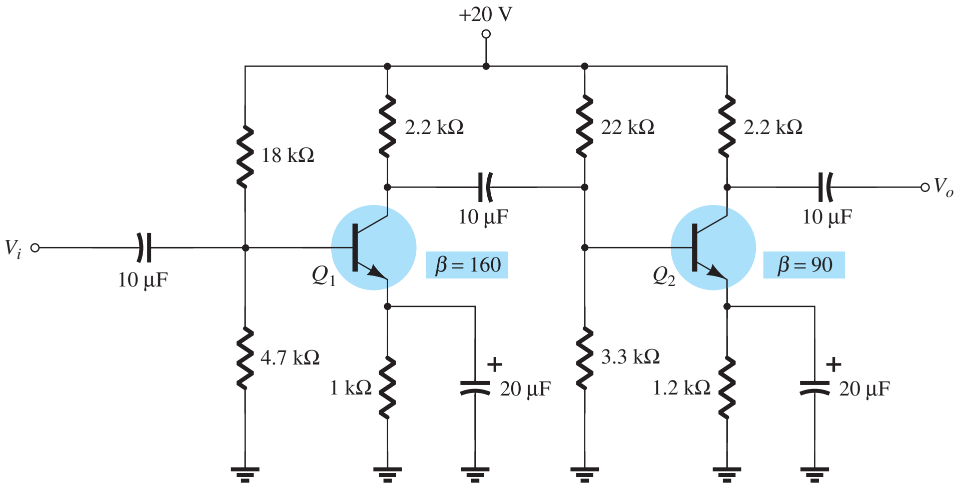
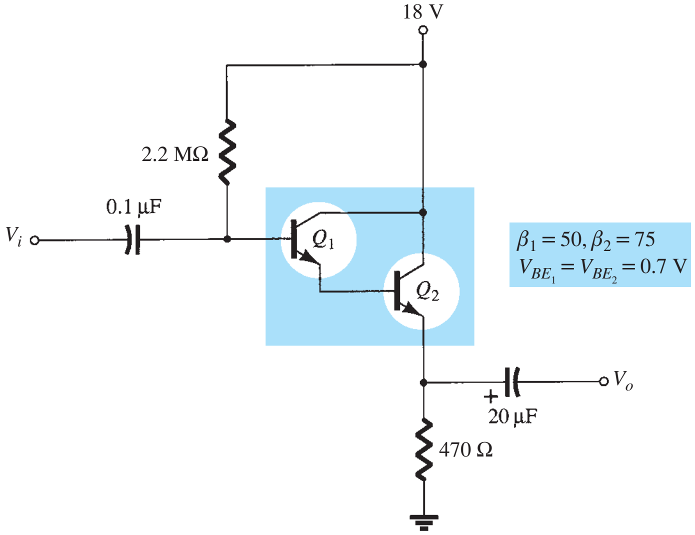

+20 V
2.2 kΩ
22 kΩ
2.2 kΩ
18 kΩ
10 μF
10 μF
V_o
V_i
10 μF
Q_1
β = 160
Q_2
β = 90
4.7 kΩ
1 kΩ
+
20 μF
3.3 kΩ
1.2 kΩ
+
20 μF

FIG. 4.141
Problem 45.

46. For the Darlington amplifier of Fig. 4.142 determine
- **a.** the level of β_D.
- **b.** the base current of each transistor.
- **c.** the collector current of each transistor.
- **d.** the voltages V_{C_1}, V_{C_2}, V_{E_1}, and V_{E_2}.



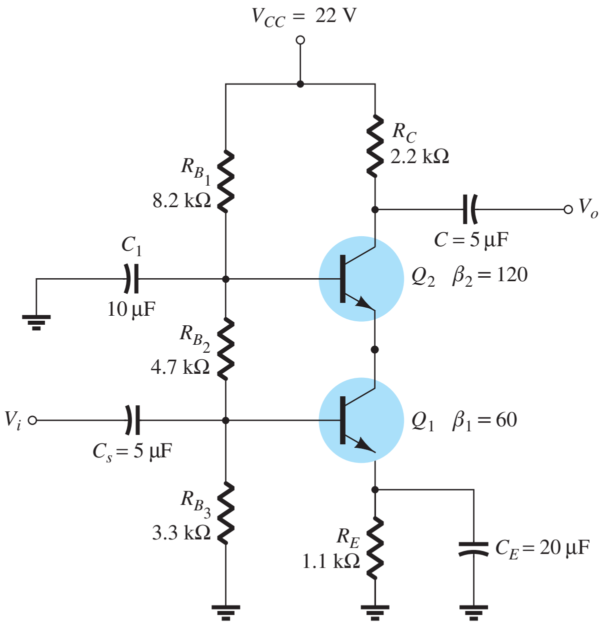
18 V
2.2 MΩ
0.1 μF
V_i
Q_1
Q_2
$\beta_1 = 50, \beta_2 = 75$
$V_{BE_1} = V_{BE_2} = 0.7$ V
+
20 μF
V_o
470 Ω

FIG. 4.142
Problem 46.

47. For the cascode amplifier of Fig. 4.143 determine

a. the base and collector currents of each transistor.

b. the voltages V_{B_1}, V_{B_2}, V_{E_1}, V_{C_1}, V_{E_2}, and V_{C_2}.



$V_{CC} = 22$ V
R_C
2.2 kΩ
R_{B_1}
8.2 kΩ
V_o
$C = 5$ μF
C_1
10 μF
Q_2 $\beta_2 = 120$
R_{B_2}
4.7 kΩ
V_i
Q_1 $\beta_1 = 60$
$C_s = 5$ μF
R_{B_3}
3.3 kΩ
R_E
1.1 kΩ
$C_E = 20$ μF

FIG. 4.143
Problem 47.

48. For the feedback amplifier of Fig. 4.144 determine

a. the base and collector current of each transistor.

b. the base, emitter, and collector voltages of each transistor.

4.13 Current Mirror Circuits

49. Calculate the mirrored current I in the circuit of Fig. 4.145.

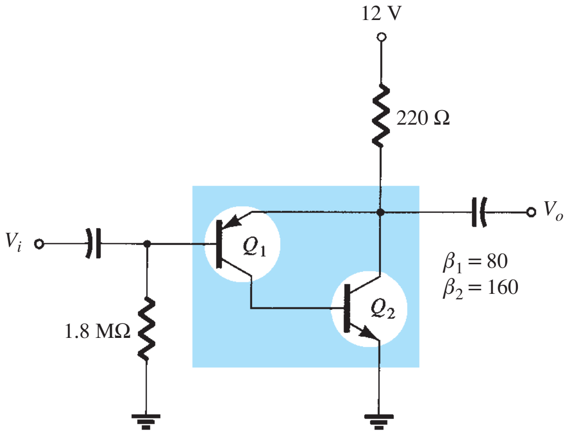

12 V
220 Ω
V_i
Q_1
Q_2
V_o
$\beta_1 = 80$
$\beta_2 = 160$
1.8 MΩ

FIG. 4.144
Problem 48.

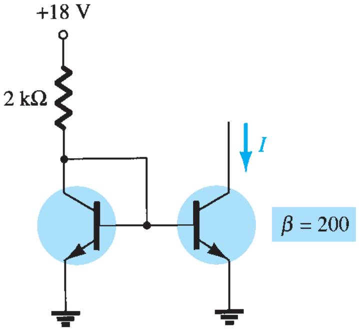

+18 V
2 kΩ
I
β = 200

FIG. 4.145
Problem 49.

***50.** Calculate collector currents for Q_1 and Q_2 in Fig. 4.146.

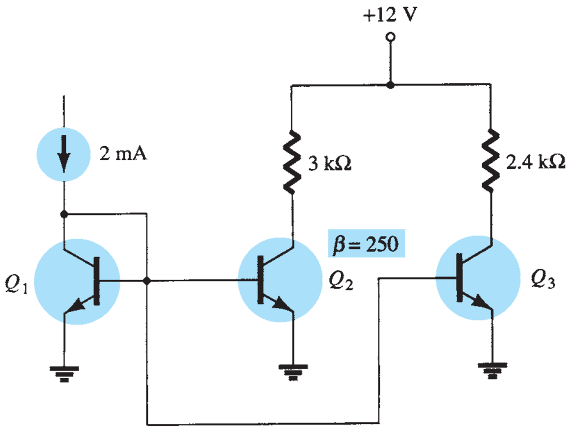

+12 V
2 mA
3 kΩ
2.4 kΩ
β= 250
Q_1
Q_2
Q_3

FIG. 4.146
Problem 50.

4.14 Current Source Circuits

51. Calculate the current through the 2.2-kΩ load in the circuit of Fig. 4.147.

52. For the circuit of Fig. 4.148, calculate the current I.

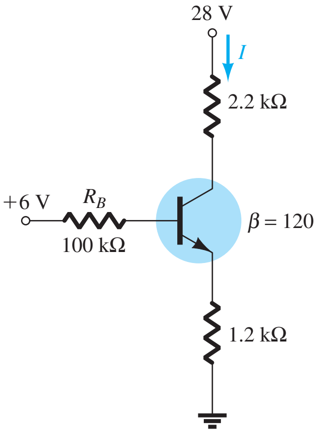

28 V
I
2.2 kΩ
+6 V
R_B
100 kΩ
β = 120
1.2 kΩ

FIG. 4.147
Problem 51.

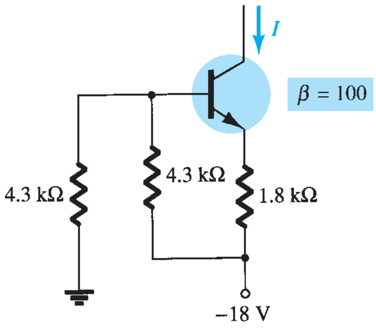

I
β = 100
4.3 kΩ
4.3 kΩ
1.8 kΩ
−18 V

FIG. 4.148
Problem 52.

***53.** Calculate the current I in the circuit of Fig. 4.149.

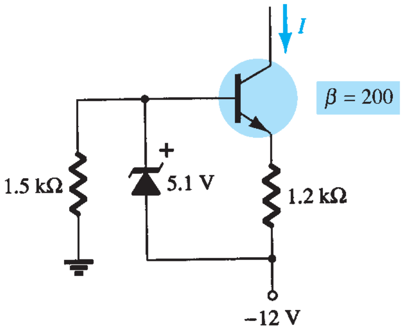

I
β = 200
1.5 kΩ
+
5.1 V
1.2 kΩ
−12 V

FIG. 4.149
Problem 53.

4.15 *pnp* Transistors

54. Determine V_C, V_{CE}, and I_C for the network of Fig. 4.150.

55. Determine V_C and I_B for the network of Fig. 4.151.

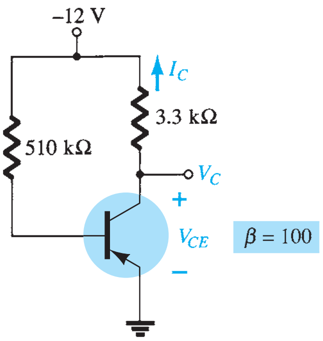

−12 V
I_C
3.3 kΩ
510 kΩ
V_C
+
V_{CE}
−
β = 100

FIG. 4.150
Problem 54.

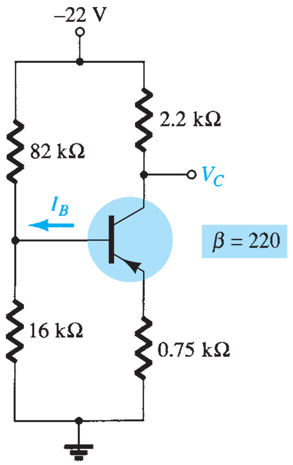

−22 V
2.2 kΩ
82 kΩ
V_C
I_B
β = 220
16 kΩ
0.75 kΩ

FIG. 4.151
Problem 55.

56. Determine I_E and V_C for the network of Fig. 4.152.

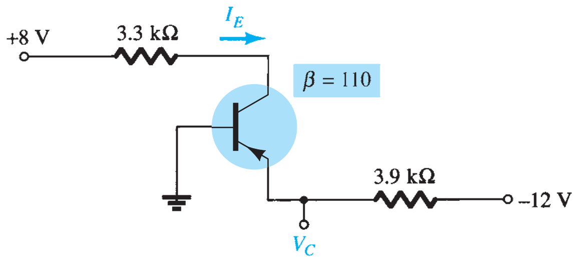
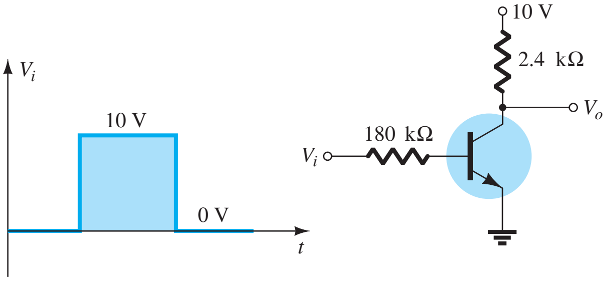

+8 V
3.3 kΩ
I_E
β = 110
3.9 kΩ
−12 V
V_C

FIG. 4.152
Problem 56.

4.16 Transistor Switching Networks

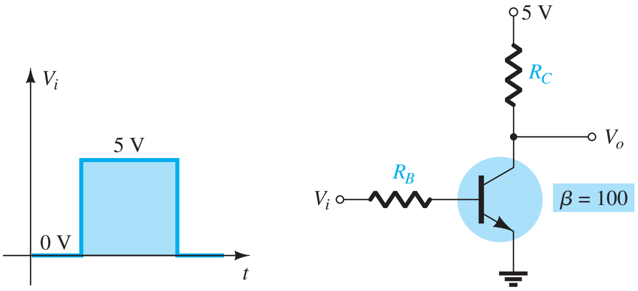
***57.** Using the characteristics of Fig. 4.121, determine the appearance of the output waveform for the network of Fig. 4.153. Include the effects of $V_{CE_{sat}}$, and determine I_B, $I_{B_{max}}$, and $I_{C_{sat}}$ when $V_i = 10$ V. Determine the collector-to-emitter resistance at saturation and cutoff.



V_i
10 V
0 V
t
10 V
2.4 kΩ
V_o
180 kΩ
V_i

FIG. 4.153
Problem 57.

***58.** Design the transistor inverter of Fig. 4.154 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B_{\max}}$ and standard resistor values.



V_i
5 V
0 V
t
5 V
R_C
V_o
R_B
V_i
β = 100

FIG. 4.154
Problem 58.

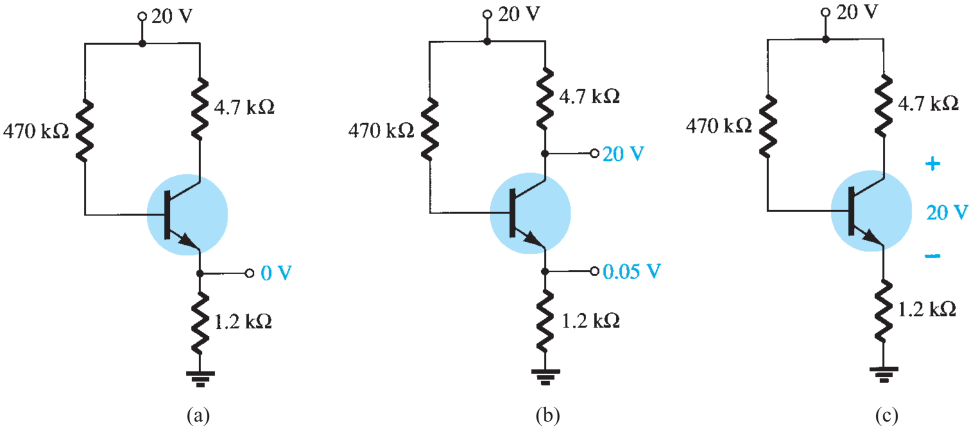
59. **a.** Using the characteristics of Fig. 3.23e, determine t_{on} and t_{off} at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 9.2.

b. Repeat part (a) at a current of 10 mA. How have t_{on} and t_{off} changed with increase in collector current?

c. For parts (a) and (b), sketch the pulse waveform of Fig. 4.91 and compare results.

4.17 Troubleshooting Techniques

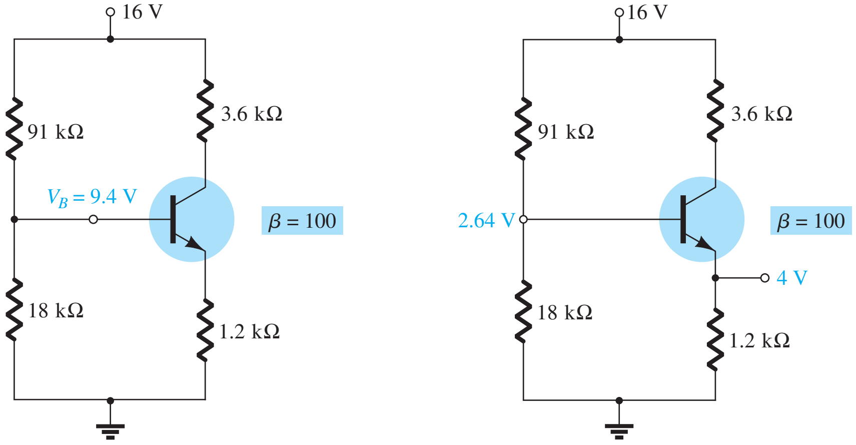
***60.** The measurements of Fig. 4.155 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.



20 V
470 kΩ
4.7 kΩ
0 V
1.2 kΩ
(a)
20 V
470 kΩ
4.7 kΩ
20 V
0.05 V
1.2 kΩ
(b)
20 V
470 kΩ
4.7 kΩ
+
20 V
–
1.2 kΩ
(c)

FIG. 4.155
Problem 60.

***61.** The measurements appearing in Fig. 4.156 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.


16 V
91 kΩ
3.6 kΩ
V_B = 9.4 V
β = 100
18 kΩ
1.2 kΩ
16 V
91 kΩ
3.6 kΩ
2.64 V
β = 100
4 V
18 kΩ
1.2 kΩ

(a)

(b)

FIG. 4.156
Problem 61.

62. For the circuit of Fig. 4.157:

a. Does V_C increase or decrease if R_B is increased?
b. Does I_C increase or decrease if β is reduced?
c. What happens to the saturation current if β is increased?
d. Does the collector current increase or decrease if V_{CC} is reduced?
e. What happens to V_{CE} if the transistor is replaced by one with smaller β?

63. Answer the following questions about the circuit of Fig. 4.158:

a. What happens to the voltage V_C if the transistor is replaced by one having a larger value of β?
b. What happens to the voltage V_{CE} if the ground leg of resistor R_{B_2} opens (does not connect to ground)?
c. What happens to I_C if the supply voltage is low?
d. What voltage V_{CE} would occur if the transistor base–emitter junction fails by becoming open?
e. What voltage V_{CE} would result if the transistor base–emitter junction fails by becoming a short?

***64.** Answer the following questions about the circuit of Fig. 4.159:

a. What happens to the voltage V_C if the resistor R_B is open?
b. What should happen to V_{CE} if β increases due to temperature?
c. How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
d. If the transistor collector connection becomes open, what will happen to V_E?
e. What might cause V_{CE} to become nearly 18 V?

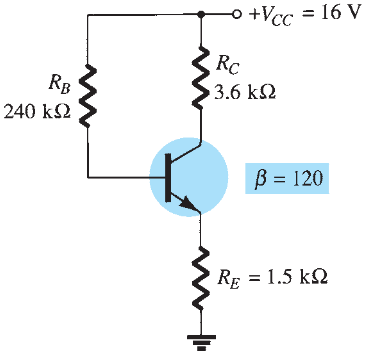

$+V_{CC}$ = 16 V
R_B
240 kΩ
R_C
3.6 kΩ
β = 120
R_E = 1.5 kΩ

FIG. 4.157
Problem 62.

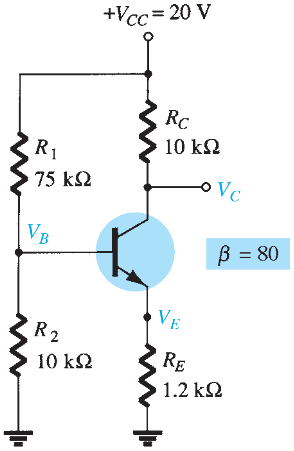

$+V_{CC}$ = 20 V
R_1
75 kΩ
R_C
10 kΩ
V_C
V_B
β = 80
V_E
R_2
10 kΩ
R_E
1.2 kΩ

FIG. 4.158
Problem 63.

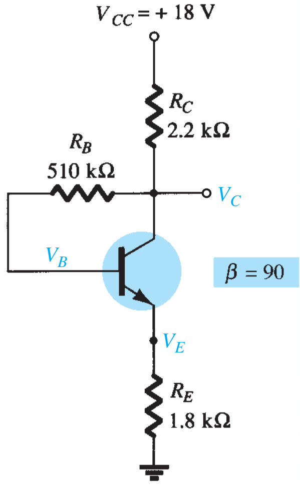

V_{CC} = + 18 V
R_C
2.2 kΩ
R_B
510 kΩ
V_C
V_B
β = 90
V_E
R_E
1.8 kΩ

FIG. 4.159
Problem 64.

4.18 Bias Stabilization

65. Determine the following for the network of Fig. 4.118:

a. $S(I_{CO})$.

b. $S(V_{BE})$.

c. $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.

d. Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***66.** For the network of Fig. 4.122, determine:

a. $S(I_{CO})$.

b. $S(V_{BE})$.

c. $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.

d. Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***67.** For the network of Fig. 4.125, determine:

a. $S(I_{CO})$.

b. $S(V_{BE})$.

c. $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.

d. Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***68.** For the network of Fig. 4.140, determine:

a. $S(I_{CO})$.

b. $S(V_{BE})$.

c. $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.

d. Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***69.** Compare the relative values of stability for Problems 65 through 68. The results for Exercises 65 and 67 can be found in Appendix E. Can any general conclusions be derived from the results?

***70.** **a.** Compare the levels of stability for the fixed-bias configuration of Problem 65.

b. Compare the levels of stability for the voltage-divider configuration of Problem 67.

c. Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

4.21 Computer Analysis

71. Perform a PSpice analysis of the network of Fig. 4.118. That is, determine I_C, V_{CE}, and I_B.

72. Repeat Problem 71 for the network of Fig. 4.122.

73. Repeat Problem 71 for the network of Fig. 4.125.

74. Repeat Problem 71 for the network of Fig. 4.129.

75. Repeat Problem 71 using Multisim.

76. Repeat Problem 72 using Multisim.

77. Repeat Problem 73 using Multisim.

78. Repeat Problem 74 using Multisim.

BJT AC Analysis

5

CHAPTER OBJECTIVES

- Become familiar with the r_e, hybrid, and hybrid π models for the BJT transistor.
- Learn to use the equivalent model to find the important ac parameters for an amplifier.
- Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
- Become aware of the general ac characteristics of a variety of important BJT configurations.
- Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
- Develop some skill in troubleshooting ac amplifier networks.

5.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 12.

There are three models commonly used in the small-signal ac analysis of transistor networks: the r_e model, the hybrid π model, and the hybrid equivalent model. This chapter introduces all three but emphasizes the r_e model.

5.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, P_o, of a system cannot be greater than its power input, P_i, and that the efficiency defined by $\eta = P_o/P_i$ cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is the principal contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an "exchange" of dc power to the ac domain that permits establishing a higher output ac power. In fact, a *conversion efficiency* is defined by $\eta = P_{o(\text{ac})}/P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 5.1. The resulting direction of flow is indicated in the figure with a plot of the current i versus time. Let us now insert a control mechanism such as that shown in Fig. 5.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

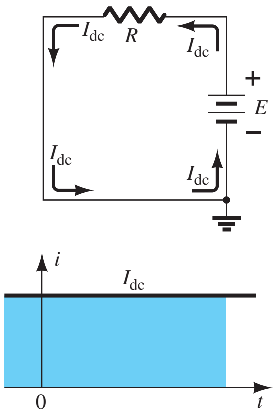


FIG. 5.1
Steady current established by a dc supply.

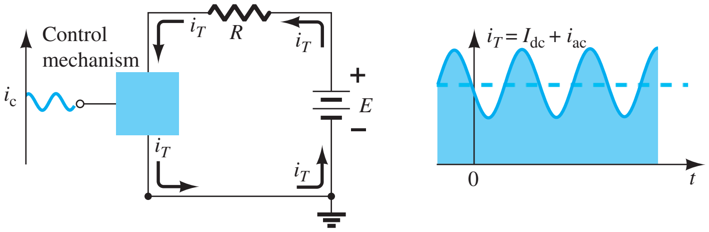


FIG. 5.2
Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

That is, for this example,

$$i_{\text{ac(p-p)}} \gg i_{c\text{(p-p)}}$$

and amplification in the ac domain has been established. The peak-to-peak value of the output current far exceeds that of the control current.

For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the peak region at the high and low end of the output signal. In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations.

However, it is extremely helpful to realize that:

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis. It happens, however, that one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions, so there is still an important link between the two types of analysis.

5.3 BJT TRANSISTOR MODELING

The key to transistor small-signal analysis is the use of the equivalent circuits (models) to be introduced in this chapter.

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

In the formative years of transistor network analysis the *hybrid equivalent network* was employed the most frequently. Specification sheets included the parameters in their listing, and analysis was simply a matter of inserting the equivalent circuit with the listed values.

The drawback to using this equivalent circuit, however, is that it is *defined for a set of operating conditions that might not match the actual operating conditions.* In most cases, this is not a serious flaw because the actual operating conditions are relatively close to the chosen operating conditions on the data sheets. In addition, there is always a variation in actual resistor values and given transistor beta values, so as an approximate approach it was quite reliable. Manufacturers continue to specify the hybrid parameter values for a particular operating point on their specification sheets. They really have no choice. They want to give the user some idea of the value of each important parameter so comparisons can be made between transistors, but they really do not know the user's actual operating conditions.

In time the use of the r_e *model* became the more desirable approach because an important parameter of the equivalent circuit was determined by the actual operating conditions rather than using a data sheet value that in some cases could be quite different. Unfortunately, however, one must still turn to the data sheets for some of the other parameters of the equivalent circuit. The r_e model also failed to include a feedback term, which in some cases can be important if not simply troublesome.

The r_e model is really a reduced version of the *hybrid* π *model* used almost exclusively for high-frequency analysis. This model also includes a connection between output and input to include the feedback effect of the output voltage and the input quantities. The full hybrid model is introduced in Chapter 9.

Throughout the text the r_e model is the model of choice unless the discussion centers on the description of each model or a region of examination that predetermines the model that should be used. Whenever possible, however, a comparison between models will be discussed to show how closely related they really are. It is also important that once you gain a proficiency with one model it will carry over to an investigation using a different model, so moving from one to another will not be a dramatic undertaking.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 5.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Because we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 5.4. The dc levels were simply important for determining the proper Q-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors C_1 and C_2 and bypass capacitor C_3 were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor R_E. Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.

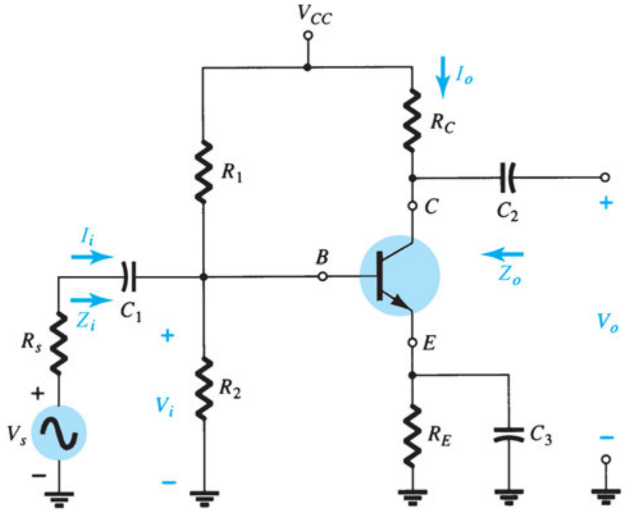


FIG. 5.3

Transistor circuit under examination in this introductory discussion.

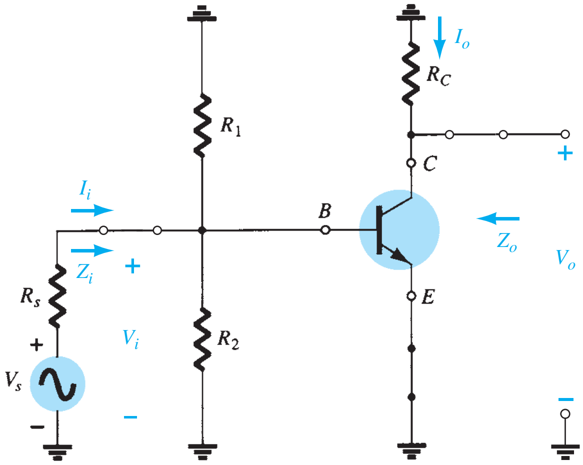


FIG. 5.4
The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as Z_i, Z_o, I_i, and I_o as defined by Fig. 5.5 be carried through properly. Even though the network appearance may change, you want to be sure the quantities you find in the reduced network are the same as defined by the original network. In both networks the input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor R_C.

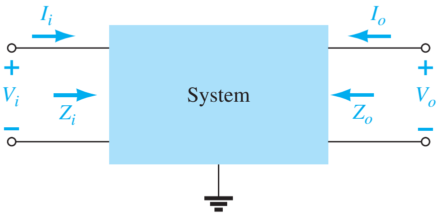


FIG. 5.5
Defining the important parameters of any system.

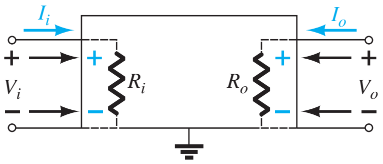


FIG. 5.6
Demonstrating the reason for the defined directions and polarities.

The parameters of Fig. 5.5 can be applied to any system whether it has one or a thousand components. For all the analysis to follow in this text, the directions of the currents, the polarities of the voltages, and the direction of interest for the impedance levels are as appearing in Fig. 5.5. In other words, the input current I_i and output current I_o are, by definition, defined to enter the system. If, in a particular example, the output current is leaving the system rather than entering the system as shown in Fig. 5.5, a minus sign must be applied. The defined polarities for the input and output voltages are also as appearing in Fig. 5.5. If V_o has the opposite polarity, the minus sign must be applied. Note that Z_i is the impedance "looking into" the system, whereas Z_o is the impedance "looking back into" the system from the output side. By choosing the defined directions for the currents and voltages as appearing in Fig. 5.5, both the input impedance and output impedance are defined as having positive values. For example, in Fig. 5.6 the input and output impedances for a particular system are both resistive. For the direction of I_i and I_o the resulting voltage across the resistive elements will have the same polarity as V_i and V_o, respectively. If I_o had been defined as the opposite direction in Fig. 5.5 a minus sign would have to be applied. For each case $Z_i = V_i/I_i$ and $Z_o = V_o/I_o$ with positive results if they all have the defined directions and polarity of Fig. 5.5. If the output current of an actual system has a direction opposite to that of Fig. 5.5 a minus sign must be applied to the result because V_o must be defined as appearing in Fig. 5.5. Keep Fig. 5.5 in mind as you analyze the BJT networks in this chapter. It is an important introduction to "System Analysis," which is becoming so important with the expanded use of packaged IC systems.

If we establish a common ground and rearrange the elements of Fig. 5.4, R_1 and R_2 will be in parallel, and R_C will appear from collector to emitter as shown in Fig. 5.7. Because the components of the transistor equivalent circuit appearing in Fig. 5.7 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

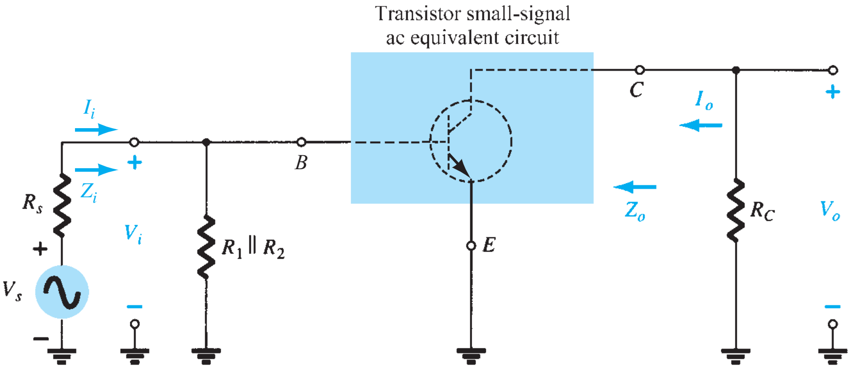


FIG. 5.7

Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

Let us further examine Fig. 5.7 and identify the important quantities to be determined for the system. Because we know that the transistor is an amplifying device, we would expect some indication of how the output voltage V_o is related to the input voltage V_i—the *voltage gain*. Note in Fig. 5.7 for this configuration that the *current gain* is defined by $A_i = I_o/I_i$.

In summary, therefore, the ac equivalent of a transistor network is obtained by:

1. ***Setting all dc sources to zero and replacing them by a short-circuit equivalent***
2. ***Replacing all capacitors by a short-circuit equivalent***
3. ***Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2***
4. ***Redrawing the network in a more convenient and logical form***

In the sections to follow, a transistor equivalent model will be introduced to complete the ac analysis of the network of Fig. 5.7.

5.4 THE r_e TRANSISTOR MODEL

The r_e model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage V_i is equal to the voltage V_{be} with the input current being the base current I_b as shown in Fig. 5.8.

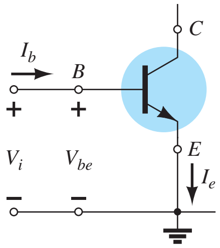
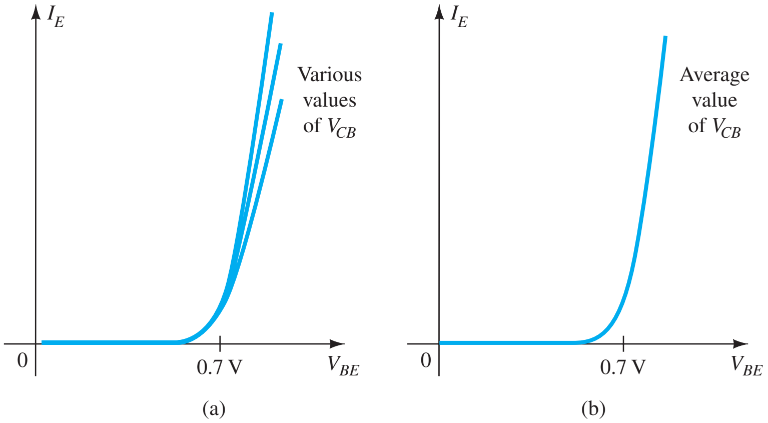


FIG. 5.8

Finding the input equivalent circuit for a BJT transistor.

Recall from Chapter 3 that because the current through the forward-biased junction of the transistor is I_E, the characteristics for the input side appear as shown in Fig. 5.9a for various levels of V_{BE}. Taking the average value for the curves of Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply that of a forward-biased diode.



(a)

(b)

FIG. 5.9
Defining the average curve for the characteristics of Fig. 5.9a.

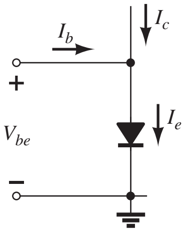


FIG. 5.10
Equivalent circuit for the input side of a BJT transistor.

For the equivalent circuit, therefore, the input side is simply a single diode with a current I_e, as shown in Fig. 5.10. However, we must now add a component to the network that will establish the current I_e of Fig. 5.10 using the output characteristics.

If we redraw the collector characteristics to have a constant β as shown in Fig. 5.11 (another approximation), the entire characteristics at the output section can be replaced by a controlled source whose magnitude is beta times the base current as shown in Fig. 5.11. Because all the input and output parameters of the original configuration are now present, the equivalent network for the common-emitter configuration has been established in Fig. 5.12.

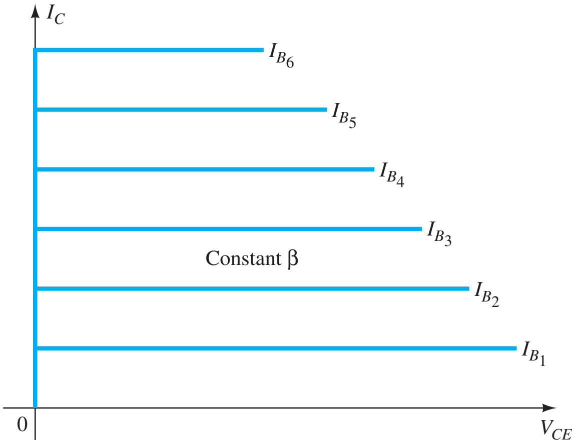


FIG. 5.11
Constant β characteristics.

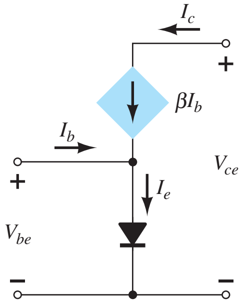


FIG. 5.12
BJT equivalent circuit.

The equivalent model of Fig. 5.12 can be awkward to work with due to the direct connection between input and output networks. It can be improved by first replacing the diode by its equivalent resistance as determined by the level of I_E, as shown in Fig. 5.13. Recall from Section 1.8 that the diode resistance is determined by $r_D = 26\text{ mV}/I_D$. Using the subscript e because the determining current is the emitter current will result in $r_e = 26\text{ mV}/I_E$.

Now, for the input side: $$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

Solving for V_{be}: $$\begin{aligned} V_{be} &= I_e r_e = (I_c + I_b)r_e = (\beta I_b + I_b)r_e \\ &= (\beta + 1)I_b r_e \end{aligned}$$

and $$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1)I_b r_e}{I_b}$$

$$\boxed{Z_i = (\beta + 1)r_e \cong \beta r_e} \tag{5.1}$$

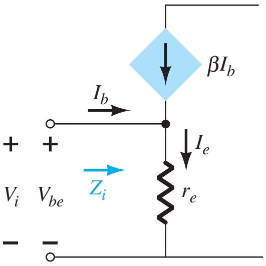


FIG. 5.13
Defining the level of Z_i.

The result is that the impedance seen "looking into" the base of the network is a resistor equal to beta times the value of r_e, as shown in Fig. 5.14. The collector output current is still linked to the input current by beta as shown in the same figure.

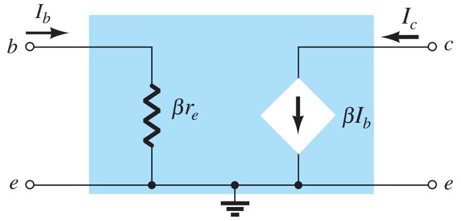


FIG. 5.14
Improved BJT equivalent circuit.

The equivalent circuit has therefore been defined for the ideal characteristics of Fig. 5.11, but now the input and output circuits are isolated and only linked by the controlled source—a form much easier to work with when analyzing networks.

Early Voltage

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of beta and I_B, we do not have a good representation for the output impedance of the device. In reality the characteristics do not have the ideal appearance of Fig. 5.11. Rather, they have a slope as shown In Fig. 5.15 that defines the output impedance of the device. The steeper the slope, the less the output impedance and the less ideal the transistor. In general, it is desirable to have large output impedances to avoid loading down the next stage of a design. If the slope of the curves is extended until they reach the horizontal axis, it is interesting to note in Fig. 5.15 that they will all intersect at a voltage called the Early voltage. This intersection was first discovered by James M. Early in 1952. As the base current increases the slope of the line increases, resulting in an increase in output impedance with increase in base and collector current. For a particular collector and base current as shown in Fig. 5.15, the output impedance can be found using the following equation:

$$\boxed{r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}} \qquad \textbf{(5.2)}$$

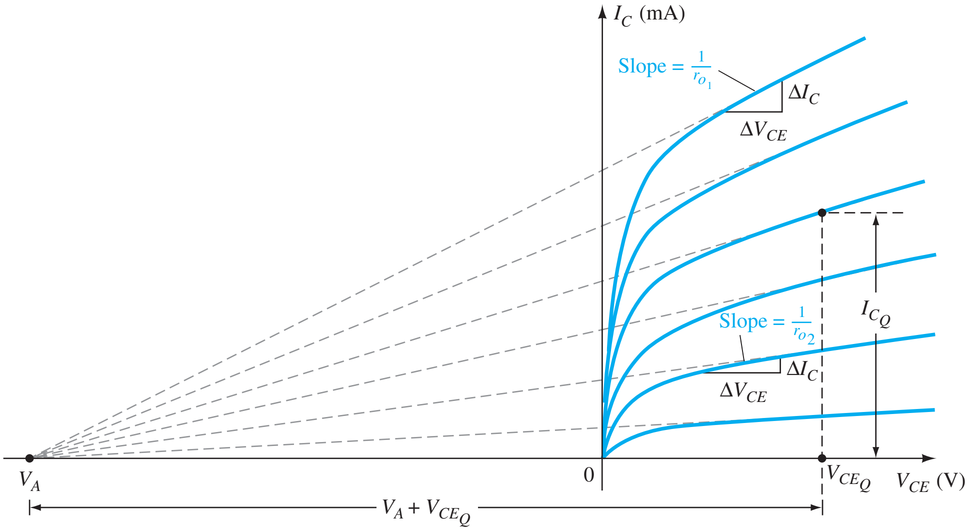


FIG. 5.15
Defining the Early voltage and the output impedance of a transistor.

Typically, however, the Early voltage is sufficiently large compared with the applied collector-to-emitter voltage to permit the following approximation.

$$\boxed{r_o \cong \frac{V_A}{I_{C_Q}}} \tag{5.3}$$

Clearly, since V_A is a fixed voltage, the larger the collector current, the less the output impedance.

For situations where the Early voltage is not available the output impedance can be found from the characteristics at any base or collector current using the following equation:

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o}$$

and

$$\boxed{r_o = \frac{\Delta V_{CE}}{\Delta I_C}} \tag{5.4}$$

For the same change in voltage in Fig. 5.15 the resulting change in current ΔI_C is significantly less for r_{o_2} than r_{o_1}, resulting in r_{o_2} being much larger than r_{o_1}.

In situations where the specification sheets of a transistor do not include the Early voltage or the output characteristics, the output impedance can be determined from the hybrid parameter h_{oe} that is normally plotted on every specification sheet. It is a quantity that will be described in detail in Section 5.19.

In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 5.16.

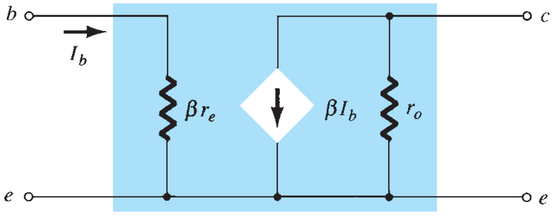


FIG. 5.16

r_e model for the common-emitter transistor configuration including effects of r_o.

The equivalent circuit of Fig. 5.16 will be used throughout the analysis to follow for the common-emitter configuration. Typical values of beta run from 50 to 200, with values of βr_e typically running from a few hundred ohms to a maximum of 6 kΩ to 7 kΩ. The output resistance r is typically in the range of 40 kΩ to 50 kΩ.

Common-Base Configuration

The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. The general characteristics of the input and output circuit will generate an equivalent circuit that will approximate the actual behavior of the device. Recall for the common-emitter configuration the use of a diode to represent the connection from base to emitter. For the common-base configuration of Fig. 5.17a the *pnp* transistor employed will present the same possibility at the input circuit. The result is the use of a diode in the equivalent circuit as shown in Fig. 5.17b. For the output circuit, if we return to Chapter 3 and review Fig. 3.8, we find that the collector current is related to the emitter current by alpha α. In this case, however, the controlled source defining the collector current as inserted in Fig. 5.17b is opposite in direction to that of the controlled source of the common-emitter configuration. The direction of the collector current in the output circuit is now opposite that of the defined output current.

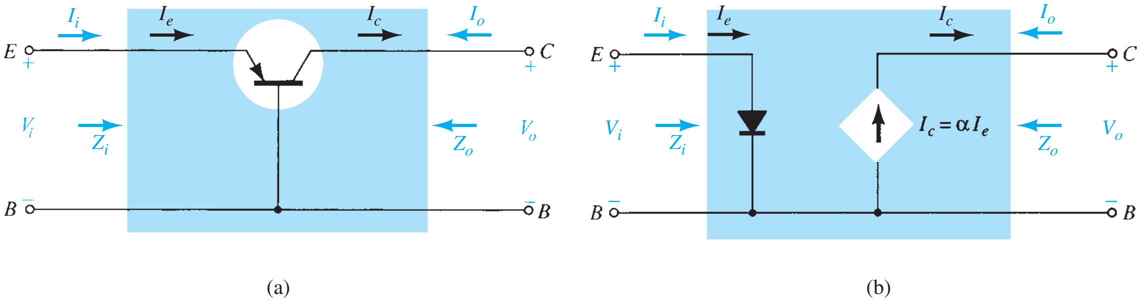


FIG. 5.17

(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

For the ac response, the diode can be replaced by its equivalent ac resistance determined by $r_e = 26\text{ mV}/I_E$ as shown in Fig. 5.18. Take note of the fact that the emitter current continues to determine the equivalent resistance. An additional output resistance can be determined from the characteristics of Fig. 5.19 in much the same manner as applied to the common-emitter configuration. The almost horizontal lines clearly reveal that the output resistance r_o as appearing in Fig. 5.18 will be quite high and certainly much higher than that for the typical common-emitter configuration.

The network of Fig. 5.18 is therefore an excellent equivalent circuit for the analysis of most common-base configurations. It is similar in many ways to that of the common-emitter configuration. In general, common-base configurations have very low input impedance because it is essentially simply r_e. Typical values extend from a few ohms to perhaps 50 Ω. The output impedance r_o will typically extend into the megohm range. Because the output current is opposite to the defined I_o direction, you will find in the analysis to follow that there is no phase shift between the input and output voltages. For the common-emitter configuration there is a 180° phase shift.

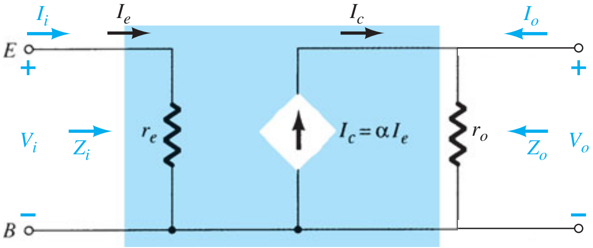


FIG. 5.18

Common base r_e equivalent circuit.

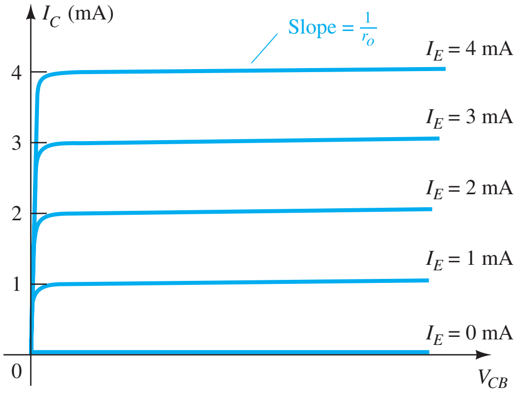


FIG. 5.19

Defining Z_o.

Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 5.16 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated, and the effect of using the same model will become quite apparent.

npn versus *pnp*

The dc analysis of *npn* and *pnp* configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities. However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

5.5 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The transistor models just introduced will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations will be relatively easy to examine once the content of this chapter is reviewed and understood. For each configuration, the effect of an output impedance is examined for completeness.

The computer analysis section includes a brief description of the transistor model employed in the PSpice and Multisim software packages. It demonstrates the range and depth of the available computer analysis systems and how relatively easy it is to enter a complex network and print out the desired results. The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 5.20. Note that the input signal V_i is applied to the base of the transistor, whereas the output V_o is off the collector. In addition, recognize that the input current I_i is not the base current, but the source current, and the output current I_o is the collector current. The small-signal ac analysis begins by removing the dc effects of V_{CC} and replacing the dc blocking capacitors C_1 and C_2 by short-circuit equivalents, resulting in the network of Fig. 5.21.

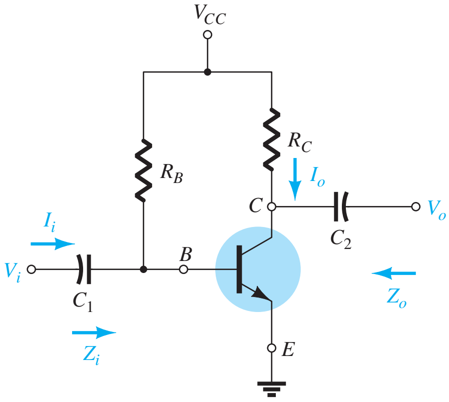


FIG. 5.20
Common-emitter fixed-bias configuration.

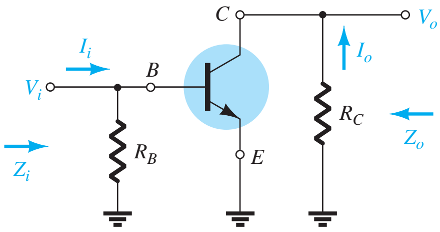


FIG. 5.21
Network of Fig. 5.20 following the removal of the effects of V_{CC}, C_1, and C_2.

Note in Fig. 5.21 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of R_B and R_C in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters Z_i, Z_o, I_i, and I_o on the redrawn network. Substituting the r_e model for the common-emitter configuration of Fig. 5.21 results in the network of Fig. 5.22.

The next step is to determine β, r_e, and r_o. The magnitude of β is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor

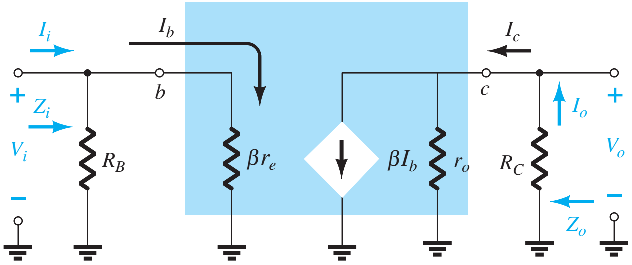


FIG. 5.22
Substituting the r_e model into the network of Fig. 5.21.

testing instrument. The value of r_e must be determined from a dc analysis of the system, and the magnitude of r_o is typically obtained from the specification sheet or characteristics. Assuming that β, r_e, and r_o have been determined will result in the following equations for the important two-port characteristics of the system.

Z_i Figure 5.22 clearly shows that

$$\boxed{Z_i = R_B \| \beta r_e} \quad \text{ohms} \tag{5.5}$$

For the majority of situations R_B is greater than βr_e by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$\boxed{Z_i \cong \beta r_e}_{R_B \geq 10\beta r_e} \quad \text{ohms} \tag{5.6}$$

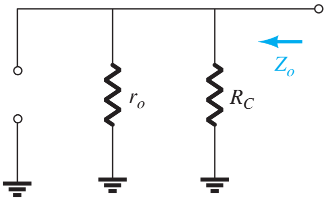


FIG. 5.23
Determining Z_o for the network of Fig. 5.22.

Z_o Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

$$\boxed{Z_o = R_C \| r_o} \quad \text{ohms} \tag{5.7}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o \cong R_C$ is frequently applied, and

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C} \tag{5.8}$$

A_v The resistors r_o and R_C are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}} \tag{5.9}$$

If $r_o \geq 10R_C$, so that the effect of r_o can be ignored,

$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.10}$$

Note the explicit absence of β in Eqs. (5.9) and (5.10), although we recognize that β must be utilized to determine r_e.

Phase Relationship The negative sign in the resulting equation for A_v reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.24. The is a result of the fact that βI_b establishes a current through R_C that will result in a voltage across R_C, the opposite of that defined by V_o.

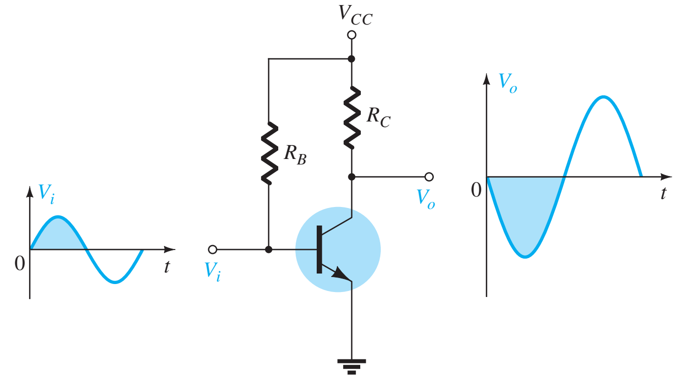


FIG. 5.24
Demonstrating the 180° phase shift between input and output waveforms.

EXAMPLE 5.1 For the network of Fig. 5.25:

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\,\Omega$).
c. Calculate Z_o (with $r_o = \infty\,\Omega$).
d. Determine A_v (with $r_o = \infty\,\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\text{ k}\Omega$ in all calculations and compare results.

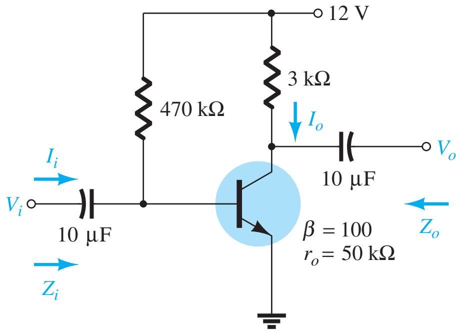


FIG. 5.25
Example 5.1.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\text{ k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\text{ k}\Omega \| 1.071\text{ k}\Omega = \mathbf{1.07\text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{3\text{ k}\Omega}$

d. $A_v = -\dfrac{R_C}{r_e} = -\dfrac{3\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

e. $Z_o = r_o \| R_C = 50\text{ k}\Omega \| 3\text{ k}\Omega = \mathbf{2.83\text{ k}\Omega}$ vs. 3 kΩ

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\text{ vs. } -280.11$$

5.6 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 5.26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of V_B.

Substituting the r_e equivalent circuit results in the network of Fig. 5.27. Note the absence of R_E due to the low-impedance shorting effect of the bypass capacitor, C_E. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to R_E that it is treated as a short circuit across R_E. When V_{CC} is set to zero, it places one end of R_1 and R_C at ground potential as shown in Fig. 5.27. In addition, note that R_1 and R_2 remain part of the input circuit, whereas R_C is part of the output circuit. The parallel combination of R_1 and R_2 is defined by

$$\boxed{R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}} \tag{5.11}$$

Z_i From Fig. 5.27

$$\boxed{Z_i = R' \| \beta r_e} \tag{5.12}$$

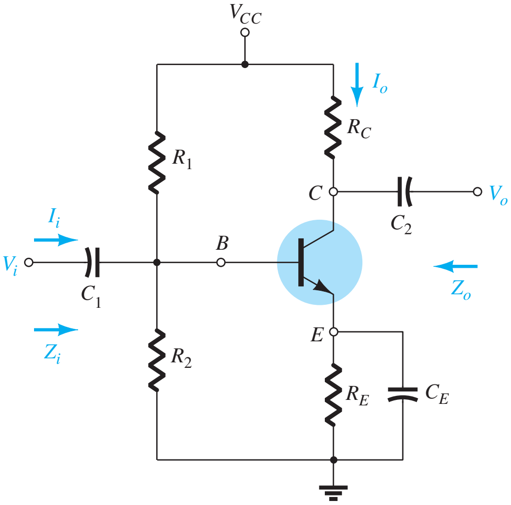


FIG. 5.26
Voltage-divider bias configuration.

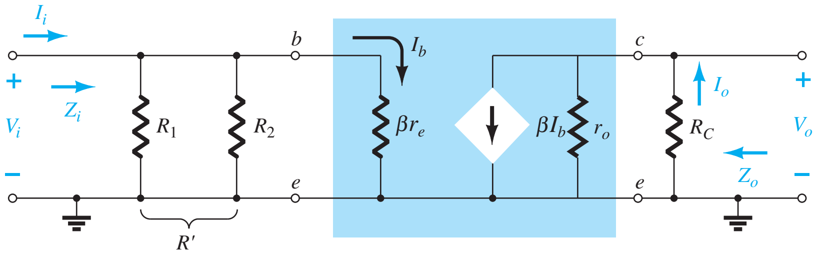


FIG. 5.27
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.26.

Z_o From Fig. 5.27 with V_i set to 0 V, resulting in $I_b = 0\ \mu A$ and $\beta I_b = 0$ mA,

$$\boxed{Z_o = R_C \| r_o} \tag{5.13}$$

If $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C} \tag{5.14}$$

A_v Because R_C and r_o are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}} \tag{5.15}$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.16}$$

Phase Relationship The negative sign of Eq. (5.15) reveals a 180° phase shift between V_o and V_i.

EXAMPLE 5.2 For the network of Fig. 5.28, determine:

a. r_e.
b. Z_i.
c. Z_o $(r_o = \infty\,\Omega)$.
d. A_v $(r_o = \infty\,\Omega)$.
e. The parameters of parts (b) through (d) if $r_o = 50\ \text{k}\Omega$ and compare results.

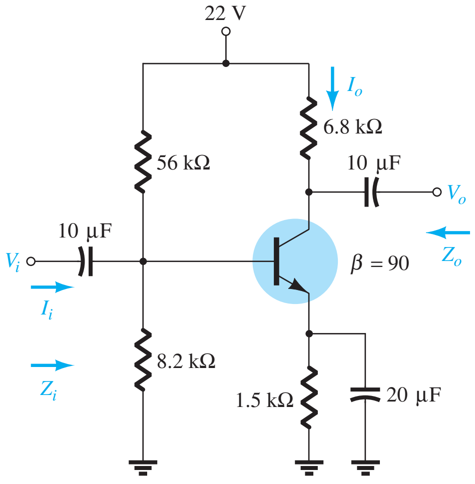


FIG. 5.28
Example 5.2.

Solution:

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\text{ k}\Omega) > 10(8.2\text{ k}\Omega)$$
$$135\text{ k}\Omega > 82\text{ k}\Omega\ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{(8.2\text{ k}\Omega)(22\text{ V})}{56\text{ k}\Omega + 8.2\text{ k}\Omega} = 2.81\text{ V}$$
$$V_E = V_B - V_{BE} = 2.81\text{ V} - 0.7\text{ V} = 2.11\text{ V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\text{ V}}{1.5\text{ k}\Omega} = 1.41\text{ mA}$$
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.41\text{ mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\text{ k}\Omega)\|(8.2\text{ k}\Omega) = 7.15\text{ k}\Omega$

$$Z_i = R'\|\beta r_e = 7.15\text{ k}\Omega\|(90)(18.44\ \Omega) = 7.15\text{ k}\Omega\|1.66\text{ k}\Omega$$
$$= \mathbf{1.35\text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{6.8\text{ k}\Omega}$

d. $A_v = -\dfrac{R_C}{r_e} = -\dfrac{6.8\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\text{ k}\Omega}$

$$Z_o = R_C\|r_o = 6.8\text{ k}\Omega\|50\text{ k}\Omega = \mathbf{5.98\text{ k}\Omega}\text{ vs. }6.8\text{ k}\Omega$$
$$A_v = -\frac{R_C\|r_o}{r_e} = -\frac{5.98\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}\text{ vs. }-368.76$$

There was a measurable difference in the results for Z_o and A_v, because the condition $r_o \geq 10R_C$ was *not* satisfied.

5.7 CE EMITTER-BIAS CONFIGURATION

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.29. The r_e equivalent model is substituted in Fig. 5.30, but note the absence of the resistance r_o. The effect of r_o is to make the analysis a great deal more complicated, and considering the fact that in

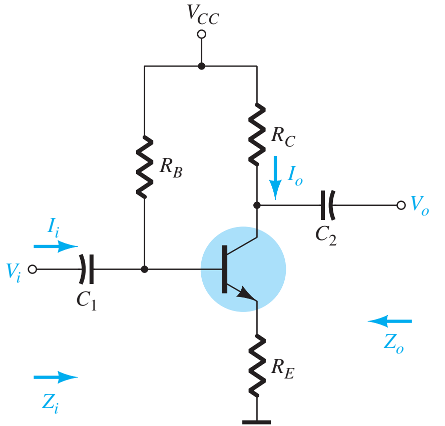


FIG. 5.29

CE emitter-bias configuration.

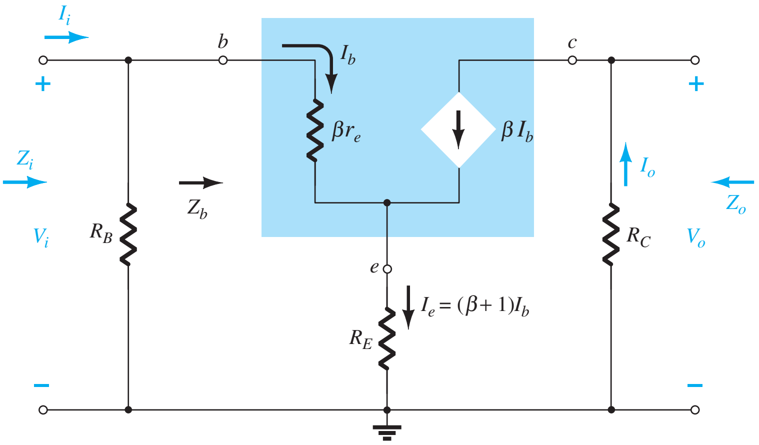


FIG. 5.30

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.29.

most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of r_o will be discussed later in this section.

Applying Kirchhoff's voltage law to the input side of Fig. 5.30 results in

$$V_i = I_b \beta r_e + I_e R_E$$

or

$$V_i = I_b \beta r_e + (\beta + I) I_b R_E$$

and the input impedance looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

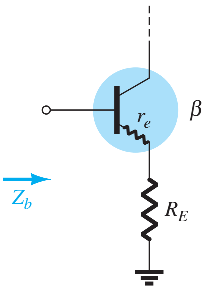


FIG. 5.31
Defining the input impedance of a transistor with an unbypassed emitter resistor.

The result as displayed in Fig. 5.31 reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1) R_E} \qquad \textbf{(5.17)}$$

Because β is normally much greater than 1, the approximate equation is

$$Z_b \cong \beta r_e + \beta R_E$$

and

$$\boxed{Z_b \cong \beta(r_e + R_E)} \qquad \textbf{(5.18)}$$

Because R_E is usually greater than r_e, Eq. (5.18) can be further reduced to

$$\boxed{Z_b \cong \beta R_E} \qquad \textbf{(5.19)}$$

Z_i Returning to Fig. 5.30, we have

$$\boxed{Z_i = R_B \| Z_b} \qquad \textbf{(5.20)}$$

Z_o With V_i set to zero, $I_b = 0$, and βI_b can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C} \qquad \textbf{(5.21)}$$

A_v

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$
$$= -\beta\left(\frac{V_i}{Z_b}\right) R_C$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}} \qquad \textbf{(5.22)}$$

Substituting $Z_b \cong \beta(r_e + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}} \qquad \textbf{(5.23)}$$

and for the approximation $Z_b \cong \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}} \qquad \textbf{(5.24)}$$

Note the absence of β from the equation for A_v demonstrating an independence in variation of β.

Phase Relationship The negative sign in Eq. (5.22) again reveals a 180° phase shift between V_o and V_i.

Effect of r_o The equations appearing below will clearly reveal the additional complexity resulting from including r_o in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through *careful* application of the basic laws of circuit analysis such as Kirchhoff's voltage and current laws, source conversions, Thévenin's theorem, and so on. The equations were included to remove the nagging question of the effect of r_o on the important parameters of a transistor configuration.

Z_i

$$\boxed{Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right]R_E} \tag{5.25}$$

Because the ratio R_C/r_o is always much less than $(\beta + 1)$,

$$Z_b \cong \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For $r_o \geq 10(R_C + R_E)$,

$$Z_b \cong \beta r_e + (\beta + 1)R_E$$

which compares directly with Eq. (5.17).

In other words, if $r_o \geq 10(R_C + R_E)$, all the equations derived earlier result. Because $\beta + 1 \cong \beta$, the following equation is an excellent one for most applications:

$$\boxed{Z_b \cong \beta(r_e + R_E)} \quad {\scriptstyle r_o \geq 10(R_C + R_E)} \tag{5.26}$$

Z_o

$$\boxed{Z_o = R_C \| \left[r_o + \frac{\beta(r_o + r_e)}{1 + \dfrac{\beta r_e}{R_E}}\right]} \tag{5.27}$$

However, $r_o \gg r_e$, and

$$Z_o \cong R_C \| r_o\left[1 + \frac{\beta}{1 + \dfrac{\beta r_e}{R_E}}\right]$$

which can be written as

$$Z_o \cong R_C \| r_o\left[1 + \frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}}\right]$$

Typically $1/\beta$ and r_e/R_E are less than one with a sum usually less than one. The result is a multiplying factor for r_o greater than one. For $\beta = 100$, $r_e = 10\ \Omega$, and $R_E = 1\ \text{k}\Omega$,

$$\frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} = \frac{1}{\dfrac{1}{100} + \dfrac{10\ \Omega}{1000\ \Omega}} = \frac{1}{0.02} = 50$$

and

$$Z_o = R_C \| 51 r_o$$

which is certainly simply R_C. Therefore,

$$\boxed{Z_o \cong R_C} \quad {\scriptstyle \text{Any level of } r_o} \tag{5.28}$$

which was obtained earlier.

A_v

$$A_v = \frac{V_o}{V_i} = \frac{-\dfrac{\beta R_C}{Z_b}\left[1 + \dfrac{r_e}{r_o}\right] + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}} \tag{5.29}$$

The ratio $\frac{r_e}{r_o} \ll 1$, and

$$A_v = \frac{V_o}{V_i} \cong \frac{-\dfrac{\beta R_C}{Z_b} + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \Bigg|_{r_o \geq 10R_C} \tag{5.30}$$

as obtained earlier.

Bypassed

If R_E of Fig. 5.29 is bypassed by an emitter capacitor C_E, the complete r_e equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.5) to (5.10) are therefore applicable.

EXAMPLE 5.3 For the network of Fig. 5.32, without C_E (unbypassed), determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

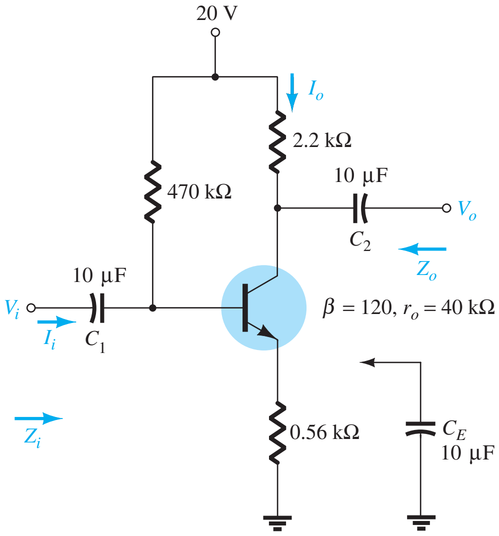


FIG. 5.32
Example 5.3.

Solution:

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$$
$$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega\ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega) = 67.92\text{ k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega = \mathbf{59.34\text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\text{ k}\Omega}$

d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\text{ k}\Omega)}{67.92\text{ k}\Omega} = \mathbf{-3.89}$$

compared to -3.93 using Eq. (5.20): $A_v \cong -R_C/R_E$.

EXAMPLE 5.4 Repeat the analysis of Example 5.3 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = 5.99\ \Omega$.

b. R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\text{ k}\Omega \| (120)(5.99\ \Omega) = 470\text{ k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

c. $Z_o = R_C = \mathbf{2.2\text{ k}\Omega}$

d. $A_v = -\dfrac{R_C}{r_e}$

$$= -\frac{2.2\text{ k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}\text{ (a significant increase)}$$

EXAMPLE 5.5 For the network of Fig. 5.33 (with C_E unconnected), determine (using appropriate approximations):

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

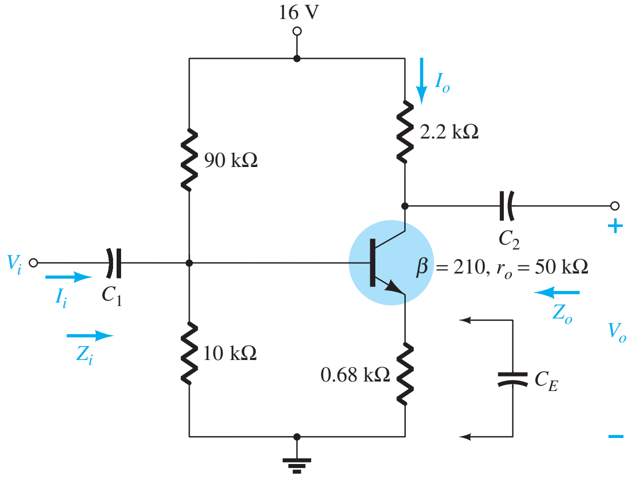


FIG. 5.33
Example 5.5.

Solution:

a. Testing $\beta R_E > 10R_2$,

$$(210)(0.68\ \text{k}\Omega) > 10(10\ \text{k}\Omega)$$
$$142.8\ \text{k}\Omega > 100\ \text{k}\Omega\ (\textit{satisfied})$$

we have

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{10\ \text{k}\Omega}{90\ \text{k}\Omega + 10\ \text{k}\Omega}(16\ \text{V}) = 1.6\ \text{V}$$
$$V_E = V_B - V_{BE} = 1.6\ \text{V} - 0.7\ \text{V} = 0.9\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{0.9\ \text{V}}{0.68\ \text{k}\Omega} = 1.324\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.324\ \text{mA}} = \mathbf{19.64\ \Omega}$$

b. The ac equivalent circuit is provided in Fig. 5.34. The resulting configuration is different from Fig. 5.30 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9\ \text{k}\Omega$$

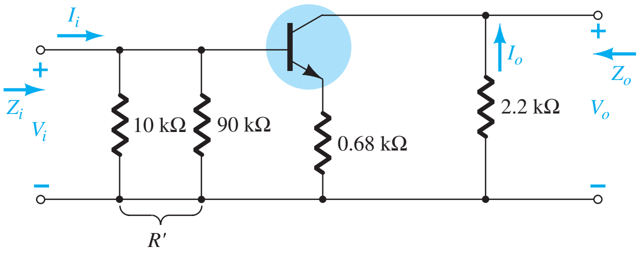


FIG. 5.34
The ac equivalent circuit of Fig. 5.33.

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\ \text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 142.8\ \text{k}\Omega$$
$$= \mathbf{8.47\ k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\ k\Omega}$

d. $A_v = -\dfrac{R_C}{R_E} = -\dfrac{2.2\ \text{k}\Omega}{0.68\ \text{k}\Omega} = \mathbf{-3.24}$

EXAMPLE 5.6 Repeat Example 5.5 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = \mathbf{19.64\ \Omega}$.

b. $Z_b = \beta r_e = (210)(19.64\ \Omega) \cong 4.12\ \text{k}\Omega$

$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 4.12\ \text{k}\Omega$$
$$= \mathbf{2.83\ k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\ k\Omega}$

d. $A_v = -\dfrac{R_C}{r_e} = -\dfrac{2.2\ \text{k}\Omega}{19.64\ \Omega} = \mathbf{-112.02}$ (a significant increase)

Another variation of an emitter-bias configuration is shown in Fig. 5.35. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, whereas for the ac analysis, the resistor R_E in the equations above is simply R_{E_1} with R_{E_2} bypassed by C_E.

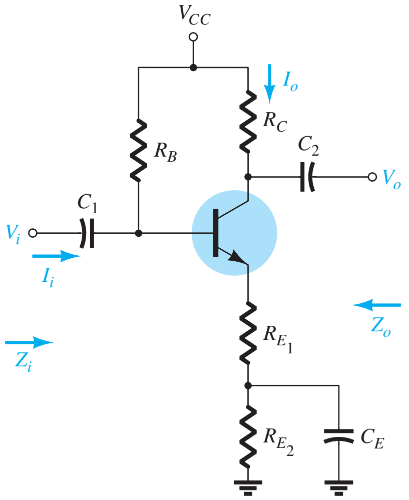


FIG. 5.35

An emitter-bias configuration with a portion of the emitter-bias resistance bypassed in the ac domain.

5.8 EMITTER-FOLLOWER CONFIGURATION

When the output is taken from the emitter terminal of the transistor as shown in Fig. 5.36, the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal V_i. That is, both V_o and V_i attain their positive and negative peak values at the same time. The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter-follower.

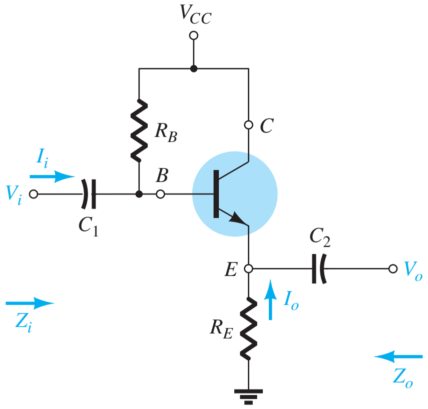


FIG. 5.36

Emitter-follower configuration.

The most common emitter-follower configuration appears in Fig. 5.36. In fact, because the collector is grounded for ac analysis, it is actually a *common-collector* configuration. Other variations of Fig. 5.36 that draw the output off the emitter with $V_o \cong V_i$ will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the r_e equivalent circuit into the network of Fig. 5.36 results in the network of Fig. 5.37. The effect of r_o will be examined later in the section.

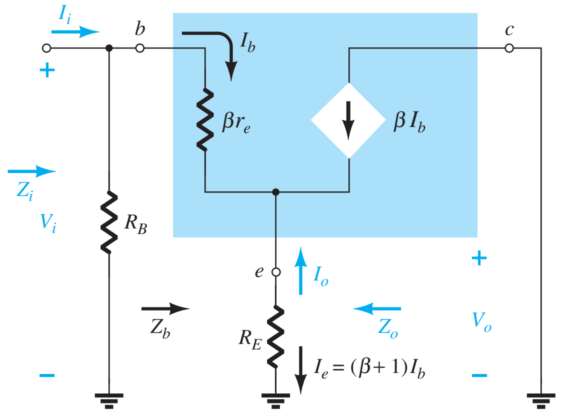


FIG. 5.37
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.36.

Z_i The input impedance is determined in the same manner as described in the preceding section:

$$\boxed{Z_i = R_B \| Z_b} \tag{5.31}$$

with

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \tag{5.32}$$

or

$$\boxed{Z_b \cong \beta(r_e + R_E)} \tag{5.33}$$

and

$$\boxed{Z_b \cong \beta R_E} \quad {}_{R_E \gg r_e} \tag{5.34}$$

Z_o The output impedance is best described by first writing the equation for the current I_b,

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by $(\beta + 1)$ to establish I_e. That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

Substituting for Z_b gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

but

$$(\beta + 1) \cong \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that

$$\boxed{I_e \cong \frac{V_i}{r_e + R_E}} \tag{5.35}$$

If we now construct the network defined by Eq. (5.35), the configuration of Fig. 5.38 results.

To determine Z_o, V_i is set to zero and

$$\boxed{Z_o = R_E \| r_e} \tag{5.36}$$

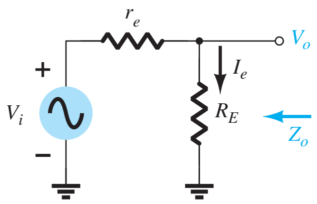


FIG. 5.38
Defining the output impedance for the emitter-follower configuration.

Because R_E is typically much greater than r_e, the following approximation is often applied:

$$\boxed{Z_o \cong r_e} \tag{5.37}$$

A_v Figure 5.38 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}} \tag{5.38}$$

Because R_E is usually much greater than r_e, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1} \tag{5.39}$$

Phase Relationship As revealed by Eq. (5.38) and earlier discussions of this section, V_o and V_i are in phase for the emitter-follower configuration.

Effect of r_o

Z_i

$$\boxed{Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}}} \tag{5.40}$$

If the condition $r_o \geq 10R_E$ is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$\boxed{Z_b \cong \beta(r_e + R_E)}\ _{r_o \geq 10R_E} \tag{5.41}$$

Z_o

$$\boxed{Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)}} \tag{5.42}$$

Using $\beta + 1 \cong \beta$, we obtain

$$Z_o = r_o \| R_E \| r_e$$

and because $r_o \gg r_e$,

$$\boxed{Z_o \cong R_E \| r_e}\ \ \text{Any } r_o \tag{5.43}$$

A_v

$$\boxed{A_v = \frac{(\beta + 1)R_E/Z_b}{1 + \dfrac{R_E}{r_o}}} \tag{5.44}$$

If the condition $r_o \geq 10R_E$ is satisfied and we use the approximation $\beta + 1 \cong \beta$, we find

$$A_v \cong \frac{\beta R_E}{Z_b}$$

But
$$Z_b \cong \beta(r_e + R_E)$$

so that
$$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and
$$\boxed{A_v \cong \frac{R_E}{r_e + R_E}}_{r_o \geq 10R_E} \tag{5.45}$$

EXAMPLE 5.7 For the emitter-follower network of Fig. 5.39, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 25\text{ k}\Omega$ and compare results.

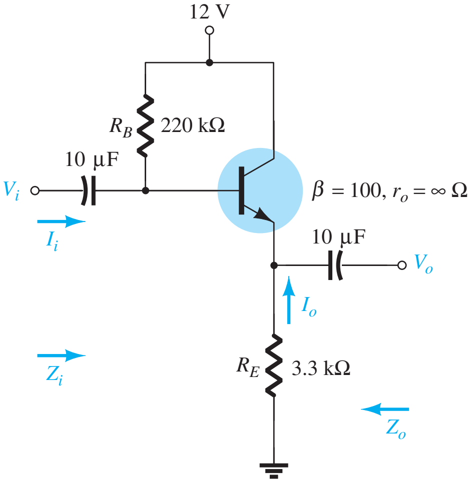


FIG. 5.39
Example 5.7.

Solution:

a.
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)3.3\text{ k}\Omega} = 20.42\ \mu\text{A}$$
$$I_E = (\beta + 1)I_B$$
$$= (101)(20.42\ \mu\text{A}) = 2.062\text{ mA}$$
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = \mathbf{12.61\ \Omega}$$

b.
$$Z_b = \beta r_e + (\beta + 1)R_E$$
$$= (100)(12.61\ \Omega) + (101)(3.3\text{ k}\Omega)$$
$$= 1.261\text{ k}\Omega + 333.3\text{ k}\Omega$$
$$= 334.56\text{ k}\Omega \cong \beta R_E$$
$$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 334.56\text{ k}\Omega$$
$$= \mathbf{132.72\text{ k}\Omega}$$

c.
$$Z_o = R_E \| r_e = 3.3\text{ k}\Omega \| 12.61\ \Omega$$
$$= \mathbf{12.56\ \Omega} \cong r_e$$

d.
$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\text{ k}\Omega}{3.3\text{ k}\Omega + 12.61\ \Omega}$$
$$= \mathbf{0.996 \cong 1}$$

e. Checking the condition $r_o \geq 10R_E$, we have

$$25\text{ k}\Omega \geq 10(3.3\text{ k}\Omega) = 33\text{ k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\text{ k}\Omega}{1 + \dfrac{3.3\text{ k}\Omega}{25\text{ k}\Omega}}$$

$$= 1.261\text{ k}\Omega + 294.43\text{ k}\Omega$$

$$= 295.7\text{ k}\Omega$$

with $Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 295.7\text{ k}\Omega$

$$= \mathbf{126.15\ k\Omega} \text{ vs. } 132.72\text{ k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \dfrac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\text{ k}\Omega)/295.7\text{ k}\Omega}{\left[1 + \dfrac{3.3\text{ k}\Omega}{25\text{ k}\Omega}\right]}$$

$$= \mathbf{0.996 \cong 1}$$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ is not satisfied, the results for Z_o and A_v are the same, with Z_i only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of r_o for this configuration.

The network of Fig. 5.40 is a variation of the network of Fig. 5.36, which employs a voltage-divider input section to set the bias conditions. Equations (5.31) to (5.34) are changed only by replacing R_B by $R' = R_1 \| R_2$.

The network of Fig. 5.41 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor R_C. In this case R_B is again replaced by the parallel combination of R_1 and R_2. The input impedance Z_i and output impedance Z_o are unaffected by R_C because it is not reflected into the base or emitter equivalent networks. In fact, the only effect of R_C is to determine the Q-point of operation.

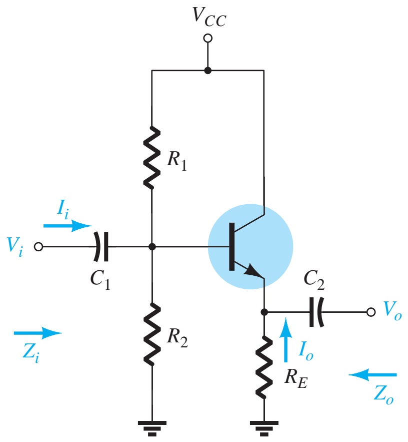


FIG. 5.40
Emitter-follower configuration with a voltage-divider biasing arrangement.

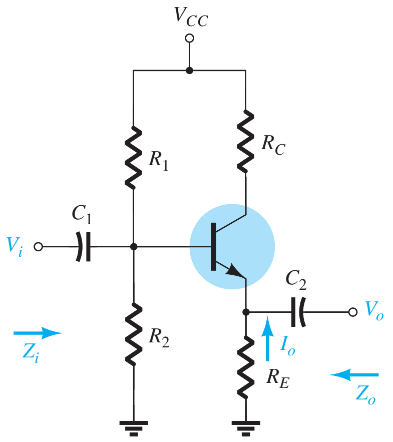


FIG. 5.41
Emitter-follower configuration with a collector resistor R_C.

5.9 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.42, with the common-base r_e equivalent model substituted in Fig. 5.43. The transistor output impedance r_o is not included for the

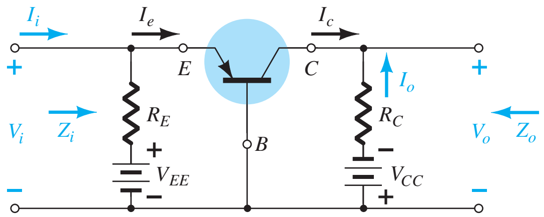

I_i
I_e
I_c
E
C
B
I_o
R_E
R_C
V_i
Z_i
V_o
Z_o
V_{EE}
V_{CC}
+
–

FIG. 5.42
Common-base configuration.

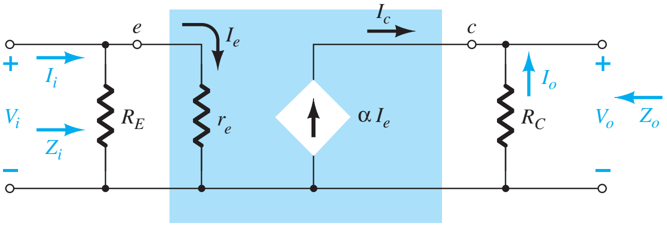

e
c
I_e
I_c
I_i
I_o
V_i
Z_i
R_E
r_e
αI_e
R_C
V_o
Z_o
+
–

FIG. 5.43
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.44.

common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor R_C.

Z_i

$$\boxed{Z_i = R_E \| r_e} \tag{5.46}$$

Z_o

$$\boxed{Z_o = R_C} \tag{5.47}$$

A_v

$$V_o = -I_oR_C = -(-I_c)R_C = \alpha I_eR_C$$

with
$$I_e = \frac{V_i}{r_e}$$

so that
$$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}} \tag{5.48}$$

A_i Assuming that $R_E \gg r_e$ yields
$$I_e = I_i$$

and
$$I_o = -\alpha I_e = -\alpha I_i$$

with
$$\boxed{A_i = \frac{I_o}{I_i} = -\alpha \cong -1} \tag{5.49}$$

Phase Relationship The fact that A_v is a positive number shows that V_o and V_i are in phase for the common-base configuration.

Effect of r_o For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

EXAMPLE 5.8 For the network of Fig. 5.44, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. A_i.

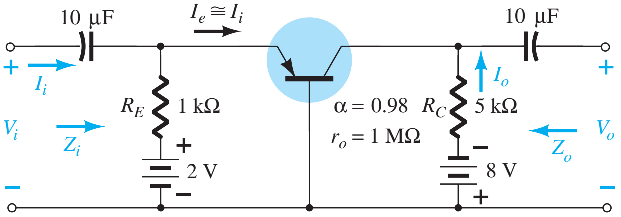

10 μF
$I_e \cong I_i$
10 μF
I_i
I_o
V_i
Z_i
R_E
1 kΩ
2 V
α = 0.98
r_o = 1 MΩ
R_C
5 kΩ
8 V
V_o
Z_o
+
–

FIG. 5.44
Example 5.8.

Solution:

a. $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \dfrac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$

$r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$

b. $Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$

$= \mathbf{19.61\ \Omega} \cong r_e$

c. $Z_o = R_C = \mathbf{5\ k\Omega}$

d. $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$

e. $A_i = \mathbf{-0.98} \cong -1$

5.10 COLLECTOR FEEDBACK CONFIGURATION

The collector feedback network of Fig. 5.45 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.46. The effects of a transistor output resistance r_o will be discussed later in the section.

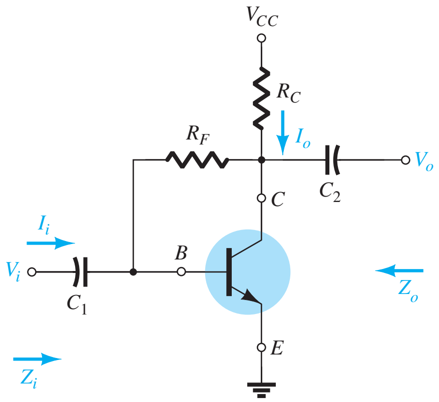


FIG. 5.45
Collector feedback configuration.

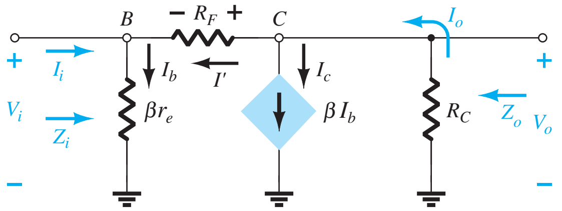


FIG. 5.46
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.45.

Z_i

$$I_o = I' + \beta I_b$$

and
$$I' = \frac{V_o - V_i}{R_F}$$

but
$$V_o = -I_o R_C = -(I' + \beta I_b)R_C$$

with
$$V_i = I_b \beta r_e$$

so that
$$I' = -\frac{(I' + \beta I_b)R_C - I_b\beta r_e}{R_F} = -\frac{I' R_C}{R_F} - \frac{\beta I_b R_C}{R_F} - \frac{I_b \beta r_e}{R_F}$$

which when rearranged in the following:

$$I'\left(1 + \frac{R_C}{R_F}\right) = -\beta I_b \frac{(R_C + r_e)}{R_F}$$

and finally,

$$I' = -\beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

Now $Z_i = \dfrac{V_i}{I_i}$:

and

$$I_i = I_b - I' = I_b + \beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

or

$$I_i = I_b\left(1 + \beta \frac{(R_C + r_e)}{R_C + R_F}\right)$$

Substituting for V_i in the above equation for Z_i leaves

$$Z_i = \frac{V_i}{I_i} = \frac{I_b \beta r_e}{I_b\left(1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}\right)} = \frac{\beta r_e}{1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}}$$

Since $R_C \gg r_e$

$$Z_i = \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_C + R_F}}$$

or

$$\boxed{Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}}} \tag{5.50}$$

Z_o If we set V_i to zero as required to define Z_o, the network will appear as shown in Fig. 5.47. The effect of βr_e is removed, and R_F appears in parallel with R_C and

$$\boxed{Z_o \cong R_C \| R_F} \tag{5.51}$$

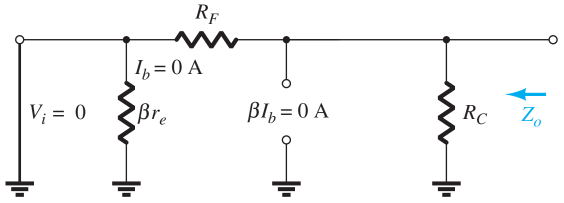


FIG. 5.47

Defining Z_o for the collector feedback configuration.

A_v

$$V_o = -I_o R_C = -(I' + \beta I_b) R_C$$

$$= -\left(-\beta I_b \frac{(R_C + r_e)}{R_C + R_F} + \beta I_b\right) R_C$$

or

$$V_o = -\beta I_b \left(1 - \frac{(R_C + r_e)}{R_C + R_F}\right) R_C$$

Then

$$A_v = \frac{V_o}{V_i} = \frac{-\beta \cancel{I_b}\left(1 - \dfrac{(R_C + r_e)}{R_C + R_F}\right) R_C}{\beta r_e \cancel{I_b}}$$

$$= -\left(1 - \frac{(R_C + r_e)}{R_C + R_F}\right) \frac{R_C}{r_e}$$

For $R_C \gg r_e$

$$A_v = -\left(1 - \frac{R_C}{R_C + R_F}\right) \frac{R_C}{r_e}$$

or
$$A_v = -\frac{(\cancel{R_C} + R_F - \cancel{R_C})R_C}{R_C + R_F \qquad r_e}$$

and
$$\boxed{A_v = -\left(\frac{R_F}{R_C + R_F}\right)\frac{R_C}{r_e}} \tag{5.52}$$

For $R_F \gg R_C$

$$\boxed{A_v \cong -\frac{R_C}{r_e}} \tag{5.53}$$

Phase Relationship The negative sign of Eq. (5.52) indicates a 180° phase shift between V_o and V_i.

Effect of r_o

Z_i A complete analysis without applying approximations results in

$$\boxed{Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{\beta r_e R_F} + \dfrac{R_C \| r_o}{R_F r_e}}} \tag{5.54}$$

Applying the condition $r_o \geq 10R_C$, we obtain

$$Z_i = \frac{1 + \dfrac{R_C}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C}{\beta r_e R_F} + \dfrac{R_C}{R_F r_e}} = \frac{r_e\left[1 + \dfrac{R_C}{R_F}\right]}{\dfrac{1}{\beta} + \dfrac{1}{R_F}\left[r_e + \dfrac{R_C}{\beta} + R_C\right]}$$

Applying $R_C \gg r_e$ and $\dfrac{R_C}{\beta}$,

$$Z_i \cong \frac{r_e\left[1 + \dfrac{R_C}{R_F}\right]}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} = \frac{r_e\left[\dfrac{R_F + R_C}{\cancel{R_F}}\right]}{\dfrac{R_F + \beta R_C}{\beta \cancel{R_F}}} = \frac{r_e}{\dfrac{1}{\beta}\left(\dfrac{R_F}{R_F + R_C}\right) + \dfrac{R_C}{R_C + R_F}}$$

but, since R_F typically $\gg R_C$, $R_F + R_C \cong R_F$ and $\dfrac{R_F}{R_F + R_C} = 1$

$$\boxed{Z_i \cong \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}}}_{r_o \gg R_C,\, R_F > R_C} \tag{5.55}$$

as obtained earlier.

Z_o Including r_o in parallel with R_C in Fig. 5.47 results in

$$\boxed{Z_o = r_o \| R_C \| R_F} \tag{5.56}$$

For $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C \| R_F}_{r_o \geq 10R_C} \tag{5.57}$$

as obtained earlier. For the common condition of $R_F \gg R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C, R_F \gg R_C} \tag{5.58}$$

A_v

$$\boxed{A_v = -\left(\frac{R_F}{R_C \| r_o + R_F}\right)\frac{R_C \| r_o}{r_e}} \tag{5.59}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v \cong -\left(\frac{R_F}{R_C + R_F}\right)\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.60}$$

and for $R_F \gg R_C$

$$\boxed{A_v \cong -\frac{R_C}{r_e}}_{r_o \geq 10R_C,\, R_F \geq R_C} \tag{5.61}$$

as obtained earlier.

EXAMPLE 5.9 For the network of Fig. 5.48. determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 20\text{ k}\Omega$ and compare results.

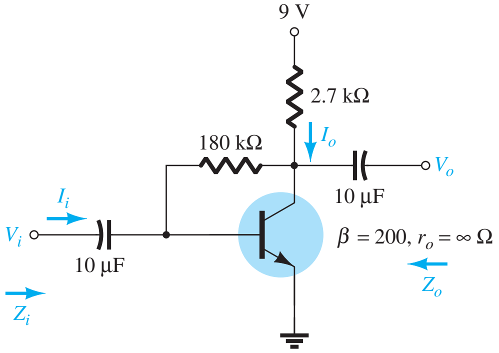


FIG. 5.48
Example 5.9.

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9\text{ V} - 0.7\text{ V}}{180\text{ k}\Omega + (200)2.7\text{ k}\Omega}$$
$$= 11.53\ \mu\text{A}$$
$$I_E = (\beta + 1)I_B = (201)(11.53\ \mu\text{A}) = 2.32\text{ mA}$$
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.32\text{ mA}} = \mathbf{11.21\ \Omega}$$

b. $$Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}} = \frac{11.21\ \Omega}{\dfrac{1}{200} + \dfrac{2.7\text{ k}\Omega}{182.7\text{ k}\Omega}} = \frac{11.21\ \Omega}{0.005 + 0.0148}$$
$$= \frac{11.21\ \Omega}{0.0198} = \mathbf{566.16\ \Omega}$$

c. $$Z_o = R_C \| R_F = 2.7\text{ k}\Omega \| 180\text{ k}\Omega = \mathbf{2.66\text{ k}\Omega}$$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{2.7\text{ k}\Omega}{11.21\ \Omega} = \mathbf{-240.86}$$

e. Z_i: The condition $r_o \geq 10R_C$ is *not* satisfied. Therefore,

$$Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{\beta r_e R_F} + \dfrac{R_C \| r_o}{R_F r_e}} = \frac{1 + \dfrac{2.7\text{ k}\Omega \| 20\text{ k}\Omega}{180\text{ k}\Omega}}{\dfrac{1}{(200)(11.21)} + \dfrac{1}{180\text{ k}\Omega} + \dfrac{2.7\text{ k}\Omega \| 20\text{ k}\Omega}{(200)(11.21\ \Omega)(180\text{ k}\Omega)} + \dfrac{2.7\text{ k}\Omega \| 20\text{ k}\Omega}{(180\text{ k}\Omega)(11.21\ \Omega)}}$$

$$= \frac{1 + \dfrac{2.38\text{ k}\Omega}{180\text{ k}\Omega}}{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 5.91 \times 10^{-6} + 1.18 \times 10^{-3}} = \frac{1 + 0.013}{1.64 \times 10^{-3}}$$

$$= \mathbf{617.7\ \Omega} \text{ vs. } 566.16\ \Omega \text{ above}$$

Z_o:

$$Z_o = r_o \| R_C \| R_F = 20\text{ k}\Omega \| 2.7\text{ k}\Omega \| 180\text{ k}\Omega$$
$$= \mathbf{2.35\ k\Omega} \text{ vs. } 2.66\text{ k}\Omega \text{ above}$$

A_v:

$$= -\left(\frac{R_F}{R_C \| r_o + R_F}\right)\frac{R_C \| r_o}{r_e} = -\left[\frac{180\text{ k}\Omega}{2.38\text{ k}\Omega + 180\text{ k}\Omega}\right]\frac{2.38\text{ k}\Omega}{11.21}$$
$$= -[0.987]212.3$$
$$= \mathbf{-209.54}$$

For the configuration of Fig. 5.49, Eqs. (5.61) through (5.63) determine the variables of interest. The derivations are left as an exercise at the end of the chapter.

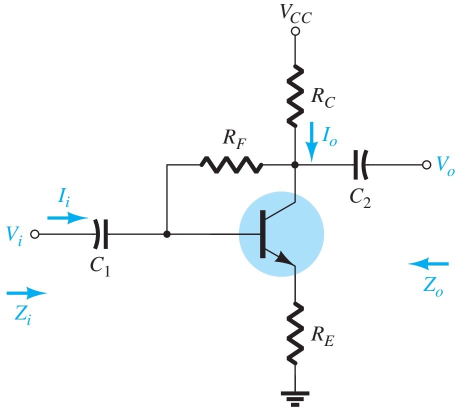


FIG. 5.49
Collector feedback configuration with an emitter resistor R_E.

Z_i

$$\boxed{Z_i \cong \frac{R_E}{\left[\dfrac{1}{\beta} + \dfrac{(R_E + R_C)}{R_F}\right]}} \tag{5.62}$$

Z_o

$$\boxed{Z_o = R_C \| R_F} \tag{5.63}$$

A_v

$$\boxed{A_v \cong -\frac{R_C}{R_E}} \tag{5.64}$$

5.11 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 5.50 has a dc feedback resistor for increased stability, yet the capacitor C_3 will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of R_F shifted to the input or output side will be determined by the desired ac input and output resistance levels.

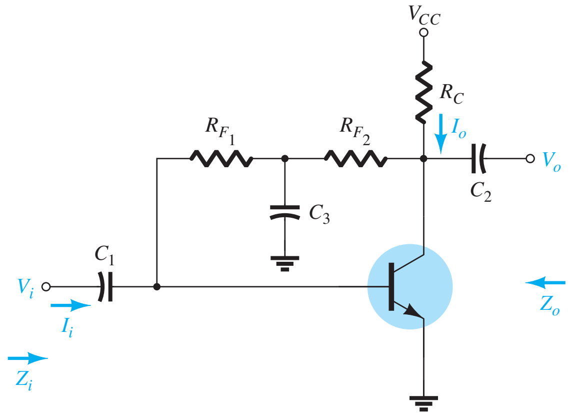


FIG. 5.50

Collector dc feedback configuration.

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 5.51.

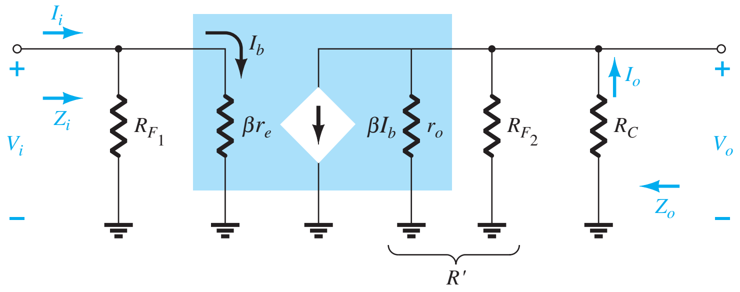


FIG. 5.51

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.50.

Z_i

$$\boxed{Z_i = R_{F_1} \| \beta r_e} \tag{5.65}$$

Z_o

$$\boxed{Z_o = R_C \| R_{F_2} \| r_o} \tag{5.66}$$

For $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C \| R_{F_2}}_{r_o \geq 10R_C} \tag{5.67}$$

A_v

$$R' = r_o \| R_{F_2} \| R_C$$

and
$$V_o = -\beta I_b R'$$

but
$$I_b = \frac{V_i}{\beta r_e}$$

and
$$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{r_o \| R_{F_2} \| R_C}{r_e}} \qquad \textbf{(5.68)}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_{F_2} \| R_C}{r_e}}_{r_o \geq 10R_C} \qquad \textbf{(5.69)}$$

Phase Relationship The negative sign in Eq. (5.68) clearly reveals a 180° phase shift between input and output voltages.

EXAMPLE 5.10 For the network of Fig. 5.52, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. V_o if $V_i = 2$ mV

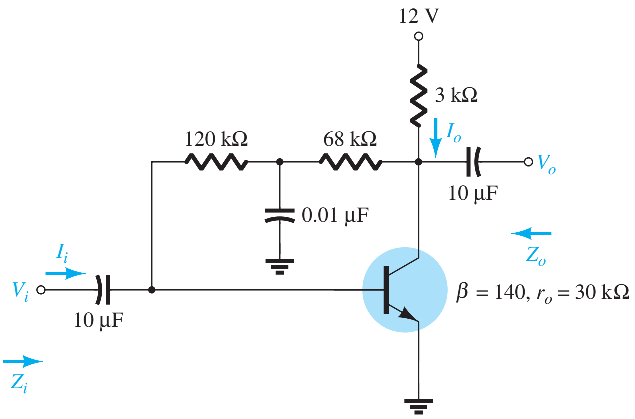


FIG. 5.52
Example 5.10.

Solution:

a. DC: $I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta R_C}$

$$= \frac{12\text{ V} - 0.7\text{ V}}{(120\text{ k}\Omega + 68\text{ k}\Omega) + (140)3\text{ k}\Omega}$$

$$= \frac{11.3\text{ V}}{608\text{ k}\Omega} = 18.6\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (141)(18.6\ \mu\text{A})$$
$$= 2.62\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = \mathbf{9.92\ \Omega}$$

b. $\beta r_e = (140)(9.92\ \Omega) = 1.39$ kΩ

The ac equivalent network appears in Fig. 5.53.

$Z_i = R_{F_1} \| \beta r_e = 120\text{ k}\Omega \| 1.39\text{ k}\Omega$

$\cong \mathbf{1.37\ k\Omega}$

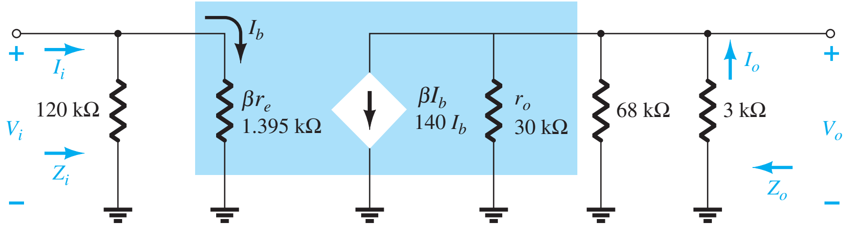


FIG. 5.53

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.52.

c. Testing the condition $r_o \geq 10R_C$, we find

$$30\text{ k}\Omega \geq 10(3\text{ k}\Omega) = 30\text{ k}\Omega$$

which is satisfied through the equals sign in the condition. Therefore,

$$Z_o \cong R_C \| R_{F_2} = 3\text{ k}\Omega \| 68\text{ k}\Omega$$
$$= \mathbf{2.87\text{ k}\Omega}$$

d. $r_o \geq 10R_C$; therefore,

$$A_v \cong -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68\text{ k}\Omega \| 3\text{ k}\Omega}{9.92\ \Omega}$$
$$\cong -\frac{2.87\text{ k}\Omega}{9.92\ \Omega}$$
$$\cong \mathbf{-289.3}$$

e. $|A_v| = 289.3 = \dfrac{V_o}{V_i}$

$$V_o = 289.3V_i = 289.3(2\text{ mV}) = \mathbf{0.579\text{ V}}$$

5.12 EFFECT OF R_L AND R_S

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load to the output terminal and the effect of using a source with an internal resistance will be investigated. The network of Fig. 5.54a is typical of those investigated in the previous section. Because a resistive load was not attached to the output terminal, the gain is commonly referred to as the no-load gain and given the following notation:

$$\boxed{A_{v_{\text{NL}}} = \frac{V_o}{V_i}} \tag{5.70}$$

In Fig. 5.54b a load has been added in the form of a resistor R_L, which will change the overall gain of the system. This loaded gain is typically given the following notation:

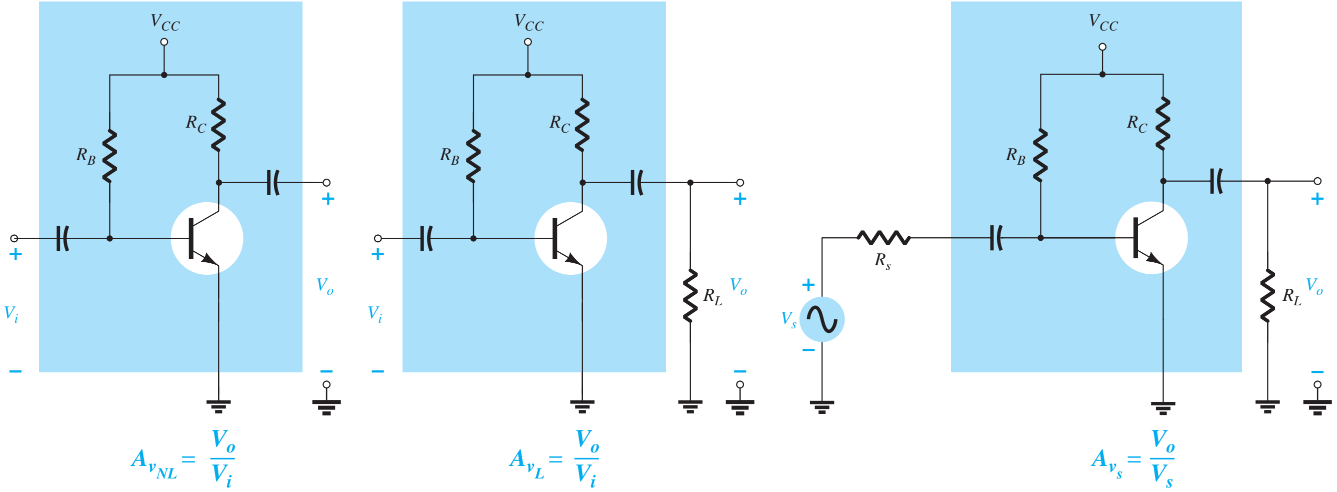
$$\boxed{A_{v_L} = \frac{V_o}{V_i}} \quad \text{with } R_L \tag{5.71}$$

In Fig. 5.54c both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation:

$$\boxed{A_{v_s} = \frac{V_o}{V_s}} \quad \text{with } R_L \text{ and } R_s \tag{5.72}$$

The analysis to follow will show that:

The loaded voltage gain of an amplifier is always less than the no-load gain.


V_{CC}
R_B
R_C
+
–
V_i
V_o
R_L
R_s
V_s
$A_{v_{NL}} = \frac{V_o}{V_i}$
$A_{v_L} = \frac{V_o}{V_i}$
$A_{v_s} = \frac{V_o}{V_s}$

(a) (b) (c)

FIG. 5.54

Amplifier configurations: (a) unloaded; (b) loaded; (c) loaded with a source resistance.

In other words, the addition of a load resistor R_L to the configuration of Fig. 5.54a will always have the effect of reducing the gain below the no-load level.

Furthermore:

The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.

In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is:

For the same configuration $A_{v_{NL}} > A_{v_L} > A_{v_s}$.

It will also be interesting to verify that:

For a particular design, the larger the level of R_L***, the greater is the level of ac gain.***

In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.

In addition:

For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.

In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain because the effect of R_s will essentially be eliminated.

For any network, such as those shown in Fig. 5.54 that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.

The conclusions listed above are all quite important in the amplifier design process. When one purchases a packaged amplifier, the listed gain and all the other parameters are for the *unloaded situation.* The gain that results due to the application of a load or source resistance can have a dramatic effect on all the amplifier parameters, as will be demonstrated in the examples to follow.

In general, there are two directions one can take to analyze networks with an applied load and/or source resistance. One approach is to simply insert the equivalent circuit, as was demonstrated in Section 5.11, and use methods of analysis to determine the quantities of interest. The second is to define a two-port equivalent model and use the parameters determined for the no-load situation. The analysis to follow in this section will use the first approach, leaving the second method for Section 5.14.

For the fixed-bias transistor amplifier of Fig. 5.54c, substituting the r_e equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig. 5.55.

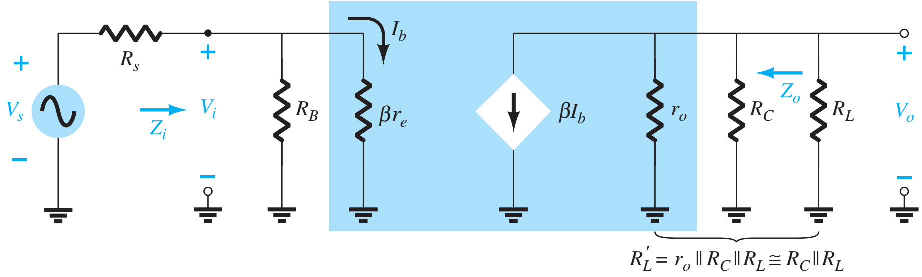


FIG. 5.55
The ac equivalent network for the network of Fig. 5.54c.

It is particularly interesting that Fig. 5.55 is exactly the same in appearance as Fig. 5.22 except that now there is a load resistance in parallel with R_C and a source resistance has been introduced in series with a source V_s.

The parallel combination of

$$R_L' = r_o \| R_C \| R_L \cong R_C \| R_L$$

and

$$V_o = -\beta I_b R_L' = -\beta I_b (R_C \| R_L)$$

with

$$I_b = \frac{V_i}{\beta r_e}$$

gives

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| R_L)$$

so that

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}} \tag{5.73}$$

The only difference in the gain equation using V_i as the input voltage is the fact that R_C of Eq. (5.10) has been replaced by the parallel combination of R_C and R_L. This makes good sense because the output voltage of Fig. 5.55 is now across the parallel combination of the two resistors.

The input impedance is

$$\boxed{Z_i = R_B \| \beta r_e} \tag{5.74}$$

as before, and the output impedance is

$$\boxed{Z_o = R_C \| r_o} \tag{5.75}$$

as before.

If the overall gain from signal source V_s to output voltage V_o is desired, it is only necessary to apply the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

or

$$A_{v_S} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_{v_L} \frac{Z_i}{Z_i + R_s}$$

so that

$$\boxed{A_{v_S} = \frac{Z_i}{Z_i + R_s} A_{v_L}} \tag{5.76}$$

Because the factor $Z_i/(Z_i + R_s)$ must always be less than one, Eq. (5.76) clearly supports the fact that the signal gain A_{v_S} is always less than the loaded gain A_{v_L}.

EXAMPLE 5.11 Using the parameter values for the fixed-bias configuration of Example 5.1 with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values:

a. A_{v_L}.
b. A_{v_s}.
c. Z_i.
d. Z_o.

Solution:

a. Eq. (5.73): $A_{v_L} = -\dfrac{R_C \| R_L}{r_e} = -\dfrac{3\text{ k}\Omega \| 4.7\text{ k}\Omega}{10.71\ \Omega} = -\dfrac{1.831\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-170.98}$

which is significantly less than the no-load gain of −280.11.

b. Eq. (5.76): $A_{v_s} = \dfrac{Z_i}{Z_i + R_s} A_{v_L}$

With $Z_i = 1.07\text{ k}\Omega$ from Example 5.1, we have

$$A_{v_s} = \frac{1.07\text{ k}\Omega}{1.07\text{ k}\Omega + 0.3\text{ k}\Omega}(-170.98) = \mathbf{-133.54}$$

which again is significantly less than $A_{v_{\text{NL}}}$ or A_{v_L}.

c. $Z_i = \mathbf{1.07\text{ k}\Omega}$ as obtained for the no-load situation.

d. $Z_o = R_C = \mathbf{3\text{ k}\Omega}$ as obtained for the no-load situation.

The example clearly demonstrates that $A_{v_{\text{NL}}} > A_{v_L} > A_{v_s}$.

For the voltage-divider configuration of Fig. 5.56 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.57.

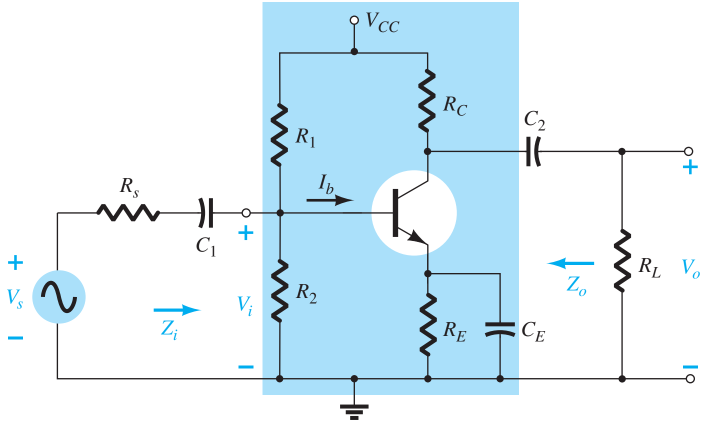


FIG. 5.56

Voltage-divider bias configuration with R_s and R_L.

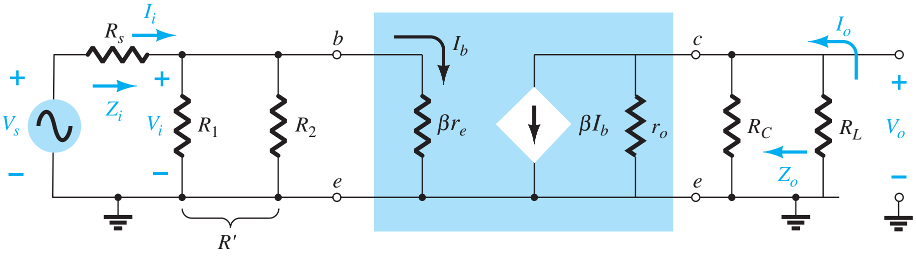


FIG. 5.57

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.56.

First note the strong similarities with Fig. 5.55, with the only difference being the parallel connection of R_1 and R_2 instead of just R_B. Everything else is exactly the same. The following equations result for the important parameters of the configuration:

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}} \tag{5.77}$$

$$\boxed{Z_i = R_1 \| R_2 \| \beta r_e} \tag{5.78}$$

$$\boxed{Z_o = R_C \| r_o} \tag{5.79}$$

For the emitter-follower configuration of Fig. 5.58 the small-signal ac equivalent network is as shown in Fig. 5.59. The only difference between Fig. 5.59 and the unloaded configuration of Fig. 5.37 is the parallel combination of R_E and R_L and the addition of the source resistor R_s. The equations for the quantities of interest can therefore be determined by simply replacing R_E by $R_E \| R_L$ wherever R_E appears. If R_E does not appear in an equation, the load resistor R_L does not affect that parameter. That is,

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}} \tag{5.80}$$

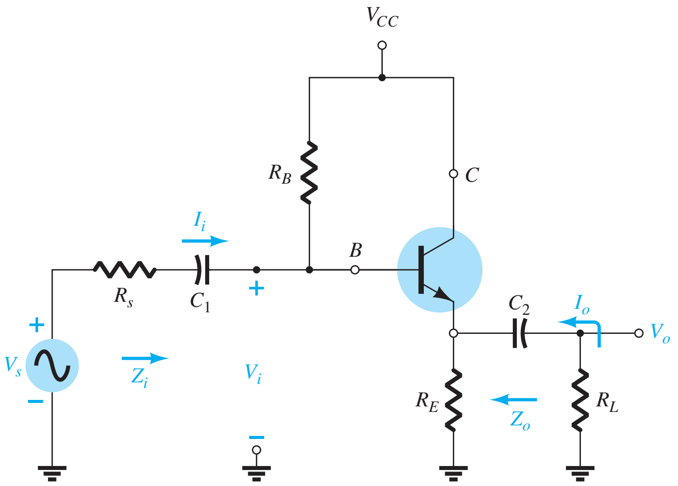


FIG. 5.58

Emitter-follower configuration with R_s and R_L.

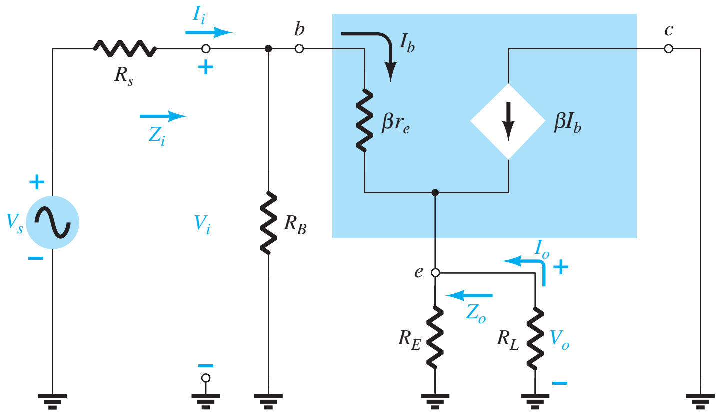


FIG. 5.59

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.58.

$$\boxed{Z_i = R_B \| Z_b} \tag{5.81}$$

$$\boxed{Z_b \cong \beta(R_E \| R_L)} \tag{5.82}$$

$$\boxed{Z_o \cong r_e} \tag{5.83}$$

The effect of a load resistor and a source impedance on the remaining BJT configurations will not be examined in detail here, although Table 5.1 in Section 5.14 will review the results for each configuration.

5.13 DETERMINING THE CURRENT GAIN

You may have noticed in the previous sections that the current gain was not determined for each configuration. Earlier editions of this text did have the details of finding that gain, but in reality the voltage gain is usually the gain of most importance. The absence of the derivations should not cause concern because:

For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 5.60.

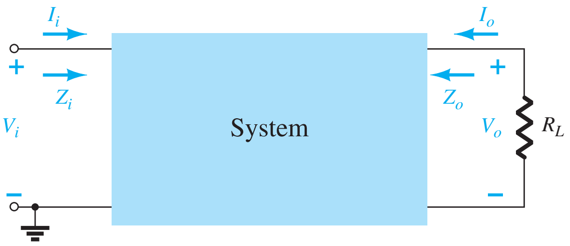


FIG. 5.60
Determining the current gain using the voltage gain.

The current gain is defined by

$$A_i = \frac{I_o}{I_i} \tag{5.84}$$

Applying Ohm's law to the input and output circuits results in

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration.

Substituting into Eq. (5.84) then results in

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\dfrac{V_o}{R_L}}{\dfrac{V_i}{Z_i}} = -\frac{V_o}{V_i} \cdot \frac{Z_i}{R_L}$$

and the following important equation:

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}} \tag{5.85}$$

The value of R_L is defined by the location of V_o and I_o.

To demonstrate the validity of Eq. (5.82), consider the voltage-divider bias configuration of Fig. 5.28.

Using the results of Example 5.2, we find

$$I_i = \frac{V_i}{Z_i} = \frac{V_i}{1.35\ \text{k}\Omega} \text{ and } I_o = -\frac{V_o}{R_L} = -\frac{V_o}{6.8\ \text{k}\Omega}$$

so that
$$A_{i_L} = \frac{I_o}{I_i} = \frac{\left(-\dfrac{V_o}{6.8\ \text{k}\Omega}\right)}{\dfrac{V_i}{1.35\ \text{k}\Omega}} = -\left(\frac{V_o}{V_i}\right)\left(\frac{1.35\ \text{k}\Omega}{6.8\ \text{k}\Omega}\right)$$

$$= -(-368.76)\left(\frac{1.35\ \text{k}\Omega}{6.8\ \text{k}\Omega}\right) = \mathbf{73.2}$$

Using Eq. 5.82:
$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = -(-368.76)\left(\frac{1.35\ \text{k}\Omega}{6.8\ \text{k}\Omega}\right) = \mathbf{73.2}$$

which has the same format as the resulting equation above and the same result.

The solution to the current gain in terms of the network parameters will be more complicated for some configurations if a solution is desired in terms of the network parameters. However, if a numerical solution is all that is desired, it is simply a matter of substituting the value of the three parameters from an analysis of the voltage gain.

As a second example, consider the common-base bias configuration of Section 5.9. In this case the voltage gain is

$$A_{v_L} \cong \frac{R_C}{r_e}$$

and the input impedance is

$$Z_i \cong R_E \| r_e \cong r_e$$

with R_L defined as R_C due to the location of I_o.

The result is the following:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = \left(-\frac{\cancel{R_C}}{\cancel{r_e}}\right)\left(\frac{\cancel{r_e}}{\cancel{R_C}}\right) \cong -1$$

which agrees with the solution of that section because $I_c \cong I_e$. Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

5.14 SUMMARY TABLES

The last few sections have included a number of derivations for unloaded and loaded BJT configurations. The material is so extensive that it seemed appropriate to review most of the conclusions for the various configurations in summary tables for quick comparisons. Although the equations using the hybrid parameters have not been discussed in detail at this point, they are included to make the tables complete. The use of hybrid parameters will be considered in a later section of this chapter. In each case the waveforms included demonstrate the phase relationship between input and output voltages. They also reveal the relative magnitude of the voltages at the input and output terminals.

Table 5.1 is for the unloaded situation, whereas Table 5.2 includes the effect of R_s and R_L.

5.15 TWO-PORT SYSTEMS APPROACH

In the design process, it is often necessary to work with the terminal characteristics of a device rather then the individual components of the system. In other words, the designer is handed a packaged product with a list of data regarding its characteristics but has no access to the internal construction. This section will relate the important parameters determined for a number of configurations in the previous sections to the important parameters of this packaged system. The result will be an understanding of how each parameter of the

TABLE 5.1

Unloaded BJT Transistor Amplifiers

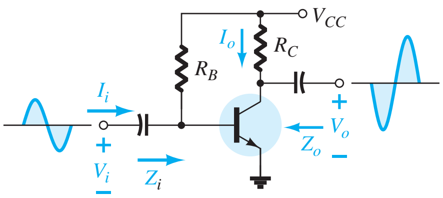
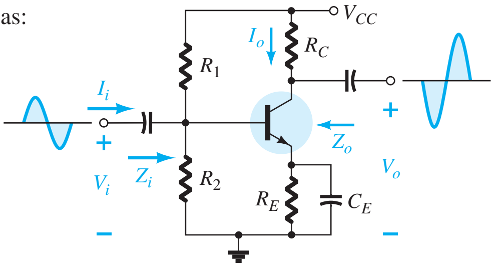
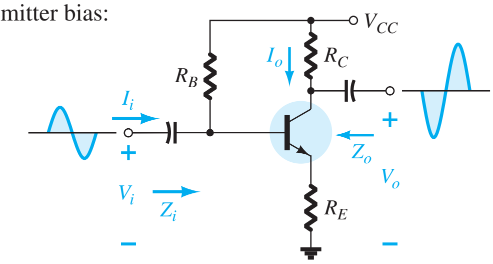
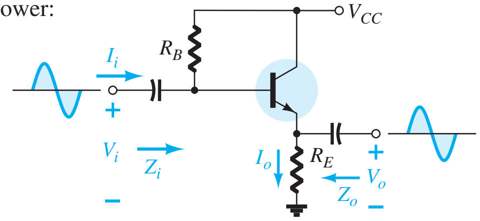
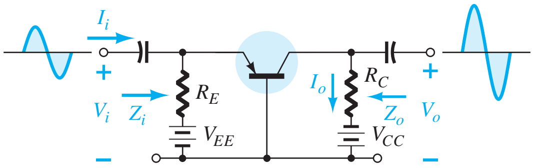
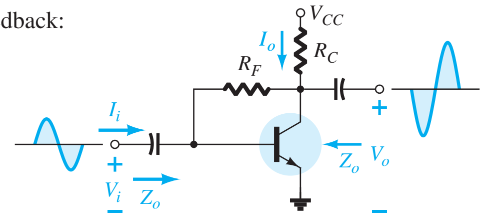
Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias:  V_{CC} I_o R_C R_B I_i + V_o Z_o − + V_i − Z_i	Medium (1 kΩ) $= \boxed{R_B \parallel \beta r_e}$ $\cong \boxed{\beta r_e}$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= \boxed{R_C \parallel r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{(R_C \parallel r_o)}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (100) $= \boxed{\frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$ $\cong \boxed{\beta}$ $(r_o \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias:  V_{CC} I_o R_C R_1 I_i + + Z_o V_i Z_i V_o R_2 R_E C_E − −	Medium (1 kΩ) $= \boxed{R_1 \parallel R_2 \parallel \beta r_e}$	Medium (2 kΩ) $= \boxed{R_C \parallel r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{R_C \parallel r_o}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (50) $= \boxed{\frac{\beta(R_1 \parallel R_2) r_o}{(r_o + R_C)(R_1 \parallel R_2 + \beta r_e)}}$ $\cong \boxed{\frac{\beta(R_1 \parallel R_2)}{R_1 \parallel R_2 + \beta r_e}}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias:  V_{CC} R_C I_o R_B I_i + + Z_o V_o V_i Z_i R_E − −	High (100 kΩ) $= \boxed{R_B \parallel Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \parallel \beta R_E}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$ (any level of r_o)	Low (−5) $= \boxed{-\frac{R_C}{r_e + R_E}}$ $\cong \boxed{-\frac{R_C}{R_E}}$ $(R_E \gg r_e)$	High (50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Emitter-follower:  V_{CC} R_B I_i + V_i Z_i I_o R_E + V_o Z_o − −	High (100 kΩ) $= \boxed{R_B \parallel Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \parallel \beta R_E}$ $(R_E \gg r_e)$	Low (20 Ω) $= \boxed{R_E \parallel r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Low (≅1) $= \boxed{\frac{R_E}{R_E + r_e}}$ $\cong \boxed{1}$	High (−50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Common-base:  I_i + R_E V_i Z_i V_{EE} − I_o R_C + Z_o V_o V_{CC} −	Low (20 Ω) $= \boxed{R_E \parallel r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$	High (200) $\cong \boxed{\frac{R_C}{r_e}}$	Low (−1) $\cong \boxed{-1}$
Collector feedback:  V_{CC} I_o R_C R_F I_i + + Z_o V_o V_i Z_o − −	Medium (1 kΩ) $= \boxed{\frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong \boxed{R_C \parallel R_F}$ $(r_o \geq 10R_C)$	High (−200) $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \boxed{\frac{\beta R_F}{R_F + \beta R_C}}$ $\cong \boxed{\frac{R_F}{R_C}}$

TABLE 5.2

BJT Transistor Amplifiers Including the Effect of R_s and R_L

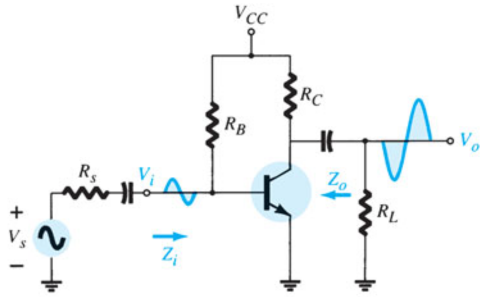
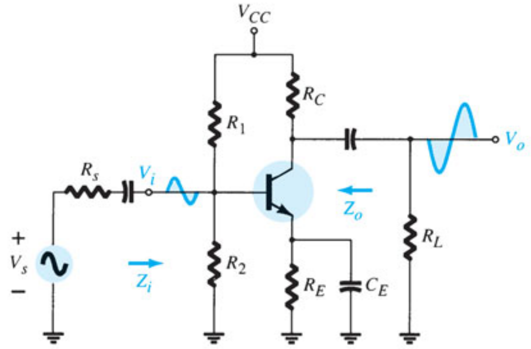
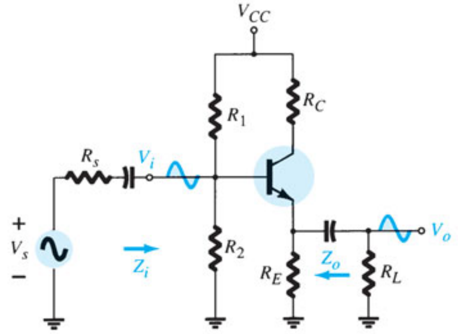
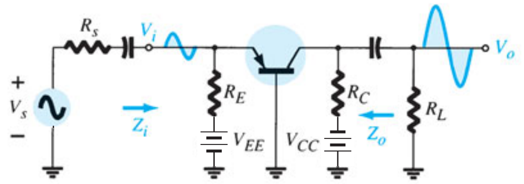
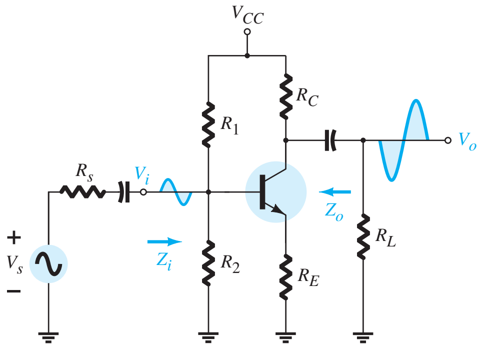
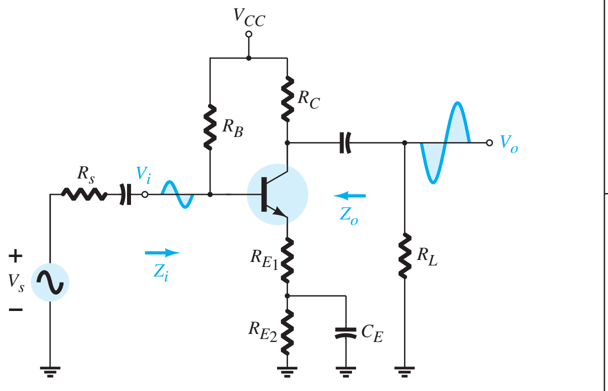
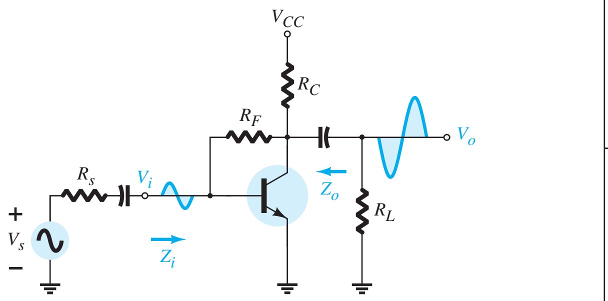
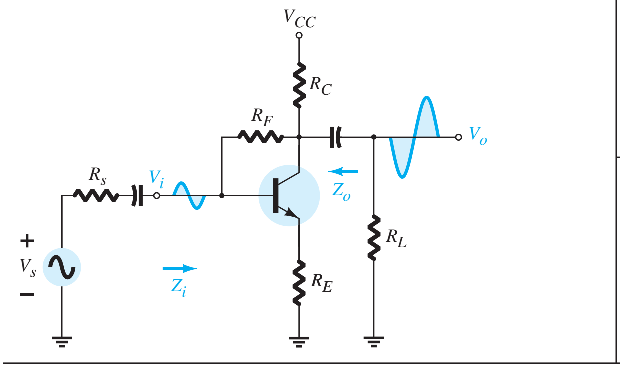
Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
 V_{CC} R_C R_B V_o R_s V_i Z_o R_L + V_s − Z_i	$-\dfrac{(R_L \| R_C)}{r_e}$	$R_B \| \beta r_e$	R_C
	Including r_o: $-\dfrac{(R_L \| R_C \| r_o)}{r_e}$	$R_B \| \beta r_e$	$R_C \| r_o$
 V_{CC} R_C R_1 V_o R_s V_i Z_o R_L + V_s − Z_i R_2 R_E C_E	$-\dfrac{(R_L \| R_C)}{r_e}$	$R_1 \| R_2 \| \beta r_e$	R_C
	Including r_o: $-\dfrac{(R_L \| R_C \| r_o)}{r_e}$	$R_1 \| R_2 \| \beta r_e$	$R_C \| r_o$
 V_{CC} R_1 R_C R_s V_i + V_s − Z_i R_2 R_E Z_o V_o R_L	$\cong 1$	$R'_E = R_L \| R_E$ $R_1 \| R_2 \| \beta(r_e + R'_E)$	$R'_s = R_s \| R_1 \| R_2$ $R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$
	Including r_o: $\cong 1$	$R_1 \| R_2 \| \beta(r_e + R'_E)$	$R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$
 R_s V_i V_o + V_s − Z_i R_E V_{EE} V_{CC} R_C Z_o R_L	$\cong -\dfrac{(R_L \| R_C)}{r_e}$	$R_E \| r_e$	R_C
	Including r_o: $\cong -\dfrac{(R_L \| R_C \| r_o)}{r_e}$	$R_E \| r_e$	$R_C \| r_o$
 V_{CC} R_C R_1 V_o R_s V_i Z_o + V_s − Z_i R_2 R_E R_L	$-\dfrac{(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_E)$	R_C
	Including r_o: $-\dfrac{(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_e)$	$\cong R_C$

TABLE 5.2 *(Continued)*

BJT Transistor Amplifiers Including the Effect of R_s and R_L

Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
 V_{CC} R_C R_B V_o R_s V_i Z_o + V_s − Z_i R_{E1} R_L R_{E2} C_E	$\frac{-(R_L\|R_C)}{R_{E_1}}$	$R_B\|\beta(r_e + R_{E_1})$	R_C
	Including r_o: $\frac{-(R_L\|R_C)}{R_{E_t}}$	$R_B\|\beta(r_e + R_E)$	$\cong R_C$
 V_{CC} R_C R_F V_o R_s V_i Z_o + V_s − R_L Z_i	$\frac{-(R_L\|R_C)}{r_e}$	$\beta r_e\|\frac{R_F}{\|A_v\|}$	R_C
	Including r_o: $\frac{-(R_L\|R_C\|r_o)}{r_e}$	$\beta r_e\|\frac{R_F}{\|A_v\|}$	$R_C\|R_F\|r_o$
 V_{CC} R_C R_F V_o R_s V_i Z_o + V_s − R_L Z_i R_E	$\frac{-(R_L\|R_C)}{R_E}$	$\beta R_E\|\frac{R_F}{\|A_v\|}$	$\cong R_C\|R_F$
	Including r_o: $\cong \frac{-(R_L\|R_C)}{R_E}$	$\cong \beta R_E\|\frac{R_F}{\|A_v\|}$	$\cong R_C\|R_F$

packaged system relates to the actual amplifier or network. The system of Fig. 5.61 is called a two-port system because there are two sets of terminals—one at the input and the other at the output. At this point it is particularly important to realize that

the data surrounding a packaged system is the no-load data.

This should be fairly obvious because the load has not been applied, nor does it come with the load attached to the package.

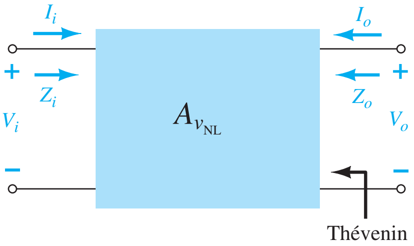

I_i
I_o
+
Z_i
V_i
−
$A_{v_{NL}}$
+
Z_o
V_o
−
Thévenin

FIG. 5.61

Two-port system.

For the two-port system of Fig. 5.61 the polarity of the voltages and the direction of the currents are as defined. If the currents have a different direction or the voltages have a different polarity from that appearing in Fig. 5.61, a negative sign must be applied. Note again the use of the label $A_{v_{\text{NL}}}$ to indicate that the provided voltage gain will be the no-load value.

For amplifiers the parameters of importance have been sketched within the boundaries of the two-port system as shown in Fig. 5.62. The input and output resistance of a packaged amplifier are normally provided along with the no-load gain. They can then be inserted as shown in Fig. 5.62 to represent the seated package.

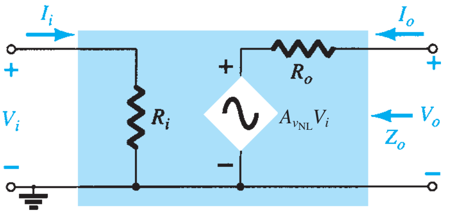


FIG. 5.62
Substituting the internal elements for the two-port system of Fig. 5.61.

For the no-load situation the output voltage is

$$\boxed{V_o = A_{v_{\text{NL}}}V_i} \tag{5.86}$$

due to the fact that $I = 0A$, resulting in $I_oR_o = 0V$.

The output resistance is defined by $V_i = 0V$. Under such conditions the quantity $A_{v_{\text{NL}}}V_i$ is zero volts also and can be replaced by a short-circuit equivalent. The result is

$$\boxed{Z_o = R_o} \tag{5.87}$$

Finally, the input impedance Z_i simply relates the applied voltage to the resulting input current and

$$\boxed{Z_i = R_i} \tag{5.88}$$

For the no-load situation, the current gain is undefined because the load current is zero. There is, however, a no-load voltage gain equal to $A_{v_{\text{NL}}}$.

The effect of applying a load to a two-port system will result in the configuration of Fig. 5.63. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance. In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once $A_{v_{\text{NL}}}$, R_i, and R_o are defined for a particular configuration, the equations about to be derived can be employed.

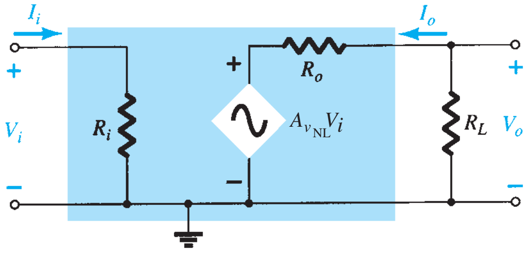


FIG. 5.63
Applying a load to the two-port system of Fig. 5.62.

Applying the voltage-divider rule to the output circuit results in

$$V_o = \frac{R_L A_{v_{\text{NL}}} V_i}{R_L + R_o}$$

and

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}} \tag{5.89}$$

Because the ratio $R_L/(R_L + R_o)$ is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level.

The current gain is then determined by

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

and

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}} \tag{5.90}$$

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters Z_i and R_L. The next example will demonstrate the usefulness and validity of Eqs. (5.89) and (5.90).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 5.64, a source with an internal resistance has been applied to the basic two-port system. The definitions of Z_i and $A_{v_{\text{NL}}}$ are such that:

The parameters Z_i and $A_{v_{\text{NL}}}$ of a two-port system are unaffected by the internal resistance of the applied source.

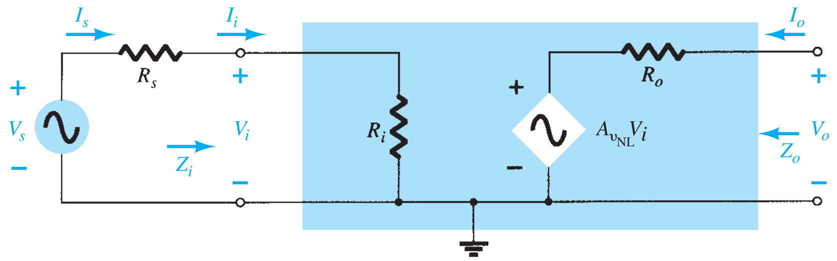


FIG. 5.64

Including the effects of the source resistance R_s.

However:

The output impedance may be affected by the magnitude of R_s.

The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 5.64 is determined by the voltage-divider rule. That is,

$$\boxed{V_i = \frac{R_i V_s}{R_i + R_s}} \tag{5.91}$$

Equation (5.91) clearly shows that the larger the magnitude of R_s, the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system.

For the two-port system of Fig. 5.64,

$$V_o = A_{v_{\text{NL}}} V_i$$

and

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

so that

$$V_o = A_{v_{\mathrm{NL}}} \frac{R_i}{R_i + R_s} V_s$$

and

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{\mathrm{NL}}}} \tag{5.92}$$

The effects of R_s and R_L have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 5.65, a source with an internal resistance R_s and a load R_L have been applied to a two-port system for which the parameters Z_i, $A_{v_{\mathrm{NL}}}$, and Z_o have been specified. For the moment, let us assume that Z_i and Z_o are unaffected by R_L and R_s, respectively.

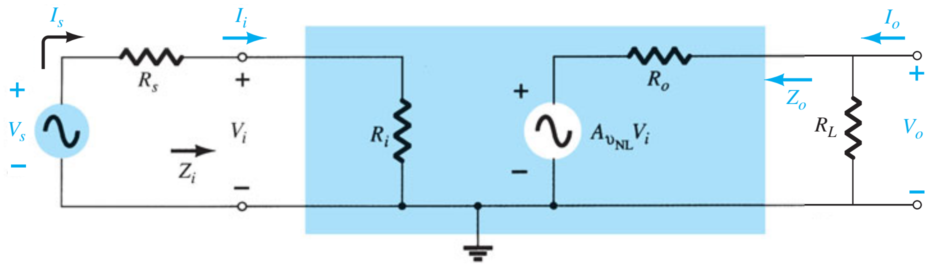


FIG. 5.65

Considering the effects of R_s and R_L on the gain of an amplifier.

At the input side we find

$$\text{Eq. (5.91):}\quad V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}} \tag{5.93}$$

and at the output side,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{\mathrm{NL}}} V_i$$

or

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{\mathrm{NL}}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{\mathrm{NL}}} \tag{5.94}$$

For the total gain $A_{v_s} = V_o/V_s$, the following mathematical steps can be performed:

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}} \tag{5.95}$$

and substituting Eqs. (5.93) and (5.94) results in

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{\mathrm{NL}}}} \tag{5.96}$$

Because $I_i = V_i/R_i$, as before,

$$\boxed{A_{i_L} = -A_{v_L} \frac{R_i}{R_L}} \tag{5.97}$$

or, using $I_s = V_s/(R_s + R_i)$,

$$\boxed{A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}} \tag{5.98}$$

However, $I_i = I_s$, so Eqs. (5.97) and (5.98) generate the same result. Equation (5.96) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (5.96) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that R_s is relatively small if the effect of the magnitude of R_L is ignored. For instance, in Eq. (5.96), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to $(0.9)(0.2) = 0.18$, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be $(0.9)(0.9) = 0.81$, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of R_s and R_L must be evaluated individually and as a product.

EXAMPLE 5.12 Determine A_{v_L} and A_{v_s} for the network of Example 5.11 and compare solutions. Example 5.1 showed that $A_{v_{\text{NL}}} = -280$, $Z_i = 1.07\ \text{k}\Omega$, and $Z_o = 3\ \text{k}\Omega$. In Example 5.11, $R_L = 4.7\ \text{k}\Omega$ and $R_s = 0.3\ \text{k}\Omega$.

Solution:

a. Eq. (5.89): $$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}$$
$$= \frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$
$$= \mathbf{-170.98}$$

as in Example 5.11.

b. Eq. (5.96): $$A_{v_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}$$
$$= \frac{1.07\ \text{k}\Omega}{1.07\ \text{k}\Omega + 0.3\ \text{k}\Omega} \cdot \frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$
$$= (0.781)(0.610)(-280.11)$$
$$= \mathbf{-133.45}$$

as in Example 5.11.

EXAMPLE 5.13 Given the packaged (no-entry-possible) amplifier of Fig. 5.66:

a. Determine the gain A_{v_L} and compare it to the no-load value with $R_L = 1.2\ \text{k}\Omega$.
b. Repeat part (a) with $R_L = 5.6\ \text{k}\Omega$ and compare solutions.
c. Determine A_{v_s} with $R_L = 1.2\ \text{k}\Omega$.
d. Find the current gain $A_i = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s}$ with $R_L = 5.6\ \text{k}\Omega$.

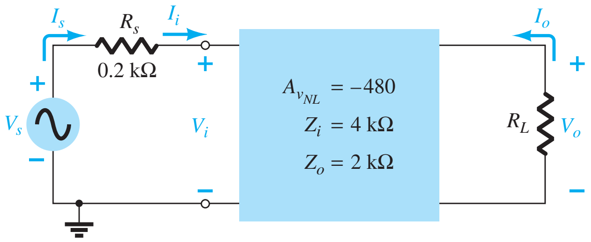


FIG. 5.66
Amplifier for Example 5.13.

Solution:

a. Eq. (5.89): $$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}} = \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.375)(-480) = \mathbf{-180}$$

which is a dramatic drop from the no-load value.

b. Eq. (5.89): $$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}} = \frac{5.6\ \text{k}\Omega}{5.6\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.737)(-480) = \mathbf{-353.76}$$

which clearly reveals that the larger the load resistor, the better is the gain.

c. Eq. (5.96): $$A_{v_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}} = \frac{4\ \text{k}\Omega}{4\ \text{k}\Omega + 0.2\ \text{k}\Omega} \cdot \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.952)(0.375)(-480) = \mathbf{-171.36}$$

which is fairly close to the loaded gain A_v because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

d. $$A_{i_L} = \frac{I_o}{I_i} = \frac{I_o}{I_s} = -A_{v_L}\frac{Z_i}{R_L} = -(-353.76)\left(\frac{4\ \text{k}\Omega}{5.6\ \text{k}\Omega}\right) = -(-353.76)(0.714) = \mathbf{252.6}$$

It is important to realize that when using the two-port equations in some configurations the input impedance is sensitive to the applied load (such as the emitter-follower and collector feedback) and in some the output impedance is sensitive to the applied source resistance (such as the emitter-follower). In such cases the no-load parameters for Z_i and Z_o have to first be calculated before substituting into the two-port equations. For most packaged systems such as op-amps this sensitivity of the input and output parameters to the applied load or source resistance is minimized to eliminate the need to be concerned about changes from the no-load levels when using the two-port equations.

5.16 CASCADED SYSTEMS

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 5.67, where $A_{v_1}, A_{v_2}, A_{v_3}$, and so on, are the voltage gains of each stage *under loaded conditions.* That is, A_{v_1} is determined with the *input impedance to A_{v_2} acting as the load on A_{v_1}.* For A_{v_2}, A_{v_1} will determine the signal strength and source impedance at the input to A_{v_2}. The total gain of the system is then determined by the product of the individual gains as follows:

$$\boxed{A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots} \tag{5.99}$$

and the total current gain is given by

$$\boxed{A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L}} \tag{5.100}$$

No matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where A_{v_1}, A_{v_2}, and so on, of Fig. 5.67 are simply the no-load values. The no-load parameters can be used to determine the loaded gains of each stage, but Eq. (5.99) requires the loaded values. The load on stage 1 is Z_{i_2}, on stage 2 Z_{i_3}, on stage 3 Z_{i_n}, and so on.

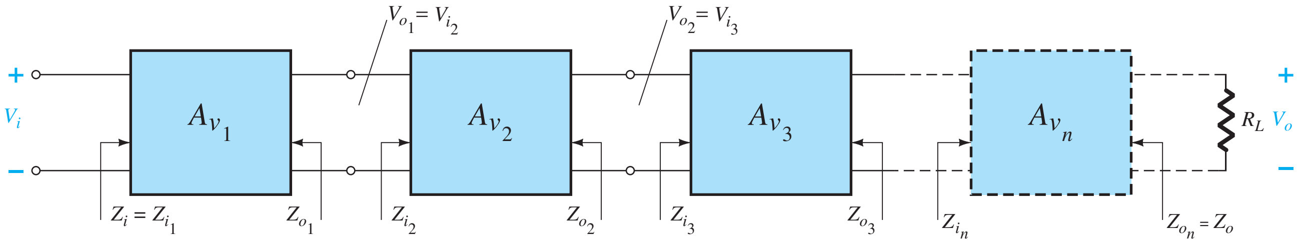

$V_{o_1} = V_{i_2}$
$V_{o_2} = V_{i_3}$
+
V_i
–
A_{v_1}
A_{v_2}
A_{v_3}
A_{v_n}
R_L
V_o
+
–
$Z_i = Z_{i_1}$
Z_{o_1}
Z_{i_2}
Z_{o_2}
Z_{i_3}
Z_{o_3}
Z_{i_n}
$Z_{o_n} = Z_o$

FIG. 5.67
Cascaded system.

EXAMPLE 5.14 The two-stage system of Fig. 5.68 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 5.68, the no-load values are provided for each system, with the exception of Z_i and Z_o for the emitter-follower, which are the loaded values. For the configuration of Fig. 5.68, determine:

a. The loaded gain for each stage.
b. The total gain for the system, A_v and A_{v_s}.
c. The total current gain for the system.
d. The total gain for the system if the emitter-follower configuration were removed.

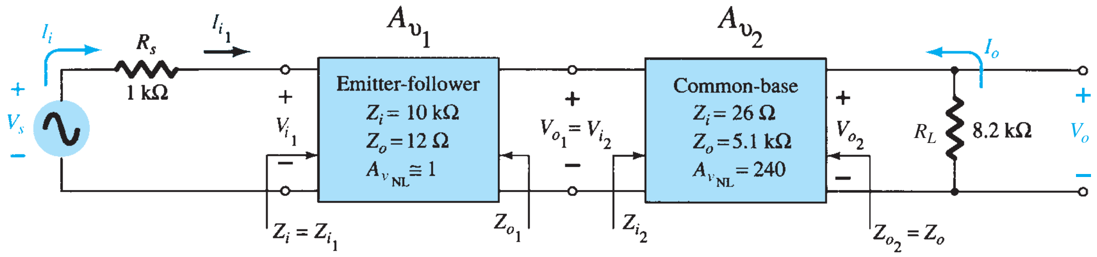

I_i
R_s
1 kΩ
I_{i_1}
+
V_s
–
+
V_{i_1}
–
A_{v_1}
Emitter-follower
$Z_i = 10$ kΩ
$Z_o = 12$ Ω
$A_{v_{NL}} \cong 1$
+
$V_{o_1} = V_{i_2}$
–
A_{v_2}
Common-base
$Z_i = 26$ Ω
$Z_o = 5.1$ kΩ
$A_{v_{NL}} = 240$
+
V_{o_2}
–
I_o
R_L
8.2 kΩ
+
V_o
–
$Z_i = Z_{i_1}$
Z_{o_1}
Z_{i_2}
$Z_{o_2} = Z_o$

FIG. 5.68
Example 5.14.

Solution:

a. For the emitter-follower configuration, the loaded gain is (by Eq. (5.94))

$$V_{o_1} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{v_{NL}} V_{i_1} = \frac{26\ \Omega}{26\ \Omega + 12\ \Omega}(1)\, V_{i_1} = 0.684\, V_{i_1}$$

and $$A_{V_i} = \frac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$$

For the common-base configuration,

$$V_{o_2} = \frac{R_L}{R_L + R_{o_2}} A_{v_{NL}}\, V_{i_2} = \frac{8.2\ \text{k}\Omega}{8.2\ \text{k}\Omega + 5.1\ \text{k}\Omega}(240)\, V_{i_2} = 147.97\, V_{i_2}$$

and $$A_{v_2} = \frac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$$

b. Eq. (5.99): $$\begin{aligned} A_{v_T} &= A_{v_1} A_{v_2} \\ &= (0.684)(147.97) \\ &= \mathbf{101.20} \end{aligned}$$

$$\text{Eq. (5.91):}\quad A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s}A_{v_T} = \frac{(10\text{ k}\Omega)(101.20)}{10\text{ k}\Omega + 1\text{ k}\Omega}$$

$$= \mathbf{92}$$

$$\text{c. Eq. (5.100):}\quad A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\text{ k}\Omega}{8.2\text{ k}\Omega}\right)$$

$$= \mathbf{-123.41}$$

$$\text{d. Eq. (5.91):}\quad V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s}V_s = \frac{26\ \Omega}{26\ \Omega + 1\text{ k}\Omega}V_s = 0.025\ V_s$$

$$\text{and}\qquad \frac{V_i}{V_s} = 0.025 \qquad \text{with} \qquad \frac{V_o}{V_i} = 147.97 \qquad \text{from above}$$

$$\text{and}\qquad A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by the voltage-divider action.

RC-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.69 in the next example. The name is derived from the capacitive coupling capacitor C_c and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

EXAMPLE 5.15

a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.69.
b. Calculate the overall gain and output voltage if a 4.7 kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

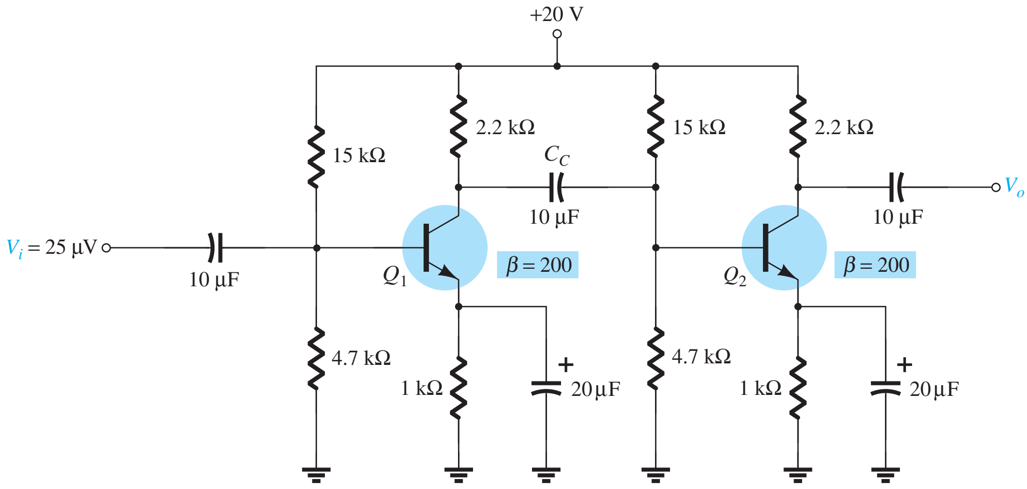


FIG. 5.69

RC-coupled BJT amplifier for Example 5.15.

Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.8\text{ V},\quad V_E = 4.1\text{ V},\quad V_C = 11\text{ V},\quad I_E = 4.1\text{ mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.1\text{ mA}} = 6.34\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$\begin{aligned} A_{v_1} &= -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e} \\ &= -\frac{(2.2\text{ k}\Omega) \| [15\text{ k}\Omega \| 4.7\text{ k}\Omega \| (200)(6.34\ \Omega)]}{6.34\ \Omega} \\ &= -\frac{659.2\ \Omega}{6.34\ \Omega} = -104 \end{aligned}$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.34\ \Omega} = -347$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-104)(-347) \cong \mathbf{36.1 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (36.1 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{902.5\ mV}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega}(36.1 \times 10^3) \cong \mathbf{24.6 \times 10^3}$$

which is considerably less than the unloaded gain because R_L is relatively close to R_C.

$$\begin{aligned} V_o &= A_{v_T} V_i \\ &= (24.6 \times 10^3)(25\ \mu\text{V}) \\ &= \mathbf{615\ mV} \end{aligned}$$

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\text{ k}\Omega \| 15\text{ k}\Omega \| (200)(6.34\ \Omega) = \mathbf{0.94\ k\Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\ k\Omega}$$

Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.70; the second is shown in Fig. 5.71 in the following example.

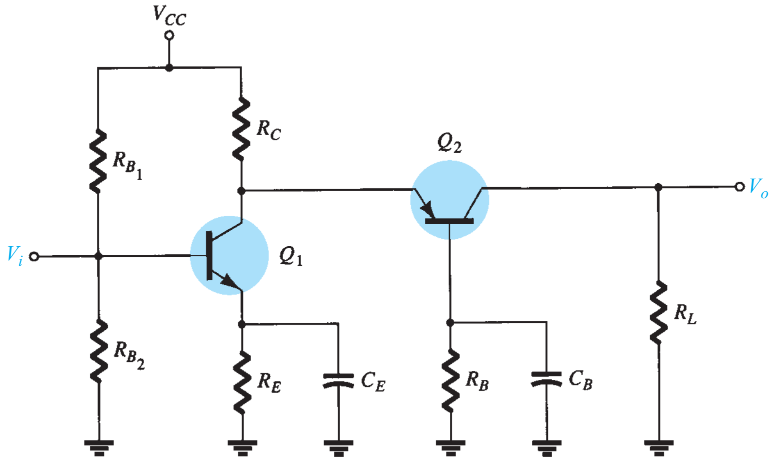


FIG. 5.70

Cascode configuration.

The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance (to be discussed in Section 9.9) is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

EXAMPLE 5.16 Calculate the no-load voltage gain for the cascode configuration of Fig. 5.71.

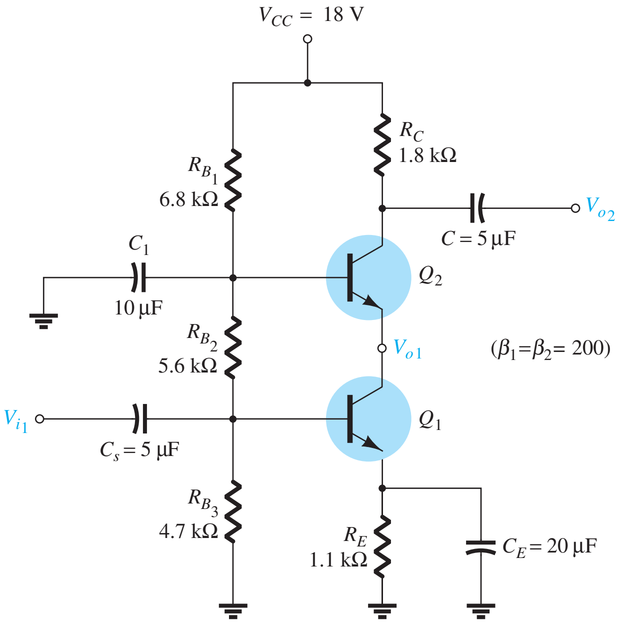

$V_{CC} = 18$ V
R_C 1.8 kΩ
R_{B_1} 6.8 kΩ
V_{o_2}
$C = 5\,\mu$F
C_1
10 µF
Q_2
R_{B_2} 5.6 kΩ
V_{o1}
(β_1=β_2= 200)
V_{i_1}
Q_1
$C_s = 5\,\mu$F
R_{B_3} 4.7 kΩ
R_E 1.1 kΩ
$C_E = 20\,\mu$F

FIG. 5.71

Practical cascode circuit for Example 5.16.

Solution: The dc analysis results in

$$V_{B_1} = 4.9\text{ V},\quad V_{B_2} = 10.8\text{ V},\quad I_{C_1} \cong I_{C_2} = 3.8\text{ mA}$$

because $I_{E_1} \cong I_{E_2}$ the dynamic resistance for each transistor is

$$r_e = \frac{26\text{ mV}}{I_E} \cong \frac{26\text{ mV}}{3.8\text{ mA}} = 6.8\ \Omega$$

The loading on the transistor Q_1 is the input impedance of the Q_2 transistor in the CB configuration as shown by r_e in Fig 5.72.

The result is the replacement of R_C in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

$$A_{v_1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

with the voltage gain for the second stage (common base) of

$$A_{v_2} = \frac{R_C}{r_e} = \frac{1.8\text{ k}\Omega}{6.8\ \Omega} = 265$$

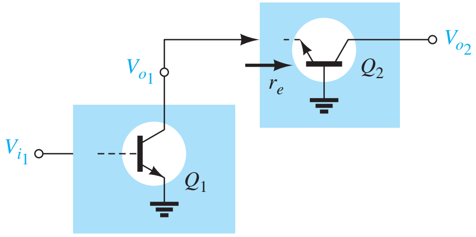

V_{o_2}
V_{o_1}
r_e
Q_2
V_{i_1}
Q_1

FIG. 5.72

Defining the load of Q_1.

The overall no-load gain is

$$A_{v_T} = A_{v_1}A_{v_2} = (-1)(265) = \mathbf{-265}$$

As expected, in Example 5.16, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.

5.17 DARLINGTON CONNECTION

A very popular connection of two bipolar junction transistors for operation as one "super-beta" transistor is the Darlington connection shown in Fig. 5.73. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of β_1 and β_2, the Darlington connection provides a current gain of

$$\boxed{\beta_D = \beta_1\beta_2} \qquad \textbf{(5.101)}$$

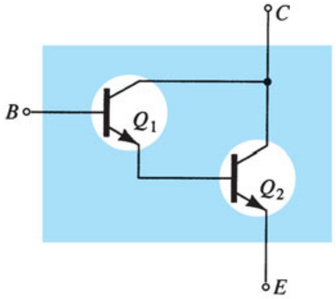


FIG. 5.73
Darlington combination.

The configuration was first introduced by Dr. Sidney Darlington in 1953. A short biography appears as Fig 5.74.

Emitter-Follower Configuration

A Darlington amplifier used in an emitter-follower configuration appears in Fig. 5.75. The primary impact of using the Darlington configuration is an input impedance much larger than

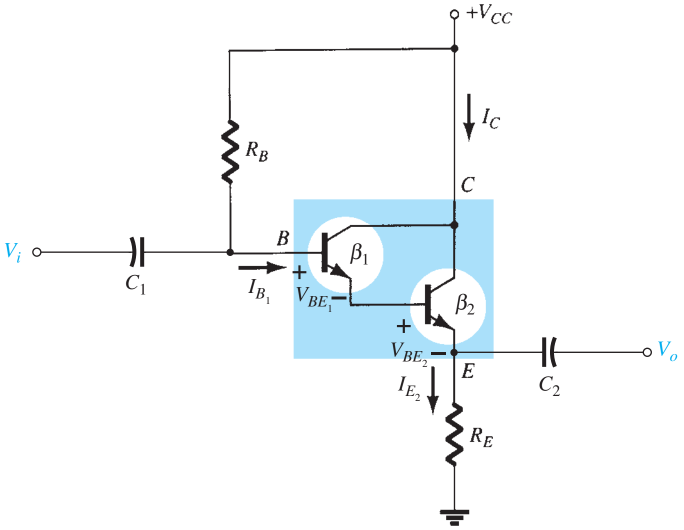
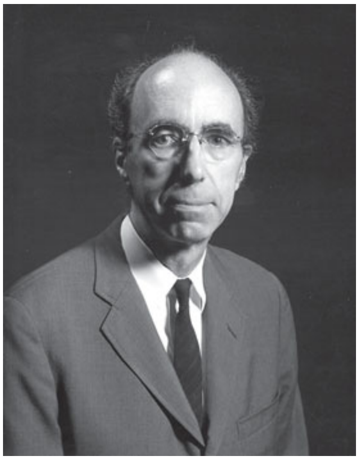


FIG. 5.75
Emitter-follower configuration with a Darlington amplifier.



American (Pittsburgh, PA; Exeter, NH)
(1906–1997)

Department Head at Bell Laboratories
Professor, Department of Electrical and Computer Engineering, University of New Hampshire

Dr. Sidney Darlington earned his B.S. in physics at Harvard, his B.S. in electrical communication at MIT, and his Ph.D. at Columbia University. In 1929 he joined Bell Laboratories, where he was head of the Circuits and Control Department. During that period he became good friends with other important contributors such as Edward Norton and Hendrik Bode. A holder of 24 U.S. patents, he was awarded the Presidential Medal of Freedom, the highest civilian honor in the United States, in 1945 for his contributions to network design during World War II. An elected member of the National Academy of Engineering, he also received the IEEE Edison Medal in 1975 and the IEEE Medal of Honor in 1981. His U.S. patent 2 663 806 titled "Semiconductor Signal Translating Device" was issued on December 22, 1953, describing how two transistors could be constructed in the Darlington configuration on the same substrate—often looked upon as the beginnings of compound IC construction. Dr. Darlington was also responsible for the introduction and development of the Chirp technique, used throughout the world in waveguide transmission and radar systems. He is a primary contributor to the Bell Laboratories Command Guidance System that guides most of the rockets used today to place satellites in orbit. It uses a combination of radar tracking on the ground with inertial control in the rocket itself. Dr. Darlington was an avid outdoorsman as a hiker and member of the Appalachian Mountain Club. One of his proudest accomplishments was being able to climb Mt. Washington at the age of 80.

FIG. 5.74
Sidney Darlington (Courtesy of AT&T Archives and History Center.)

that obtained with a single-transistor network. The current gain is also larger, but the voltage gain for a single-transistor or Darlington configuration remains slightly less than one.

DC Bias The case current is determined using a modified version of Eq. 4.44. There are now two base-to-emitter voltage drops to include and the beta of a single transistor is replaced by the Darlington combination of Eq. 5.101.

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E}} \tag{5.102}$$

The emitter current of Q_1 is equal to the base current of Q_2 so that

$$I_{E_2} = \beta_2 I_{B_2} = \beta_2 I_{E_1} = \beta_2(\beta_1 I_{E_1}) = \beta_1 \beta_2 I_{B_1}$$

resulting in

$$\boxed{I_{C_2} \cong I_{E_2} = \beta_D I_{B_1}} \tag{5.103}$$

The collector voltage of both transistors is

$$\boxed{V_{C_1} = V_{C_2} = V_{CC}} \tag{5.104}$$

the emitter voltage of Q_2

$$\boxed{V_{E_2} = I_{E_2} R_E} \tag{5.105}$$

the base voltage of Q_1

$$\boxed{V_{B_1} = V_{CC} - I_{B_1} R_B = V_{E_2} + V_{BE_1} + V_{BE_2}} \tag{5.106}$$

the collector-emitter voltage of Q

$$\boxed{V_{CE_2} = V_{C_2} - V_{E_2} = V_{CC} - V_{E_2}} \tag{5.107}$$

EXAMPLE 5.17 Calculate the dc bias voltages and currents for the Darlington configuration of Fig. 5.76.

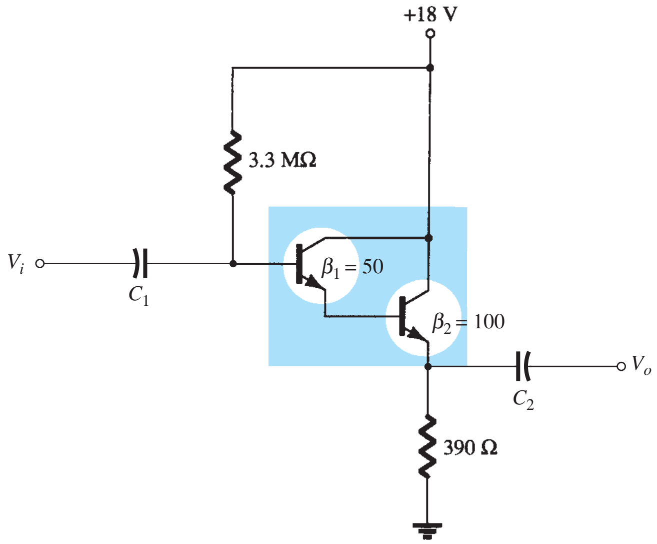


FIG. 5.76

Circuit for Example 5.17.

Solution:

$$\beta_D = \beta_1\beta_2 = (50)(100) = \mathbf{5000}$$

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} = \frac{18\text{ V} - 0.7\text{ V} - 0.7\text{ V}}{3.3\text{ M}\Omega + (5000)(390\ \Omega)}$$

$$= \frac{18\text{ V} - 1.4\text{ V}}{3.3\text{ M}\Omega + 1.95\text{ M}\Omega} = \frac{16.6\text{ V}}{5.25\text{ M}\Omega} = \mathbf{3.16\ \mu A}$$

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} = (5000)(3.16\text{ mA}) = \mathbf{15.80\ mA}$$

$$V_{C_1} = V_{C_2} = \mathbf{18\ V}$$

$$V_{E_2} = I_{E_2}R_E = (15.80\text{ mA})(390\ \Omega) = \mathbf{6.16\ V}$$

$$V_{B_1} = V_{E_2} + V_{BE_1} + V_{BE_2} = 6.16\text{ V} + 0.7\text{ V} + 0.7\text{ V} = \mathbf{7.56\ V}$$

$$V_{CE_2} = V_{CC} - V_{E_2} = 18\text{ V} - 6.16\text{ V} = \mathbf{11.84\ V}$$

AC Input Impedance The ac input impedance can be determined using the ac equivalent network of Fig. 5.77.

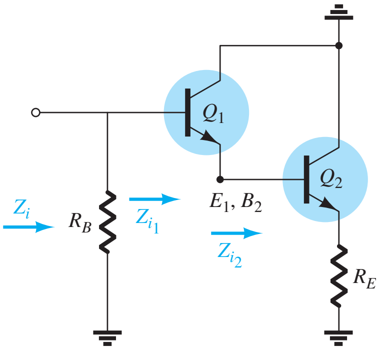


FIG. 5.77
Finding Z_i.

As defined in Fig. 5.77:

$$Z_{i_2} = \beta_2(r_{e_2} + R_E)$$

$$Z_{i_1} = \beta_1(r_{e_1} + Z_{i_2})$$

so that $$Z_{i_1} = \beta_1(r_{e_1} + \beta_2(r_{e_2} + R_E))$$

Assuming $$R_E \gg r_{e_2}$$

and $$Z_{i_1} = \beta_1(r_{e_1} + \beta_2 R_E)$$

Since $$\beta_2 R_E \gg r_{e_1}$$

$$Z_{i_1} \cong \beta_1\beta_2 R_E$$

and since $$Z_i = R_B \| Z_i$$

$$\boxed{Z_i = R_B \| \beta_1\beta_2 R_E = R_B \| \beta_D R_E} \qquad \textbf{(5.108)}$$

For the network of Fig. 5.76

$$Z_i = R_B \| \beta_D R_E$$
$$= 3.3\text{ M}\Omega \| (5000)(390\ \Omega) = 3.3\text{ M}\Omega \| 1.95\text{ M}\Omega$$
$$= \mathbf{1.38\ M\Omega}$$

Note in the preceding analysis that the values of r_e were not compared but dropped compared to much larger quantites. In a Darlington configuration the values of r_e will be different because the emitter current through each transistor will be different. Also, keep in mind that chances are the beta values for each transistor will be different because thay deal with different current levels. The fact remains, however, that the product of the two beta values will equal β_D, as indicated on the specification sheet.

AC Current Gain The current gain can be determined from the equivalent network of Fig. 5.78. The output impedance of each transistor is ignored and the parameters for each transistor are employed.

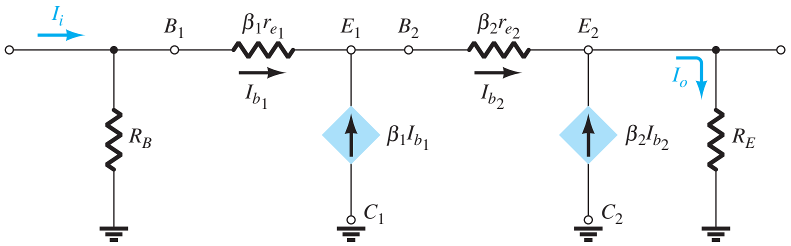


FIG. 5.78

Determining A_i for the network of Fig. 5.75.

Solving for the output current: $I_o = I_{b_2} + \beta_2 I_{b_2} = (\beta_2 + 1)I_{b_2}$

with $I_{b_2} = \beta_1 I_{b_1} + I_{b_1} = (\beta_1 + 1)I_{b_1}$

Then $I_o = (\beta_2 + 1)(\beta_1 + 1)I_{b_1}$

Using the current-divider rule on the input circuit:

$$I_{b_1} = \frac{R_B}{R_B + Z_i} I_i = \frac{R_B}{R_B + \beta_1\beta_2 R_E} I_i$$

and $$I_o = (\beta_2 + 1)(\beta_1 + 1)\left(\frac{R_B}{R_B + \beta_1\beta_2 R_E}\right) I_i$$

so that $$A_i = \frac{I_o}{I_i} = \frac{(\beta_1 + 1)(\beta_2 + 1)R_B}{R_B + \beta_1\beta_2 R_E}$$

Using $\beta_1, \beta_2 \gg 1$

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_E}} \qquad \textbf{(5.109)}$$

or $$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta_D R_B}{R_B + \beta_D R_E}} \qquad \textbf{(5.110)}$$

For Fig. 5.76:

$$A_i = \frac{I_o}{I_i} = \frac{\beta_D R_B}{R_B + \beta_D R_E} = \frac{(5000)(3.3\text{ M}\Omega)}{3.3\text{ M}\Omega + 1.95\text{ M}\Omega}$$
$$= \mathbf{3.14 \times 10^3}$$

AC Voltage Gain The voltage gain can be determined using Fig. 5.77 and the following derivation:

$$V_o = I_o R_E$$
$$V_i = I_i(R_B \| Z_i)$$
$$R_B \| Z_i = R_B \| \beta_D R_E = \frac{\beta_D R_B R_E}{R_B + \beta_D R_E}$$

and $$A_v = \frac{V_o}{V_i} = \frac{I_o R_E}{I_i(R_B \| Z_i)} = (A_i)\left(\frac{R_E}{R_B \| Z_i}\right)$$
$$= \left[\frac{\beta_D R_B}{R_B + \beta_D R_E}\right]\left[\frac{R_E}{\dfrac{\beta_D R_B R_E}{R_B + \beta_D R_E}}\right]$$

and $$\boxed{A_v \cong 1 \text{ (in reality less than one)}} \qquad \textbf{(5.111)}$$

an expected result for the emitter-follower configuration.

AC Output Impedance The output impedance will be determined by going back to Fig. 5.78 and setting V_i to zero volts as shown in Fig. 5.79. The resistor R_B is "shorted out," resulting in the configuration of Fig. 5.80. Note in Figs. 5.82 and 5.83 that the output current has been redefined to match standard nomenclature and properly defined Z_o.

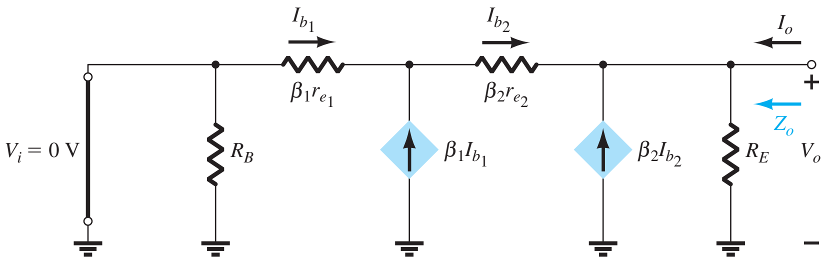

I_{b_1}
I_{b_2}
I_o
$\beta_1 r_{e_1}$
$\beta_2 r_{e_2}$
+
Z_o
$V_i = 0$ V
R_B
$\beta_1 I_{b_1}$
$\beta_2 I_{b_2}$
R_E
V_o
–

FIG. 5.79
Determining Z_o.

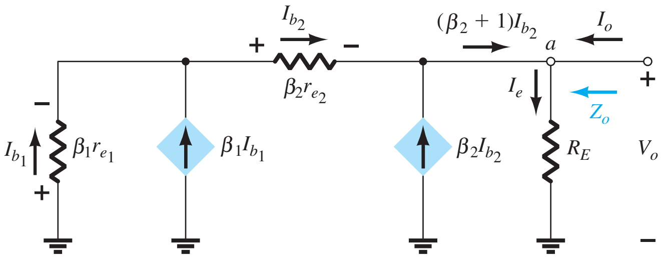

I_{b_2}
+
–
$(\beta_2 + 1)I_{b_2}$
a
I_o
$\beta_2 r_{e_2}$
I_e
+
Z_o
–
I_{b_1}
$\beta_1 r_{e_1}$
+
$\beta_1 I_{b_1}$
$\beta_2 I_{b_2}$
R_E
V_o
–

FIG. 5.80
Redrawn of network of Fig. 5.79.

At point a Kirchhoff's current law will result in $I_o + (\beta_2 + 1)I_{b_2} = I_e$:

$$I_o = I_e - (\beta_2 + 1)I_{b_2}$$

Applying Kirchhoff's voltage law around the entire outside loop will result in

$$-I_{b_1}\beta_1 r_{e_1} - I_{b_2}\beta_2 r_{e_2} - V_o = 0$$

and $$V_o = I_{b_1}\beta_1 r_{e_1} + I_{b_2}\beta_2 r_{e_2}$$

Substituting $$I_{b_2} = (\beta_1 + 1)I_{b_1}$$

$$V_o = -I_{b_1}\beta_1 r_{e_1} - (\beta_1 + 1)I_{b_1}\beta_2 r_{e_2}$$

$$= -I_{b_1}[\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}]$$

and $$I_{b_1} = -\frac{V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}$$

with $$I_{b_2} = (\beta_1 + 1)I_{b_1} = (\beta_1 + 1)\left[-\frac{V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right]$$

so that $$I_{b_2} = -\left[\frac{\beta_1 + 1}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right]V_o$$

Going back $$I_o = I_e - (\beta_2 + 1)I_{b_2} = I_e - (\beta_2 + 1)\left(-\frac{(\beta_1 + 1)V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right)$$

or $$I_o = \frac{V_o}{R_E} + \frac{(\beta_1 + 1)(\beta_2 + 1)V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}$$

Because $\beta_1, \beta_2 \gg 1$

$$I_o = \frac{V_o}{R_E} + \frac{\beta_1\beta_2 V_o}{\beta_1 r_{e_1} + \beta_1\beta_2 r_{e_2}} = \frac{V_o}{R_E} + \frac{V_o}{\dfrac{\beta_1 r_{e_1}}{\beta_1\beta_2} + \dfrac{\beta_1\beta_2 r_{e_2}}{\beta_1\beta_2}}$$

$$I_o = \frac{V_o}{R_E} + \frac{V_o}{\dfrac{r_{e_1}}{\beta_2} + r_{e_2}}$$

which defines the parallel resistance network of Fig. 5.81.

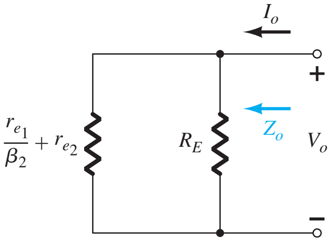


FIG. 5.81
Resulting network defined by Z_o.

In general, $R_E \gg \left(\frac{r_{e_1}}{\beta_2} + r_{e_2}\right)$ so the output impedance is defined by

$$\boxed{Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2}} \tag{5.112}$$

Using the dc results, the value of r_{e_2} and r_{e_1} can be determined as follows.

$$r_{e_2} = \frac{26\text{ mV}}{I_{E_2}} = \frac{26\text{ mV}}{15.80\text{ mA}} = 1.65\ \Omega$$

and $$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{15.80\text{ mA}}{100} = 0.158\text{ mA}$$

so that $$r_{e_1} = \frac{26\text{ mV}}{0.158\text{ mA}} = 164.5\ \Omega$$

The output impedance for the network of Fig. 5.78 is therefore:

$$Z_o \cong \frac{r_{e_1}}{\beta_2} + r_{e_2} = \frac{164.5\ \Omega}{100} + 1.65\ \Omega = 1.645\ \Omega + 1.65\ \Omega = \mathbf{3.30\ \Omega}$$

In general, the output impedance for the configuration of Fig. 5.78 is very low—in the order of a few ohms at most.

Voltage-Divider Amplifier

DC Bias Let us now investigate the effect of the Darlington configuration in a basic amplifier configuration as shown in Fig. 5.82. Note that now there is a collector resistor R_C, and the emitter terminal of the Darlington circuit is connected to ground for ac conditions. As noted on Fig. 5.82, the beta of each transistor is provided along with the resulting voltage from base to emitter.

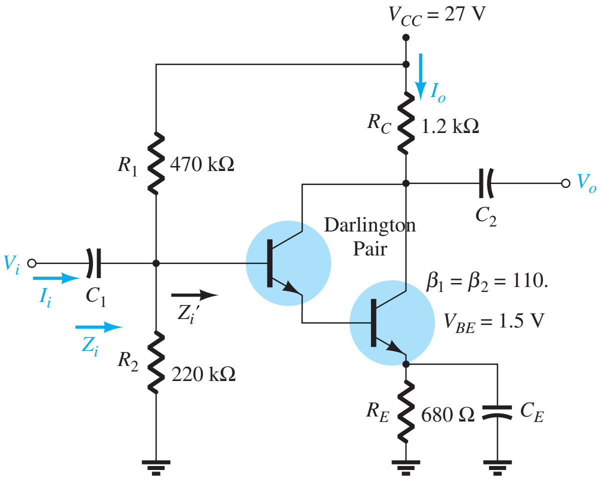


FIG. 5.82
Amplifier configuration using a Darlington pair.

The dc analysis can proceed as follows:

$$\beta_D = \beta_1\beta_2 = (110 \times 110) = 12{,}100$$

$$V_B = \frac{R_2}{R_2 + R_1}V_{CC} = \frac{220\text{ k}\Omega(27\text{ V})}{220\text{ k}\Omega + 470\text{ k}\Omega} = \mathbf{8.61\text{ V}}$$

$$V_E = V_B - V_{BE} = 8.61\text{ V} - 1.5\text{ V} = \mathbf{7.11\text{ V}}$$

$$I_E = \frac{V_E}{R_E} = \frac{7.11\text{ V}}{680\ \Omega} = \mathbf{10.46\text{ mA}}$$

$$I_B = \frac{I_E}{\beta_D} = \frac{10.46\text{ mA}}{12{,}100} = \mathbf{0.864\ \mu A}$$

Using the preceding results the values of r_{e_2} and r_{e_1} can be determined:

$$r_{e_2} = \frac{26\text{ mV}}{I_{E_2}} = \frac{26\text{ mV}}{10.46\text{ mA}} = \mathbf{2.49\ \Omega}$$

$$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{10.46\text{ mA}}{110} = 0.095\text{ mA}$$

and
$$r_{e_1} = \frac{26\text{ mV}}{I_{E_1}} = \frac{26\text{ mV}}{0.095\text{ mA}} = \mathbf{273.7\ \Omega}$$

AC Input Impedance The ac equivalent of Fig. 5.82 appears as Fig. 5.83. The resistors R_1 and R_2 are in parallel with the input impedance to the Darlington pair, assuming the second transistor found by assuming the second transistor acts like an R_E load on the first as shown in Fig. 5.83.

That is, $Z_i' = \beta_1 r_{e_1} + \beta_1(\beta_2 r_{e_2})$

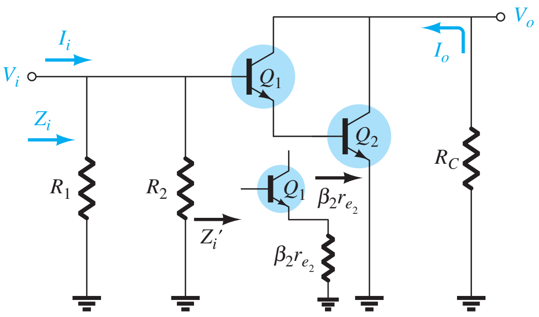


FIG. 5.83
Defining Z'_i and Z_i.

and
$$\boxed{Z_i' = \beta_1[r_{e_1} + \beta_2 r_{e_2}]} \tag{5.113}$$

For the network of Fig. 5.82:

$$\begin{aligned} Z_i' &= 110[273.7\ \Omega + (110)(2.49\ \Omega)] \\ &= 110[273.7\ \Omega + 273.9\ \Omega] \\ &= 110[547.6\ \Omega] \\ &= \mathbf{60.24\text{ k}\Omega} \end{aligned}$$

and
$$\begin{aligned} Z_i &= R_1 \| R_2 \| Z_i' \\ &= 470\text{ k}\Omega \| 220\text{ k}\Omega \| 60.24\text{ k}\Omega \\ &= 149.86\text{ k}\Omega \| 60.24\text{ k}\Omega \\ &= \mathbf{42.97\text{ k}\Omega} \end{aligned}$$

AC Current Gain The complete ac equivalent of Fig. 5.82 appears as Fig. 5.84.

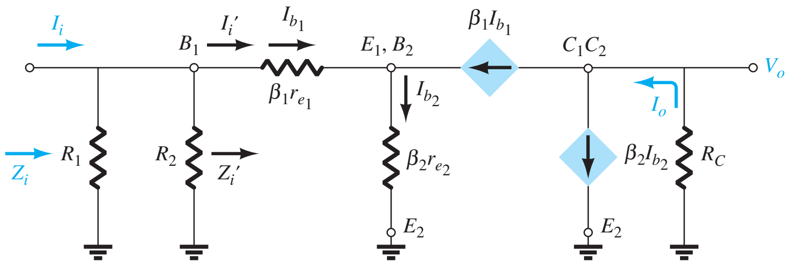


FIG. 5.84

ac equivalent network for Fig. 5.82.

The output current $I_o = \beta_1 I_{b_1} + \beta_2 I_{b_2}$

with $I_{b_2} = (\beta_1 + 1)I_{b_1}$

so that $I_o = \beta_1 I_{b_1} + \beta_2(\beta_1 + 1)I_{b_1}$

and with $I_{b_1} = I_i'$

we find $I_o = \beta_1 I_i' + \beta_2(\beta_1 + 1)I_i'$

and

$$A_i' = \frac{I_o}{I_i} = \beta_1 + \beta_2(\beta + 1)$$

$$\cong \beta_1 + \beta_2\beta_1 = \beta_1(1 + \beta_2)$$

$$\cong \beta_1\beta_2$$

and finally

$$\boxed{A_i' = \frac{I_o}{I_i'} = \beta_1\beta_2 = \beta_D} \tag{5.114}$$

For the original structure: $I_i' = \dfrac{R_1 \| R_2 I_i}{R_1 \| R_2 + Z_i'}$ or $\dfrac{I_i'}{I_i} = \dfrac{R_1 \| R_2}{R_1 \| R_2 + Z_i'}$

but

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_i'}\right)\left(\frac{I_i'}{I_i}\right)$$

so that

$$\boxed{A_i = \frac{\beta_D(R_1 \| R_2)}{R_1 \| R_2 + Z_i'}} \tag{5.115}$$

For Fig. 5.82

$$A_i = \frac{(12{,}100)(149.86\text{ k}\Omega)}{149.86\text{ k}\Omega + 60.24\text{ k}\Omega}$$

$$= \mathbf{8630.7}$$

Note the significant drop in current gain due to R_1 and R_2.

AC Voltage Gain The input voltage is the same across R_1 and R_2 and at the base of the first transistor as shown in Fig. 5.84.

The result is

$$A_v = \frac{V_o}{V_i} = -\frac{I_o R_C}{I_i' Z_i'} = -A_i\left(\frac{R_C}{Z_i'}\right)$$

and

$$\boxed{A_v = -\frac{\beta_D R_C}{Z_i'}} \tag{5.116}$$

For the network of Fig. 5.82,

$$A_v = -\frac{\beta_D R_C}{Z_i'} = -\frac{(12{,}000)(1.2\text{ k}\Omega)}{60.24\text{ k}\Omega} = \mathbf{-241.04}$$

AC Output Impedence Because the output impedance in R_C is parallel with the collector to emitter terminals of the transistor, we can look back on similar situations and find that the output impedance is defined by

$$\boxed{Z_o \cong R_C \| r_{o_2}} \tag{5.117}$$

where r_{o_2} is the output resistance of the transistor Q_2.

Packaged Darlington Amplifier

Because the Darlington connection is so popular, a number of manufacturers provide packaged units such as shown in Fig. 5.85. Typically, the two BJTs are constructed on a single chip rather than separate BJT units. Note that only one set of collector, base, and emitter terminals is provided for each configuration. These, of course, are the base of the transistor Q_1, the collector of Q_1 and Q_2, and the emitter of Q_2.

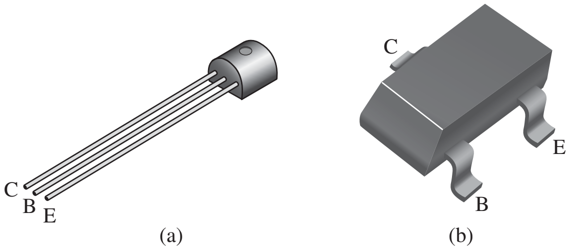


FIG. 5.85
Packaged Darlington amplifiers: (a) TO-92 package; (b) Super SOT™-3 package.

In Fig. 5.86 some of the ratings for an MPSA28 Fairchild Semiconductor Darlington amplifier are provided. In particular, note that the maximum collector-to-emitter voltage of 80 V is also the breakdown voltage. The same is true for the collector-to-base and emitter-to-base voltages, although notice how much lower the maximum ratings are for the base-to-emitter junction. Because of the Darlington configuration, the maximum current rating for the collector current has jumped to 800 mA—far exceeding levels we have encountered

Absolute Maximum Ratings		
V_{CES}	Collector-Emitter Voltage	80 V
V_{CBO}	Collector-Base Voltage	80 V
V_{EBO}	Emitter-Base Voltage	12 V
I_C	Collector Current–Continuous	800 mA
Electrical Characteristics		
$V_{(BR)CES}$	Collector-Emitter Breakdown Voltage	80 V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	80 V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	12 V
I_{CBO}	Collector Cutoff Current	100 mA
I_{EBO}	Emitter Cutoff Current	100 mA
On Characteristics		
h_{FE}	DC Current Gain	10,000
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	1.2 V
$V_{BE(\text{on})}$	Base-Emitter on Voltage	2.0 V

FIG. 5.86
MPSA 28 Fairchild Semiconductor Darlington amplifier ratings.

for single-transistor networks. The dc current gain is rated at the high level of 10,000 and the base-to-emitter potential in the "on" state is 2 V, which certainly exceeds the 1.4 V we have used for individual transistors. Finally, it is interesting to note that the level of I_{CEO} is much higher at 500 nA than for a typical single-transistor unit.

In the packaged format the network of Fig. 5.75 would appear as shown in Fig. 5.87. Using β_D and the provided value of $V_{BE}\,(=V_{BE_1} + V_{BE_2})$, all the equations appearing in this section can be applied.

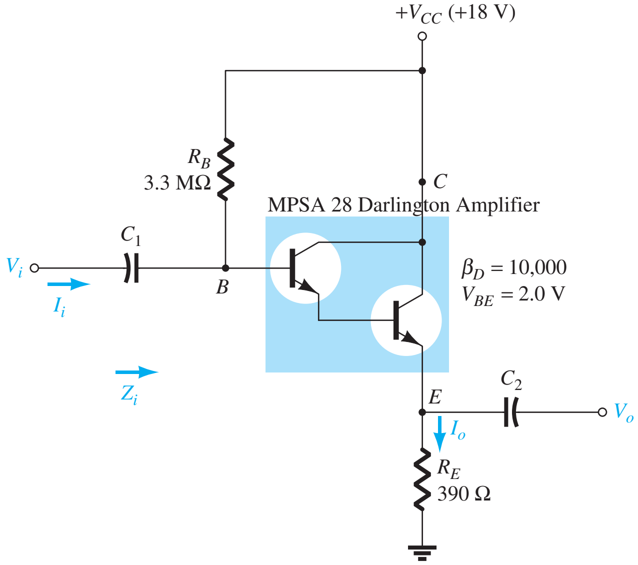


FIG. 5.87
Darlington emitter-follower circuit.

5.18 FEEDBACK PAIR

The feedback pair connection (see Fig. 5.88) is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains), high input impedance, low output impedance, and a voltage gain slightly less than one. Initially, it may appear that it would have a high voltage gain because the output is taken off the collector with a resistor R_C in place. However, the *pnp–npn* combination results in terminal characteristics very similar to that of the emitter–follower configuration. A typical application (see Chapter 12) uses a Darlington and a feedback-pair connection to provide complementary transistor operation. A practical network employing a feedback pair is provided in Fig. 5.89 for investigation.

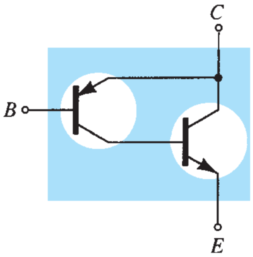


FIG. 5.88
Feedback pair connection.

DC Bias

The dc bias calculations that follow use practical simplifications wherever possible to provide simpler results. From the Q_1 base–emitter loop, one obtains

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

$$V_{CC} - (\beta_1 \beta_2 I_{B_1}) R_C - V_{EB_1} - I_{B_1} R_B = 0$$

The base current is then

$$\boxed{I_{B_1} = \frac{V_{CC} - V_{BE_1}}{R_B + \beta_1 \beta_2 R_C}} \qquad \textbf{(5.118)}$$

The collector current of Q_1 is

$$I_{C_1} = \beta_1 I_{B_1} = I_{B_2}$$

which is also the base Q_2 current. The transistor Q_2 collector current is

$$I_{C_2} = \beta_2 I_{B_2} \approx I_{E_2}$$

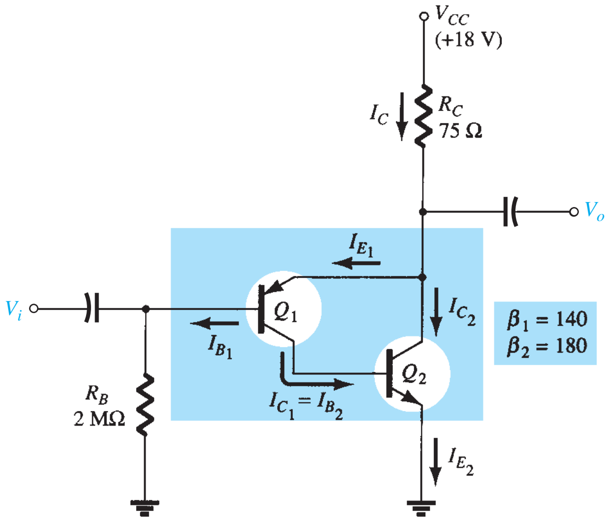


FIG. 5.89
Operation of a feedback pair.

so that the current through R_C is

$$\boxed{I_C = I_{E_1} + I_{C_2} \approx I_{B_2} + I_{C_2}} \tag{5.119}$$

The voltages

$$\boxed{V_{C_2} = V_{E_1} = V_{CC} - I_C R_C} \tag{5.120}$$

and

$$\boxed{V_{B_1} = I_{B_1} R_B} \tag{5.121}$$

with

$$\boxed{V_{BC_1} = V_{B_1} - V_{BE_2} = V_{B_1} - 0.7\text{ V}} \tag{5.122}$$

EXAMPLE 5.18 Calculate the dc bias currents and voltages for the circuit of Fig. 5.89 to provide V_o at one-half the supply voltage (9 V).

Solution:

$$I_{B_1} = \frac{18\text{ V} - 0.7\text{ V}}{2\text{ M}\Omega + (140)(180)(75\ \Omega)} = \frac{17.3\text{ V}}{3.89 \times 10^6} = \mathbf{4.45\ \mu A}$$

The base Q_2 current is then

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1} = 140(4.45\ \mu\text{A}) = \mathbf{0.623\ mA}$$

resulting in a Q_2 collector current of

$$I_{C_2} = \beta_2 I_{B_2} = 180(0.623\text{ mA}) = \mathbf{112.1\ mA}$$

and the current through R_C is then

$$\text{Eq. (5.119): } I_C = I_{E_1} + I_{C_2} = 0.623\text{ mA} + 112.1\text{ mA} \approx I_{C_2} = \mathbf{112.1\ mA}$$

$$\begin{aligned} V_{C_2} &= V_{E_1} = 18\text{ V} - (112.1\text{ mA})(75\ \Omega) \\ &= 18\text{ V} - 8.41\text{ V} \\ &= \mathbf{9.59\ V} \\ V_{B_1} &= I_{B_1} R_B = (4.45\ \mu\text{A})(2\text{ M}\Omega) \\ &= \mathbf{8.9\ V} \\ V_{BC_1} &= V_{B_1} - 0.7\text{ V} = 8.9\text{ V} - 0.7\text{ V} \\ &= \mathbf{8.2\ V} \end{aligned}$$

AC Operation

The ac equivalent circuit for that of Fig. 5.89 is drawn in Fig. 5.90.

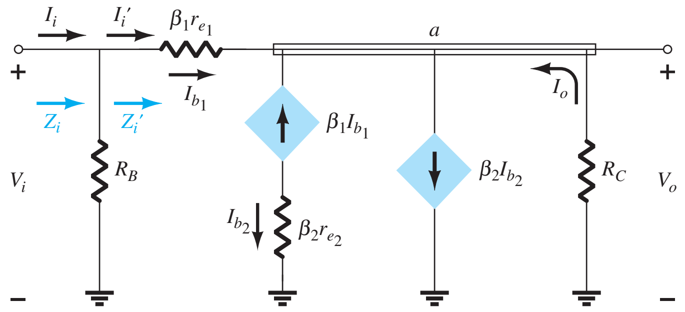


FIG. 5.90
ac equivalent for the network of Fig. 5.89.

Input Impedance, Z_i The ac input impedance seen looking into the base of transistor Q_1 is determined as follows:

$$Z_i' = \frac{V_i}{I_i'}$$

Applying Kirchhoff's current law at node a and defining $I_c = I_o$:

$$I_{b_1} + \beta_1 I_{b_1} - \beta_2 I_{b_2} + I_o = 0$$

with $I_{b_2} = -\beta_1 I_{b_1}$ as noted in Fig. 5.90.

The result is $$I_{b_1} + \beta_1 I_{b_1} - \beta_2(-\beta_1 I_{b_1}) + I_o = 0$$

and $$I_o = -I_{b_1} - \beta_1 I_{b_1} - \beta_1\beta_2 I_{b_1}$$

or $$I_o = -I_{b_1}(1 + \beta_1) - \beta_1\beta_2 I_{b_1}$$

but $$\beta_1 \gg 1$$

and $$I_o = -\beta_1 I_{b_1} - \beta_1\beta_2 I_{b_1} = -I_{b_1}(\beta_1 + \beta_1\beta_2)$$
$$= -I_{b_1}\beta_1(1 + \beta_2)$$

resulting in: $$\boxed{I_o \cong -\beta_1\beta_2 I_{b_1}} \qquad \textbf{(5.123)}$$

Now, $I_{b_1} = \dfrac{V_i - V_o}{\beta_1 r_{e_1}}$ from Fig. 5.90

and $$V_o = -I_o R_C = -(-\beta_1\beta_2 I_{b_1})R_C = \beta_1\beta_2 I_{b_1} R_C$$

so $$I_{b_1} = \frac{V_i - \beta_1\beta_2 I_{b_1} R_C}{\beta_1 r_{e_1}}$$

Rearranging: $$I_{b_1}\beta_1 r_{e_1} = V_i - \beta_1\beta_2 I_{b_1} R_C$$

and $$I_{b_1}(\beta_1 r_{e_1} + \beta_1\beta_2 R_C) = V_i$$

so $$I_{b_1} = I_i' = \frac{V_i}{\beta_1 r_{e_1} + \beta_1\beta_2 R_C}$$

and $$V_i' = \frac{V_i}{I_i'} = \frac{V_i}{\dfrac{V_i}{\beta_1 r_e + \beta_1\beta_2 R_C}}$$

so that $$\boxed{Z_i' = \beta_1 r_{e_1} + \beta_1\beta_2 R_C} \qquad \textbf{(5.124)}$$

In general, $$\beta_1\beta_2 R_C \gg \beta_1 r_{e_1}$$

and $$\boxed{Z_i' \cong \beta_1\beta_2 R_C} \qquad \textbf{(5.125)}$$

with
$$\boxed{Z_i = R_B \| Z_i'} \qquad \textbf{(5.126)}$$

For the network of Fig. 5.89:
$$r_{e_1} = \frac{26\text{ mV}}{I_{E_1}} = \frac{26\text{ mV}}{0.623\text{ mA}} = 41.73\ \Omega$$

and
$$\begin{aligned} Z_i' &= \beta_1 r_{e_1} + \beta_1\beta_2 R_C \\ &= (140)(41.73\ \Omega) + (140)(180)(75\ \Omega) \\ &= 5842.2\ \Omega + 1.89\text{ M}\Omega \\ &= \mathbf{1.895\ M\Omega} \end{aligned}$$

where Eq. (5.125) results in $Z_i' \cong \beta_1\beta_2 R_C = (140)(180)(75\ \Omega) = \mathbf{1.89\ M\Omega}$, validating the above approximations.

Current Gain

Defining $I_{b_1} = I_i'$ as shown in Fig. 5.90 will permit finding the current gain $A_i' = I_o/I_i'$. Looking back on the derivation of Z_i we found $I_o = -\beta_1\beta_2 I_{b_1} = -\beta_1\beta_2 I_i'$

resulting in
$$\boxed{A_i' = \frac{I_o}{I_i'} = -\beta_1\beta_2} \qquad \textbf{(5.127)}$$

The current gain $A_i = I_o/I_i$ can be determined using the fact that
$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_i'}\cdot\frac{I_i'}{I_i}$$

For the input side:
$$I_i' = \frac{R_B I_i}{R_B + Z_i'} = \frac{R_B I_i}{R_B + \beta_1\beta_2 R_C}$$

Substituting:
$$A_i = \frac{I_o}{I_i'}\cdot\frac{I_i'}{I_i} = (-\beta_1\beta_2)\left(\frac{R_B}{R_B + \beta_1\beta_2 R_C}\right)$$

So that
$$\boxed{A_i = \frac{I_o}{I_i} = \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_C}} \qquad \textbf{(5.128)}$$

The negative sign appears because both I_i and I_o are defined as entering the network.

For the network of Fig. 5.89:
$$\begin{aligned} A_i' &= \frac{I_o}{I_i'} = -\beta_1\beta_2 \\ &= -(140)(180) \\ &= \mathbf{-25.2 \times 10^3} \end{aligned}$$
$$\begin{aligned} A_i &= \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_c} = -\frac{(140)(180)(2\text{ M}\Omega)}{2\text{ M}\Omega + 1.89\text{ M}\Omega} \\ &= -\frac{50{,}400\text{ M}\Omega}{3.89\text{ M}\Omega} \\ &= \mathbf{-12.96 \times 10^3}\ (\cong \text{ half of } A_i') \end{aligned}$$

Voltage Gain

The voltage gain can quickly be determined using the results obtained above.

That is,
$$\begin{aligned} A_v &= \frac{V_o}{V_i} = \frac{-I_o R_C}{I_i' Z_i'} \\ &= -\frac{(-\beta_1\beta_2 I_i')R_C}{I_i'(\beta_1 r_{e_1} + \beta_1\beta_2 R_C)} \end{aligned}$$

$$\boxed{A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C}} \qquad \textbf{(5.129)}$$

which is simply the following if we apply the approximation: $\beta_2 R_C \gg r_{e_1}$

$$A_v \cong \frac{\beta_2 R_C}{\beta_2 R_C} = 1$$

For the network of Fig. 5.89:

$$A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C} = \frac{(180)(75\ \Omega)}{41.73\ \Omega + (180)(75\ \Omega)}$$

$$= \frac{13.5 \times 10^3\ \Omega}{41.73\ \Omega + 13.5 \times 10^3\ \Omega}$$

$$= \mathbf{0.997} \cong 1 \text{ (as indicated above)}$$

Output Impedance

The output impedance Z_o' is defined in Fig. 5.91 when V_i is set to zero volts.

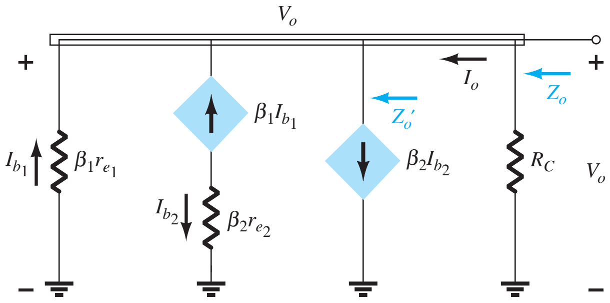


FIG. 5.91

Determining Z_o' and Z_o.

Using the fact that $I_o = -\beta_1 \beta_2 I_{b_1}$ from calculations above, we find that

$$Z_o' = \frac{V_o}{I_o} = \frac{V_o}{-\beta_1 \beta_2 I_{b_1}}$$

but

$$I_{b_1} = -\frac{V_o}{\beta_1 r_{e_1}}$$

and

$$Z_o' = \frac{V_o}{-\beta_1 \beta_2 \left(-\dfrac{V_o}{\beta_1 r_{e_1}}\right)} = \frac{\beta_1 r_{e_1}}{\beta_1 \beta_2}$$

so that

$$\boxed{Z_o' = \frac{r_{e_1}}{\beta_2}} \tag{5.130}$$

with

$$\boxed{Z_o = R_C \left\| \frac{r_{e_1}}{\beta_2} \right.} \tag{5.131}$$

However,

$$R_C \gg \frac{r_{e_1}}{\beta_2}$$

leaving

$$\boxed{Z_o \cong \frac{r_{e_1}}{\beta_2}} \tag{5.132}$$

which will be a very low value.

For the network of Fig. 5.89:

$$Z_o \cong \frac{41.73\ \Omega}{180} = \mathbf{0.23\ \Omega}$$

The preceding analysis shows that the feedback pair connection of Fig. 5.89 provides operation with voltage gain very near 1 (just as with a Darlington emitter-follower), a very high current gain, a very low output impedance, and a high input impedance.

5.19 THE HYBRID EQUIVALENT MODEL

The hybrid equivalent model was mentioned in the earlier sections of this chapter as one that was used in the early years before the popularity of the r_e model developed. Today there is a mix of usage depending on the level and direction of the investigation.

The r_e model has the advantage that the parameters are defined by the actual operating conditions,

whereas

the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.

In other words, the hybrid parameters may not reflect the actual operating conditions but simply provide an indication of the level of each parameter to expect for general use. The r_e model suffers from the fact that parameters such as the output impedance and the feedback elements are not available, whereas the hybrid parameters provide the entire set on the specification sheet. In most cases, if the r_e model is employed, the investigator will simply examine the specification sheet to have some idea of what the additional elements might be. This section will show how one can go from one model to the other and how the parameters are related. Because all specification sheets provide the hybrid parameters and the model is still extensively used, it is important to be aware of both models. The hybrid parameters as shown in Fig. 5.92 are derived from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

		Min.	Max.	
Input impedance ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{ie}	0.5	7.5	kΩ
Voltage feedback ratio ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{fe}	20	250	—
Output admittance ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{oe}	1.0	30	1μS

FIG. 5.92
Hybrid parameters for the 2N4400 transistor.

The description of the hybrid equivalent model will begin with the general two-port system of Fig. 5.93. The following set of equations (5.131) and (5.132) is only one of a number of ways in which the four variables of Fig. 5.93 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.

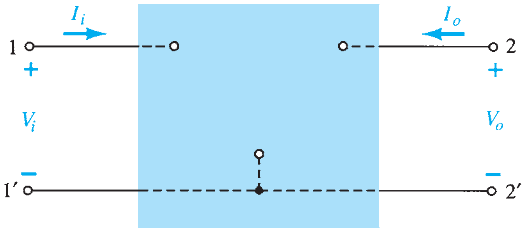


FIG. 5.93
Two-port system.

$$\boxed{V_i = h_{11}I_i + h_{12}V_o} \tag{5.133}$$

$$\boxed{I_o = h_{21}I_i + h_{22}V_o} \tag{5.134}$$

The parameters relating the four variables are called *h-parameters*, from the word "hybrid." The term *hybrid* was chosen because the mixture of variables (V and I) in each equation results in a "hybrid" set of units of measurement for the h-parameters. A clearer understanding of what the various h-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

h_{11} If we arbitrarily set $V_o = 0$ (short circuit the output terminals) and solve for h_{11} in Eq. (5.133), we find

$$\boxed{h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}} \quad \text{ohms} \tag{5.135}$$

The ratio indicates that the parameter h_{11} is an impedance parameter with the units of ohms. Because it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted*, it is called the *short-circuit input-impedance parameter.* The subscript 11 of h_{11} refers to the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

h_{12} If I_i is set equal to zero by opening the input leads, the following results for h_{12}:

$$\boxed{h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}} \quad \text{unitless} \tag{5.136}$$

The parameter h_{12}, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units because it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter.* The subscript 12 of h_{12} indicates that the parameter is a transfer quantity determined by a ratio of input (1) to output (2) measurements. The first integer of the subscript defines the measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term *reverse* is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

h_{21} If in Eq. (5.134) V_o is set equal to zero by again shorting the output terminals, the following results for h_{21}:

$$\boxed{h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}} \quad \text{unitless} \tag{5.137}$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for h_{12}. The parameter h_{21} is the ratio of the output current to the input current with the output terminals shorted. This parameter, like h_{12}, has no units because it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter.* The subscript 21 again indicates that it is a transfer parameter with the output quantity (2) in the numerator and the input quantity (1) in the denominator.

h_{22} The last parameter, h_{22}, can be found by again opening the input leads to set $I_1 = 0$ and solving for h_{22} in Eq. (5.134):

$$\boxed{h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}} \quad \text{siemens} \tag{5.138}$$

Because it is the ratio of the output current to the output voltage, it is the output conductance parameter, and it is measured in siemens (S). It is called the *open-circuit output admittance parameter.* The subscript 22 indicates that it is determined by a ratio of output quantities.

Because each term of Eq. (5.133) has the unit volt, let us apply Kirchhoff's voltage law "in reverse" to find a circuit that "fits" the equation. Performing this operation results in the circuit of Fig. 5.94. Because the parameter h_{11} has the unit ohm, it is represented by a resistor in Fig. 5.94. The quantity h_{12} is dimensionless and therefore simply appears as a multiplying factor of the "feedback" term in the input circuit.

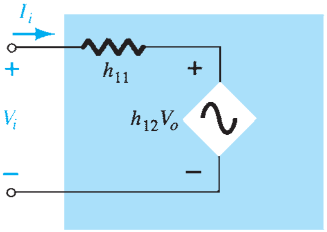


FIG. 5.94
Hybrid input equivalent circuit.

Because each term of Eq. (5.134) has the units of current, let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 5.95. Because h_{22} has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ($1/h_{22}$).

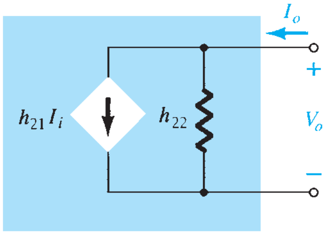


FIG. 5.95
Hybrid output equivalent circuit.

The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig. 5.96 with a new set of subscripts for the *h*-parameters. The notation of Fig. 5.96 is of a more practical nature because it relates the *h*-parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

h_{11} → *i*nput resistance → h_i
h_{12} → *r*everse transfer voltage ratio → h_r
h_{21} → *f*orward transfer current ratio → h_f
h_{22} → *o*utput conductance → h_o

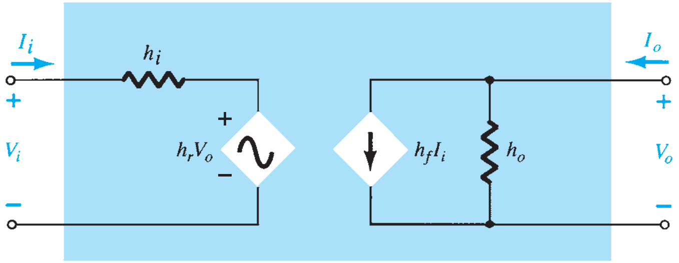


FIG. 5.96
Complete hybrid equivalent circuit.

The circuit of Fig. 5.96 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations*, so that the resulting equivalent circuit will have the same format as shown in Fig. 5.96. In each case, the bottom of the input and output sections of the network of Fig. 5.96 can be connected as shown in Fig. 5.97 because the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The *h*-parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second

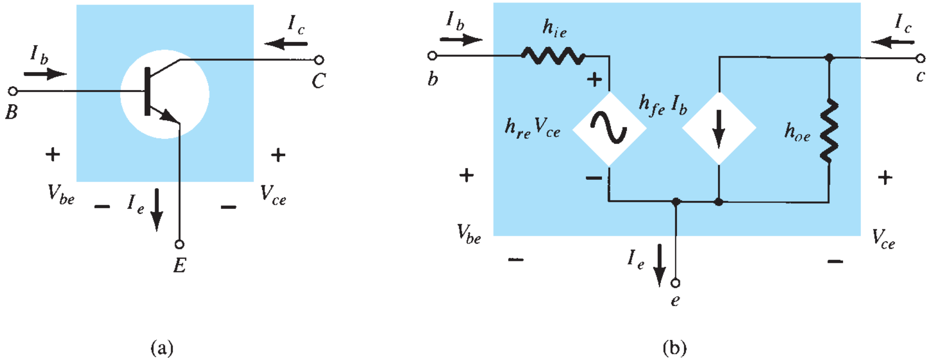
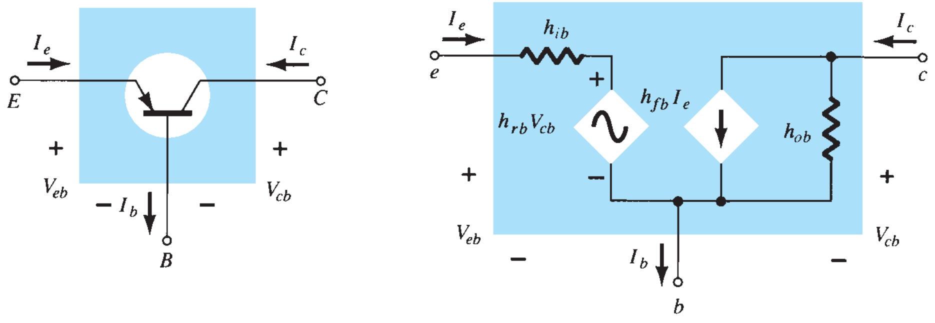


FIG. 5.97
Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

subscript has been added to the *h*-parameter notation. For the common-base configuration, the lowercase letter *b* was added, whereas for the common-emitter and common-collector configurations, the letters *e* and *c* were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 5.97. Note that $I_i = I_b$, $I_o = I_c$, and, through an application of Kirchhoff's current law, $I_e = I_b + I_c$. The input voltage is now V_{be}, with the output voltage V_{ce}. For the common-base configuration of Fig. 5.98, $I_i = I_e$, $I_o = I_c$ with $V_{eb} = V_i$ and $V_{cb} = V_o$. The networks of Figs. 5.97 and 5.98 are applicable for *pnp* or *npn* transistors.



(a)

(b)

FIG. 5.98

Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

The fact that both a Thévenin and a Norton circuit appear in the circuit of Fig. 5.96 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the **z**-parameter and **y**-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Appendix A the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired *small-signal equivalent network* for the transistor.

For the common-emitter and common-base configurations, the magnitude of h_r and h_o is often such that the results obtained for the important parameters such as Z_i, Z_o, A_v, and A_i are only slightly affected if h_r and h_o are not included in the model.

Because h_r is normally a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short-circuit equivalent for the feedback element as shown in Fig. 5.99. The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 5.99.

The resulting equivalent of Fig. 5.100 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the r_e model. In fact,

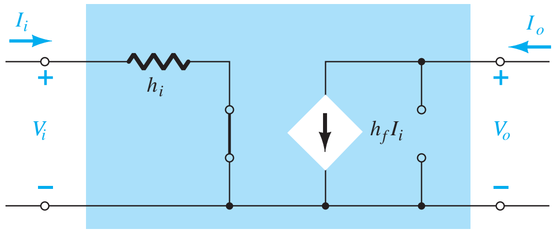


FIG. 5.99

Effect of removing h_{re} and h_{oe} from the hybird equivalent circuit.

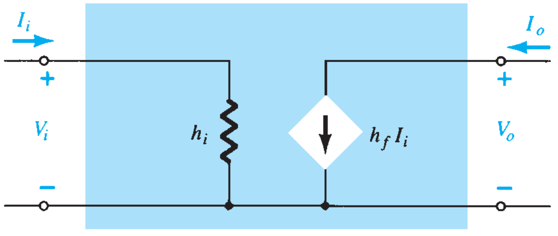


FIG. 5.100

Approximate hybrid equivalent model.

the hybrid equivalent and the r_e models for each configuration are repeated in Fig. 5.101 for comparison. It should be reasonably clear from Fig. 5.101a that

$$\boxed{h_{ie} = \beta r_e} \tag{5.139}$$

and

$$\boxed{h_{fe} = \beta_{\text{ac}}} \tag{5.140}$$

From Fig. 5.101b,

$$\boxed{h_{ib} = r_e} \tag{5.141}$$

and

$$\boxed{h_{fb} = -\alpha \cong -1} \tag{5.142}$$

In particular, note that the minus sign in Eq. (5.142) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the r_e model of Fig. 5.101b.

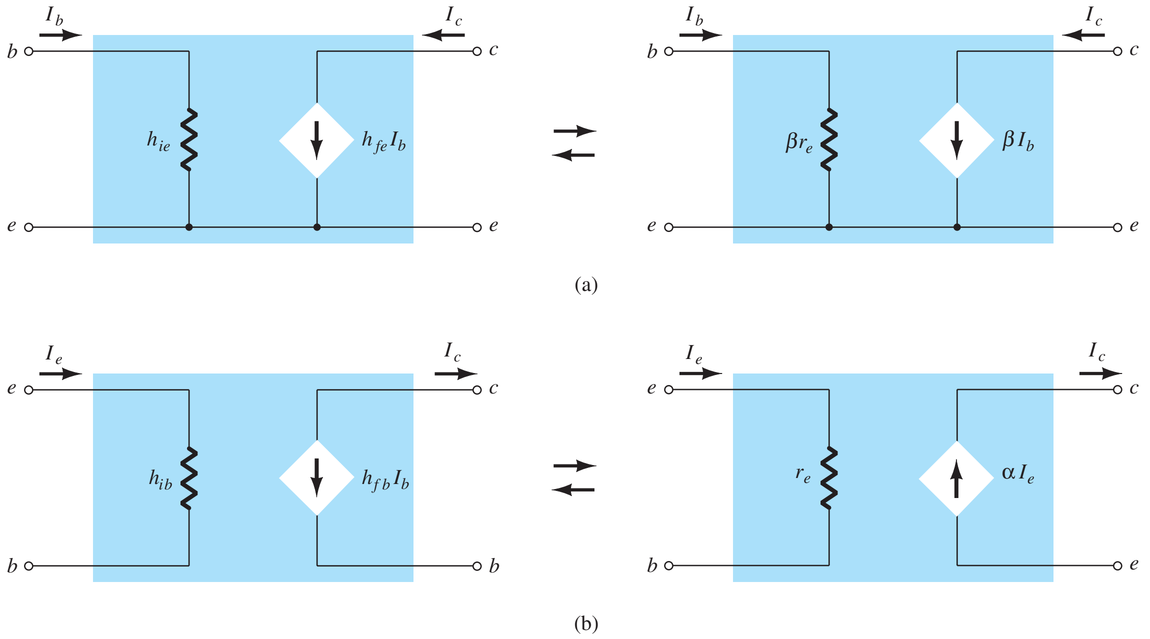


FIG. 5.101

Hybrid versus r_e model: (a) common-emitter configuration; (b) common-base configuration.

EXAMPLE 5.19 Given $I_E = 2.5$ mA, $h_{fe} = 140$, $h_{oe} = 20\ \mu$S (μmho), and $h_{ob} = 0.5\ \mu$S, determine:

a. The common-emitter hybrid equivalent circuit.
b. The common-base r_e model.

Solution:

a. $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.5\text{ mA}} = \mathbf{10.4\ \Omega}$$

$$h_{ie} = \beta r_e = (140)(10.4\ \Omega) = \mathbf{1.456\ k\Omega}$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

Note Fig. 5.102.

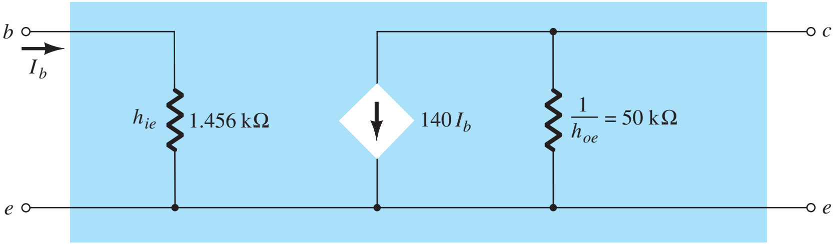


FIG. 5.102
Common-emitter hybrid equivalent circuit for the parameters of Example 5.19.

b. $r_e = \mathbf{10.4\ \Omega}$

$$\alpha \cong 1, \qquad r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\ \mu\text{S}} = \mathbf{2\ M\Omega}$$

Note Fig. 5.103.

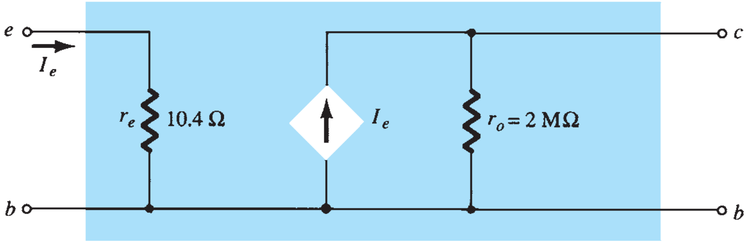


FIG. 5.103
Common-base r_e model for the parameters of Example 5.19.

A series of equations relating the parameters of each configuration for the hybrid equivalent circuit is provided in Appendix B. In Section 5.23 it is demonstrated that the hybrid parameter h_{fe} (β_{ac}) is the least sensitive of the hybrid parameters to a change in collector current. Assuming, therefore, that $h_{fe} = \beta$ is a constant for the range of interest, is a fairly good approximation. It is $h_{ie} = \beta r_e$ that will vary significantly with I_C and should be determined at operating levels because it can have a real effect on the gain levels of a transistor amplifier.

5.20 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

The analysis using the approximate hybrid equivalent circuit of Fig. 5.104 for the common-emitter configuration and of Fig. 5.105 for the common-base configuration is very similar to that just performed using the r_e model. A brief overview of some of the most important configurations will be included in this section to demonstrate the similarities in approach and the resulting equations.

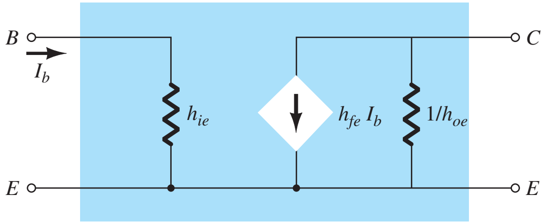


FIG. 5.104
Approximate common-emitter hybrid equivalent circuit.

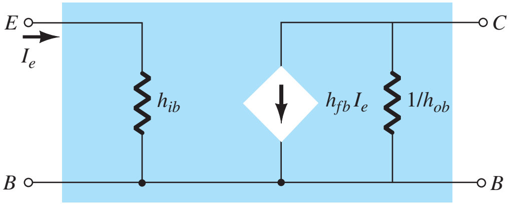


FIG. 5.105
Approximate common-base hybrid equivalent circuit.

Because the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the r_e model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as h_{ie}, h_{fe}, h_{ib}, and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the r_e model are related by the following equations, as discussed earlier in this chapter: $h_{ie} = \beta r_e$, $h_{fe} = \beta$, $h_{oe} = 1/r_o$, $h_{fb} = -\alpha$, and $h_{ib} = r_e$.

Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 5.106, the small-signal ac equivalent network will appear as shown in Fig. 5.107 using the approximate common-emitter hybrid equivalent model. Compare the similarities in appearance with Fig. 5.22 and the r_e model analysis. The similarities suggest that the analyses will be quite similar, and the results of one can be directly related to the other.

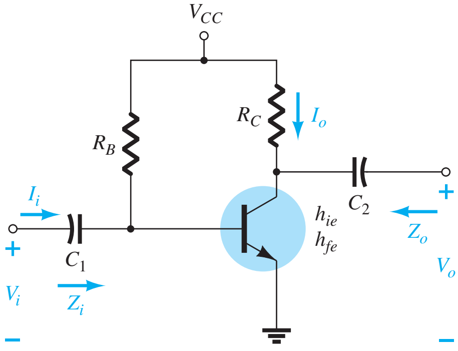


FIG. 5.106
Fixed-bias configuration.

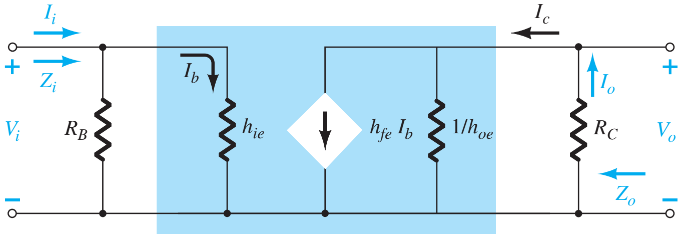


FIG. 5.107
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.106.

Z_i From Fig. 5.107,

$$\boxed{Z_i = R_B \| h_{ie}} \tag{5.143}$$

Z_o From Fig. 5.107,

$$\boxed{Z_o = R_C \| 1/h_{oe}} \tag{5.144}$$

A_v Using $R' = 1/h_{oe} \| R_C$, we obtain

$$\begin{aligned} V_o &= -I_o R' = -I_C R' \\ &= -h_{fe} I_b R' \end{aligned}$$

and
$$I_b = \frac{V_i}{h_{ie}}$$

with
$$V_o = -h_{fe}\frac{V_i}{h_{ie}}R'$$

so that
$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}}} \tag{5.145}$$

A_i Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, we find $I_b \cong I_i$ and $I_o = I_c = h_{fe}I_b = h_{fe}I_i$, and so

$$\boxed{A_i = \frac{I_o}{I_i} \cong h_{fe}} \tag{5.146}$$

EXAMPLE 5.20 For the network of Fig. 5.108, determine:

a. Z_i.
b. Z_o.
c. A_v.
d. A_i.

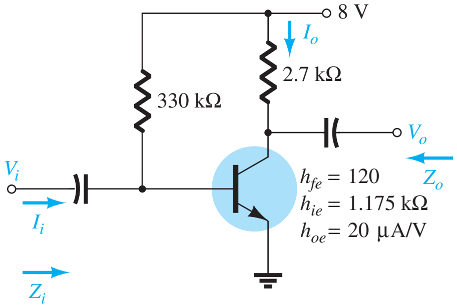

8 V
I_o
2.7 kΩ
330 kΩ
V_o
V_i
Z_o
$h_{fe} = 120$
$h_{ie} = 1.175\ \text{k}\Omega$
$h_{oe} = 20\ \mu\text{A/V}$
I_i
Z_i

FIG. 5.108
Example 5.20.

Solution:

a. $Z_i = R_B \| h_{ie} = 330\ \text{k}\Omega \| 1.175\ \text{k}\Omega$
$\quad \cong h_{ie} = \mathbf{1.171\ k\Omega}$

b. $$r_o = \frac{1}{h_{oe}} = \frac{1}{20\ \mu\text{A/V}} = 50\ \text{k}\Omega$$

$$Z_o = \frac{1}{h_{oe}} \| R_C = 50\ \text{k}\Omega \| 2.7\ \text{k}\Omega = \mathbf{2.56\ k\Omega} \cong R_C$$

c. $$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\frac{(120)(2.7\ \text{k}\Omega \| 50\ \text{k}\Omega)}{1.171\ \text{k}\Omega} = \mathbf{-262.34}$$

d. $A_i \cong h_{fe} = \mathbf{120}$

Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 5.109, the resulting small-signal ac equivalent network will have the same appearance as Fig. 5.107, with R_B replaced by $R' = R_1 \| R_2$.

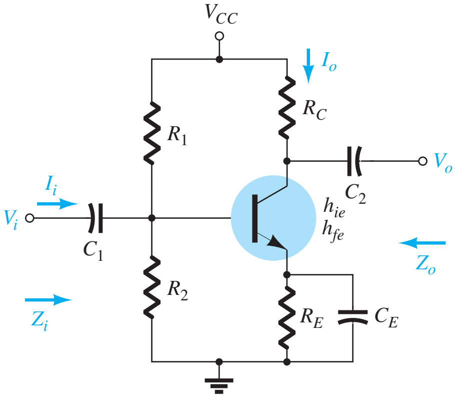

V_{CC}
I_o
R_C
R_1
V_o
I_i
C_2
h_{ie}
h_{fe}
V_i
C_1
Z_o
R_2
Z_i
R_E
C_E

FIG. 5.109
Voltage-divider bias configuration.

Z_i From Fig. 5.107 with $R_B = R'$,

$$\boxed{Z_i = R_1 \| R_2 \| h_{ie}} \tag{5.147}$$

Z_o From Fig. 5.107,

$$\boxed{Z_o \cong R_C} \tag{5.148}$$

A_v

$$\boxed{A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}}} \tag{5.149}$$

A_i

$$\boxed{A_i = \frac{h_{fe}(R_1 \| R_2)}{R_1 \| R_2 + h_{ie}}} \tag{5.150}$$

Unbypassed Emitter-Bias Configuration

For the CE unbypassed emitter-bias configuration of Fig. 5.110, the small-signal ac model will be the same as Fig. 5.30, with βr_e replaced by h_{ie} and βI_b by $h_{fe} I_b$. The analysis will proceed in the same manner.

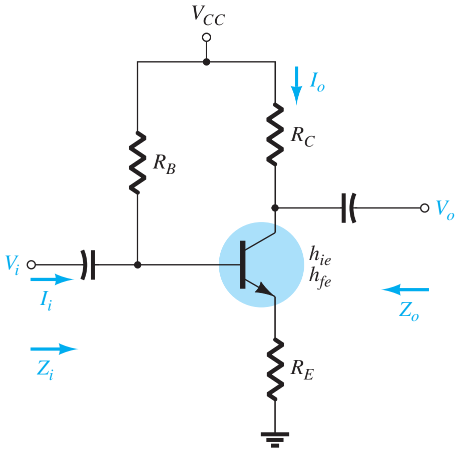


FIG. 5.110

CE unbypassed emitter-bias configuration.

Z_i

$$\boxed{Z_b \cong h_{fe} R_E} \tag{5.151}$$

and

$$\boxed{Z_i = R_B \| Z_b} \tag{5.152}$$

Z_o

$$\boxed{Z_o = R_C} \tag{5.153}$$

A_v

$$A_v = -\frac{h_{fe} R_C}{Z_b} \cong -\frac{h_{fe} R_C}{h_{fe} R_E}$$

and

$$\boxed{A_v \cong -\frac{R_C}{R_E}} \tag{5.154}$$

A_i

$$\boxed{A_i = -\frac{h_{fe}R_B}{R_B + Z_b}} \qquad \textbf{(5.155)}$$

or

$$\boxed{A_i = -A_v\frac{Z_i}{R_C}} \qquad \textbf{(5.156)}$$

Emitter-Follower Configuration

For the emitter-follower of Fig. 5.38, the small-signal ac model will match that of Fig. 5.111, with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$. The resulting equations will therefore be quite similar.

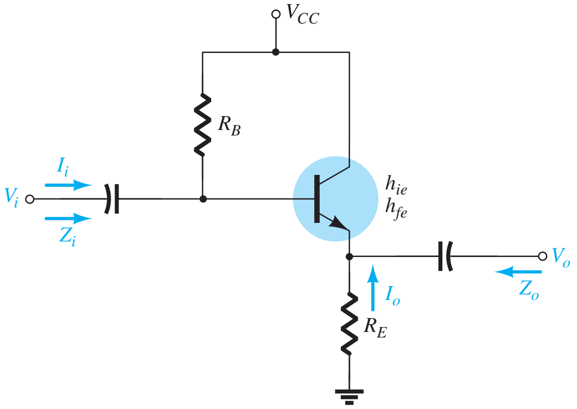


FIG. 5.111
Emitter-follower configuration.

Z_i

$$\boxed{Z_b \cong h_{fe}R_E} \qquad \textbf{(5.157)}$$

$$\boxed{Z_i = R_B \| Z_b} \qquad \textbf{(5.158)}$$

Z_o For Z_o, the output network defined by the resulting equations will appear as shown in Fig. 5.112. Review the development of the equations in Section 5.8 and

$$Z_o = R_E \| \frac{h_{ie}}{1 + h_{fe}}$$

or, because $1 + h_{fe} \cong h_{fe}$,

$$\boxed{Z_o \cong R_E \| \frac{h_{ie}}{h_{fe}}} \qquad \textbf{(5.159)}$$

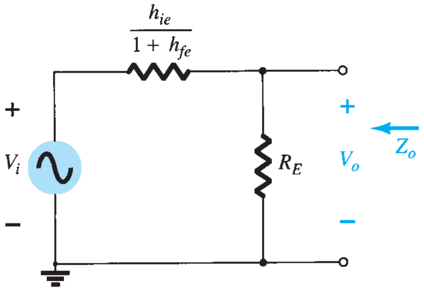


FIG. 5.112
Defining Z_o for the emitter-follower configuration.

A_v For the voltage gain, the voltage-divider rule can be applied to Fig. 5.112 as follows:

$$V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but, since $1 + h_{fe} \cong h_{fe}$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{R_E}{R_E + h_{ie}/h_{fe}}} \qquad \textbf{(5.160)}$$

A_i

$$\boxed{A_i = \frac{h_{fe} R_B}{R_B + Z_b}} \qquad \textbf{(5.161)}$$

or

$$\boxed{A_i = -A_v \frac{Z_i}{R_E}} \qquad \textbf{(5.162)}$$

Common-Base Configuration

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 5.113. Substituting the approximate common-base hybrid equivalent model results in the network of Fig. 5.114, which is very similar to Fig. 5.44.

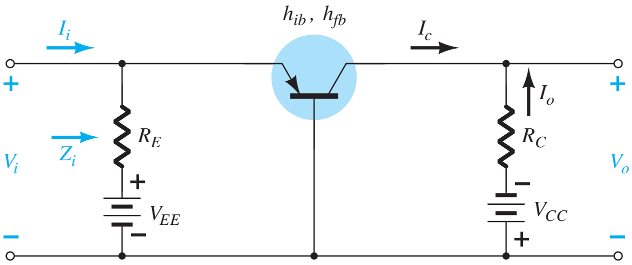


FIG. 5.113
Common-base configuration.

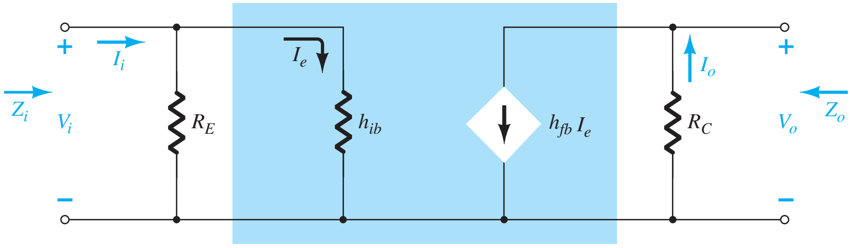


FIG. 5.114
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.113.

We have the following results from Fig. 5.114.

Z_i

$$\boxed{Z_i = R_E \| h_{ib}} \qquad \textbf{(5.163)}$$

Z_o

$$\boxed{Z_o = R_C} \qquad \textbf{(5.164)}$$

A_v

$$V_o = -I_oR_C = -(h_{fb}I_e)R_C$$

with $$I_e = \frac{V_i}{h_{ib}} \quad \text{and} \quad V_o = -h_{fb}\frac{V_i}{h_{ib}}R_C$$

so that $$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{fb}R_C}{h_{ib}}} \tag{5.165}$$

A_i

$$\boxed{A_i = \frac{I_o}{I_i} = h_{fb} \cong -1} \tag{5.166}$$

EXAMPLE 5.21 For the network of Fig. 5.115, determine:

a. Z_i.
b. Z_o.
c. A_v.
d. A_i.

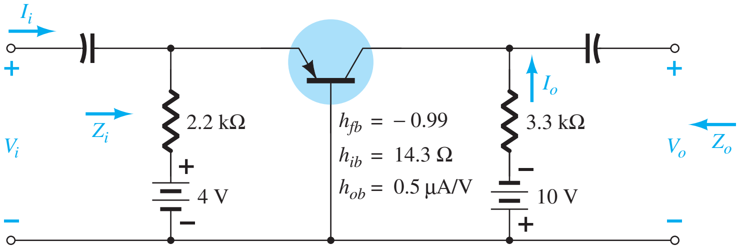


FIG. 5.115
Example 5.21.

Solution:

a. $Z_i = R_E \| h_{ib} = 2.2\,\text{k}\Omega \| 14.3\,\Omega = \mathbf{14.21\,\Omega} \cong h_{ib}$

b. $r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\,\mu\text{A/V}} = \mathbf{2\,M\Omega}$

$Z_o = \dfrac{1}{h_{ob}} \| R_C \cong R_C = \mathbf{3.3\,k\Omega}$

c. $A_v = -\dfrac{h_{fb}R_C}{h_{ib}} = -\dfrac{(-0.99)(3.3\,\text{k}\Omega)}{14.21} = \mathbf{229.91}$

d. $A_i \cong h_{fb} = \mathbf{-1}$

The remaining configurations that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the r_e or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

5.21 COMPLETE HYBRID EQUIVALENT MODEL

The analysis of Section 5.20 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the effect of h_r and define in more specific terms the effect of h_o. It is important to realize that because the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to insert the parameters defined for each configuration. That is, for a common-base configuration, h_{fb}, h_{ib}, and so on, are employed, whereas for a common-emitter configuration, h_{fe}, h_{ie}, and so on, are used. Recall that Appendix A permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 5.116 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 5.117 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of h_i, h_r, h_f, and h_o. Unlike the analysis of previous sections of this chapter, here the current gain A_i will be determined first because the equations developed will prove useful in the determination of the other parameters.

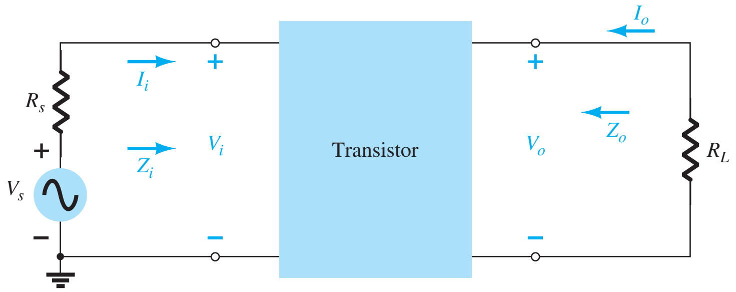


FIG. 5.116
Two-port system.

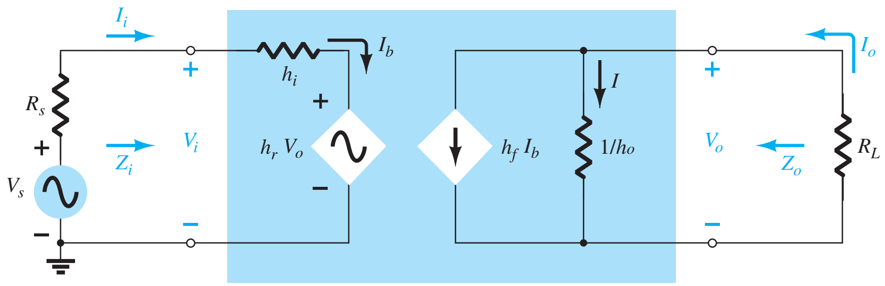


FIG. 5.117
Substituting the complete hybrid equivalent circuit into the two-port system of Fig. 5.116.

Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}} \tag{5.167}$$

Note that the current gain reduces to the familiar result of $A_i = h_f$ if the factor $h_o R_L$ is sufficiently small compared to 1.

Voltage Gain, $A_v = V_o/V_i$

Applying Kirchhoff's voltage law to the input circuit results in

$$V_i = I_i h_i + h_r V_o$$

Substituting $I_i = (1 + h_oR_L)I_o/h_f$ from Eq. (5.167) and $I_o = -V_o/R_L$ from above results in

$$V_i = \frac{-(1 + h_oR_L)h_i}{h_fR_L}V_o + h_rV_o$$

Solving for the ratio V_o/V_i yields

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-h_fR_L}{h_i + (h_ih_o - h_fh_r)R_L}} \tag{5.168}$$

In this case, the familiar form of $A_v = -h_fR_L/h_i$ returns if the factor $(h_ih_o - h_fh_r)R_L$ is sufficiently small compared to h_i.

Input Impedance, $Z_i = V_i/I_i$

For the input circuit,

$$V_i = h_iI_i + h_rV_o$$

Substituting $V_o = -I_oR_L$

we have $V_i = h_iI_i - h_rR_LI_o$

Because $A_i = \dfrac{I_o}{I_i}$

$$I_o = A_iI_i$$

so that the equation above becomes

$$V_i = h_iI_i - h_rR_LA_iI_i$$

Solving for the ratio V_i/I_i, we obtain

$$Z_i = \frac{V_i}{I_i} = h_i - h_rR_LA_i$$

and substituting

$$A_i = \frac{h_f}{1 + h_oR_L}$$

yields $$\boxed{Z_i = \frac{V_i}{I_i} = h_i - \frac{h_fh_rR_L}{1 + h_oR_L}} \tag{5.169}$$

The familiar form of $Z_i = h_i$ is obtained if the second factor in the denominator (h_oR_L) is sufficiently smaller than one.

Output Impedance, $Z_o = V_o/I_o$

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal V_s set to zero. For the input circuit with $V_s = 0$,

$$I_i = -\frac{h_rV_o}{R_s + h_i}$$

Substituting this relationship into the equation from the output circuit yields

$$\begin{aligned} I_o &= h_fI_i + h_oV_o \\ &= -\frac{h_fh_rV_o}{R_s + h_i} + h_oV_o \end{aligned}$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_fh_r/(h_i + R_s)]}} \tag{5.170}$$

In this case, the output impedance is reduced to the familiar form $Z_o = 1/h_o$ for the transistor when the second factor in the denominator is sufficiently smaller than the first.

EXAMPLE 5.22 For the network of Fig. 5.118, determine the following parameters using the complete hybrid equivalent model and compare to the results obtained using the approximate model.

a. Z_i and Z_i'.
b. A_v.
c. $A_i = I_o/I_i$.
d. Z_o' (within R_C) and Z_o (including R_C).

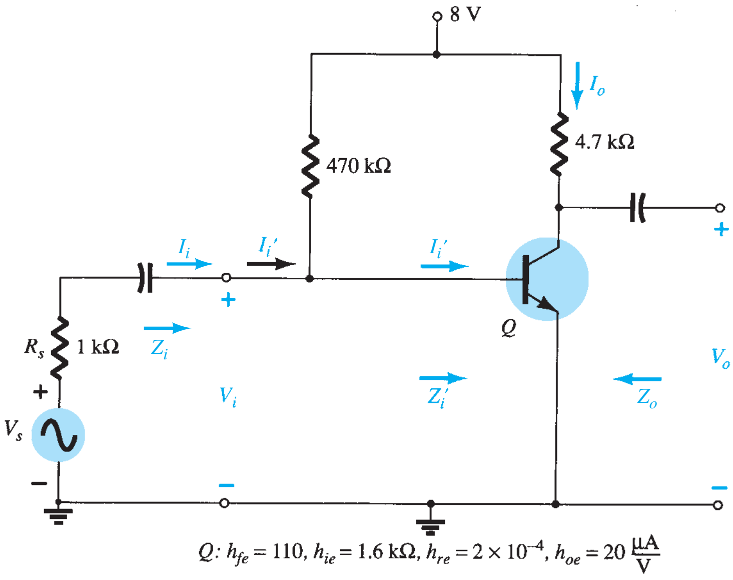

8 V
I_o
470 kΩ
4.7 kΩ
I_i
I_i'
I_i'
+
+
R_s
1 kΩ
Z_i
Q
V_o
V_i
Z_i'
Z_o
V_s
–
–
–
Q: $h_{fe} = 110$, $h_{ie} = 1.6\text{ k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 20\ \frac{\mu A}{V}$

FIG. 5.118
Example 5.22.

Solution: Now that the basic equations for each quantity have been derived, the order in which they are calculated is arbitrary. However, the input impedance is often a useful quantity to know, and therefore will be calculated first. The complete common-emitter hybrid equivalent circuit has been substituted and the network redrawn as shown in Fig. 5.119. A Thévenin equivalent circuit for the input section of Fig. 5.119 results in the input equivalent of Fig. 5.120 because $E_{\text{Th}} \cong V_s$ and $R_{\text{Th}} \cong R_s = 1\text{ k}\Omega$ (a result of $R_B = 470\text{ k}\Omega$ being much greater than $R_s = 1\text{ k}\Omega$). In this example, $R_L = R_C$, and I_o is defined as the current through R_C as in previous examples of this chapter. The output impedance Z_o as defined by Eq. (5.170) is for the output transistor terminals only. It does not include the effects of R_C. Z_o is simply the parallel combination of Z_o and R_L. The resulting configuration of

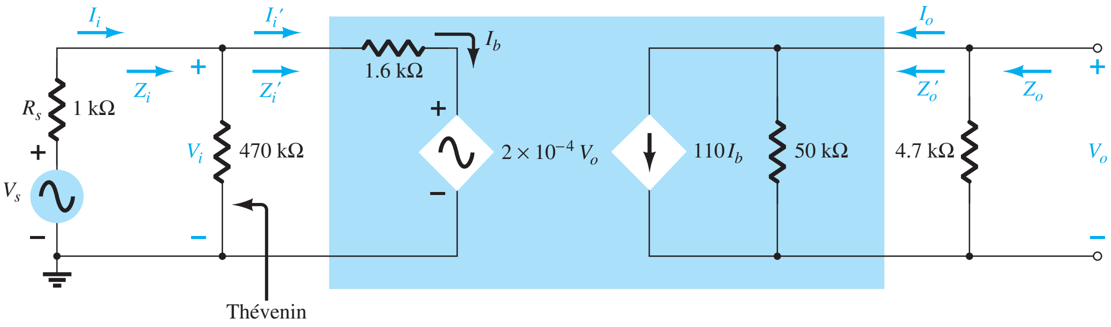

I_i
I_i'
I_b
I_o
Z_i
Z_i'
1.6 kΩ
Z_o'
Z_o
R_s
1 kΩ
+
+
+
V_i
470 kΩ
$2 \times 10^{-4} V_o$
$110 I_b$
50 kΩ
4.7 kΩ
V_o
V_s
–
–
–
–
Thévenin

FIG. 5.119
Substituting the complete hybrid equivalent circuit into the ac equivalent network of Fig. 5.118.

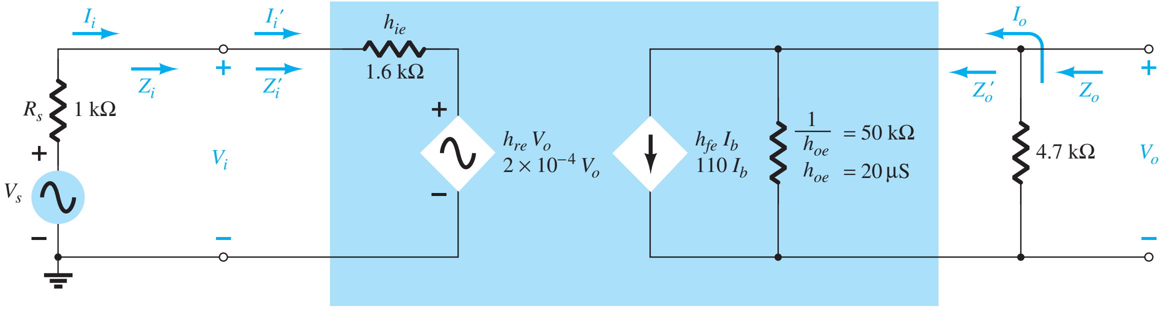


FIG. 5.120

Replacing the input section of Fig. 5.119 with a Thévenin equivalent circuit.

Fig. 5.120 is then an exact duplicate of the defining network of Fig. 5.117, and the equations derived above can be applied.

a. Eq. (5.169):

$$Z_i = \frac{V_i}{I_i} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1 + h_{oe}R_L}$$

$$= 1.6\,\text{k}\Omega - \frac{(110)(2 \times 10^{-4})(4.7\,\text{k}\Omega)}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$

$$= 1.6\,\text{k}\Omega - 94.52\,\Omega$$

$$= \mathbf{1.51\,k\Omega}$$

versus 1.6 kΩ using simply h_{ie}; and

$$Z_i' = 470\,\text{k}\Omega \| Z_i \cong Z_i = \mathbf{1.51\,k\Omega}$$

b. Eq. (5.168):

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L}$$

$$= \frac{-(110)(4.7\,\text{k}\Omega)}{1.6\,\text{k}\Omega + [(1.6\,\text{k}\Omega)(20\,\mu\text{S}) - (110)(2 \times 10^{-4})]4.7\,\text{k}\Omega}$$

$$= \frac{-517 \times 10^3\,\Omega}{1.6\,\text{k}\Omega + (0.032 - 0.022)4.7\,\text{k}\Omega}$$

$$= \frac{-517 \times 10^3\,\Omega}{1.6\,\text{k}\Omega + 47\,\Omega}$$

$$= \mathbf{-313.9}$$

versus −323.125 using $A_v \cong -h_{fe}R_L/h_{ie}$.

c. Eq. (5.167):

$$A_i' = \frac{I_o}{I_i'} = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{110}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$

$$= \frac{110}{1 + 0.094} = \mathbf{100.55}$$

versus 110 using simply h_{fe}. Because $470\,\text{k}\Omega \gg Z_i'$, $I_i \cong I_i'$ and $A_i \cong$ **100.55** also.

d. Eq. (5.170):

$$Z_o' = \frac{V_o}{I_o} = \frac{1}{h_{oe} - [h_{fe}h_{re}/(h_{ie} + R_s)]}$$

$$= \frac{1}{20\,\mu\text{S} - [(110)(2 \times 10^{-4})/(1.6\,\text{k}\Omega + 1\,\text{k}\Omega)]}$$

$$= \frac{1}{20\,\mu\text{S} - 8.46\,\mu\text{S}}$$

$$= \frac{1}{11.54\,\mu\text{S}}$$

$$= \mathbf{86.66\,k\Omega}$$

which is greater than the value determined from $1/h_{oe}$, 50 kΩ; and

$$Z_o = R_C \| Z_o' = 4.7\text{ k}\Omega \| 86.66\text{ k}\Omega = \mathbf{4.46\text{ k}\Omega}$$

versus 4.7 kΩ using only R_C.

Note from the results above that the approximate solutions for A_v and Z_i were very close to those calculated with the complete equivalent model. In fact, even A_i was off by less than 10%. The higher value of Z_o' only contributed to our earlier conclusion that Z_o' is often so high that it can be ignored compared to the applied load. However, keep in mind that when there is a need to determine the effect of h_{re} and h_{oe}, the complete hybrid equivalent model must be used, as described earlier.

The specification sheet for a particular transistor typically provides the common-emitter parameters as noted in Fig. 5.92. The next example will employ the same transistor parameters appearing in Fig. 5.118 in a *pnp* common-base configuration to introduce the parameter conversion procedure and emphasize the fact that the hybrid equivalent model maintains the same layout.

EXAMPLE 5.23 For the common-base amplifier of Fig. 5.121, determine the following parameters using the complete hybrid equivalent model and compare the results to those obtained using the approximate model.

a. Z_i
b. A_i
c. A_v.
d. Z_o

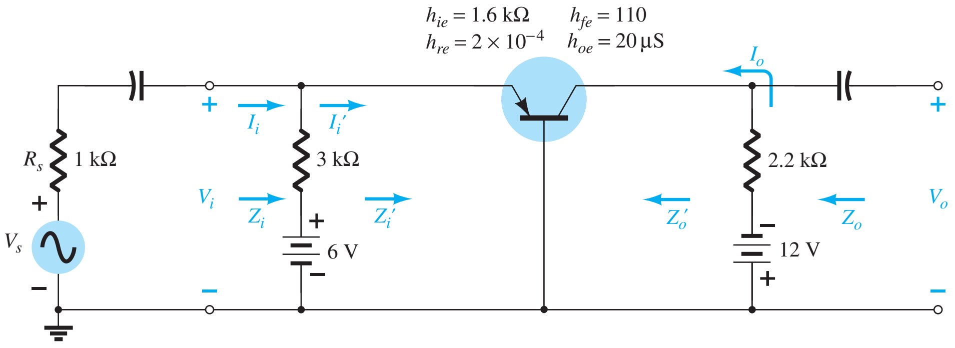


FIG. 5.121
Example 5.23.

Solution: The common-base hybrid parameters are derived from the common-emitter parameters using the approximate equations of Appendix B:

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} = \frac{1.6\text{ k}\Omega}{1 + 110} = \mathbf{14.41\ \Omega}$$

Note how closely the magnitude compares with the value determined from

$$h_{ib} = r_e = \frac{h_{ie}}{\beta} = \frac{1.6\text{ k}\Omega}{110} = 14.55\ \Omega$$

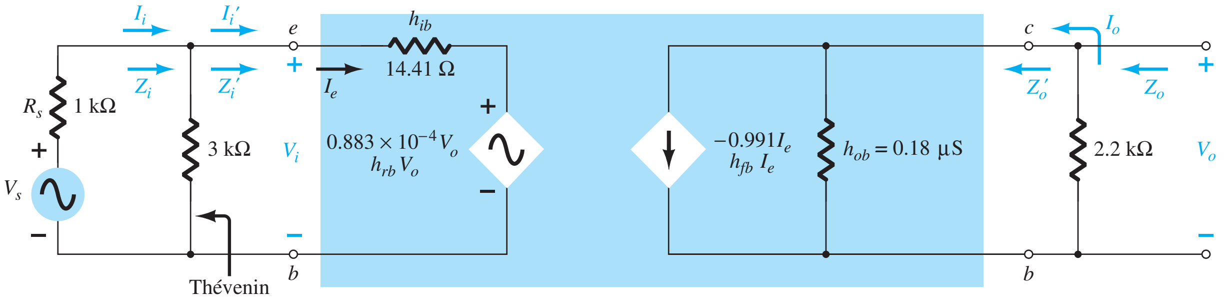
Also,

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} = \frac{(1.6\text{ k}\Omega)(20\ \mu\text{S})}{1 + 110} - 2 \times 10^{-4}$$

$$= \mathbf{0.883 \times 10^{-4}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} = \frac{-110}{1 + 110} = \mathbf{-0.991}$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} = \frac{20\ \mu\text{S}}{1 + 110} = \mathbf{0.18\ \mu S}$$



I_i
I_i'
e
h_{ib}
$14.41\ \Omega$
c
I_o
Z_i
Z_i'
I_e
Z_o'
Z_o
R_s
$1\ \text{k}\Omega$
$3\ \text{k}\Omega$
V_i
$0.883 \times 10^{-4} V_o$
$h_{rb} V_o$
$-0.991 I_e$
$h_{fb} I_e$
$h_{ob} = 0.18\ \mu\text{S}$
$2.2\ \text{k}\Omega$
V_o
V_s
Thévenin
b
b

FIG. 5.122

Small-signal equivalent for the network of Fig. 5.121.

Substituting the common-base hybrid equivalent circuit into the network of Fig. 5.121 results in the small-signal equivalent network of Fig. 5.122. The Thévenin network for the input circuit results in $R_{\text{Th}} = 3\ \text{k}\Omega \| 1\ \text{k}\Omega = 0.75\ \text{k}\Omega$ for R_s in the equation for Z_o.

a. Eq. (5.169):

$$\begin{aligned} Z_i' = \frac{V_i}{I_i'} &= h_{ib} - \frac{h_{fb}h_{rb}R_L}{1 + h_{ob}R_L} \\ &= 14.41\ \Omega - \frac{(-1.991)(0.883 \times 10^{-4})(2.2\ \text{k}\Omega)}{1 + (0.18\ \mu\text{S})(2.2\ \text{k}\Omega)} \\ &= 14.41\ \Omega + 0.19\ \Omega \\ &= 14.60\ \Omega \end{aligned}$$

versus $14.41\ \Omega$ using $Z_i \cong h_{ib}$; and

$$Z_i = 3\ \text{k}\Omega \| Z_i' \cong Z_i' = \mathbf{14.60\ \Omega}$$

b. Eq. (5.167):

$$\begin{aligned} A_i' = \frac{I_o}{I_i'} &= \frac{h_{fb}}{1 + h_{ob}R_L} \\ &= \frac{-0.991}{1 + (0.18\ \mu\text{S})(2.2\ \text{k}\Omega)} \\ &= -0.991 \end{aligned}$$

Because $3\ \text{k}\Omega \gg Z_i'$, $I_i \cong I_i'$ and $A_i = I_o/I_i \cong \mathbf{-1}$.

c. Eq. (5.168):

$$\begin{aligned} A_v = \frac{V_o}{V_i} &= \frac{-h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{fb}h_{rb})R_L} \\ &= \frac{-(-0.991)(2.2\ \text{k}\Omega)}{14.41\ \Omega + [(14.41\Omega)(0.18\ \mu\text{S}) - (-0.991)(0.883 \times 10^{-4})]2.2\ \text{k}\Omega} \\ &= \mathbf{149.25} \end{aligned}$$

versus 151.3 using $A_v \cong -h_{fb}R_L/h_{ib}$.

d. Eq. (5.170):

$$\begin{aligned} Z_o' &= \frac{1}{h_{ob} - [h_{fb}h_{rb}/(h_{ib} + R_s)]} \\ &= \frac{1}{0.18\ \mu\text{S} - [(-0.991)(0.883 \times 10^{-4})/(14.41\ \Omega + 0.75\ \text{k}\Omega)]} \\ &= \frac{1}{0.295\ \mu\text{S}} \\ &= \mathbf{3.39\ M\Omega} \end{aligned}$$

versus $5.56\ \text{M}\Omega$ using $Z_o' \cong 1/h_{ob}$. For Z_o as defined by Fig. 5.122,

$$Z_o = R_C \| Z_o' = 2.2\ \text{k}\Omega \| 3.39\ \text{M}\Omega = \mathbf{2.199\ k\Omega}$$

versus $2.2\ \text{k}\Omega$ using $Z_o \cong R_C$.

5.22 HYBRID π MODEL

The last transistor model to be introduced is the hybrid π model of Fig. 5.123 which includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects.

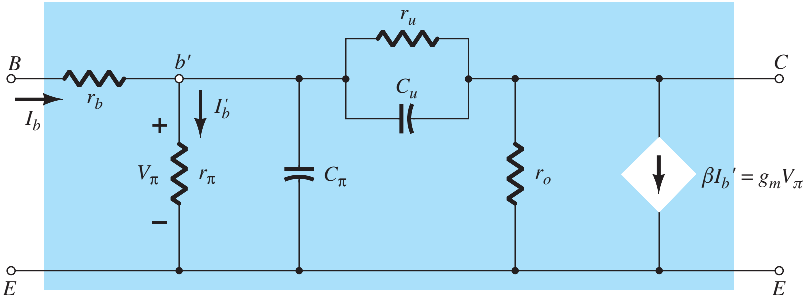


FIG. 5.123

Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

r_π, r_o, r_b, and r_u

The resistors r_π, r_o, r_b, and r_u are the resistances between the indicated terminals of the device when the device is in the active region. The resistance r_π (using the symbol π to agree with the hybrid π terminology) is simply βr_e as introduced for the common-emitter r_e model.

That is,

$$\boxed{r_\pi = \beta r_e} \tag{5.171}$$

The output resistance r_o is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 kΩ and 40 kΩ, is determined from the hybrid parameter h_{oe}, the Early voltage, or the output characteristics.

The resistance r_b includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms.

The resistance r_u (the subscript u refers to the *union* it provides between collector and base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than βr_o, which places it in the megohm range.

C_π and C_u

All the capacitors that appear in Fig. 5.123 are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large, and they can be considered open circuits. The capacitor C_π across the input terminals can range from a few *pF* to tens of *pF*. The capacitor C_u from base to collector is usually limited to a few *pF* but is magnified at the input and output by an effect called the Miller effect, to be introduced in Chapter 9.

$\beta I_b'$ or $g_m V_\pi$

It is important to note in Fig. 5.123 that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

Note the following parameter equivalence in Fig. 5.123:

$$\boxed{g_m = \frac{1}{r_e}} \tag{5.172}$$

and

$$\boxed{r_o = \frac{1}{h_{oe}}} \tag{5.173}$$

with

$$\boxed{\frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_u} \cong h_{re}} \tag{5.174}$$

Take particular note of the fact that the equivalent sources $\beta I'_b$ and $g_m V_\pi$ are both controlled current sources. One is controlled by a current at another place in the network and the other by a voltage at the input side of the network. The equivalence between the two is defined by

$$\beta I'_b = \frac{1}{r_e} \cdot r_e \beta I'_b = g_m I'_b \beta r_e = g_m(I'_b r_\pi) = g_m V_\pi$$

For the broad range of low- to mid-frequency analysis, the effect of the stray capacitive effects can be ignored due to the very high reactance levels associated with each. The resistance r_b is usually small enough with other series elements to be ignored while the resistance r_u is usually large enough compared to parallel elements to be ignored. The result is an equivalent network similar to the r_e model introduced and applied in this chapter.

In Chapter 9, when high-frequency effects are considered, the hybrid π model will be the model of choice.

5.23 VARIATIONS OF TRANSISTOR PARAMETERS

A variety of curves can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the variations with junction temperature and collector voltage and current.

The effect of the collector current on the r_e model and hybrid equivalent model is shown in Fig. 5.124. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in detail in Chapter 9. The parameters have all been normalized (a process described in detail in Section 9.5) to unity so that the relative change in magnitude with collector current can easily be determined. On each set of curves, such as in Figs. 5.124 to 5.126, the operating point at which the parameters were determined is always indicated. For this particular situation, the quiescent point is at the fairly typical values of $V_{CE} = 5.0$ V and $I_C = 1.0$ mA. Because the frequency and temperature of operation

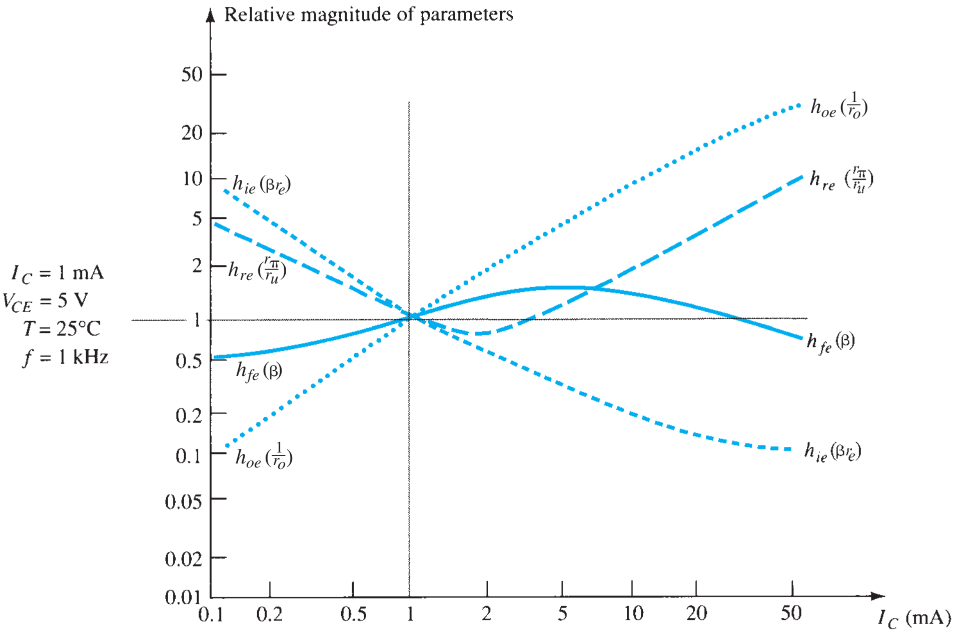


FIG. 5.124

Hybrid parameter variations with collector current.

also affect the parameters, these quantities are also indicated on the curves. Figure 5.124 shows the variation of the parameters with collector current. Note that at $I_C = 1$ mA the value of all the parameters has been normalized to 1 on the vertical axis. The result is that the magnitude of each parameter is compared to the values at the defined operating point. Because manufacturers typically use the hybrid parameters for plots of this type, they are the curves of choice in Fig. 5.124. However, to broaden the use of the curves the r_e and hybrid π equivalent parameters have also been added.

At first glance it is particularly interesting to note that:

The parameter $h_{fe}(\beta)$ varies the least of all the parameters of a transistor equivalent circuit when plotted against variations in collector current.

Figure 5.124 clearly reveals that for the full range of collector current the parameter $h_{fe}(\beta)$ varies from 0.5 of its Q-point value to a peak of about 1.5 times that value at a current of about 6 mA. For a transistor with a β of 100, it therefore varies from about 50 to 150. This seems like quite a bit, but look at h_{oe}, which jumps to almost 40 times its Q-point value at a collector current of 50 mA.

Figure 5.124 also shows that $h_{oe}(1/r_o)$ and $h_{ie}(\beta r_e)$ vary the most for the chosen current range. The parameter h_{ie} varies from about 10 times its Q-point value down to about one tenth the Q point value at 50 mA. This variation, however, should be expected because we know that the value of r_e is directly related to the emitter current by $r_e = 26\text{ mV}/I_E$. As $I_E(\cong I_C)$ increases, the value of r_e and therefore βr_e will decrease, as shown in Fig. 5.124.

Keep in mind as you review the curve of h_{oe} versus current that the actual output resistance r_o is $1/h_{oe}$. Therefore, as the curve increases with current, the value of r_o becomes less and less. Because r_o is a parameter that normally appears in parallel with the applied load, decreasing values of r_o can become a critical problem. The fact that r_o has dropped to almost 1/40 of its value at the Q-point could spell a real reduction in gain at 50 mA.

The parameter h_{re} varies quite a bit, but because its Q-point value is usually small enough to permit ignoring its effect, it is a parameter that is only of concern for collector currents that are much less, or quite a bit more, than the Q-point level.

This may seem like an extensive description of a set of characteristic curves. However, experience has revealed that graphs of this nature are too often reviewed without taking the time to fully appreciate the broad impact of what they are providing. These plots reveal a lot of information that could be extremely useful in the design process.

Figure 5.125 shows the variation in magnitude of the parameters due to changes in collector-to-emitter voltage. This set of curves is normalized at the same operating point as the curves of Fig. 5.124 to permit comparisons between the two. In this case, however, the vertical scale is in percent rather than whole numbers. The 200% level defines a set of parameters twice that at the 100% level. A level of 1000% would reflect a 10:1 change. Note that h_{fe} and h_{ie} are relatively steady in magnitude with variations in collector-to-emitter voltage, whereas for changes in collector current the variation is a great deal more

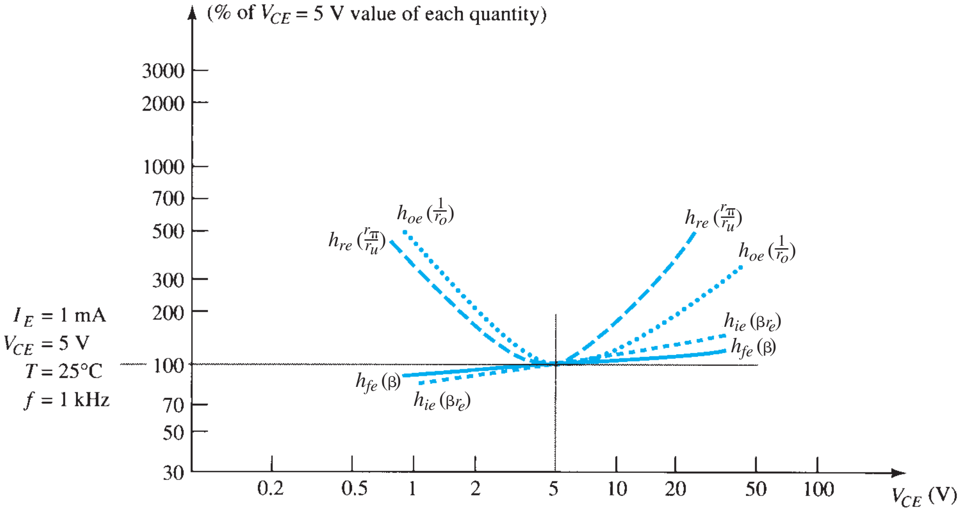


FIG. 5.125

Hybrid parameter variations with collector–emitter potential.

significant. In other words, if you want a parameter such as $h_{ie}(\beta r_e)$ to remain fairly steady, keep the variation of I_C to a minimum while worrying less about variations in the collector-to-emitter voltage. The variation of h_{oe} and h_{ie} remains significant for the indicated range of collector-to-emitter voltage.

In Fig. 5.126, the variation in parameters is plotted for changes in junction temperature. The normalization value is taken to be room temperature, $T = 25°\text{C}$. The horizontal scale is now a linear scale rather than the logarithmic scale employed in the two previous figures. In general:

All the parameters of a hybrid transistor equivalent circuit increase with temperature.

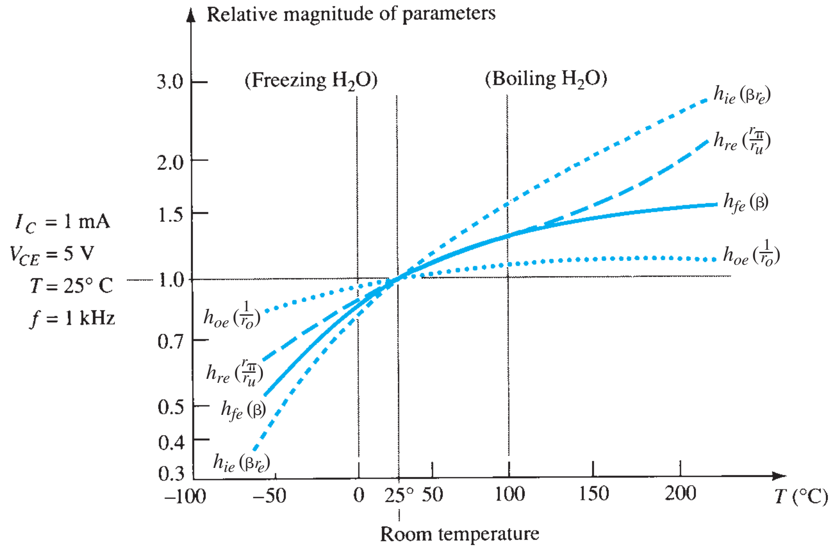


FIG. 5.126

Hybrid parameter variations with temperature.

However, again keep in mind that the actual output resistance r_o is inversely related to h_{oe}, so its value drops with an increase in h_{oe}. The greatest change is in h_{ie}, although note that the range of the vertical scale is considerably less than in the other plots. At a temperature of 200°C the value of h_{ie} is almost 3 times its Q-point value, but in Fig. 5.124 parameters jumped to almost 40 times the Q-point value.

Of the three parameters, therefore, the variation in collector current has by far the greatest effect on the parameters of a transistor equivalent circuit. Temperature is always a factor, but the effect of the collector current can be significant.

5.24 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, and isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain.

In general, therefore, if a system is not working properly, first disconnect the ac source and check the dc biasing levels.

In Fig. 5.127 we have four transistor configurations with specific voltage levels provided as measured by a DMM in the dc mode. The first test of any transistor network is to simply measure the base-to-emitter voltage of the transistor. The fact that it is only 0.3 V in this case suggests that the transistor is not "on" and perhaps sitting in its saturation mode. If this is a switching design then the result is expected, but if in the amplifier mode there is an open connection preventing the base voltage from reaching an operating level.

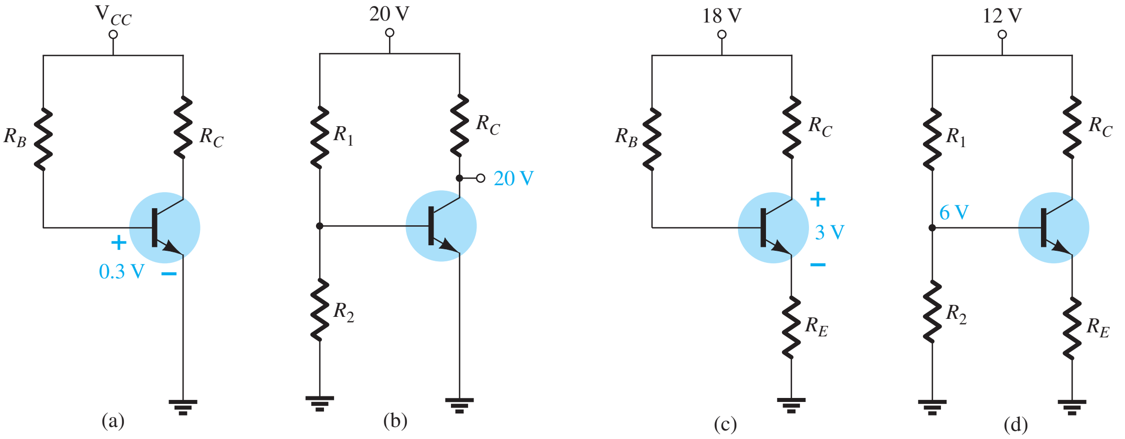


FIG. 5.127

Checking the dc levels to determine if a network is properly biased.

In Fig. 5.127b the fact that the voltage at the collector equals the supply voltage reveals that there is no drop across the resistor R_C and the collector current is zero. The resistor R_C is connected properly because it made the connection from the dc source to the collector. However, any one of the other elements may not have been connected properly, resulting in the absence of a base or collector current. In Fig. 5.127c the voltage drop across the collector-to-emitter voltage is too small compared with the applied dc voltage. Normally the voltage V_{CE} is in the mid-range of perhaps 6 V to 14 V. A reading of 18 V would cause the same concern as the reading of 3 V. The fact that the voltage levels exist at all suggests that all the elements are connected but the value of one or more of the resistive elements may be wrong. In Fig. 5.127d we find that the voltage at the base is exactly half the supply voltage. We know from this chapter that the resistance R_E will reflect back to the base by a factor of beta and appear in parallel with R_2. The result would be a base voltage less than half the supply voltage. The measurement suggests that the base lead is not connected to the voltage divider, causing an even split of the 20-V source.

In a typical laboratory setting, the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 5.128. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the

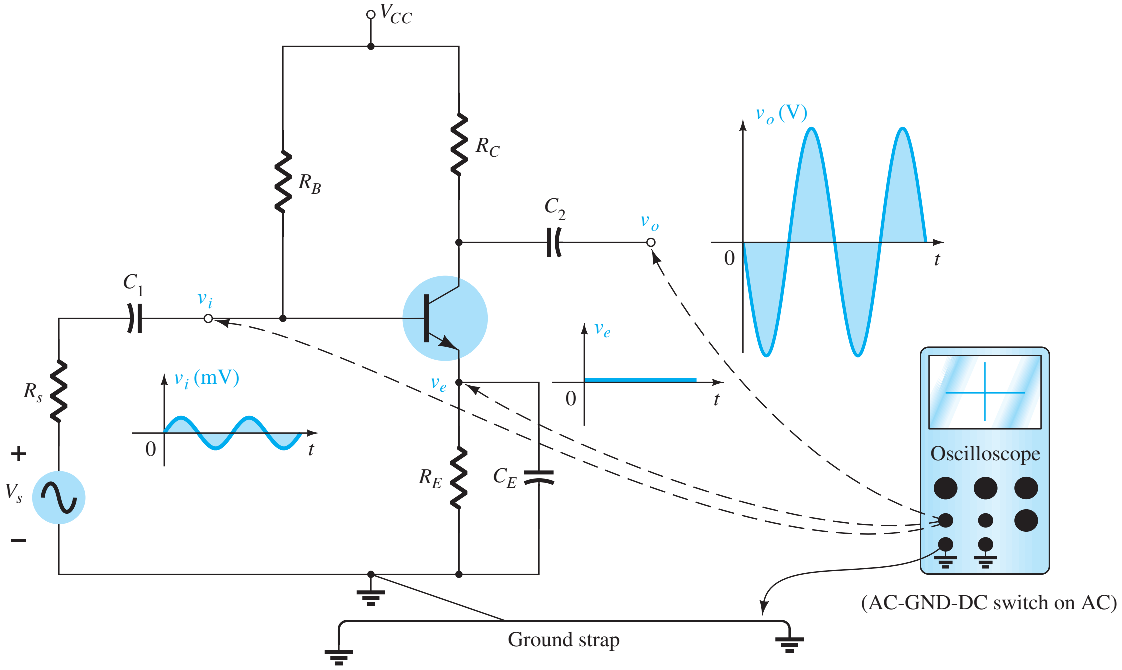


FIG. 5.128

Using the oscilloscope to measure and display various voltages of a BJT amplifier.

network, providing the patterns appearing in Fig. 5.128. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that v_o is measured in volts and v_i in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check V_{BE} and the levels of V_B, V_{CE}, and V_E to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

A poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted, and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it is good procedure to start with the applied signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby defining the region that must be investigated further. The waveform obtained on the oscilloscope will certainly help in defining the possible problems with the system.

If the response for the network of Fig. 5.128 is as appears in Fig. 5.129, the network has a malfunction that is probably in the emitter area. An ac response across the emitter is unexpected, and the gain of the system as revealed by v_o is much lower. Recall for this configuration that the gain is much greater if R_E is bypassed. The response obtained suggests that R_E is not bypassed by the capacitor, and the terminal connections of the capacitor and the capacitor itself should be checked. In this case, a checking of the dc levels will probably not isolate the problem area because the capacitor has an "open-circuit" equivalent for dc. In general, prior knowledge of what to expect, familiarity with the instrumentation, and, most important, experience are all factors that contribute to the development of an effective approach to the art of troubleshooting.

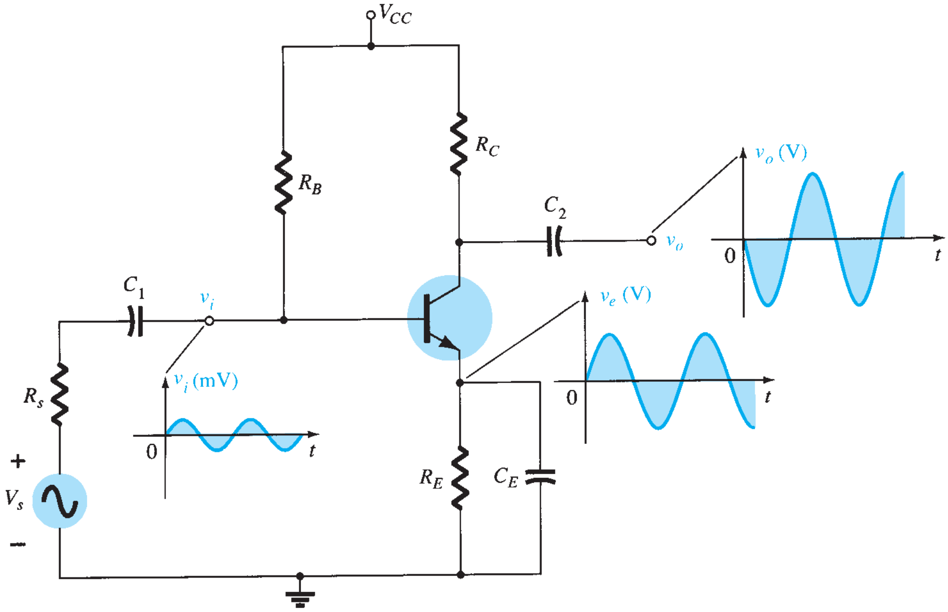


FIG. 5.129

The waveforms resulting from a malfunction in the emitter area.

5.25 PRACTICAL APPLICATIONS

Audio Mixer

When two or more signals are to be combined into a single audio output, mixers such as shown in Fig. 5.130 are employed. The potentiometers at the input are the volume controls for each channel, with potentiometer R_3 included to provide additional balance between

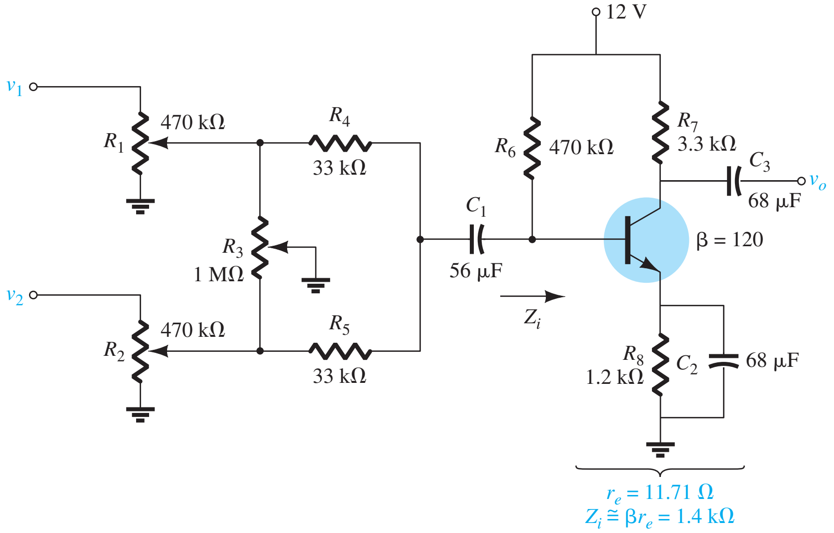


FIG. 5.130

Audio mixer.

the two signals. Resistors R_4 and R_5 are there to ensure that one channel does not load down the other, that is, to ensure that one signal does not appear as a load to the other, draw power, and affect the desired balance on the mixed signal.

The effect of resistors R_4 and R_5 is an important one that should be discussed in some detail. A dc analysis of the transistor configuration results in $r_e = 11.71\ \Omega$, which will establish an input impedance to the transistor of about 1.4 kΩ. The parallel combination of $R_6 \| Z_i$ is also approximately 1.4 kΩ. Setting both volume controls to their maximum value and the balance control R_3 to its midpoint result in the equivalent network of Fig. 5.131a. The signal at v_1 is assumed to be a low-impedance microphone with an internal resistance of 1 kΩ. The signal at v_2 is assumed to be a guitar amplifier with a higher internal impedance of 10 kΩ. Because the 470-kΩ and 500-kΩ resistors are in parallel for the above conditions, they can be combined and replaced with a single resistor of about 242 kΩ. Each source will then have an equivalent such as shown in Fig. 5.131b for the microphone. Applying Thévenin's theorem shows that it is an excellent approximation to simply drop the 242 kΩ and assume that the equivalent network is as shown for each channel. The result is the equivalent network of Fig. 5.131c for the input section of the mixer. Applying the superposition theorem results in the following equation for the ac voltage at the base of the transistor:

$$v_b = \frac{(1.4\text{ k}\Omega \| 43\text{ k}\Omega)v_{s_1}}{34\text{ k}\Omega + (1.4\text{ k}\Omega \| 43\text{ k}\Omega)} + \frac{(1.4\text{ k}\Omega \| 34\text{ k}\Omega)v_{s_2}}{43\text{ k}\Omega + (1.4\text{ k}\Omega \| 34\text{ k}\Omega)}$$

$$= 38 \times 10^{-3}v_{s_1} + 30 \times 10^{-3}v_{s_2}$$

With $r_e = 11.71\ \Omega$, the gain of the amplifier is $-R_C/r_e = 3.3\text{ k}\Omega/11.71\ \Omega = -281.8$, and the output voltage is

$$v_o = -10.7v_{s_1} - 8.45v_{s_2}$$

which provides a pretty good balance between the two signals, even though they have a 10:1 ratio in internal impedance. In general, the system will respond quite well. However, if we now remove the 33-kΩ resistors from the diagram of Fig. 5.131c, the equivalent network of Fig. 5.132 results, and the following equation for v_b is obtained using the superposition theorem:

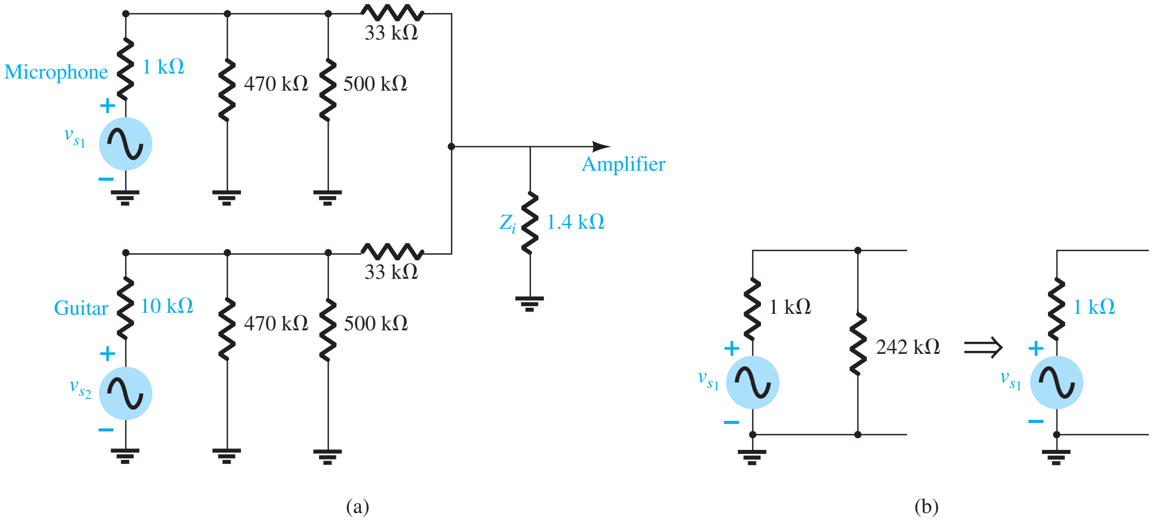
$$v_b = \frac{(1.4\text{ k}\Omega \| 10\text{ k}\Omega)v_{s_1}}{1\text{ k}\Omega + 1.4\text{ k}\Omega \| 10\text{ k}\Omega} + \frac{(1.4\text{ k}\Omega \| 1\text{ k}\Omega)v_{s_2}}{10\text{ k}\Omega + (1.4\text{ k}\Omega \| 1\text{ k}\Omega)}$$

$$= 0.55v_{s_1} + 0.055v_{s_2}$$

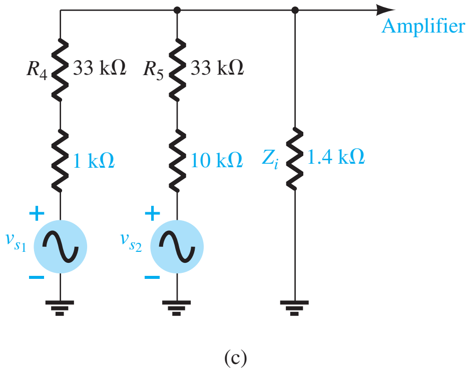
Using the same gain as before, we obtain the output voltage as

$$v_o = 155v_{s_1} + 15.5v_{s_2} \cong 155v_{s_1}$$

which indicates that the microphone will be quite loud and clear and the guitar input essentially lost.



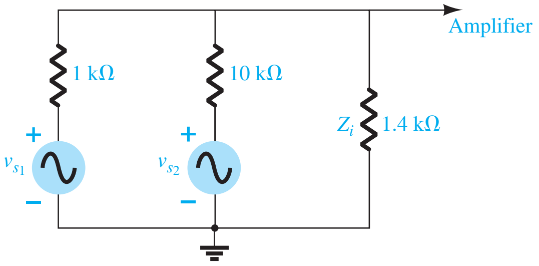
33 kΩ
Microphone
1 kΩ
470 kΩ
500 kΩ
v_{s_1}
Amplifier
Z_i
1.4 kΩ
33 kΩ
Guitar
10 kΩ
470 kΩ
500 kΩ
v_{s_2}
1 kΩ
242 kΩ
v_{s_1}
1 kΩ
v_{s_1}
(a)
(b)



Amplifier
R_4
33 kΩ
R_5
33 kΩ
1 kΩ
10 kΩ
Z_i
1.4 kΩ
v_{s_1}
v_{s_2}
(c)

FIG. 5.131

(a) Equivalent network with R_3 set at the midpoint and the volume controls on their maximum settings; (b) finding the Thévenin equivalent for channel 1; (c) substituting the Thévenin equivalent networks into Fig. 5.131a.



Amplifier
1 kΩ
10 kΩ
Z_i
1.4 kΩ
v_{s_1}
v_{s_2}

FIG. 5.132

Redrawing the network of Fig. 5.131c with the 33-kΩ resistors removed.

The importance of the 33-kΩ resistors is therefore defined. It makes each applied signal appear to have a similar impedance level so that there is good balance at the output. One might suggest that the larger resistor improves the balance. However, even though the balance at the base of the transistor may be better, the strength of the signal at the base of the transistor will be less, and the output level reduced accordingly. In other words, the choice of resistors R_4 and R_5 is a give-and-take situation between the input level at the base of the transistor and the balance of the output signal.

To demonstrate that the capacitors are truly short-circuit equivalents in the audio range, substitute a very low audio frequency of 100 Hz into the reactance equation of a 56-μF capacitor:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(100\text{ Hz})(56\ \mu\text{F})} = 28.42\ \Omega$$

A level of 28.42 Ω compared to any of the neighboring impedances is certainly small enough to be ignored. Higher frequencies will have even less effect.

A similar mixer will be discussed in connection with the junction field effect transistor (JFET) in the following chapter. The major difference will be the fact that the input impedance of the JFET can be approximated by an open circuit rather than the rather low-level input impedance of the BJT configuration. The result will be a higher signal level at the input to the JFET amplifier. However, the gain of the FET is much less than that of the BJT transistor, resulting in output levels that are actually quite similar.

Preamplifier

The primary function of a **preamplifier** is as its name implies: **an amplifier used to pick up the signal from its primary source and then operate on it in preparation for its passage into the amplifier section.** Typically, a preamplifier will amplify the signal, control its volume, perhaps change its input impedance characteristics, and if necessary determine its route through the stages to follow—in total, a stage of any system with a multitude of functions.

A preamplifier such as shown in Fig. 5.133 is often used with dynamic microphones to bring the signal level up to levels that are suitable for further amplification or power amplifiers. Typically, dynamic microphones are low-impedance microphones because their internal resistance is determined primarily by the winding of the voice coil. The basic construction consists of a voice coil attached to a small diaphragm that is free to move within a permanent magnet. When one speaks into the microphone, the diaphragm moves accordingly and causes the voice coil to move in the same manner within the magnetic field. In accord with Faraday's law, a voltage will be induced across the coil that will carry the audio signal.

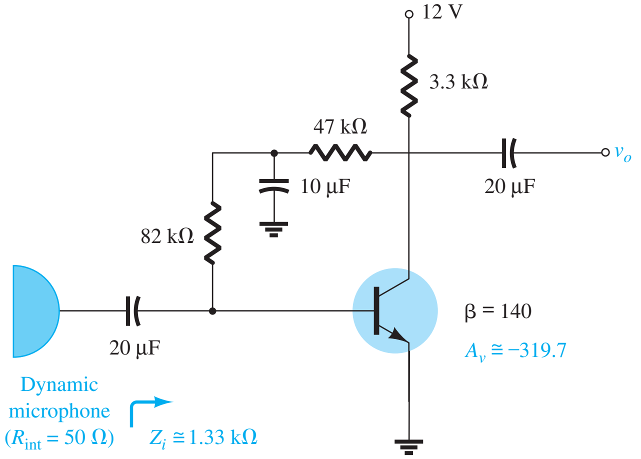


FIG. 5.133

Preamplifier for a dynamic microphone.

Because it is a low-impedance microphone, the input impedance of the transistor amplifier does not have to be that high to pick up most of the signal. Because the internal impedance of a dynamic microphone may be as low as 20 Ω to 100 Ω, most of the signal would be picked up with an amplifier having an input impedance as low as 1 to 2 kΩ. This, in fact, is the case for the preamplifier of Fig. 5.133. For dc biasing conditions, the collector dc feedback configuration was chosen because of its high stablity characteristics.

In the ac domain, the 10-μF capacitor will assume a short-circuit state (on an approximate basis), placing the 82-kΩ resistor across the input impedance of the transistor and the 47 kΩ across the output of the transistor. A dc analysis of the transistor configuration results in $r_e = 9.64\ \Omega$, giving an ac gain determined by

$$A_v = -\frac{(47\ \text{k}\Omega \| 3.3\ \text{k}\Omega)}{9.64\ \Omega} = \mathbf{-319.7}$$

which is excellent for this application. Of course, the gain will drop when this pickup stage of the design is connected to the input of the amplifier section. That is, the input resistance of the next stage will appear in parallel with the 47-kΩ and 3.3-kΩ resistors and will drop the gain below the unloaded level of 319.7.

The input impedance of the preamplifier is determined by

$$Z_i = 82\ \text{k}\Omega \| \beta r_e = 82\ \text{k}\Omega \| (140)(9.64\ \Omega) = 82\ \text{k}\Omega \| 1.34\ \text{k}\Omega = \mathbf{1.33\ k\Omega}$$

which is also fine for most low-impedance dynamic microphones. In fact, for a microphone with an internal impedance of 50 Ω, the signal at the base would be over 98% of that available. This discussion is important because if the impedance of the microphone is a great deal more, say, 1 kΩ, the preamplifier would have to be designed differently to ensure that the input impedance was at least 10 kΩ or more.

Random-Noise Generator

There is often a need for a random-noise generator to test the response of a speaker, microphone, filter, and, in fact, any system designed to work over a wide range of frequencies. A **random-noise generator** is just as its name implies: **a generator that generates signals of random amplitude and frequency.** The fact that these signals are usually totally unintelligible and unpredictable is the reason that they are simply referred to as *noise*. **Thermal noise** is noise generated due to thermal effects resulting from the interaction between free electrons and the vibrating ions of a material in conduction. The result is an uneven flow of electrons through the medium, which will result in a varying potential across the medium. In most cases, these randomly generated signals are in the microvolt range, but with sufficient amplification they can wreak havoc on a system's response. This thermal noise is also called **Johnson noise** (named after the original researcher in the area) or **white noise** (because in optics, white light contains all frequencies). This type of noise has a fairly flat frequency response such as shown in Fig. 5.134a, that is, a plot of its power versus frequency from the very low to the very high end is fairly uniform. A second type of noise is called **shot noise**, a name derived from the fact that its noise sounds like a shower of lead shot hitting a solid surface or like heavy rain on a window. Its source is pockets of carriers passing through a medium at uneven rates. A third is **pink**, **flicker**, or **1/*f* noise**, which is due to the variation in transit times for carriers crossing various junctions of semiconductor devices. It is called 1/*f* noise because its magnitude drops off with increase in frequency. **Its effect is usually the most dramatic for frequencies below 1 kHz**, as shown in Fig. 5.134b.

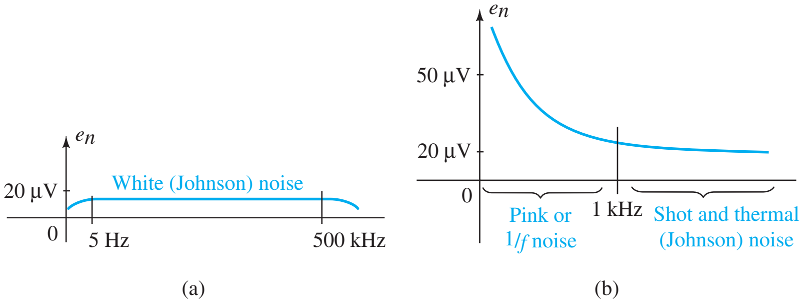


FIG. 5.134

Typical noise frequency spectra: (a) white or Johnson; (b) pink, thermal, and shot.

The network of Fig. 5.135 is designed to generate both a white noise and a pink noise. Rather than a separate source for each, first white noise is developed (level across the entire frequency spectrum), and then a filter is applied to remove the mid- and high-frequency components, leaving only the low-frequency noise response. The filter is further designed to modify the flat response of the white noise in the low-frequency region (to create a 1/*f* drop-off) by having sections of the filter "drop in" as the frequency increases. The white noise is created by leaving the collector terminal of transistor Q_1 open and reverse-biasing the base-to-emitter junction. In essence, the transistor is being used as a diode biased in the Zener avalanche region. Biasing a transistor in this region creates a very unstable situation that is conducive to the generation of random white noise. The combination of the avalanche region with its rapidly changing charge levels, sensitivity of the current level to

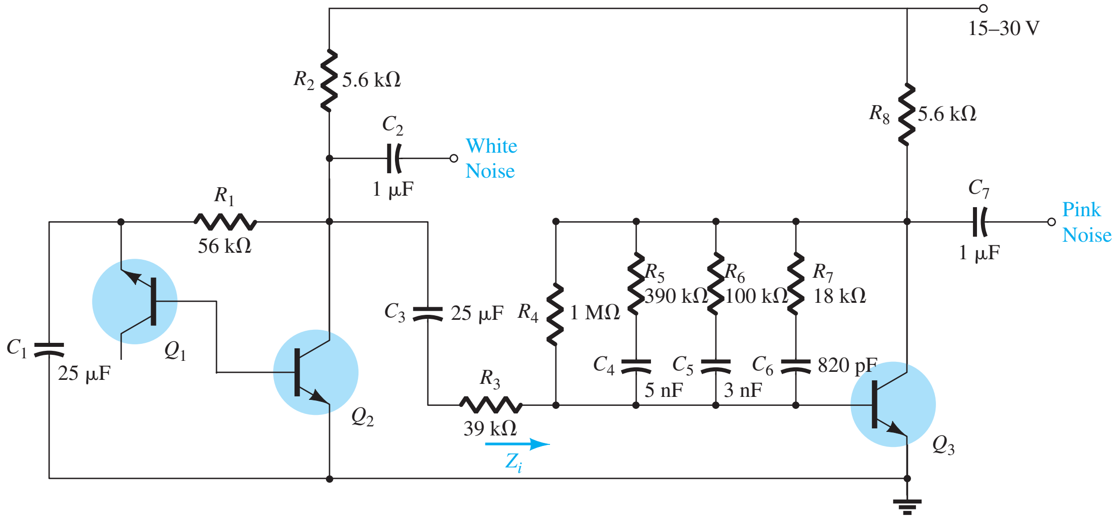


FIG. 5.135

White- and pink-noise generator.

temperature, and quickly changing impedance levels contributes to the level of noise voltage and current generated by the transistor. Germanium transistors are often used because the avalanche region is less defined and less stable than in silicon transistors. In addition, there are diodes and transistors designed specifically for random-noise generation.

The source of the noise is not some specially designed generator. It is simply due to the fact that current flow is not an ideal phenomenon but actually varies with time at a level that generates unwanted variations in the terminal voltage across elements. In fact, that variation in flow is so broad that it can generate frequencies that extend across a wide spectrum—a very interesting phenomenon.

The generated noise current of Q_1 will then be the base current for Q_2, which will be amplified to generate a white noise of perhaps 100 mV, which for this design would suggest an input noise voltage of about 170 μV. Capacitor C_1 will have a low impedance throughout the frequency range of interest to provide a "shorting effect" on any spurious signals in the air from contributing to the signal at the base of Q_1. The capacitor C_2 is there to isolate the dc biasing of the white-noise generator from the dc levels of the filter network to follow. The 39 kΩ and the input impedance of the next stage create the simple voltage-divider network of Fig. 5.136. If the 39 kΩ were not present, the parallel combination of R_2 and Z_i would load down the first stage and reduce the gain of Q_1 considerably. In the gain equation, R_2 and Z_i would appear in parallel (discussed in Chapter 9).

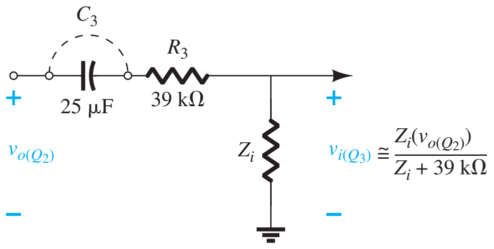

C_3
R_3
25 µF
39 kΩ
+
$v_{o(Q_2)}$
−
Z_i
+
$v_{i(Q_3)} \cong \dfrac{Z_i(v_{o(Q_2)})}{Z_i + 39\text{ k}\Omega}$
−

FIG. 5.136

Input circuit for the second stage.

The filter network is actually part of the feedback loop from collector to base appearing in the collector feedback network of Section 5.10. To describe its behavior, let us first consider the extremes of the frequency spectrum. For very low frequencies all the capacitors can be approximated by an open circuit, and the only resistance from collector to base is the 1-MΩ resistor. Using a beta of 100, we find that the gain of the section is about 280 and the input impedance about 1.28 kΩ. At a sufficiently high frequency all the capacitors could be replaced by short circuits, and the total resistance combination between collector and base would be reduced to about 14.5 kΩ, which would result in a very high unloaded gain of about 731, more than twice that just obtained with $R_F = 1\ \text{M}\Omega$. Because the $1/f$ filter is supposed to reduce the gain at high frequencies, it initially appears as though there is an error in design. However, the input impedance has dropped to about 19.33 Ω, which is a 66-fold drop from the level obtained with $R_F = 1\ \text{M}\Omega$. This would have a significant impact on the input voltage appearing at the second stage when we consider the voltage-divider action of Fig. 5.136. In fact, when compared to the series 39-kΩ resistor, the signal at the second stage can be assumed to be negligible or at a level where even a gain in excess of 700 cannot raise it to a level of any consequence. In total, therefore, the effect of doubling the gain is totally lost due to the tremendous drop in Z_i, and the output at very high frequencies can be ignored entirely.

For the range of frequencies between the very low and the very high, the three capacitors of the filter will cause the gain to drop off with increase in frequency. First, capacitor C_4 will be dropped in and cause a reduction in gain (around 100 Hz). Then capacitor C_5 will be included and will place the three branches in parallel (around 500 Hz). Finally, capacitor C_6 will result in four parallel branches and the minimum feedback resistance (around 6 kHz).

The result is a network with an excellent random-noise signal for the full frequency spectrum (white) and the low-frequency spectrum (pink).

Sound-Modulated Light Source

The light from the 12-V bulb of Fig. 5.137 will vary at a frequency and an intensity that are sensitive to the applied signal. The applied signal may be the output of an acoustical amplifier, a musical instrument, or even a microphone. Of particular interest is the fact that the applied voltage is 12 V ac rather than the typical dc biasing supply. The immediate question, in the absence of a dc supply, is how the dc biasing levels for the transistor will be established. In actuality, the dc level is obtained through the use of diode D_1, which rectifies the ac signal, and capacitor C_2, which acts as a power supply filter to generate a dc level across the output branch of the transistor. The peak value of a 12-V rms supply is about 17 V, resulting in a dc level after the capacitive filtering in the neighborhood of 16 V. If the potentiometer is set so that R_1 is about 320 Ω, the voltage from base to emitter of the transistor will be about 0.5 V, and the transistor will be in the "off" state. In this state the collector and emitter currents are essentially 0 mA, and the voltage across resistor R_3 is approximately 0 V. The voltage at the junction of the collector terminal and the diode is therefore 0 V, resulting in D_2 being in the "off" state and 0 V at the gate terminal of the silicon-controlled rectifier (SCR). The SCR (see Section 17.3) is fundamentally a diode whose state is controlled by an applied voltage at the gate terminal. The absence of a voltage at the gate means that the SCR and bulb are off.

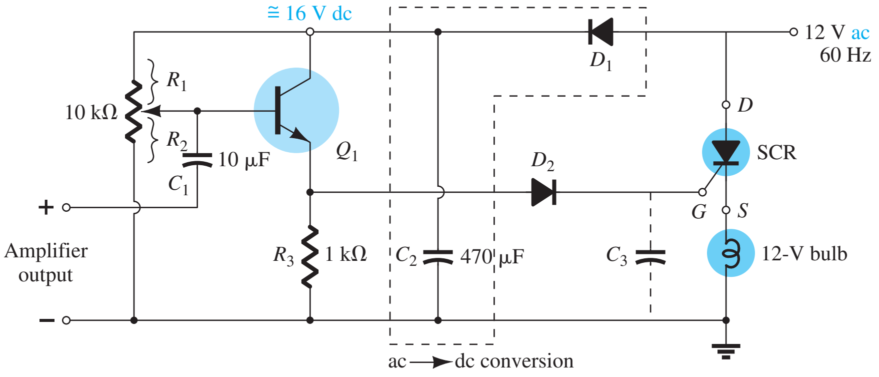


FIG. 5.137

Sound-modulated light source. SCR, Silicon-controlled rectifier.

If a signal is now applied to the gate terminal, the combination of the established biasing level and the applied signal can establish the required 0.7-V turn-on voltage, and the transistor will be turned on for periods of time dependent on the applied signal. When the transistor turns on, it will establish a collector current through resistor R_3 that will establish a voltage from collector to ground. If the voltage is more than the required 0.7 V for diode D_2, a voltage will appear at the gate of the SCR that may be sufficient to turn it on and establish conduction from the drain to the source of the SCR. However, we must now examine one of the most interesting aspects of this design. Because the applied voltage across the SCR is ac, which will vary in magnitude with time as shown in Fig. 5.138, the conduction strength of the SCR will vary with time also. As shown in the figure, if the SCR is turned on when the sinusoidal voltage is a maximum, the resulting current through the SCR will be a maximum also, and the bulb will be its brightest. If the SCR should turn on when the sinusoidal voltage is near its minimum, the bulb may turn on, but the lower current will result in considerably less illumination. The result is that the lightbulb turns on in sync with when the input signal is peaking, but the strength of turn-on will be determined by where one is on the applied 12-V signal. One can imagine the interesting and varied responses of such a system. Each time one applies the same audio signal, the response will have a different character.

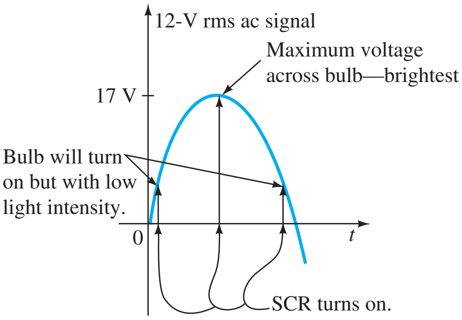


FIG. 5.138
Demonstrating the effect of an ac voltage on the operation of the SCR of Fig. 5.137.

In the above action, the potentiometer was set below the turn-on voltage of the transistor. The potentiometer can also be adjusted so that the transistor is "just on," resulting in a low-level base current. The result is a low-level collector current and insufficient voltage to forward-bias diode D_2 and turn on the SCR at the gate. However, when the system is set up in this manner, the resultant light output will be more sensitive to lower amplitude components of the applied signal. In the first case, the system acts more like a peak detector, whereas in the latter case it is sensitive to more components of the signal.

Diode D_2 was included to be sure that there is sufficient voltage to turn on both the diode and the SCR, in other words, to eliminate the possibility of noise or some other low-level unexpected voltage on the line turning the SCR on. Capacitor C_3 can be inserted to slow down the response by ensuring the voltage charge across the capacitor before the gate will reach sufficient voltage to turn on the SCR.

5.26 SUMMARY

Important Conclusions and Concepts

1. Amplification in the ac domain cannot be obtained **without the application of dc biasing level**.
2. For most applications the BJT amplifier can be considered linear, permitting the use of the **superposition theorem** to separate the dc and ac analyses and designs.
3. When introducing the **ac model** for a BJT:
   a. All **dc sources are set to zero** and replaced by a short-circuit connection to ground.
   b. All **capacitors** are replaced by a **short-circuit equivalent**.
   c. All elements **in parallel with** an introduced short-circuit equivalent should be removed from the network.
   d. The network should be **redrawn** as often as possible.
4. The **input impedance** of an ac network **cannot be measured** with an ohmmeter.

5. The **output impedance** of an amplifier is measured with the **applied signal set to zero**. It cannot be measured with an ohmmeter.
6. The **output impedance** for the r_e model **can be included** only if obtained from a data sheet or from a graphical measurement from the characteristic curves.
7. Elements that were isolated by capacitors for the dc analysis **will appear in the ac analysis** due to the short-circuit equivalent for the capacitive elements.
8. The **amplification factor** (beta, β, or h_{fe}) is the least sensitive to changes **in collector current**, whereas the **output impedance** parameter is the most sensitive. The output impedance is also quite sensitive to changes in $\boldsymbol{V_{CE}}$, whereas the **amplification** factor is the **least sensitive**. However, the **output impedance** is the **least sensitive** to changes in **temperature**, whereas the amplification factor is somewhat sensitive.
9. The r_e **model** for a BJT in the ac domain is sensitive to the **actual dc operating conditions of the network**. This parameter is normally not provided on a specification sheet, although h_{ie} of the normally provided hybrid parameters is equal to βr_e, but only under specific operating conditions.
10. Most **specification sheets** for BJTs include a **list of hybrid parameters** to establish an ac model for the transistor. One must be aware, however, that they are provided for a particular set of dc operating conditions.
11. The **CE fixed-bias configuration** can have a **significant voltage gain** characteristic, although its **input impedance can be relatively low**. The approximate **current gain** is given by simply **beta**, and the **output impedance** is normally assumed to be $\boldsymbol{R_C}$.
12. The **voltage-divider bias configuration** has a **higher stability** than the fixed-bias configuration, but it has about the **same voltage gain, current gain, and output impedance**. Due to the biasing resistors, its input impedance may be lower than that of the fixed-bias configuration.
13. The **CE emitter-bias configuration** with an unbypassed emitter resistor has a **larger input resistance** than the bypassed configuration, but it will have a **much smaller voltage gain** than the bypassed configuration. For the unbypassed or bypassed situation, the **output impedance** is normally assumed to be simply $\boldsymbol{R_C}$.
14. The **emitter-follower configuration** will always have an **output voltage slightly less than the input signal**. However, the **input impedance** can be **very large**, making it very useful for situations where a high-input first stage is needed to "pick up" as much of the applied signal as possible. Its **output impedance** is **extremely low**, making it an excellent signal source for the second stage of a multistage amplifier.
15. The **common-base configuration** has a **very low input impedance**, but it can have a **significant voltage gain**. The **current gain** is just **less than 1**, and the **output impedance** is simply $\boldsymbol{R_C}$.
16. The **collector feedback configuration** has an **input impedance** that is **sensitive to beta** and that can be quite low depending on the parameters of the configuration. However, the **voltage gain** can be **significant** and the **current gain** of **some magnitude** if the parameters are chosen properly. The **output impedance** is most often simply the collector resistance $\boldsymbol{R_C}$.
17. The **collector dc feedback configuration** uses the dc feedback to **increase its stability** and the changing state of a capacitor from dc to ac to establish a **higher voltage gain** than obtained with a straight feedback connection. The **output impedance** is usually close to $\boldsymbol{R_C}$ and the **input impedance** relatively close to that obtained with the **basic common-emitter configuration**.
18. The **approximate hybrid equivalent network** is very **similar** in composition to that used with the $\boldsymbol{r_e}$ **model**. In fact, the **same methods** of analysis can be applied to both models. For the hybrid model the results will be in terms of the network parameters and the hybrid parameters, whereas for the r_e model they will be in terms of the network parameters and β, r_e, and r_o.
19. The **hybrid model** for common-emitter, common-base, and common-collector configurations **is the same**. The only difference will be the magnitude of the parameters of the equivalent network.
20. The total gain of a cascaded system is determined by the **product of the gains of each stage**. The gain of each stage, however, must be determined **under loaded conditions**.
21. Because the total gain is the product of the individual gains of a cascaded system, the **weakest link** can have a major effect on the total gain.

Equations

$$r_e = \frac{26\text{ mV}}{I_E}$$

Hybrid parameters:

$$h_{ie} = \beta r_e, \qquad h_{fe} = \beta_{\text{ac}}, \qquad h_{ib} = r_e, \qquad h_{fb} = -\alpha \cong -1$$

CE fixed bias:

$$Z_i \cong \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2 \| \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

CE emitter-bias:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong R_C$$

$$A_v \cong -\frac{R_C}{R_E}, \qquad A_i \cong \frac{\beta R_B}{R_B + \beta R_E}$$

Emitter-follower:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong r_e$$

$$A_v \cong 1, \qquad A_i = -A_v\frac{Z_i}{R_E}$$

Common-base:

$$Z_i \cong R_E \| r_e, \qquad Z_o \cong R_C$$

$$A_v \cong \frac{R_C}{r_e}, \qquad A_i \cong -1$$

Collector feedback:

$$Z_i \cong \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}}, \qquad Z_o \cong R_C \| R_F$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i \cong \frac{R_F}{R_C}$$

Collector dc feedback:

$$Z_i \cong R_{F_1} \| \beta r_e, \qquad Z_o \cong R_C \| R_{F_2}$$

$$A_v = -\frac{R_{F_2} \| R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C}$$

Effect of load impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{\text{NL}}}, \qquad A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}A_{v_{\text{NL}}}$$

$$I_s = \frac{V_s}{R_s + R_i}$$

Combined effect of load and source impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{\text{NL}}}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}\cdot\frac{R_L}{R_L + R_o}A_{v_{\text{NL}}}$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{R_i}{R_L}, \qquad A_{i_s} = \frac{I_o}{I_s} = -A_{v_s}\frac{R_s + R_i}{R_L}$$

Cascode connection:

$$A_v = A_{v_1}A_{v_2}$$

Darlington connection (with R_E):

$$\beta_D = \beta_1\beta_2,$$

$$Z_i = R_B \| (\beta_1\beta_2 R_E), \qquad A_i = \frac{\beta_1\beta_2 R_B}{(R_B + \beta_1\beta_2 R_E)}$$

$$Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2} \qquad A_v = \frac{V_o}{V_i} \approx 1$$

Darlington connection (without R_E):

$$Z_i = R_1 \| R_2 \| \beta_1(r_{e_1} + \beta_1\beta_2 r_{e_2}) \qquad A_i = \frac{\beta_1\beta_2(R_1 \| R_2)}{R_1 \| R_2 + Z_i'}$$

where $Z_i' = \beta_1(r_{e_1} + \beta_2 r_{e_2})$

$$Z_o \cong R_C \| r_{o_2} \qquad A_v = \frac{V_o}{V_i} = \frac{\beta_1\beta_2 R_C}{Z_i'}$$

Feedback pair:

$$Z_i = R_B \| \beta_1\beta_2 R_C \qquad A_i = \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_C}$$

$$Z_o \approx \frac{r_{e_1}}{\beta_2} \qquad A_v \cong 1$$

5.27 COMPUTER ANALYSIS

PSpice Windows

BJT Voltage-Divider Configuration The last few chapters have been limited to the dc analysis of electronic networks using PSpice and Multisim. This section will consider the application of an ac source to a BJT network and describe how the results are obtained and interpreted.

Most of the construction of the network of Fig. 5.139 can be accomplished using the procedures introduced in earlier chapters. The ac source can be found in the **SOURCE** library as **VSIN**. You can scroll down the list of options or simply type in **VSIN** at the head of the listing. Once this is selected and placed, a number of labels will appear that define

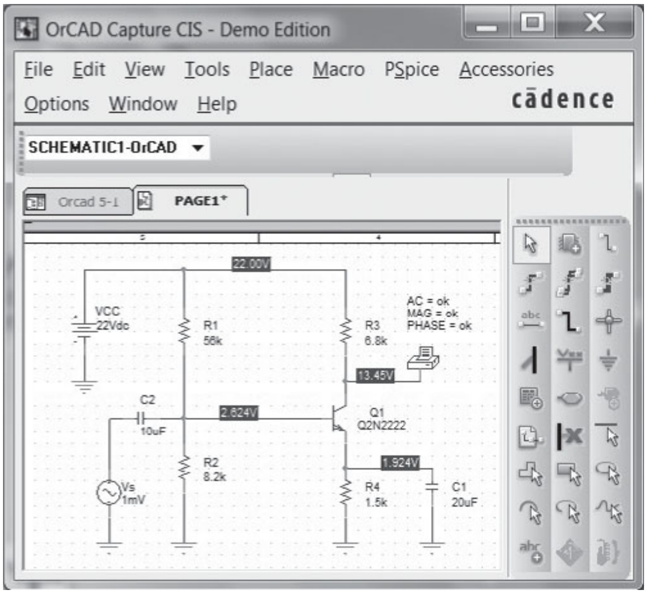

OrCAD Capture CIS - Demo Edition
File
Edit
View
Tools
Place
Macro
PSpice
Accessories
Options
Window
Help
cādence
SCHEMATIC1-OrCAD
Orcad 5-1
PAGE1*
22.00V
VCC
22Vdc
R1
56k
R3
6.8k
AC = ok
MAG = ok
PHASE = ok
13.45V
C2
10uF
2.624V
Q1
Q2N2222
1.924V
R2
8.2k
R4
1.5k
C1
20uF
Vs
1mV

FIG. 5.139

Using PSpice Windows to analyze the network of Fig. 5.28 (Example 5.2).

the parameters of the source. Double-clicking the source symbol or using the sequence **Edit-Properties** will result in the **Property Editor** dialog box, which lists all the parameters appearing on the screen and more. By scrolling all the way to the left, you will find a listing for **AC**. Select the blank rectangle under the heading and enter the **1 mV** value. Be aware that the entries can use prefixes such as m (milli) and k (kilo). Moving to the right, the heading **FREQ** will appear, in which you can enter **10 kHz**. Moving again to **PHASE**, you will find the default value is **0**, so it can be left alone. It represents the initial phase angle for the sinusoidal signal. Next you will find **VAMPL**, which is set at 1 mV, also followed by **VOFF** at **0** V. Now that each of the properties has been set, we have to decide what to display on the screen to define the source. In Fig. 5.139 the only labels are Vs and 1 mV, so a number of items have to be deleted and the name of the source has to be modified. For each quantity simply return to the heading and select it for modification. If you choose **AC**, select **Display** to obtain the **Display Properties** dialog box. Select **Value Only** because we prefer not to have the label **AC** appear. Leave all the other choices blank. An **OK**, and you can move to the other parameters within the **Property Editor** dialog box. We do not want the **FREQ**, **PHASE**, **VAMPL** and **VOFF** labels to appear with their values, so in each case select **Do Not Display**. To change **V1** to **Vs**, simply go to the **Part Reference**, and after selecting it, type in **Vs**. Then go to **Display** and select **Value Only**. Finally, to apply all the changes, select **Apply** and exit the dialog box; the source will appear as shown in Fig. 5.139.

The ac response for the voltage at a point in the network is obtained using the **VPRINT1** option found in the **SPECIAL** library. If the library does not appear, simply select **Add Library** followed by **special.olb**. When **VPRINT1** is chosen, it will appear on the screen as a printer with three labels: **AC**, **MAG**, and **PHASE**. Each has to be set to an OK status to reflect the fact that you desire this type of information about the voltage level. This is accomplished by simply clicking on the printer symbol to obtain the dialog box and setting each to **OK**. For each entry select **Display** and choose **Name and Label**. Finally, select **Apply** and exit the dialog box. The result appears in Fig. 5.139.

The transistor **Q2N2222** can be found under the **EVAL** library by typing it under the **Part** heading or simply scrolling through the possibilities. The levels of I_s and β can be set by first selecting the Q2N2222 transistor to make it red and then applying the sequence **Edit-PSpice Model** to obtain the **PSpice Model Editor Lite** dialog box and changing **Is** to **2E-15A** and **Bf** to 90. The level of **Is** is the result of numerous runs of the network to find the value that would result in V_{BE} being closest to 0.7 V.

Now that all the components of the network have been set, it is time to ask the computer to analyze the network and provide some results. If improper entries were made, the computer will quickly respond with an error listing. First select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. Then, after entering **Name** as **OrCAD 5-1**, select **Create** and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC Sweep/Noise** and then under **AC Sweep Type** choose **Linear**. The **Start Frequency** is **10 kHz**, the **End Frequency** is **10 kHz**, and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key (white arrow). A schematic will result with a graph that extends from 5 kHz to 15 kHz with no vertical scale. Through the sequence **View-Output File** the listing of Fig. 5.140 can be obtained. It starts with a list of all the elements of the network and their settings followed by all the parameters of the transistor. In particular, note the level of **IS** and **BF**. Next the dc levels are provided under the **SMALL SIGNAL BIAS SOLUTION**, which match those appearing on the schematic of Fig. 5.139. The dc levels appear on Fig. 5.139 due to the selection of the **V** option. Also note that $V_{BE} = 2.624\text{ V} - 1.924\text{ V} = 0.7\text{ V}$, as stated above, due to the choice of **Is**.

The next listing, **OPERATING POINT INFORMATION**, reveals that even though beta of the **BJT MODEL PARAMETERS** listing was set at 90, the operating conditions of the network resulted in a dc beta of 48.3 and an ac beta of 55. Fortunately, however, the voltage-divider configuration is less sensitive to changes in beta in the dc mode, and the dc results are excellent. However, the drop in ac beta had an effect on the resulting level of V_o: 296.1 mV versus the handwritten solution (with $r_o = 50\text{ k}\Omega$) of 324.3 mV—a 9% difference. The results are certainly close, but probably not as close as one would like. A closer result (within 7%) could be obtained by setting all the parameters of the device except I_s and beta to zero. However, for the moment, the impact of the remaining parameters has been demonstrated, and the results will be accepted as sufficiently close to the handwritten levels. Later in this chapter, an ac model for the transistor will be introduced with results

```
****          CIRCUIT DESCRIPTION

****************************************************************************************************

*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"
* source ORCAD 5-1
Q_Q1        N00286 N00282 N00319 Q2N2222
R_R1        N00282 N00254  56k TC=0,0
R_R2        0 N00282  8.2k TC=0,0
R_R3        N00286 N00254  6.8k TC=0,0
R_R4        0 N00319  1.5k TC=0,0
V_VCC         N00254 0 22Vdc
C_C1        0 N00319  20uF  TC=0,0
V_Vs        N00342 0  AC 1mV
+SIN 0V 1mV 10kHz 0 0 0
. PRINT        AC
+  VM ([N00286])
+  VP ([N00286])
C_C2        N00342 N00282  10uF  TC=0,0
.END

****     BJT MODEL PARAMETERS

****************************************************************************************************

                    Q2N2222
                    NPN
          LEVEL    1
               IS    2.000000E-15
              BF   90
              NF     1
             VAF   74.03
             IKF       .2847
             ISE   14.340000E-15
              NE     1.307
              BR     6.092
              NR     1
             ISS     0
              RB    10
              RE     0
              RC     1
             CJE   22.010000E-12
             VJE       .75
             MJE       .377
             CJC     7.306000E-12
             VJC       .75
             MJC       .3416

           XCJC     1

             CJS    0
             VJS       .75
               TF 411.100000E-12
             XTF     3
             VTF     1.7
             ITF       .6
              TR   46.910000E-09
             XTB     1.5
              KF     0
              AF     1
              CN     2.42
               D       .87

****     SMALL SIGNAL BIAS SOLUTION                              TEMPERATURE  =  27.000  DEG  C

****************************************************************************************************

NODE          VOLTAGE       NODE          VOLTAGE       NODE          VOLTAGE        NODE          VOLTAGE
(N00254)      22.0000        (N00282)      2.6239         (N00286)      13.4530        (N00319)      1.9244
(N00342)        0.0000

   VOLTAGE SOURCE CURRENTS
   NAME        CURRENT
   V_VCC       -1.603E-03
   V_Vs        0.000E+00

   TOTAL POWER DISSIPATION   3.53E-02  WATTS

****     OPERATING POINT INFORMATION                             TEMPERATURE  =  27.000  DEG  C

****************************************************************************************************

**** BIPOLAR JUNCTION TRANSISTORS

NAME              Q_Q1
MODEL             Q2N2222
IB                2.60E-05
IC                 1.26E-03
VBE                6.99E-01
VBC              -1.08E+01
VCE                1.15E+01
BETADC             4.83E+01
GM                 4.84E-02
RPI                1.14E+03
RX                 1.00E+01
RO                 6.75E+04
CBE               5.78E-11
CBC               2.87E-12
CJS                0.00E+00
BETAAC            5.50E+01
CBX/CBX2          0.00E+00
FT/FT2            1.27E+08

****     AC ANALYSIS                                             TEMPERATURE  =  27.000  DEG  C

****************************************************************************************************

  FREQ       VM(N00286)    VP(N00286)
1.000E+04     2.961E-01     -1.780E+02
```

FIG. 5.140

Output file for the network of Fig. 5.139.

that will be an exact match with the handwritten solution. The phase angle is −178° versus the ideal of −180°, a very close match.

A plot of the voltage at the collector of the transistor can be obtained by setting up a new simulation process to calculate the value of the desired voltage at a number of data points. The more points, the more accurate is the plot. The process is initiated by returning to the

Simulation Settings dialog box and under **Analysis type** selecting **Time Domain(Transient)**. Time domain is chosen because the horizontal axis will be a time axis, requiring that the collector voltage be determined at a specified time interval to permit the plot. Because the period of the waveform is $1/10\text{ kHz} = 0.1\text{ ms} = 100\ \mu\text{s}$, and it would be convenient to display five cycles of the waveform, the **Run to time(TSTOP)** is set at 500 μs. The **Start saving data after** point is left at 0 s and under **Transient option**, the **Maximum step size** is set at 1 μs to ensure 100 data points for each cycle of the waveform. An **OK**, and a **SCHEMATIC** window will appear with a horizontal axis broken down in units of time but with no vertical axis defined. The desired waveform can then be added by first selecting **Trace** followed by **Add Trace** to obtain the **Add Trace** dialog box. In the provided listing **V(Q1:c)** is selected as the voltage at the collector of the transistor. The instant it is selected it will appear as the **Trace Expression** at the bottom of the dialog box. Referring to Fig. 5.139, we find that because the capacitor C_E will essentially be in the short-circuit state at 10 kHz, the voltage from collector to ground is the same as that across the output terminals of the transistor. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key.

The result will be the waveform of Fig. 5.141 having an average value of about 13.45 V, which corresponds exactly with the bias level of the collector voltage in Fig. 5.139. The range of the vertical axis was chosen automatically by the computer. Five full cycles of the output voltage are displayed with 100 data points for each cycle. The data points appear in Fig. 5.139 because the sequence **Tools-Options-Mark Data Points** was applied. The data points appear as small dark circles on the plot curve. Using the scale of the graph, we see that the peak-to-peak value of the curve is approximately $13.76\text{ V} - 13.16\text{ V} = 0.6\text{ V} = 600\text{ mV}$, resulting in a peak value of 300 mV. Because a 1-mV signal was applied, the gain is 300, or very close to the calculator solution of 296.1.

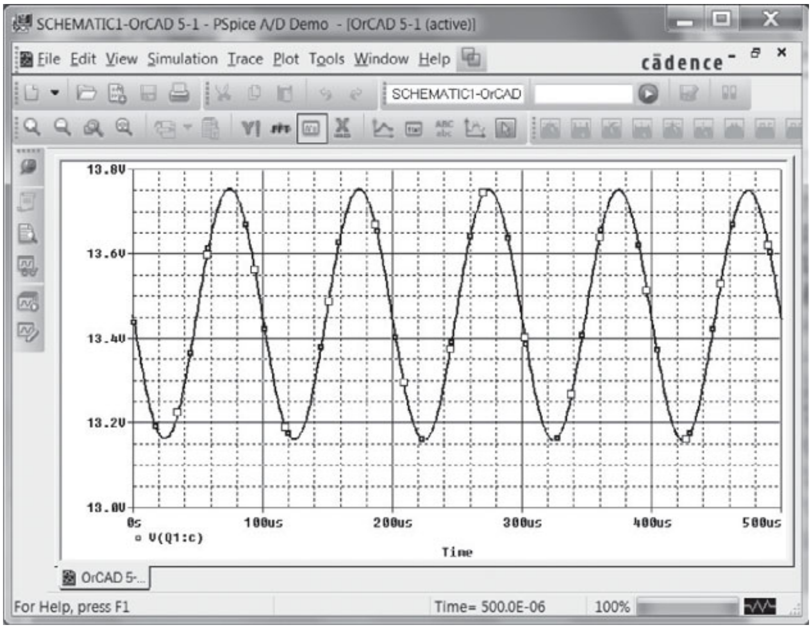


FIG. 5.141
Voltage v_C for the network Fig. 5.139.

If a comparison is to be made between the input and output voltages on the same screen, the **Add Y-Axis** option under **Plot** can be used. After you select it, choose the **Add Trace** icon and select **V(Vs:+)** from the provided list. The result is that both waveforms will appear on the same screen as shown in Fig. 5.142, each with its own vertical scale.

If two separate graphs are preferred, we can start by selecting **Plot** followed by **Add Plot to Window** after the graph of Fig. 5.141 is in place. The result will be a second set of axes waiting for a decision about which curve to plot. Using **Trace-Add Trace-V(Vs:+)** will result in the graphs of Fig. 5.143. The **SEL ≫** (from **SELECT**) appearing next to one of the plots defines the "active" plot.

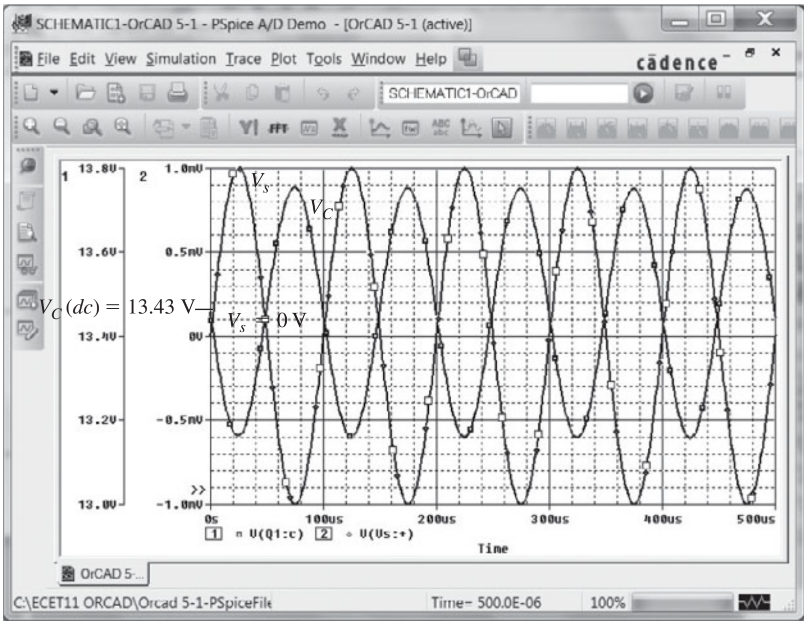

SCHEMATIC1-OrCAD 5-1 - PSpice A/D Demo - [OrCAD 5-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
1
13.8V
13.6V
13.4V
13.2V
13.0V
2
1.0mV
0.5mV
0V
-0.5mV
-1.0mV
V_s
V_C
$V_C(dc) = 13.43$ V
$V_s = 0$ V
0s
100us
200us
300us
400us
500us
1 ▫ V(Q1:c) 2 ◇ V(Us:+)
Time
OrCAD 5-...
C:\ECET11 ORCAD\Orcad 5-1-PSpiceFile
Time= 500.0E-06
100%

FIG. 5.142
The voltages v_C and v_s for the network of Fig. 5.139.

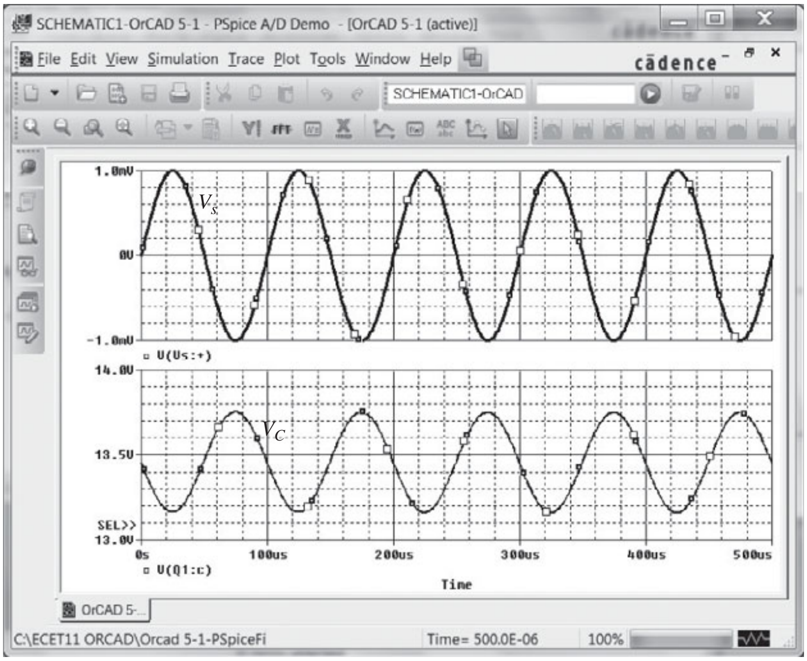
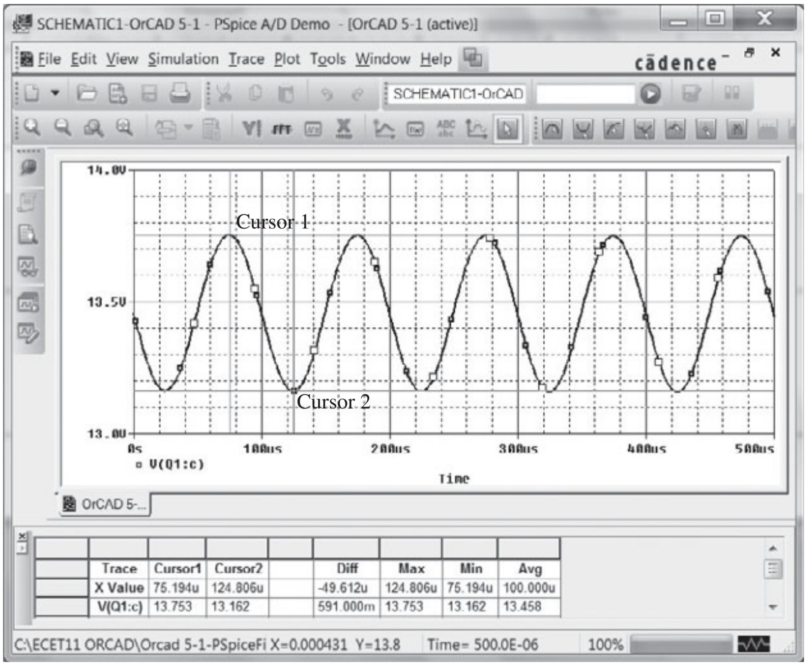

SCHEMATIC1-OrCAD 5-1 - PSpice A/D Demo - [OrCAD 5-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
1.0mV
0V
-1.0mV
V_s
▫ V(Us:+)
14.0V
13.5V
SEL>>
13.0V
V_C
0s
100us
200us
300us
400us
500us
▫ V(Q1:c)
Time
OrCAD 5-...
C:\ECET11 ORCAD\Orcad 5-1-PSpiceFi
Time= 500.0E-06
100%

FIG. 5.143
Two separate plots of v_C and v_s in Fig. 5.139.

The last operation to be introduced in this coverage of graph displays is the use of the cursor option. The result of the sequence **Trace-Cursor-Display** is a line at the dc level of the graph of Fig. 5.144 intersecting with a vertical line. The level and time both appear in the small dialog box in the bottom right corner of the screen. The first number for **Cursor 1** is the time intersection and the second is the voltage level at that instant. A left-click of the mouse will provide control of the intersecting vertical and horizontal lines at this level. Clicking on the vertical line and holding down on the clicker will allow you to move the intersection horizontally along the curve, simultaneously displaying the time and voltage level in the data box at the bottom right of the screen. If it is moved to the first peak of the waveform, the time appears as 75.194 μs with a voltage level of 13.753 V, as shown in Fig. 5.144. On right-clicking of the mouse, a second intersection, defined by **Cursor 2**, will appear, which can be moved in the same way with its time and voltage appearing in the same dialog box. Note that if **Cursor 2** is placed close to the negative peak, the difference in time is 49.61 μs (as displayed in the same box), which is very close to one-half the period of the waveform. The difference in magnitude is 591 mV, which is very close to the 600 mV obtained earlier.


SCHEMATIC1-OrCAD 5-1 - PSpice A/D Demo - [OrCAD 5-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
14.0V
13.5V
13.0V
Cursor 1
Cursor 2
0s
100us
200us
300us
400us
500us
V(Q1:c)
Time
OrCAD 5-...
C:\ECET11 ORCAD\Orcad 5-1-PSpiceFi X=0.000431 Y=13.8
Time= 500.0E-06
100%

	Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
	X Value	75.194u	124.806u		-49.612u	124.806u	75.194u	100.000u
	V(Q1:c)	13.753	13.162		591.000m	13.753	13.162	13.458

FIG. 5.144

Demonstrating the use of cursors to read specific points on a plot.

Voltage-Divider Configuration—Controlled Source Substitution The results obtained for any analysis using the transistors provided in the PSpice listing will always be somewhat different from those obtained with an equivalent model that only includes the effect of beta and r_e. This was clearly demonstrated for the network of Fig. 5.139. If a solution is desired that is limited to the approximate model used in the hand calculations, then the transistor must be represented by a model such as appearing in Fig. 5.145.

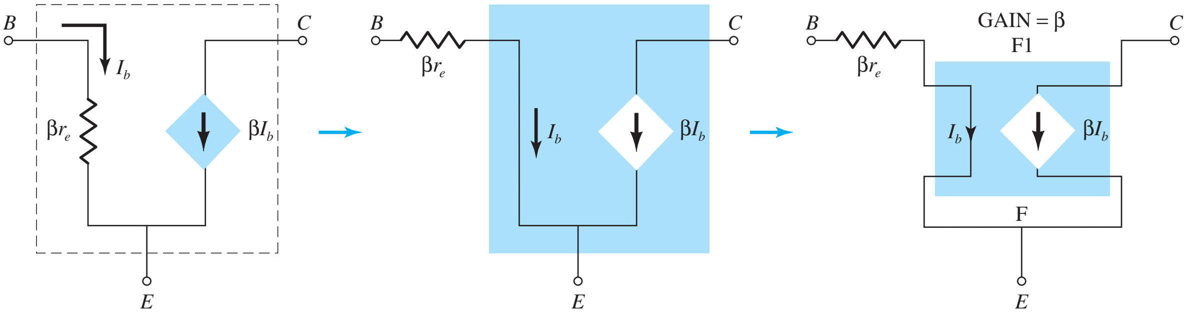

B
C
I_b
βr_e
βI_b
E
B
βr_e
C
I_b
βI_b
E
B
βr_e
GAIN = β
F1
C
I_b
βI_b
F
E

FIG. 5.145

Using a controlled source to represent the transistor of Fig. 5.139.

For Example 5.2, β is 90, with $\beta r_e = 1.66\text{ k}\Omega$. The current-controlled current source (CCCS) is found in the **ANALOG** library as part **F**. After selection, an **OK**, and the graphical symbol for the CCCS will appear on the screen as shown in Fig. 5.146. Because it does not appear within the basic structure of the CCCS, it must be added in series with the controlling current that appears as an arrow in the symbol. Note the added 1.66-kΩ resistor, labeled **beta-re** in Fig. 5.146. Double-clicking on the CCCS symbol will result in the **Property Editor** dialog box, in which the **GAIN** can be set to 90. It is the only change to be made in the listing. Then select **Display** followed by **Name and Value** and exit **(x)** the dialog box. The result is the **GAIN = 90** label appearing in Fig. 5.146.

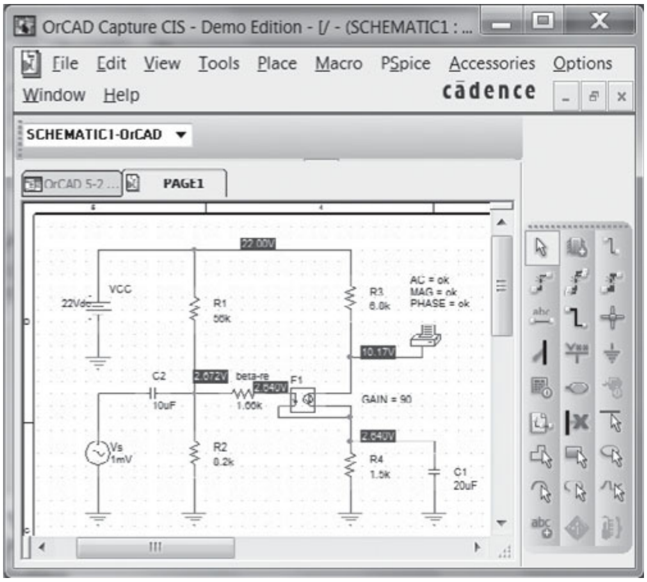
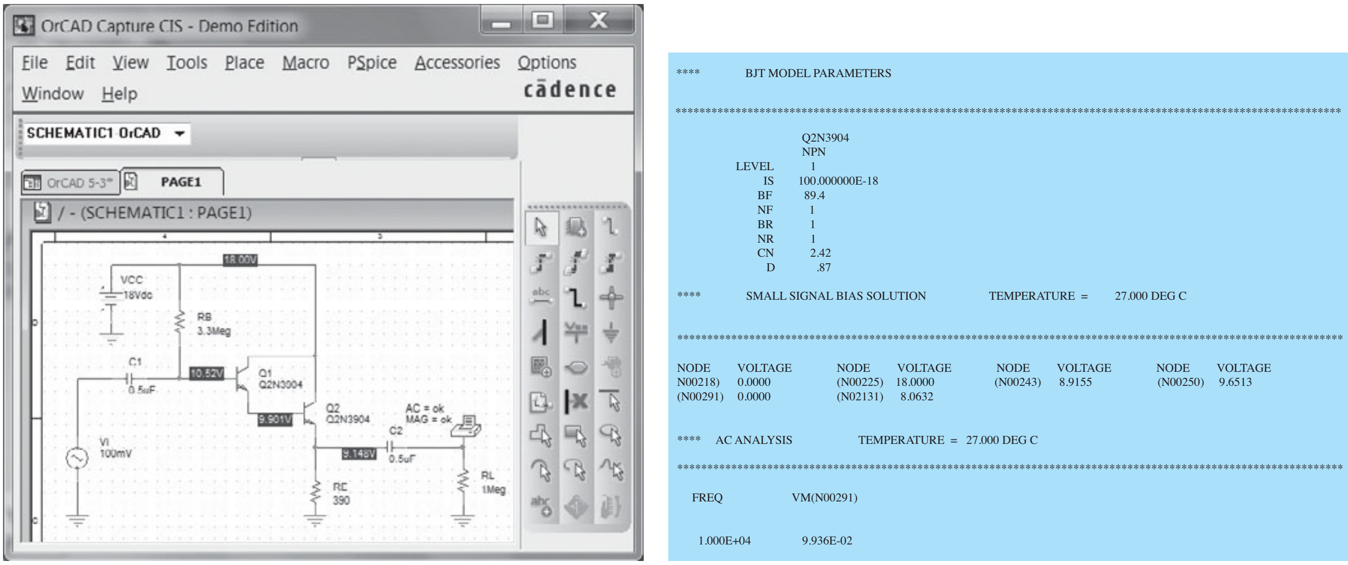

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : ...
File Edit View Tools Place Macro PSpice Accessories Options
Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 5-2 ...
PAGE1
22.00V
VCC
22Vdc
R1
56k
R3
6.8k
AC = ok
MAG = ok
PHASE = ok
10.17V
C2
10uF
2.672V
beta-re
1.66k
2.640V
F1
GAIN = 90
2.640V
Vs
1mV
R2
8.2k
R4
1.5k
C1
20uF

FIG. 5.146

Substituting the controlled source of Fig. 5.145 for the transistor of Fig. 5.139.

A simulation and the dc levels of Fig. 5.146 will appear. The dc levels do not match the earlier results because the network is a mix of dc and ac parameters. The equivalent model substituted in Fig. 5.146 is a representation of the transistor under ac conditions, not dc biasing conditions. When the software package analyzes the network from an ac viewpoint it will work with an ac equivalent of Fig. 5.146, which will not include the dc parameters. The **Output File** will reveal that the output collector voltage is 368.3 mV, or a gain of 368.3, essentially an exact match with the handwritten solution of 368.76. The effects of r_o could be included by simply placing a resistor in parallel with the controlled source.

Darlington Configuration Although PSpice does have two Darlington pairs in the library, individual transistors are employed in Fig. 5.147 to test the solution to Example 5.17. The details of setting up the network have been covered in the preceding sections and chapters. For each transistor I_s is set to 100E-18 and β to 89.4. The applied frequency is 10 kHz. A simulation of the network results in the dc levels appearing in Fig. 5.147a and the **Output File** in Fig. 5.147b. In particular, note that the voltage drop between base and emitter for both transistors is $10.52\text{ V} - 9.148\text{ V} = 1.37\text{ V}$ compared to the 1.6 V assumed in the example. Recall that the drop across Darlington pairs is typically about 1.6 V and not simply twice that of a single transistor, or $2(0.7\text{ V}) = 1.4\text{ V}$. The output voltage of 99.36 mV is very close to the 99.80 mV obtained in Section 5.17.


OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options
Window Help
cādence
SCHEMATIC1 OrCAD
OrCAD 5-3*
PAGE1
/ - (SCHEMATIC1 : PAGE1)
18.00V
VCC
18Vdc
RB
3.3Meg
C1
0.5uF
10.52V
Q1
Q2N3904
9.901V
Q2
Q2N3904
AC = ok
MAG = ok
C2
9.148V
0.5uF
VI
100mV
RE
390
RL
1Meg

```
****          BJT MODEL PARAMETERS

**********************************************************************************************

                      Q2N3904
                      NPN
          LEVEL         1
             IS       100.000000E-18
             BF         89.4
             NF         1
             BR         1
             NR         1
             CN         2.42
              D          .87

****          SMALL SIGNAL BIAS SOLUTION            TEMPERATURE  =     27.000 DEG C

**********************************************************************************************

NODE      VOLTAGE         NODE      VOLTAGE         NODE      VOLTAGE         NODE       VOLTAGE
N00218)   0.0000          (N00225)  18.0000         (N00243)   8.9155         (N00250)   9.6513
(N00291)  0.0000          (N02131)   8.0632

****    AC ANALYSIS              TEMPERATURE  =  27.000 DEG C

**********************************************************************************************

   FREQ              VM(N00291)


    1.000E+04          9.936E-02
```

(a)

(b)

FIG. 5.147

(a) Design Center schematic of Darlington network; (b) output listing for circuit of part (a) (edited).

Multisim

Collector Feedback Configuration Because the collector feedback configuration generated the most complex equations for the various parameters of a BJT network, it seems appropriate that Multisim be used to verify the conclusions of Example 5.9. The network appears as shown in Fig. 5.148 using the "virtual" transistor from the **Transistor family** toolbar. Recall from the previous chapter that transistors are obtained by first selecting the **Transistor** keypad appearing as the fourth option over on the **component**

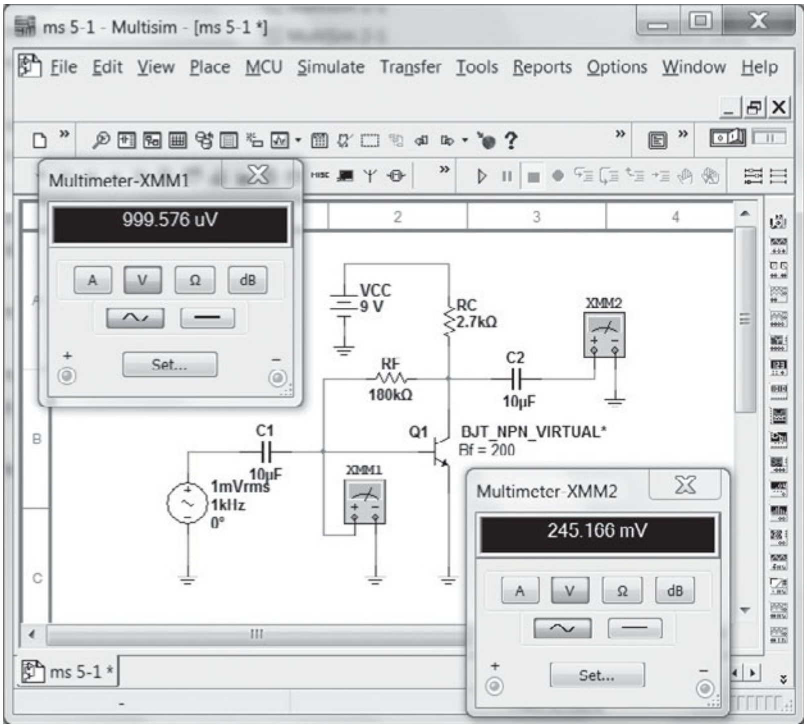

ms 5-1 - Multisim - [ms 5-1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Multimeter-XMM1
999.576 uV
A
V
Ω
dB
Set...
+
-
2
3
4
VCC
9 V
RC
2.7kΩ
XMM2
RF
180kΩ
C2
10µF
C1
Q1
BJT_NPN_VIRTUAL*
Bf = 200
10µF
XMM1
1mVrms
1kHz
0°
B
C
Multimeter-XMM2
245.166 mV
A
V
Ω
dB
Set...
+
-
ms 5-1 *

FIG. 5.148

Network of Example 5.9 redrawn using Multisim.

toolbar. Once chosen, the **Select a Component** dialog box will appear; under the **Family** heading, select **TRANSISTORS_VIRTUAL** followed by **BJT_NPN_VIRTUAL**. Following an **OK** the symbols and labels will appear as shown in Fig. 5.148. We must now check that the beta value is 200 to match the example under investigation. This can be accomplished using one of two paths. In Chapter 4 we used the **EDIT-PROPERTIES** sequence, but here we will simply double-click on the symbol to obtain the **TRANSISTORS_VIRTUAL** dialog box. Under **Value**, select **Edit Model** to obtain the **Edit Model** dialog box (the dialog box has a different appearance from that obtained with the other route and requires a different sequence to change its parameters). The value of **BF** appears as **100**, which must be changed to 200. First select the **BF** line to make it blue all the way across. Then place the cursor directly over the 100 value and select it to isolate it as the quantity to be changed. After deleting the 100, type in the desired 200 value. Then click the **BF** line directly under the **Name** heading and the entire line will be blue again, but now with the 200 value. Then choose **Change Part Model** at the bottom left of the dialog box and the **TRANSISTORS-VIRTUAL** dialog box will appear again. Select **OK** and $\beta = 200$ will be set for the virtual transistor. Note the asterisk next to the BJT label to indicate the parameters of the device have been changed from the default values. The label **Bf = 100** was set using **Place-Text** as described in the previous chapter.

This will be the first opportunity to set up an ac source. First, it is important to realize that there are two types of ac sources available, one whose value is in rms units, the other with its peak value displayed. The option under **Power Sources** uses **rms** values, whereas the ac source under **Signal Sources** uses **peak** values. Because meters display rms values, the **Power Sources** option will be used here. Once **Source** is selected, the **Select a Component** dialog box will appear. Under the **Family** listing select **POWER_SOURCES** and then select **AC_POWER** under the **Component** listing. An **OK**, and the source will appear on the screen with four pieces of information. The label **V1** can be deleted by first double-clicking on the source symbol to obtain the **AC_POWER** dialog box. Select **Display** and disengage **Use Schematic Global Settings**. To remove the label **V1**, disengage the **Show RefDes** option. An **OK**, and the **V1** will disappear from the screen. Next the value has to be set at 1 mV, a process initiated by selecting **Value** in the **AC_POWER** dialog box and then changing the **Voltage (RMS)** to 1 mV. The units of mV can be set using the scroll keys to the right of the magnitude of the source. After you change the **Voltage** to **1 mV**, an **OK** will place this new value on the screen. The frequency of **1000 Hz** can be set in the same way. The **0**-degree phase shift happens to be the default value.

The label **Bf = 200** is set in the same way as described in Chapter 4. The two multimeters are obtained using the first option at the top of the right vertical toolbar. The meter faces appearing in Fig. 5.148 were obtained by simply double-clicking on the multimeter symbols on the schematic. Both were set to read voltages, the magnitudes of which will be in rms units.

After simulation the results of Fig. 5.148 appear. Note that the meter **XMM1** is not reading the 1 mV expected. This is due to the small drop in voltage across the input capacitor at 1 kHz. Certainly, however, it is very close to 1 mV. The output of 245.166 mV quickly reveals that the gain of the transistor configuration is about 245.2, which is a very close match with the 240 obtained in Example 5.9.

Darlington Configuration Applying Multisim to the network of Fig. 5.147 with a packaged Darlington amplifier results in the printout of Fig. 5.149. For each transistor the parameters were changed to **Is = 100E-18 A** and **Bf = 89.4** using the technique described earlier. For practice purposes the ac signal source was employed rather than the power source. The peak value of the applied signal is set at 100 mV, but note that the multimeter reads the effective or rms value of 99.991 mV. The indicators reveal that the base voltage of Q_1 is 7.736 V, and the emitter voltage of Q_2 is 6.193 V. The rms value of the output voltage is 99.163 mV, resulting in a gain of 0.99 as expected for the emitter follower configuration. The collector current is 16 mA with a base current of 1.952 mA, resulting in a β_D of about 8200.

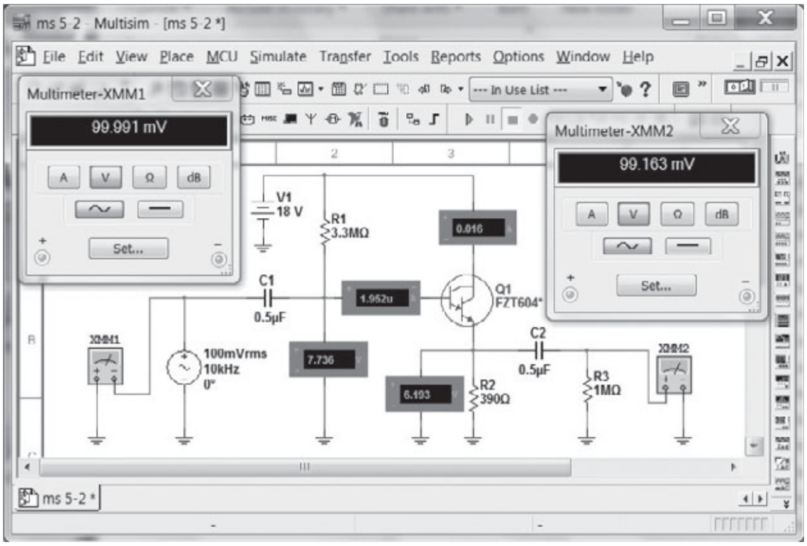

ms 5-2 - Multisim - [ms 5-2 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Multimeter-XMM1
99.991 mV
A V Ω dB
Set...
--- In Use List ---
Multimeter-XMM2
99.163 mV
A V Ω dB
Set...
V1
18 V
R1
3.3MΩ
0.016
C1
0.5µF
1.952u
Q1
FZT604*
C2
0.5µF
XMM1
100mVrms
10kHz
0°
7.736
6.193
R2
390Ω
R3
1MΩ
XMM2
ms 5-2 *

FIG. 5.149

Network of Example 5.9 redrawn using Multisim.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

5.2 Amplification in the AC Domain

1. **a.** What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
   b. What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
   c. What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?
2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?
3. If a transistor amplifier has more than one dc source, can the superposition theorem be applied to obtain the response of each dc source and algebraically add the results?

5.3 BJT Transistor Modeling

4. What is the reactance of a 10-μF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?
5. Given the common-base configuration of Fig. 5.150, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 5.7.

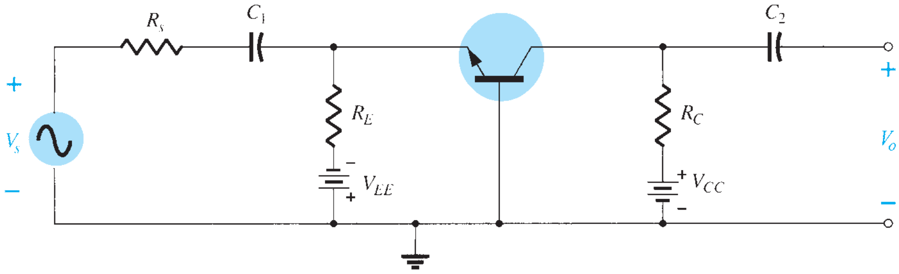

R_s
C_1
C_2
+
V_s
–
R_E
–
V_{EE}
+
R_C
+
V_{CC}
–
+
V_o
–

FIG. 5.150

Problem 5.

5.4 The r_e Transistor Model

6. **a.** Given an Early voltage of $V_A = 100$ V, determine r_o if $V_{CE_Q} = 8$ V and $I_{C_Q} = 4$ mA.
   b. Using the results of part (a), find the change in I_C for a change in V_{CE} of 6 V at the same Q-point as part (a).

7. For the common-base configuration of Fig. 5.18, an ac signal of 10 mV is applied, resulting in an ac emitter current of 0.5 mA. If $\alpha = 0.980$, determine:
  - **a.** Z_i.
  - **b.** V_o if $R_L = 1.2\ \text{k}\Omega$.
  - **c.** $A_v = V_o/V_i$.
  - **d.** Z_o with $r_o = \infty\ \Omega$.
  - **e.** $A_i = I_o/I_i$.
  - **f.** I_b.

8. Using the model of Fig. 5.16, determine the following for a common-emitter amplifier if $\beta = 80$, $I_E(\text{dc}) = 2\ \text{mA}$, and $r_o = 40\ \text{k}\Omega$.
  - **a.** Z_i.
  - **b.** I_b.
  - **c.** $A_i = I_o/I_i = I_L/I_b$ if $R_L = 1.2\ \text{k}\Omega$.
  - **d.** A_v if $R_L = 1.2\ \text{k}\Omega$.

9. The input impedance to a common-emitter transistor amplifier is $1.2\ \text{k}\Omega$ with $\beta = 140$, $r_o = 50\ \text{k}\Omega$, and $R_L = 2.7\ \text{k}\Omega$. Determine:
  - **a.** r_e.
  - **b.** I_b if $V_i = 30\ \text{mV}$.
  - **c.** I_c.
  - **d.** $A_i = I_o/I_i = I_L/I_b$.
  - **e.** $A_v = V_o/V_i$.

10. For the common-base configuration of Fig. 5.18, the dc emitter current is 3.2 mA and α is 0.99. Determine the following if the applied voltage is 48 mV and the load is $2.2\ \text{k}\Omega$.
  - **a.** r_e.
  - **b.** Z_i.
  - **c.** I_c.
  - **d.** V_o.
  - **e.** A_v.
  - **f.** I_b.

5.5 Common-Emitter Fixed-Bias Configuration

11. For the network of Fig. 5.151:
  - **a.** Determine Z_i and Z_o.
  - **b.** Find A_v.
  - **c.** Repeat parts (a) and (b) with $r_o = 20\ \text{k}\Omega$.

12. For the network of Fig. 5.152, determine V_{CC} for a voltage gain of $A_v = -160$.

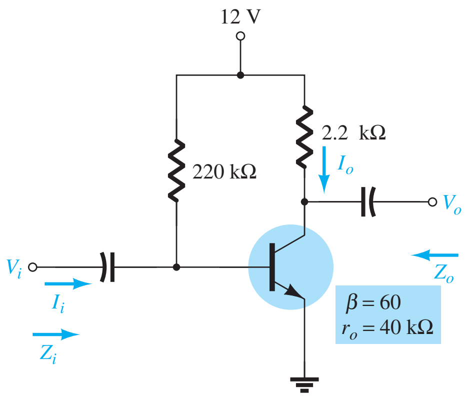


FIG. 5.151
Problem 11.

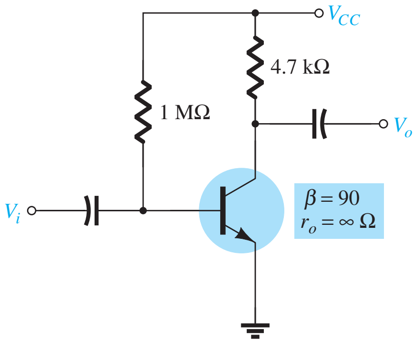


FIG. 5.152
Problem 12.

***13.** For the network of Fig. 5.153:
  - **a.** Calculate I_B, I_C, and r_e.
  - **b.** Determine Z_i and Z_o.
  - **c.** Calculate A_v.
  - **d.** Determine the effect of $r_o = 30\ \text{k}\Omega$ on A_v.

14. For the network of Fig. 5.153, what value of R_C will cut the voltage gain to half the value obtained in problem 13?

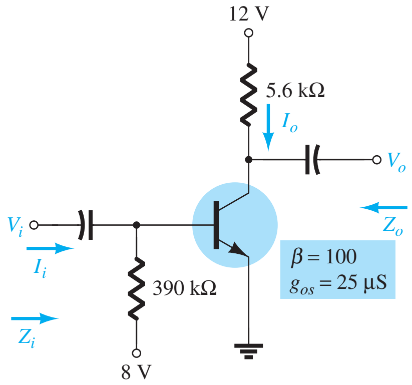

12 V
5.6 kΩ
I_o
V_o
Z_o
V_i
I_i
390 kΩ
Z_i
8 V
β = 100
g_{os} = 25 μS

FIG. 5.153
Problem 13.

5.6 Voltage-Divider Bias

15. For the network of Fig. 5.154:
- **a.** Determine r_e.
- **b.** Calculate Z_i and Z_o.
- **c.** Find A_v.
- **d.** Repeat parts (b) and (c) with $r_o = 25\text{ k}\Omega$.

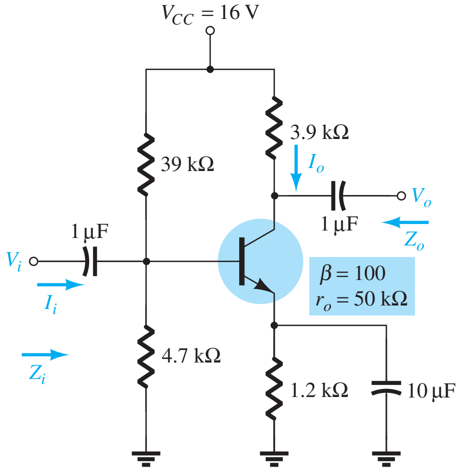

V_{CC} = 16 V
39 kΩ
3.9 kΩ
I_o
V_o
1 μF
Z_o
1 μF
V_i
I_i
β = 100
r_o = 50 kΩ
Z_i
4.7 kΩ
1.2 kΩ
10 μF

FIG. 5.154
Problem 15.

16. Determine V_{CC} for the network of Fig. 5.155 if $A_v = -160$ and $r_o = 100\text{ k}\Omega$.

17. For the network of Fig. 5.156:
- **a.** Determine r_e.
- **b.** Calculate V_B and V_C.
- **c.** Determine Z_i and $A_v = V_o/V_i$.

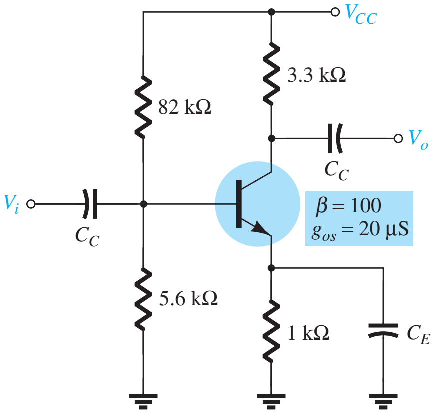

V_{CC}
82 kΩ
3.3 kΩ
V_o
C_C
V_i
C_C
β = 100
g_{os} = 20 μS
5.6 kΩ
1 kΩ
C_E

FIG. 5.155
Problem 16.

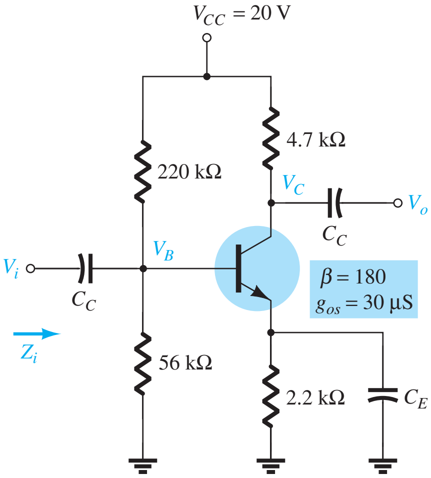

V_{CC} = 20 V
220 kΩ
4.7 kΩ
V_C
V_o
C_C
V_B
V_i
C_C
β = 180
g_{os} = 30 μS
Z_i
56 kΩ
2.2 kΩ
C_E

FIG. 5.156
Problem 17.

18. For the network of Fig. 5.157:
  a. Determine r_e.
  b. Find the dc voltages V_B, V_{CB}, and V_{CE}.
  c. Determine Z_i and Z_o.
  d. Calculate $A_v = V_o/V_i$.

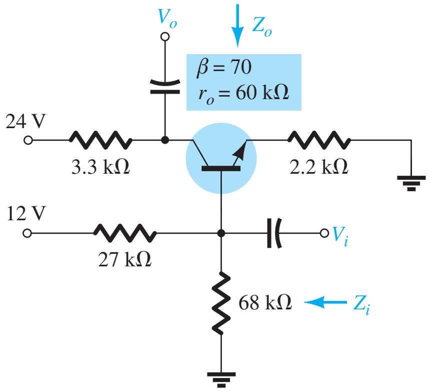

V_o
Z_o
$\beta = 70$
$r_o = 60\ \text{k}\Omega$
24 V
3.3 kΩ
2.2 kΩ
12 V
27 kΩ
V_i
68 kΩ
Z_i

FIG. 5.157
Problem 18.

5.7 CE Emitter-Bias Configuration

19. For the network of Fig. 5.158:
  a. Determine r_e.
  b. Find Z_i and Z_o.
  c. Calculate A_v.
  d. Repeat parts (b) and (c) with $r_o = 20\ \text{k}\Omega$.

20. Repeat Problem 19 with R_E bypassed. Compare results.

21. For the network of Fig. 5.159, determine R_E and R_B if $A_v = -10$ and $r_e = 3.8\ \Omega$. Assume that $Z_b = \beta R_E$.

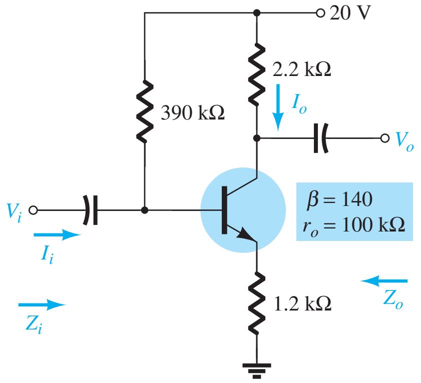

20 V
2.2 kΩ
390 kΩ
I_o
V_o
$\beta = 140$
$r_o = 100\ \text{k}\Omega$
V_i
I_i
1.2 kΩ
Z_o
Z_i

FIG. 5.158
Problems 19 and 20.

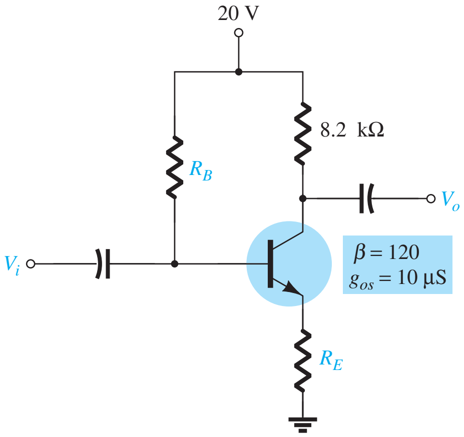

20 V
8.2 kΩ
R_B
V_o
V_i
$\beta = 120$
$g_{os} = 10\ \mu\text{S}$
R_E

FIG. 5.159
Problem 21.

***22.** For the network of Fig. 5.160:
  a. Determine r_e.
  b. Find Z_i and A_v.

23. For the network of Fig. 5.161:
  a. Determine r_e.
  b. Calculate V_B, V_{CE}, and V_{CB}.
  c. Determine Z_i and Z_o.
  d. Calculate $A_v = V_o/V_i$.
  e. Determine $A_i = I_o/I_i$.

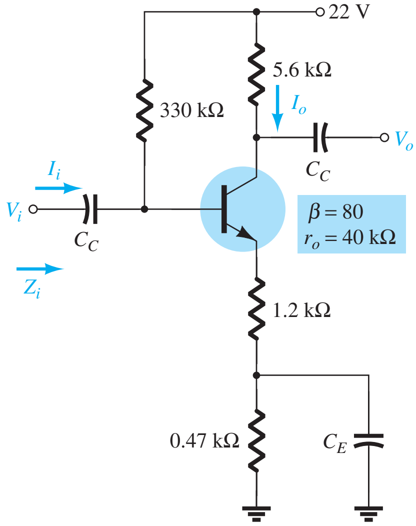

22 V
5.6 kΩ
I_o
330 kΩ
V_o
C_C
I_i
V_i
C_C
$\beta = 80$
$r_o = 40$ kΩ
Z_i
1.2 kΩ
0.47 kΩ
C_E

FIG. 5.160
Problem 22.

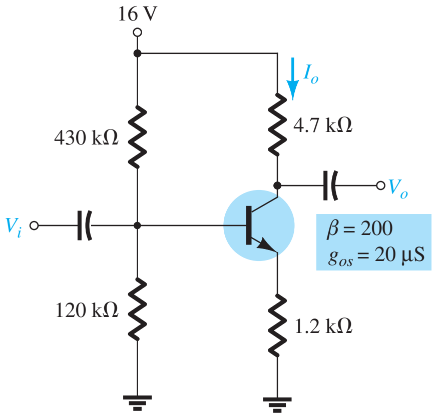

16 V
I_o
4.7 kΩ
430 kΩ
V_o
V_i
$\beta = 200$
$g_{os} = 20$ μS
120 kΩ
1.2 kΩ

FIG. 5.161
Problem 23.

5.8 Emitter-Follower Configuration

24. For the network of Fig. 5.162:
  a. Determine r_e and βr_e.
  b. Find Z_i and Z_o.
  c. Calculate A_v.

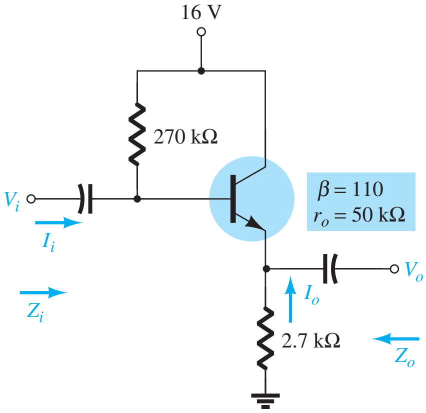

16 V
270 kΩ
V_i
$\beta = 110$
$r_o = 50$ kΩ
I_i
V_o
Z_i
I_o
2.7 kΩ
Z_o

FIG. 5.162
Problem 24.

***25.** For the network of Fig. 5.163:
  a. Determine Z_i and Z_o.
  b. Find A_v.
  c. Calculate V_o if $V_i = 1$ mV.

***26.** For the network of Fig. 5.164:
  a. Calculate I_B and I_C.
  b. Determine r_e.
  c. Determine Z_i and Z_o.
  d. Find A_v.

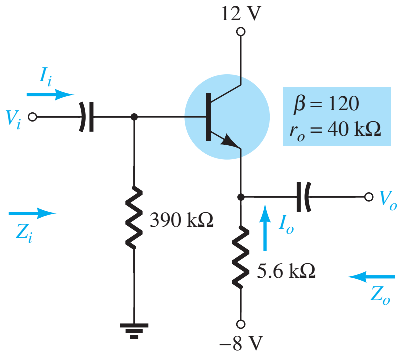

12 V
I_i
V_i
$\beta = 120$
$r_o = 40$ kΩ
Z_i
390 kΩ
V_o
I_o
5.6 kΩ
Z_o
–8 V

FIG. 5.163
Problem 25.

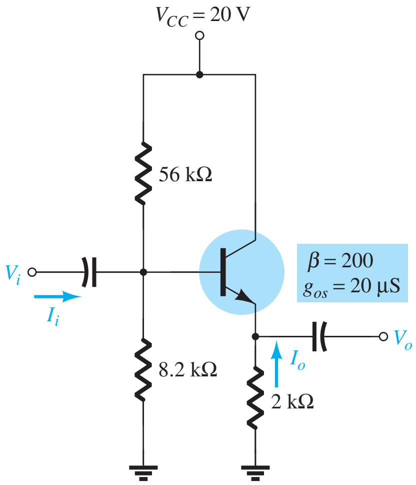

$V_{CC} = 20$ V
56 kΩ
V_i
$\beta = 200$
$g_{os} = 20$ μS
I_i
V_o
8.2 kΩ
I_o
2 kΩ

FIG. 5.164
Problem 26.

5.9 Common-Base Configuration

27. For the common-base configuration of Fig. 5.165:
- **a.** Determine r_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

***28.** For the network of Fig. 5.166, determine A_v.

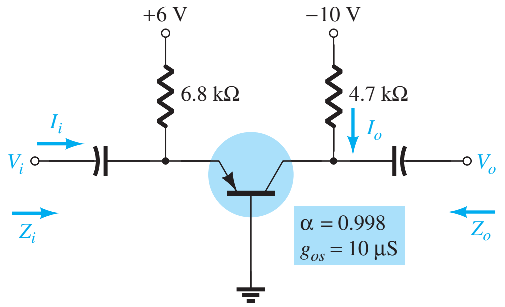

+6 V
−10 V
6.8 kΩ
4.7 kΩ
I_i
I_o
V_i
V_o
Z_i
Z_o
α = 0.998
g_{os} = 10 μS

FIG. 5.165
Problem 27.

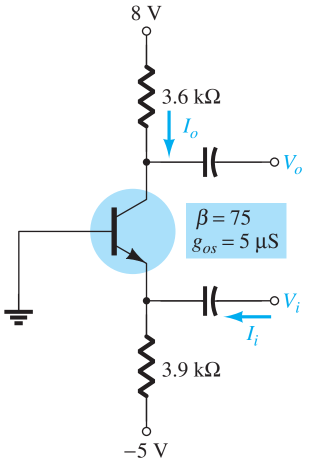

8 V
3.6 kΩ
I_o
V_o
β = 75
g_{os} = 5 μS
V_i
I_i
3.9 kΩ
−5 V

FIG. 5.166
Problem 28.

5.10 Collector Feedback Configuration

29. For the collector feedback configuration of Fig. 5.167:
- **a.** Determine r_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

***30.** Given $r_e = 10\ \Omega$, $\beta = 200$, $A_v = -160$, and $A_i = 19$ for the network of Fig. 5.168, determine R_C, R_F, and V_{CC}.

***31.** For the network of Fig. 5.49:
- **a.** Derive the approximate equation for A_v.
- **b.** Derive the approximate equations for Z_i and Z_o.
- **c.** Given $R_C = 2.2\ \text{k}\Omega$, $R_F = 120\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $\beta = 90$, and $V_{CC} = 10$ V, calculate the magnitudes of A_v, Z_i, and Z_o using the equations of parts (a) and (b).

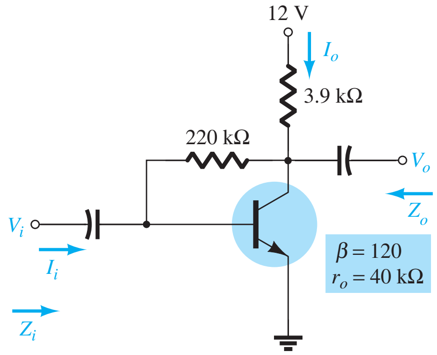

12 V
I_o
3.9 kΩ
220 kΩ
V_o
Z_o
V_i
I_i
Z_i
β = 120
r_o = 40 kΩ

FIG. 5.167
Problem 29.

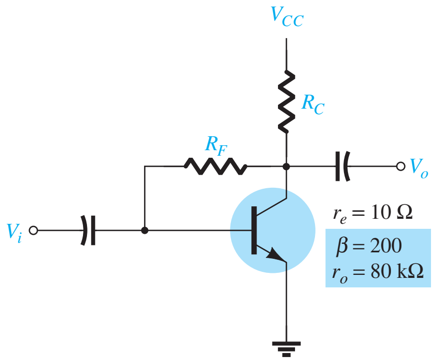

V_{CC}
R_C
R_F
V_o
V_i
r_e = 10 Ω
β = 200
r_o = 80 kΩ

FIG. 5.168
Problem 30.

5.11 Collector DC Feedback Configuration

32. For the network of Fig. 5.169:
- **a.** Determine Z_i and Z_o.
- **b.** Find A_v.

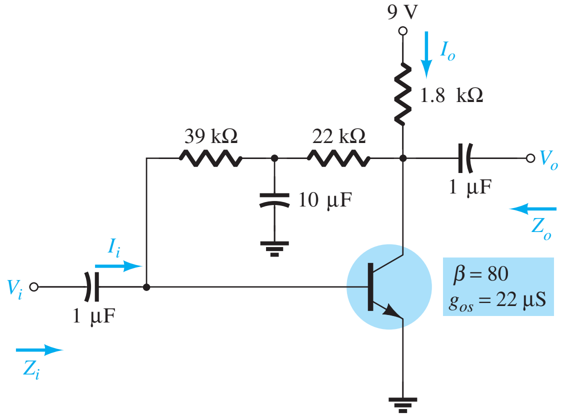


FIG. 5.169
Problems 32 and 33.

33. Repeat problem 32 with the addition of an emitter resistor $R_E = 0.68\ \text{k}\Omega$.

5.12–5.15 Effect of R_L and R_s and Two-Port Systems Approach

***34.** For the fixed-bias configuration of Fig. 5.170:

- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Calculate the gain $A_{v_L} = V_o/V_i$.
- **d.** Determine the current gain $A_{i_L} = I_o/I_i$.

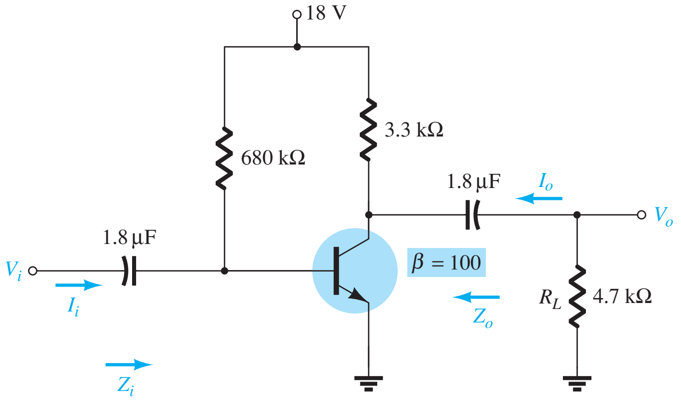


FIG. 5.170
Problems 34 and 35.

35. **a.** Determine the voltage gain A_{v_L} for the network of Fig. 5.170 for $R_L = 4.7\ \text{k}\Omega$, $2.2\ \text{k}\Omega$, and $0.5\ \text{k}\Omega$. What is the effect of decreasing levels of R_L on the voltage gain?

- **b.** How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing values of R_L?

***36.** For the network of Fig. 5.171:

- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Determine $A_v = V_o/V_i$.
- **d.** Determine $A_{v_s} = V_o/V_s$.
- **e.** Change R_s to 1 kΩ and determine A_v. How does A_v change with the level of R_s?
- **f.** Change R_s to 1 kΩ and determine A_{v_s}. How does A_{v_s} change with the level of R_s?
- **g.** Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. How do they change with the change in R_s?
- **h.** For the original network of Fig. 5.171 calculate $A_i = I_o/I_i$.

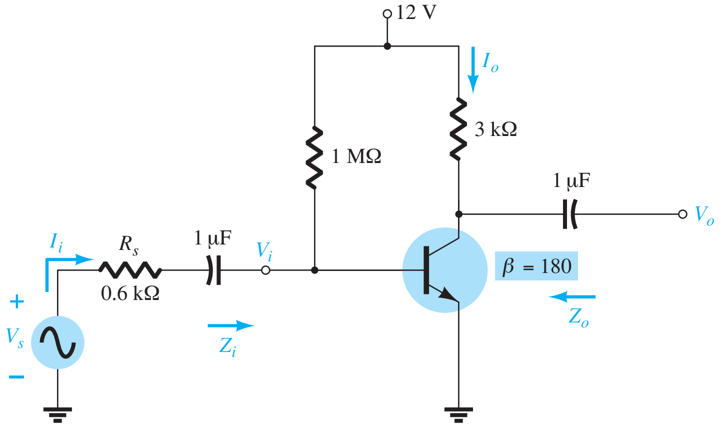


FIG. 5.171
Problem 36.

***37.** For the network of Fig. 5.172:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Calculate A_{i_L}.

e. Change R_L to 5.6 kΩ and calculate A_{v_s}. What is the effect of increasing levels of R_L on the gain?

f. Change R_s to 0.5 kΩ (with R_L at 2.7 kΩ) and comment on the effect of reducing R_s on A_{v_s}.

g. Change R_L to 5.6 kΩ and R_s to 0.5 kΩ and determine the new levels of Z_i and Z_o. How are the impedance parameters affected by changing levels of R_L and R_s?

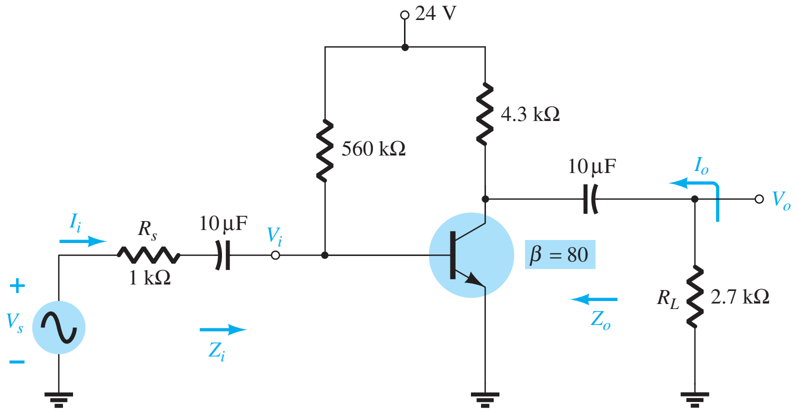


FIG. 5.172
Problem 37.

38. For the voltage-divider configuration of Fig. 5.173:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.

c. Calculate the gain A_{v_L}.

d. Determine the current gain A_{i_L}.

e. Determine A_{v_L}, A_{i_L}, and Z_o using the r_e model and compare solutions.

39. **a.** Determine the voltage gain A_{v_L} for the network of Fig. 5.173 with $R_L = 4.7$ kΩ, 2.2 kΩ, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?

b. How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing levels of R_L?

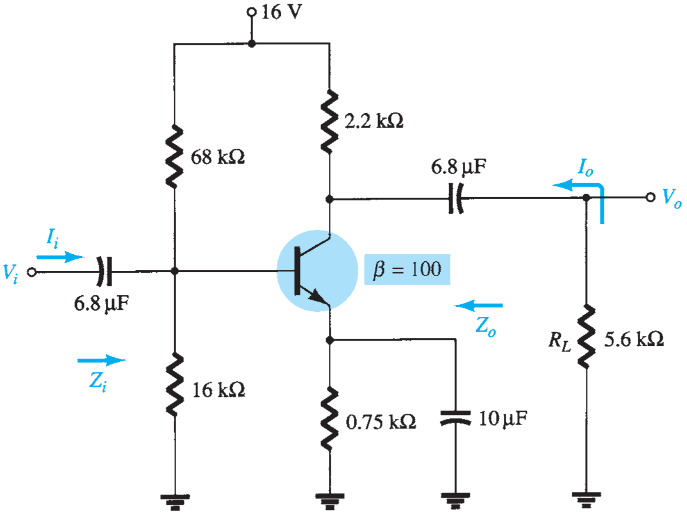

16 V
2.2 kΩ
68 kΩ
6.8 μF
I_o
V_o
I_i
V_i
6.8 μF
β = 100
Z_o
R_L
5.6 kΩ
Z_i
16 kΩ
0.75 kΩ
10 μF

FIG. 5.173
Problems 38 and 39.

40. For the emitter-stabilized network of Fig. 5.174:

a. Determine $A_{v_{\mathrm{NL}}}$, Z_i, and Z_o.
b. Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
c. Determine A_{v_L} and A_{v_s}.
d. Change R_s to 1 kΩ. What is the effect on $A_{v_{\mathrm{NL}}}$, Z_i, and Z_o?
e. Change R_s to 1 kΩ and determine A_{v_L} and A_{v_s}. What is the effect of increasing levels of R_s on A_{v_L} and A_{v_s}?
f. Determine $A_i = I_o/I_i$.

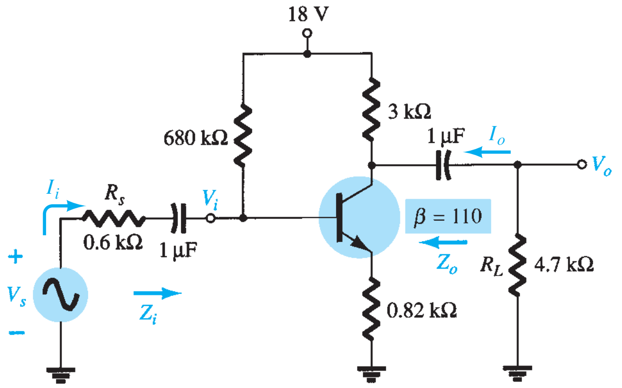

18 V
3 kΩ
680 kΩ
1 μF
I_o
V_o
I_i
R_s
V_i
0.6 kΩ
1 μF
β = 110
+
V_s
–
Z_i
Z_o
R_L
4.7 kΩ
0.82 kΩ

FIG. 5.174
Problem 40.

***41.** For the network of Fig. 5.175:

a. Determine $A_{v_{\mathrm{NL}}}$, Z_i, and Z_o.
b. Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
c. Determine A_{v_L} and A_{v_s}.
d. Change R_s to 1 kΩ and determine A_{v_L} and A_{v_s}. What is the effect of increasing levels of R_s on the voltage gains?
e. Change R_s to 1 kΩ and determine $A_{v_{\mathrm{NL}}}$, Z_i, and Z_o. What is the effect of increasing levels of R_s on the parameters?
f. Change R_L to 5.6 kΩ and determine A_{v_L} and A_{v_s}. What is the effect of increasing levels of R_L on the voltage gains? Maintain R_s at its original level of 0.6 kΩ.
g. Determine $A_i = \dfrac{I_o}{I_i}$ with $R_L = 2.7\ \mathrm{k\Omega}$ and $R_s = 0.6\ \mathrm{k\Omega}$.

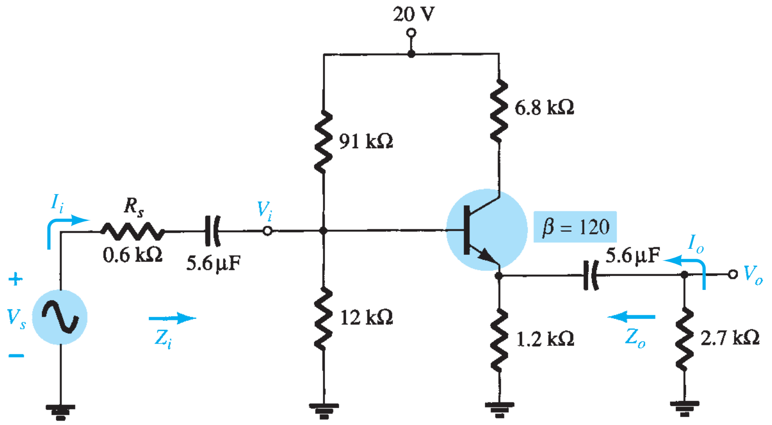

20 V
6.8 kΩ
91 kΩ
I_i
R_s
V_i
0.6 kΩ
5.6 μF
$\beta = 120$
5.6 μF
I_o
V_o
+
V_s
−
Z_i
12 kΩ
1.2 kΩ
Z_o
2.7 kΩ

FIG. 5.175

Problem 41.

*42. For the common-base network of Fig. 5.176:

a. Determine Z_i, Z_o, and $A_{v_{\text{NL}}}$.

b. Sketch the two-port model of Fig. 5.63 with the parameters of part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Determine A_{v_L} and A_{v_s} using the r_e model and compare with the results of part (c).

e. Change R_s to 0.5 kΩ and R_L to 2.2 kΩ and calculate A_{v_L} and A_{v_s}. What is the effect of changing levels of R_s and R_L on the voltage gains?

f. Determine Z_o if R_s changed to 0.5 kΩ with all other parameters as appearing in Fig. 5.176. How is Z_o affected by changing levels of R_s?

g. Determine Z_i if R_L is reduced to 2.2 kΩ. What is the effect of changing levels of R_L on the input impedance?

h. For the original network of Fig. 5.176 determine $A_i = I_o/I_i$.

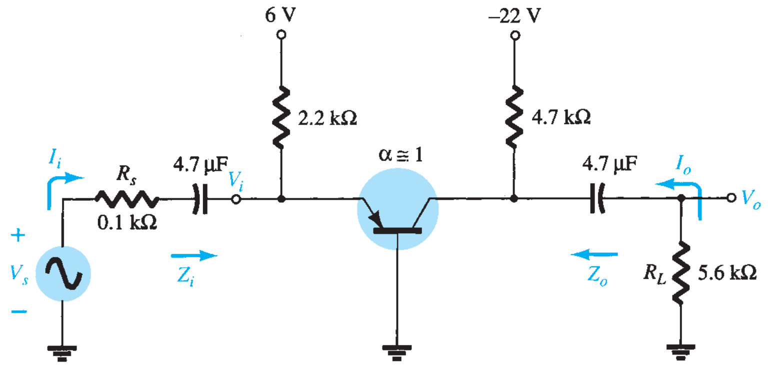

6 V
−22 V
2.2 kΩ
4.7 kΩ
$\alpha \cong 1$
I_i
R_s
4.7 μF
V_i
0.1 kΩ
4.7 μF
I_o
V_o
+
V_s
−
Z_i
Z_o
R_L
5.6 kΩ

FIG. 5.176

Problem 42.

5.16 Cascaded Systems

*43. For the cascaded system of Fig. 5.177 with two identical stages, determine:

a. The loaded voltage gain of each stage.

b. The total gain of the system, A_v and A_{v_s}.

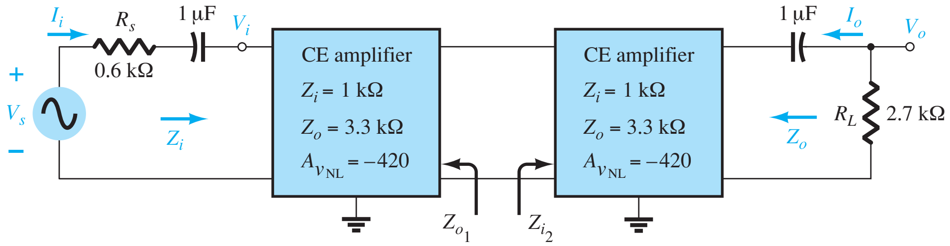
c. The loaded current gain of each stage.

d. The total current gain of the system $A_{i_L} = I_o/I_i$.

e. How Z_i is affected by the second stage and R_L.

f. How Z_o is affected by the first stage and R_s.

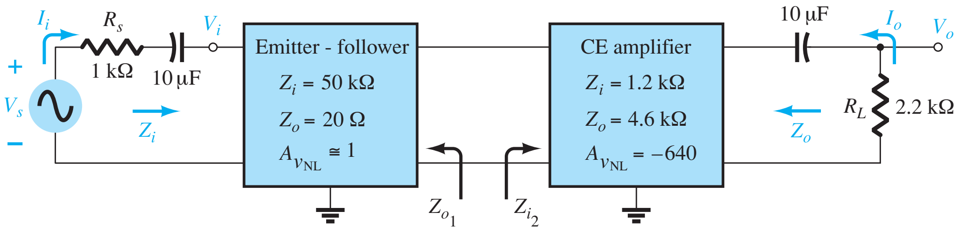
g. The phase relationship between V_o and V_i.



I_i
R_s
0.6 kΩ
1 μF
V_i
+
V_s
−
Z_i
CE amplifier
Z_i = 1 kΩ
Z_o = 3.3 kΩ
$A_{v_{NL}}$ = −420
Z_{o_1}
Z_{i_2}
CE amplifier
Z_i = 1 kΩ
Z_o = 3.3 kΩ
$A_{v_{NL}}$ = −420
1 μF
I_o
V_o
R_L
2.7 kΩ
Z_o

FIG. 5.177
Problem 43.

***44.** For the cascaded system of Fig. 5.178, determine:
- **a.** The loaded voltage gain of each stage.
- **b.** The total gain of the system, A_{v_L} and A_{v_s}.
- **c.** The loaded current gain of each stage.
- **d.** The total current gain of the system.
- **e.** How Z_i is affected by the second stage and R_L.
- **f.** How Z_o is affected by the first stage and R_s.
- **g.** The phase relationship between V_o and V_i.

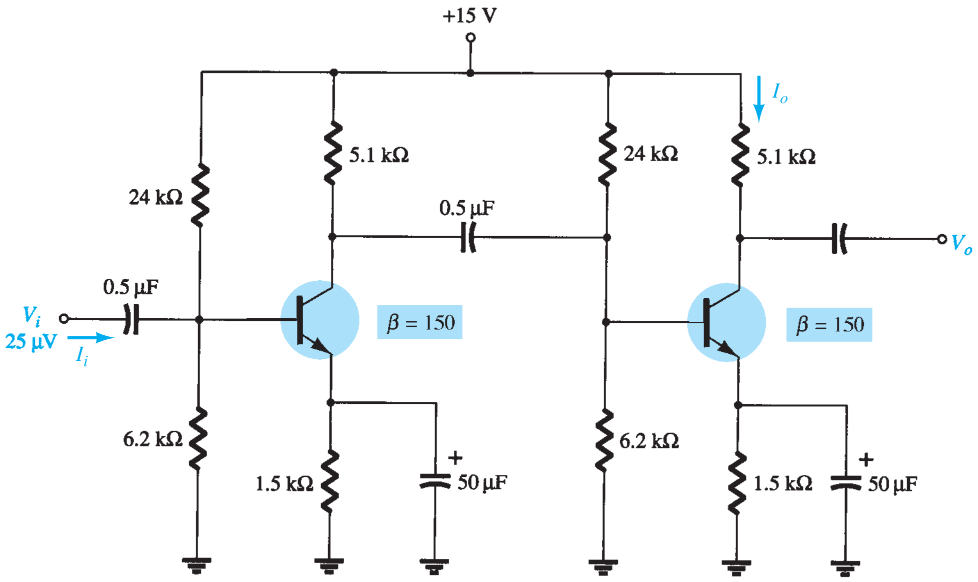


I_i
R_s
1 kΩ
10 μF
V_i
+
V_s
−
Z_i
Emitter - follower
Z_i = 50 kΩ
Z_o = 20 Ω
$A_{v_{NL}}$ ≅ 1
Z_{o_1}
Z_{i_2}
CE amplifier
Z_i = 1.2 kΩ
Z_o = 4.6 kΩ
$A_{v_{NL}}$ = −640
10 μF
I_o
V_o
R_L
2.2 kΩ
Z_o

FIG. 5.178
Problem 44.

45. For the BJT cascade amplifier of Fig. 5.179, calculate the dc bias voltages and collector current for each stage.

46. **a.** Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig. 5.179.
- **b.** Find $A_{i_T} = I_o/I_i$.



+15 V
I_o
24 kΩ
5.1 kΩ
24 kΩ
5.1 kΩ
0.5 μF
V_o
0.5 μF
V_i
25 μV
I_i
β = 150
β = 150
6.2 kΩ
1.5 kΩ
+
50 μF
6.2 kΩ
1.5 kΩ
+
50 μF

FIG. 5.179
Problems 45 and 46.

47. For the cascode amplifier circuit of Fig. 5.180, calculate the dc bias voltages V_{B_1}, V_{B_2}, and V_{C_2}.

***48.** For the cascode amplifier circuit of Fig. 5.180, calculate the voltage gain A_v and output voltage V_o.

49. Calculate the ac voltage across a 10-kΩ load connected at the output of the circuit in Fig. 5.180.

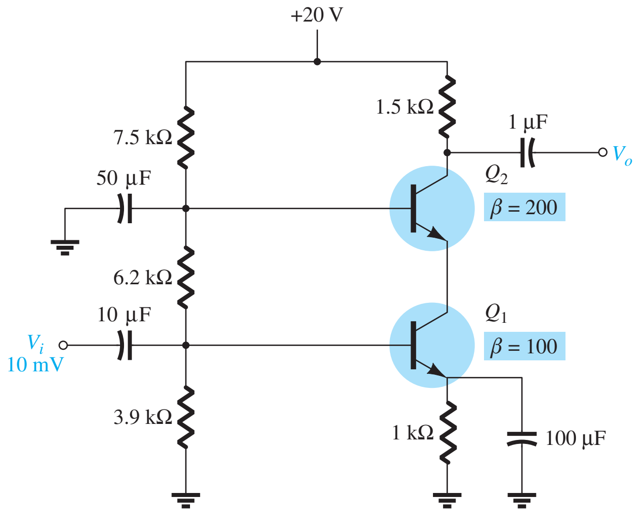

+20 V
1.5 kΩ
1 μF
V_o
7.5 kΩ
50 μF
Q_2
$\beta = 200$
6.2 kΩ
10 μF
Q_1
$\beta = 100$
V_i
10 mV
3.9 kΩ
1 kΩ
100 μF

FIG. 5.180

Problems 47 and 49.

5.17 Darlington Connection

50. For the Darlington network of Fig. 5.181:

a. Determine the dc levels of V_{B_1}, V_{C_1}, V_{E_2}, V_{CB_1}, and V_{CE_2}.

b. Find the currents I_{B_1}, I_{B_2}, and I_{E_2}.

c. Calculate Z_i and Z_o.

d. Determine the voltage gain $A_v = V_o/V_i$ and current gain $A_i = I_o/I_i$.

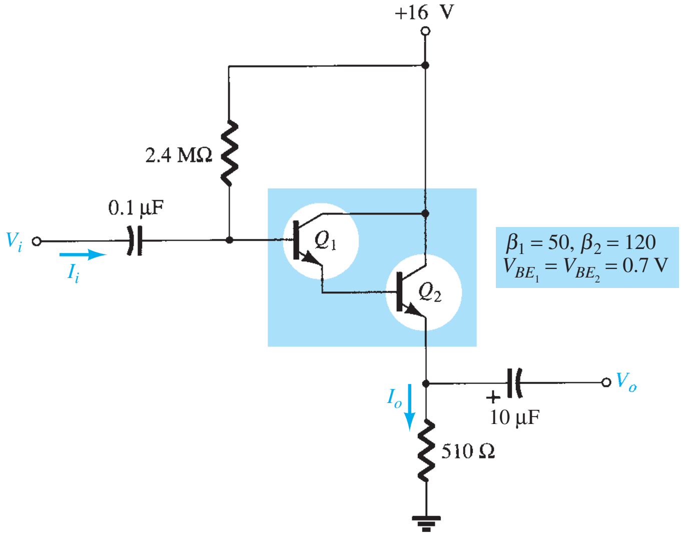

+16 V
2.4 MΩ
0.1 μF
V_i
I_i
Q_1
Q_2
$\beta_1 = 50, \beta_2 = 120$
$V_{BE_1} = V_{BE_2} = 0.7$ V
I_o
+
10 μF
V_o
510 Ω

FIG. 5.181

Problems 50 through 53.

51. Repeat problem 50 with a load resistor of 1.2 kΩ.

52. Determine $A_v = V_o/V_s$ for the network of Fig. 5.181 if the source has an internal resistance of 1.2 kΩ and the applied load is 10 kΩ.

53. A resistor $R_C = 470\ \Omega$ is added to the network of Fig. 5.181 along with a bypass capacitor $C_E = 5\ \mu$F across the emitter resistor. If $\beta_D = 4000$, $V_{BE_T} = 1.6$ V, and $r_{o_1} = r_{o_2} = 40$ kΩ for a packaged Darlington amplifier:

a. Find the dc levels of V_{B_1}, V_{E_2}, and V_{CE_2}.

b. Determine Z_i and Z_o.

c. Determine the voltage gain $A_v = V_o/V_i$ if the output voltage V_o is taken off the collector terminal via a coupling capacitor of 10 μF.

5.18 Feedback Pair

54. For the feedback pair of Fig. 5.182:
- **a.** Calculate the dc voltages V_{B_1}, V_{B_2}, V_{C_1}, V_{C_2}, V_{E_1}, and V_{E_2}.
- **b.** Determine the dc currents I_{B_1}, I_{C_1}, I_{B_2}, I_{C_2}, and I_{E_2}.
- **c.** Calculate the impedances Z_i and Z_o.
- **d.** Find the voltage gain $A_v = V_o/V_i$.
- **e.** Determine the current gain $A_i = I_o/I_i$.

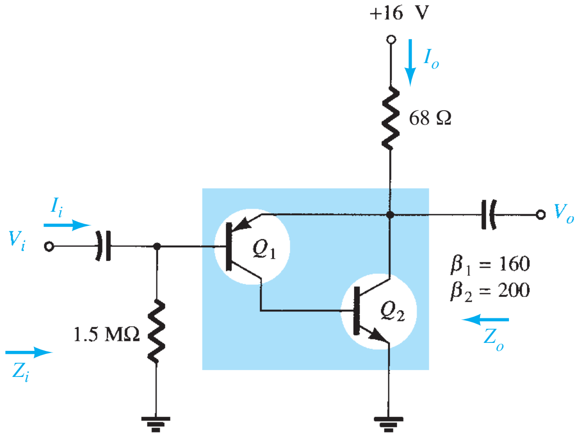


FIG. 5.182
Problems 54 and 55.

55. Repeat problem 54 if a 22-Ω resistor is added between V_{E_2} and ground.

56. Repeat problem 54 if a load resistance of 1.2 kΩ is introduced.

5.19 The Hybrid Equivalent Model

57. Given $I_E(\text{dc}) = 1.2$ mA, $\beta = 120$, and $r_o = 40$ kΩ, sketch the following:
- **a.** Common-emitter hybrid equivalent model.
- **b.** Common-emitter r_e equivalent model.
- **c.** Common-base hybrid equivalent model.
- **d.** Common-base r_e equivalent model.

58. Given $h_{ie} = 2.4\ \text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 4 \times 10^{-4}$, and $h_{oe} = 25\ \mu\text{S}$, sketch the following:
- **a.** Common-emitter hybrid equivalent model.
- **b.** Common-emitter r_e equivalent model.
- **c.** Common-base hybrid equivalent model.
- **d.** Common-base r_e equivalent model.

59. Redraw the common-emitter network of Fig. 5.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.

60. Redraw the network of Fig. 5.183 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

61. Redraw the network of Fig. 5.184 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

62. Given the typical values of $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, and $A_v = -160$ for the input configuration of Fig. 5.185:
- **a.** Determine V_o in terms of V_i.
- **b.** Calculate I_b in terms of V_i.
- **c.** Calculate I_b if $h_{re}V_o$ is ignored.
- **d.** Determine the percentage difference in I_b using the following equation:

$$\%\ \text{difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

- **e.** Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example?

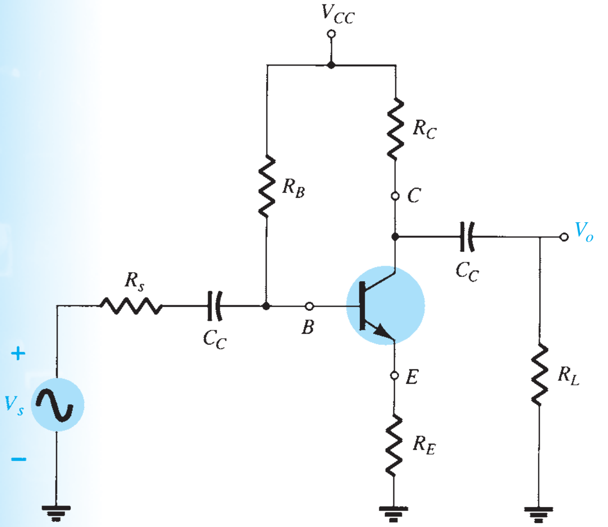


FIG. 5.183
Problem 60.

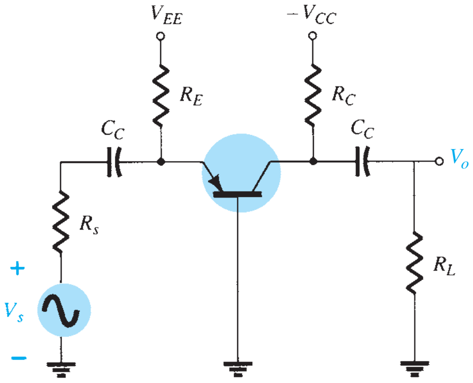


FIG. 5.184
Problem 61.

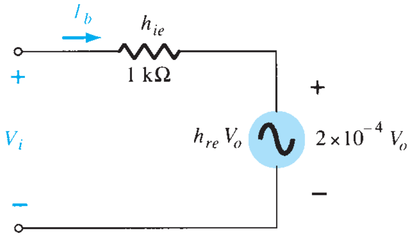


FIG. 5.185
Problems 62 and 64.

63. Given the typical values of $R_L = 2.2\ \text{k}\Omega$ and $h_{oe} = 20\ \mu\text{S}$, is it a good approximation to ignore the effects of $1/h_{oe}$ on the total load impedance? What is the percentage difference in total loading on the transistor using the following equation?

$$\%\ \text{difference in total load} = \frac{R_L - R_L\|(1/h_{oe})}{R_L} \times 100\%$$

64. Repeat Problem 62 using the average values of the parameters of Fig. 5.92 with $A_v = -180$.

65. Repeat Problem 63 for $R_L = 3.3\ \text{k}\Omega$ and the average value of h_{oe} in Fig. 5.92.

5.20 Approximate Hybrid Equivalent Circuit

66. a. Given $\beta = 120$, $r_e = 4.5\ \Omega$, and $r_o = 40\ \text{k}\Omega$, sketch the approximate hybrid equivalent circuit.

b. Given $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 90$, and $h_{oe} = 20\ \mu\text{S}$, sketch the r_e model.

67. For the network of Problem 11:

a. Determine r_e.
b. Find h_{fe} and h_{ie}.
c. Find Z_i and Z_o using the hybrid parameters.
d. Calculate A_v and A_i using the hybrid parameters.
e. Determine Z_i and Z_o if $h_{oe} = 50\ \mu\text{S}$.
f. Determine A_v and A_i if $h_{oe} = 50\ \mu\text{S}$.
g. Compare the solutions above with those of Problem 9. (Note: The solutions are available in Appendix E if Problem 11 was not performed.)

68. For the network of Fig. 5.186:

a. Determine Z_i and Z_o.
b. Calculate A_v and A_i.
c. Determine r_e and compare βr_e to h_{ie}.

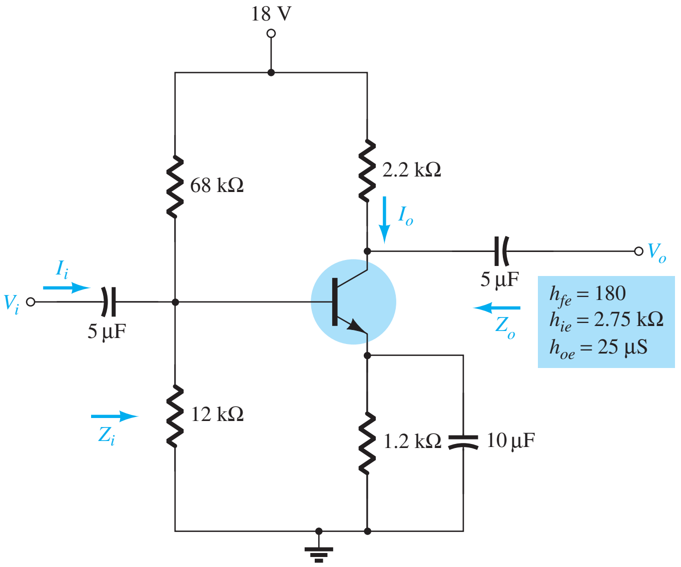

18 V
68 kΩ
2.2 kΩ
I_o
V_o
I_i
V_i
5 µF
5 µF
Z_o
$h_{fe} = 180$
$h_{ie} = 2.75$ kΩ
$h_{oe} = 25$ µS
12 kΩ
Z_i
1.2 kΩ
10 µF

FIG. 5.186
Problem 68.

***69.** For the common-base network of Fig. 5.187:
- **a.** Determine Z_i and Z_o.
- **b.** Calculate A_v and A_i.
- **c.** Determine α, β, r_e, and r_o.

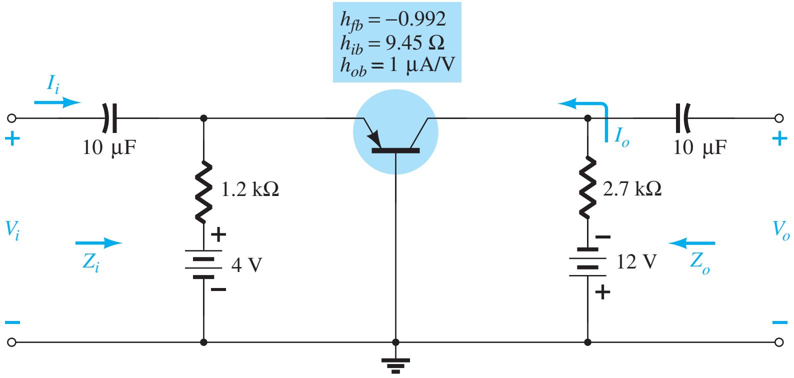

$h_{fb} = -0.992$
$h_{ib} = 9.45\ \Omega$
$h_{ob} = 1$ µA/V
I_i
10 µF
+
V_i
Z_i
–
1.2 kΩ
+
4 V
–
I_o
10 µF
+
2.7 kΩ
–
12 V
+
Z_o
V_o
–

FIG. 5.187
Problem 69.

5.21 Complete Hybrid Equivalent Model

***70.** Repeat parts (a) and (b) of Problem 68 with $h_{re} = 2 \times 10^{-4}$ and compare results.

***71.** For the network of Fig. 5.188, determine:
- **a.** Z_i.
- **b.** A_v.
- **c.** $A_i = I_o/I_i$.
- **d.** Z_o.

***72.** For the common-base amplifier of Fig. 5.189, determine:
- **a.** Z_i.
- **b.** A_i.
- **c.** A_v.
- **d.** Z_o.

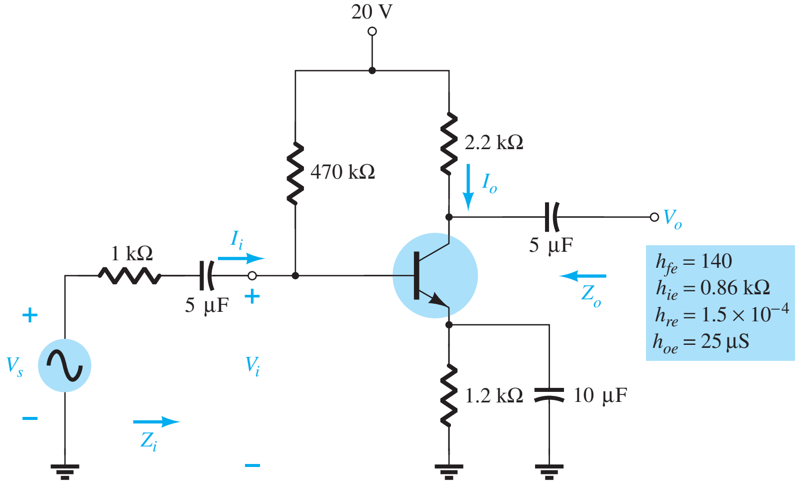

20 V
470 kΩ
2.2 kΩ
I_o
5 μF
V_o
1 kΩ
I_i
5 μF
+
+
V_s
−
V_i
Z_i
−
Z_o
1.2 kΩ
10 μF
$h_{fe} = 140$
$h_{ie} = 0.86$ kΩ
$h_{re} = 1.5 \times 10^{-4}$
$h_{oe} = 25$ μS

FIG. 5.188
Problem 71.

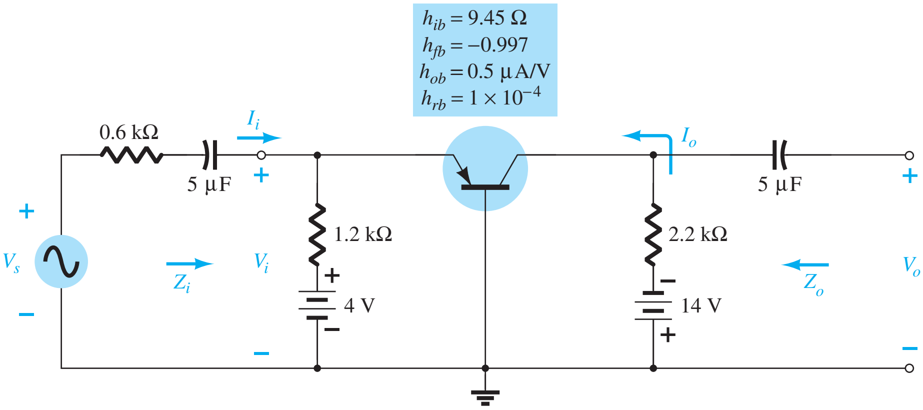

$h_{ib} = 9.45$ Ω
$h_{fb} = -0.997$
$h_{ob} = 0.5$ μA/V
$h_{rb} = 1 \times 10^{-4}$
0.6 kΩ
I_i
5 μF
+
+
V_s
−
Z_i
V_i
−
1.2 kΩ
+
4 V
−
I_o
2.2 kΩ
−
14 V
+
5 μF
+
Z_o
V_o
−

FIG. 5.189
Problem 72.

5.22 Hybrid π Model

73. **a.** Sketch the Giacoletto (hybrid π) model for a common-emitter transistor if $r_b = 4\ \Omega$, $C_\pi = 5$ pF, $C_u = 1.5$ pF, $h_{oe} = 18\ \mu$S, $\beta = 120$, and $r_e = 14$.

b. If the applied load is 1.2 kΩ and the source resistance is 250 Ω, draw the approximate hybrid π model for the low- and mid-frequency range.

5.23 Variations of Transistor Parameters

For Problems 74 through 80, use Figs. 5.124 through 5.126.

74. **a.** Using Fig. 5.124, determine the magnitude of the percentage change in h_{fe} for an I_C change from 0.2 mA to 1 mA using the equation

$$\%\ \text{change} = \left|\frac{h_{fe}(0.2\text{ mA}) - h_{fe}(1\text{ mA})}{h_{fe}(0.2\text{ mA})}\right| \times 100\%$$

b. Repeat part (a) for an I_C change from 1 mA to 5 mA.

75. Repeat Problem 74 for h_{ie} (same changes in I_C).

76. **a.** If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA on Fig. 5.124, what is the approximate value of h_{oe} at $I_C = 0.2$ mA?

b. Determine its resistive value at 0.2 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

77. **a.** If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA of Fig. 5.124, what is the approximate value of h_{oe} at $I_C = 10$ mA?

b. Determine its resistive value at 10 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

78. **a.** If $h_{re} = 2 \times 10^{-4}$ at $I_C = 1$ mA on Fig. 5.124, determine the approximate value of h_{re} at 0.1 mA.

b. For the value of h_{re} determined in part (a), can h_{re} be ignored as a good approximation if $A_v = 210$?

79. a. Based on a review of the characteristics of Fig. 5.124, which parameter changed the least for the full range of collector current?

b. Which parameter changed the most?

c. What are the maximum and minimum values of $1/h_{oe}$? Is the approximation $1/h_{oe} \| R_L \cong R_L$ more appropriate at high or low levels of collector current?

d. In which region of current spectrum is the approximation $h_{re}V_{ce} \cong 0$ the most appropriate?

80. a. Based on a review of the characteristics of Fig. 5.126, which parameter changed the most with increase in temperature?

b. Which changed the least?

c. What are the maximum and minimum values of h_{fe}? Is the change in magnitude significant? Was it expected?

d. How does r_e vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.

e. In which temperature range do the parameters change the least?

5.24 Troubleshooting

***81.** Given the network of Fig. 5.190:

a. Is the network properly biased?

b. What problem in the network construction could cause V_B to be 6.22 V and obtain the given waveform of Fig. 5.190?

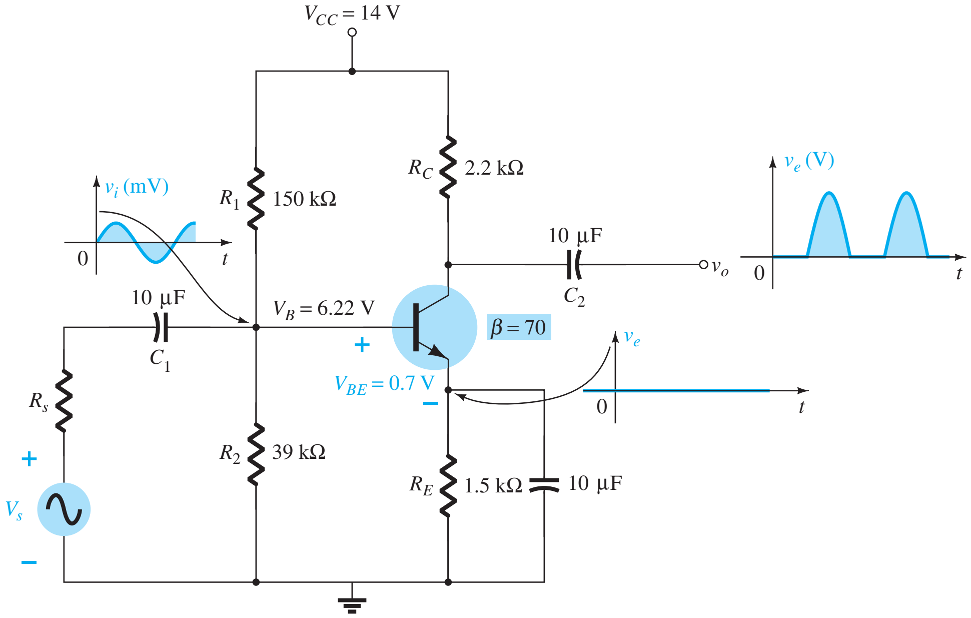


FIG. 5.190
Problem 81.

5.27 Computer Analysis

82. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.25. Display the input and output waveforms.

83. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.32. Display the input and output waveforms.

84. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.44. Display the input and output waveforms.

85. Using Multisim, determine the voltage gain for the network of Fig. 5.28.

86. Using Multisim, determine the voltage gain for the network of Fig. 5.39.

87. Using PSpice Windows, determine the level of V_o for $V_i = 1$ mV for the network of Fig. 5.69. For the capacitive elements assume a frequency of 1 kHz.

88. Repeat Problem 87 for the network of Fig. 5.71.

89. Repeat Problem 87 for the network of Fig. 5.82.

90. Repeat Problem 87 using Multisim.

91. Repeat Problem 87 using Multisim.

6

Field-Effect Transistors

CHAPTER OBJECTIVES

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET), and Metal-Semiconductor FET (MESFET) transistors.
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET, and MESFET transistor.
- Understand the vast amount of information provided on the specification sheet for each type of FET.
- Be aware of the differences between the dc analysis of the various types of FETs.

6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

The BJT transistor is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

In other words, the current I_C in Fig. 6.1a is a direct function of the level of I_B. For the FET the current I_D will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 6.1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi* indicates that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term *field effect* in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

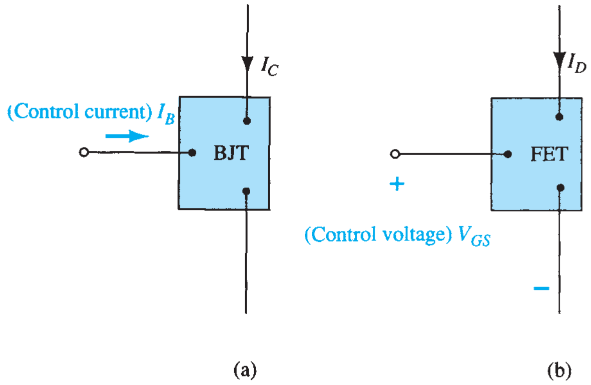


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

There is a natural tendency when introducing a device with a range of applications similar to one already introduced to compare some of the general characteristics of one to those of the other:

One of the most important characteristics of the FET is its high input impedance.

At a level of 1 MΩ to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage. For this reason:

Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.

However,

FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Three types of FETs are introduced in this chapter: the *junction field-effect transistor* (JFET), *the metal–oxide–semiconductor field-effect transistor* (MOSFET), and the *metal–semiconductor field-effect transistor* (MESFET). The MOSFET category is further broken down into *depletion* and *enhancement* types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section). The MESFET is a more recent development and takes full advantage of the high-speed characteristics of GaAs as the base semiconductor material. Although currently the more expensive option, the cost issue is often outweighed by the need for higher speeds in RF and computer designs.

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 7. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Ian Munro Ross and G. C. Dacey (Fig. 6.2) were instrumental in the early stages of development of the field-effect transistor. Take particular note of the equipment used in 1955 for their research.

Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955.

Dr. Ross Born: Southport, England; PhD, Gonville and Caius College, Cambridge University; President Emeritus, AT&T Bell Labs; Fellow, IEEE; Member, the National Science Board; Chairman, National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois; PhD, California Institute of Technology; Director of Solid-State Electronics Research, Bell Labs; Vice President, Research, Sandia Corporation; Member IRE, Tau Beta Pi, Eta Kappa Nu

FIG. 6.2
Early development of the field-effect transistor.
(Courtesy of AT&T Archives and History Center.)

6.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a section devoted to the effect of using a *pnp* transistor. For the JFET transistor the *n*-channel device will be the prominent device, with paragraphs and sections devoted to the effect of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 6.3. Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 6.3, that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

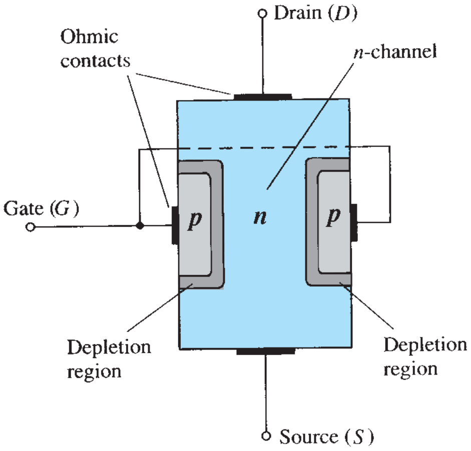


FIG. 6.3

Junction field-effect transistor (JFET).

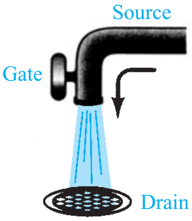


FIG. 6.4

Water analogy for the JFET control mechanism.

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 6.4 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The “gate,” through an applied signal (potential), controls the flow of water (charge) to the “drain.” The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 6.3 because the terminology is defined for electron flow.

V_{GS} = 0 V, V_{DS} Some Positive Value

In Fig. 6.5, a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 6.3. The instant the voltage V_{DD} $(=V_{DS})$ is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in Fig. 6.5, the flow of charge is relatively uninhibited and is limited solely by the resistance of the *n*-channel between drain and source.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 6.6. Assuming a uniform resistance in the *n*-channel, we can break down

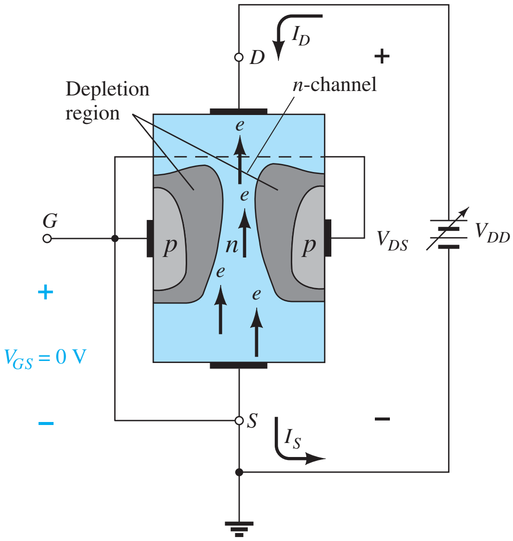


FIG. 6.5

JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

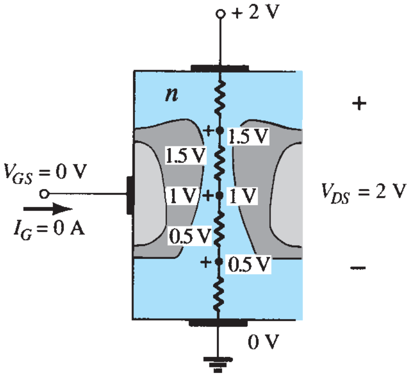


FIG. 6.6

Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

the resistance of the channel into the divisions appearing in Fig. 6.6. The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider is the depletion region—hence the distribution of the depletion region as shown in Fig. 6.6. The fact that the *p–n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes, as shown in the same figure. The fact that $I_G = 0$ A is an important characteristic of the JFET.

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 6.7. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 6.7, the depletion regions of Fig. 6.5 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 6.7 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would

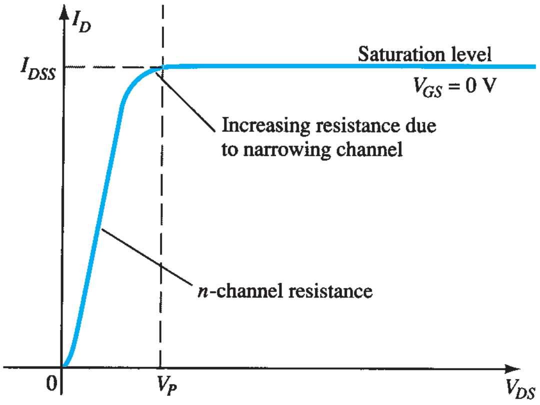


FIG. 6.7

I_D versus V_{DS} for $V_{GS} = 0$ V.

"touch" as shown in Fig. 6.8, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P, as shown in Fig. 6.7. In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 6.7, however, this is hardly the case— I_D maintains a saturation level defined as I_{DSS} in Fig. 6.7. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 6.7 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p–n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

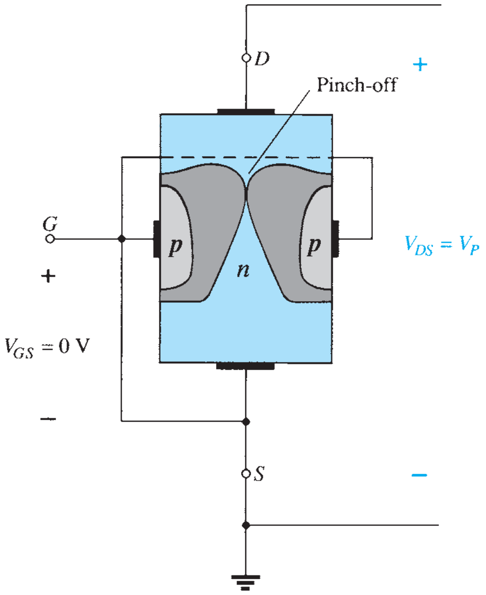


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

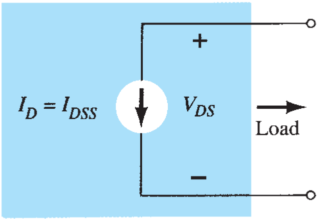


FIG. 6.9
Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. As shown in Fig. 6.9, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the *d*rain-to-*s*ource current with a *s*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.

Note in Fig. 6.7 that $V_{GS} = 0$ V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig. 6.7 are affected by changes in the level of V_{GS}.

$V_{GS} < 0$ V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

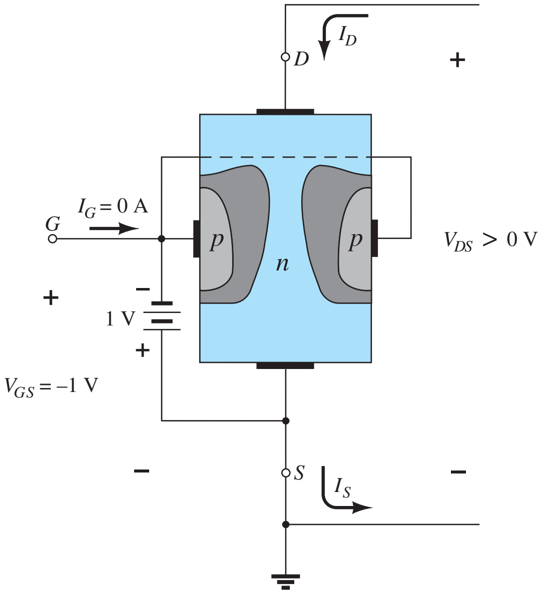


FIG. 6.10
Application of a negative voltage to the gate of a JFET.

In Fig. 6.10 a negative voltage of -1 V is applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V, but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in Fig. 6.11 for $V_{GS} = -1$ V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also in Fig. 6.11 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

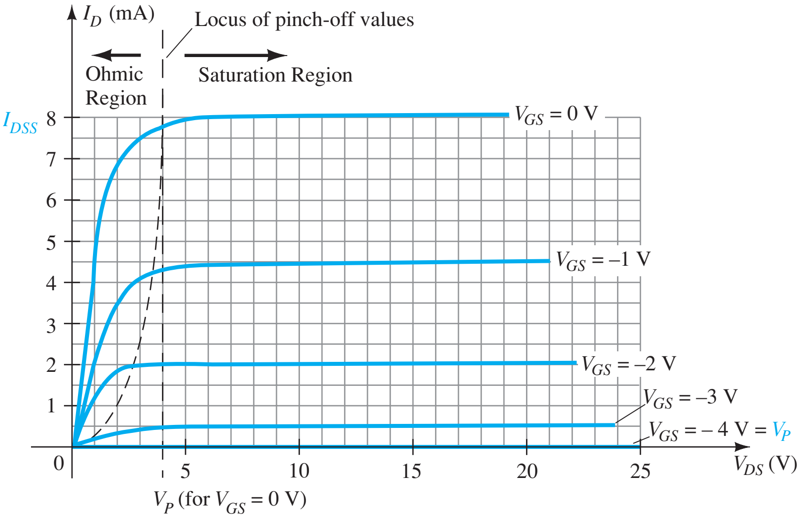


FIG. 6.11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

On most specification sheets the pinch-off voltage is specified as $V_{GS(\text{off})}$ rather than V_P. A specification sheet will be reviewed later in the chapter when the majority of the controlling elements have been introduced. The region to the right of the pinch-off locus of Fig. 6.11 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 6.11 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ are a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding to an increasing resistance level. The following equation provides a good first approximation to the resistance level in terms of the applied voltage V_{GS}:

$$\boxed{r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}} \qquad \textbf{(6.1)}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d is the resistance at a particular level of V_{GS}.

For an n-channel JFET with $r_o = 10\ \text{k}\Omega$ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (6.1) results in 40 kΩ at $V_{GS} = -3$ V.

p-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 6.3 but with a reversal of the *p*- and *n*-type materials as shown in Fig. 6.12. The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.13, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

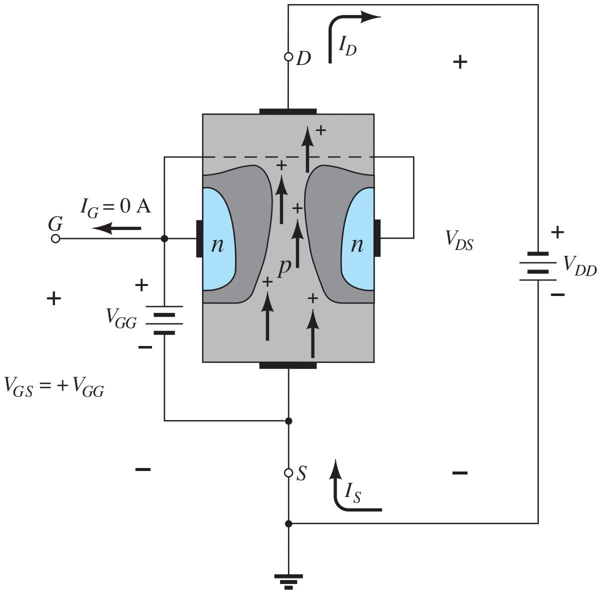


FIG. 6.12
p-Channel JFET.

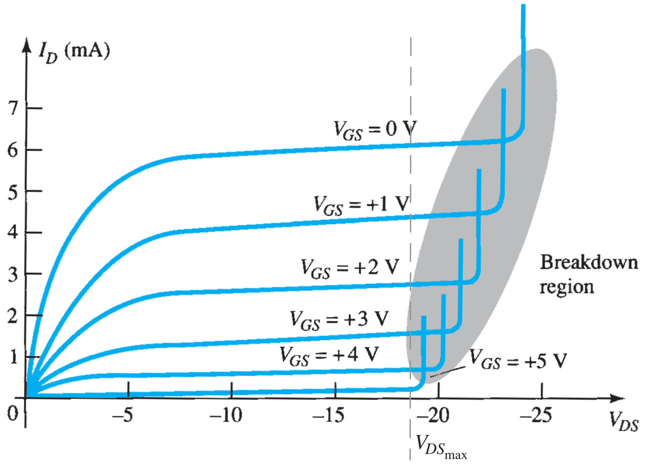


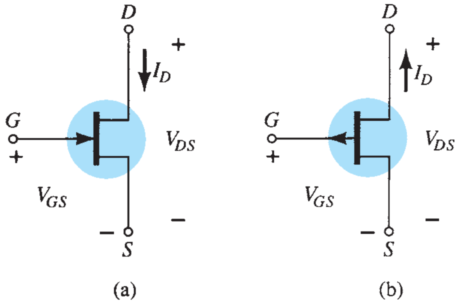
FIG. 6.13

p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 6.11 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS_{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 6.14. Note that the arrow is pointing in for the *n*-channel device of Fig. 6.14a to represent the direction in which I_G would flow if the *p–n* junction were forward-biased. For the *p*-channel device (Fig. 6.14b) the only difference in the symbol is the direction of the arrow in the symbol.



(a) (b)

FIG. 6.14

JFET symbols: (a) n-channel; (b) p-channel.

Summary

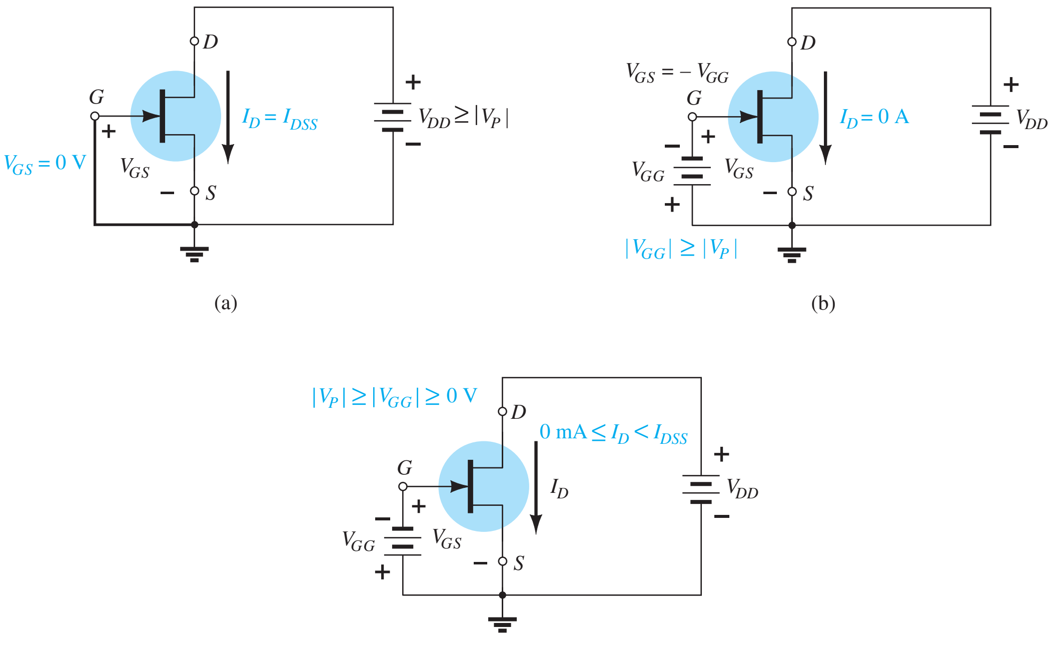
A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n*-channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$, as shown in Fig. 6.15a.

For gate-to-source voltages V_{GS} is less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A), as in Fig. 6.15b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as in Fig. 6.15c.

A similar list can be developed for p-channel JFETs.



(a) (b) (c)

FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

6.3 TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,

$$\boxed{I_C = f(I_B) = \underset{\text{constant}}{\beta}\overset{\text{control variable}}{I_B}} \tag{6.2}$$

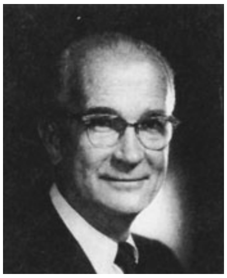
In Eq. (6.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):

$$\boxed{I_D = \underset{\text{constants}}{I_{DSS}}\left(1 - \frac{\overset{\text{control variable}}{V_{GS}}}{\underset{\text{constants}}{V_P}}\right)^2} \tag{6.3}$$

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

For the dc analysis to be performed in Chapter 7, a graphical rather than a mathematical approach will in general be more direct and easier to apply. The graphical approach, however, will require a plot of Eq. (6.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed.



William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of the transistor and the FET.

Shockley	Born: London, England; PhD, Harvard, 1936; Head, Transistor Physics Department, Bell Laboratories; President, Shockley Transistor Corp.; Poniatoff Professor of Engineering Science, Stanford University; Nobel Prize in physics in 1956 with Walter Brattain and John Bardeen

FIG. 6.16

Dr. William Bradford Shockley.
(Courtesy of AT&T Archives and History Center.)

The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (6.3) is unaffected. In general, therefore:

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 6.11. In Fig. 6.17 two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS}, whereas the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, we can draw a horizontal line from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.

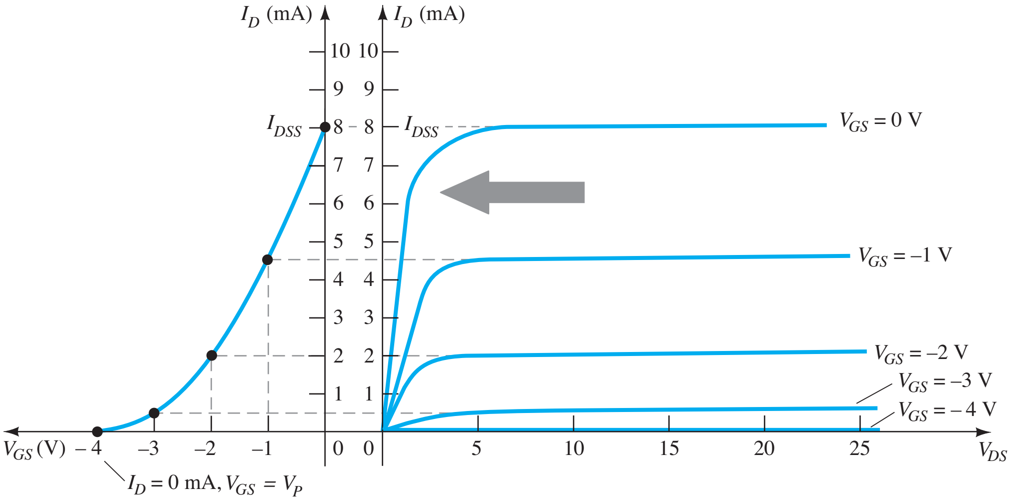


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

In review:

$$\boxed{\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS}} \qquad \textbf{(6.4)}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA}} \qquad \textbf{(6.5)}$$

Before continuing, it is important to realize that the drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 6.17. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 6.17 decreases noticeably as V_{GS} becomes more and more negative. Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

If a horizontal line is drawn from the $V_{GS} = -1$ V curve to the I_D axis and then extended to the other axis, another point on the transfer curve can be located. Note that $V_{GS} = -1$ V on the bottom axis of the transfer curve with $I_D = 4.5$ mA. Note in the definition of I_D at $V_{GS} = 0$ V and -1 V that the saturation levels of I_D are employed and the ohmic region ignored. Continuing with $V_{GS} = -2$ V and -3 V, we can complete the transfer curve. It is the transfer curve of I_D versus V_{GS} that will receive extended use in the analysis of Chapter 7 and not the drain characteristics of Fig. 6.17. The next few paragraphs will introduce a quick, efficient method of plotting I_D versus V_{GS} given only the levels of I_{DSS} and V_P and Shockley's equation.

Applying Shockley's Equation

The transfer curve of Fig. 6.17 can also be obtained directly from Shockley's equation (6.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (6.3) as a source of the transfer curve of Fig. 6.17 is best demonstrated by examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (6.3):}\quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}\,|_{V_{GS}=0\text{ V}}} \tag{6.6}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$

$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0\text{ A}\,|_{V_{GS}=V_P}} \tag{6.7}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}\,(0.75)^2$$

$$= 8\text{ mA}\,(0.5625)$$

$$= \mathbf{4.5\ mA}$$

as shown in Fig. 6.17. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets), the level of I_D can be found for any level of V_{GS}. Conversely, by using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)} \tag{6.8}$$

Let us test Eq. (6.8) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$V_{GS} = -4\text{ V}\left(1 - \sqrt{\frac{4.5\text{ mA}}{8\text{ mA}}}\right)$$

$$= -4\text{ V}(1 - \sqrt{0.5625}) = -4\text{ V}(1 - 0.75)$$

$$= -4\text{ V}(0.25)$$

$$= \mathbf{-1\ V}$$

as substituted in the above calculation and verified by Fig. 6.17.

Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (6.3) is such that specific levels of V_{GS} will result in levels of I_D that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2 \\ &= I_{DSS}(0.25) \end{aligned}$$

and

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}} \tag{6.9}$$

Now it is important to realize that Eq. (6.9) is not for a particular level of V_P. It is a general equation for any level of V_P as long as $V_{GS} = V_P/2$. The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of I_D for $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$ in Fig. 6.17.

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$\begin{aligned} V_{GS} &= V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \\ &= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293) \end{aligned}$$

and

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}} \tag{6.10}$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 6.1. In fact, in the analysis of Chapter 7, a maximum of four plot points are used to sketch the transfer curves. On most occasions using just the plot point defined by $V_{GS} = V_P/2$ and the axis intersections at I_{DSS} and V_P will provide a curve accurate enough for most calculations.

TABLE 6.1

V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\ mA} \quad \text{and} \quad V_{GS} = \mathbf{0\ V}$$

and

$$I_D = \mathbf{0\ mA} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\ V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\ mA}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\ V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

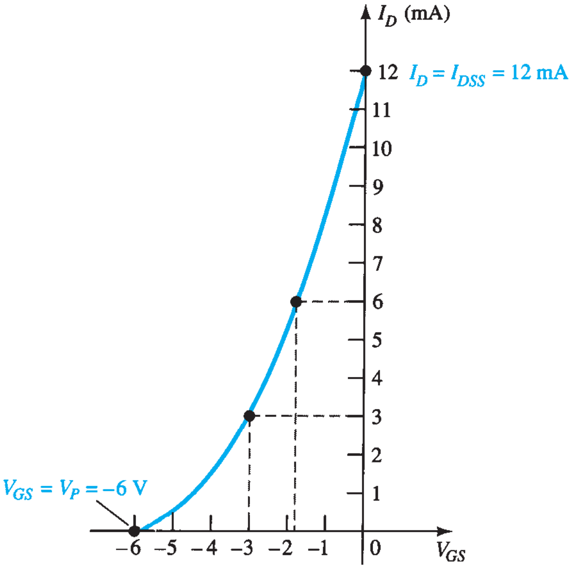


FIG. 6.18

Transfer curve for Example 6.1.

For *p*-channel devices Shockley's equation (6.3) can still be applied exactly as it appears. In this case, both V_P and V_{GS} will be positive and the curve will be the mirror image of the transfer curve obtained with an *n*-channel and the same limiting values.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

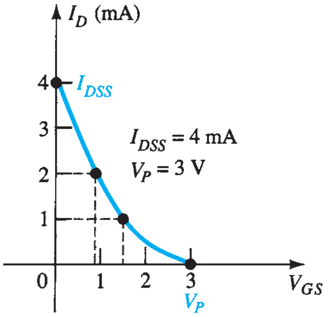


FIG. 6.19

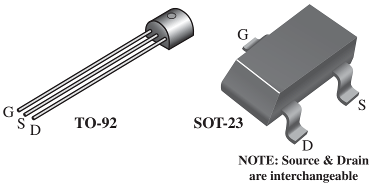
Transfer curve for the p-channel device of Example 6.2.

6.4 SPECIFICATION SHEETS (JFETs)

As with any electronic device it is important to be able to understand the data provided on a specification sheet. Often times the notation used is different than we normally apply so a measure of translation may have to be applied. In general, however, the headings for the data are uniform and include **Maximum Ratings, Thermal Characteristics, Electrical Characteristics**, and sets of **Typical Characteristics**. In Fig. 6.20 the specification sheets for a Fairchild Semiconductor 2N5457 *n*-channel JFET appears with two types of packaging techniques. The TO-92 package is for a higher power device than the surface mount SOT-23 unit.

FAIRCHILD
SEMICONDUCTOR ™

2N5457 **MMBF5457**



N-Channel General Purpose Amplifier
This device is a low-level audio amplifier and switching transistor, and can be used for analog switching applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	25	V
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	–25	V
I_{GF}	Forward Gate Current	10	mA
T_j, T_{stg}	Operating and Storage Junction Temperature Range	–55 to +150	°C

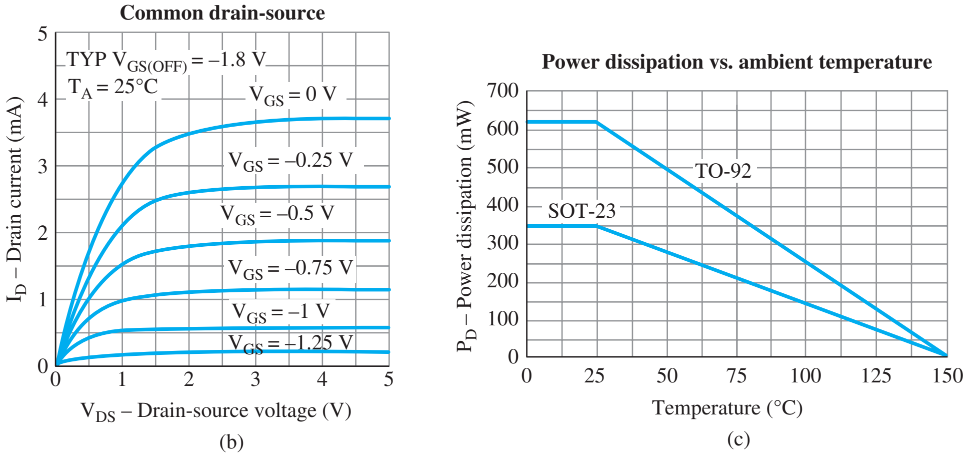
THERMAL CHARACTERISTICS

Symbol	Characteristic	Max		Units
		2N5457	*MMBF5457	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise noted

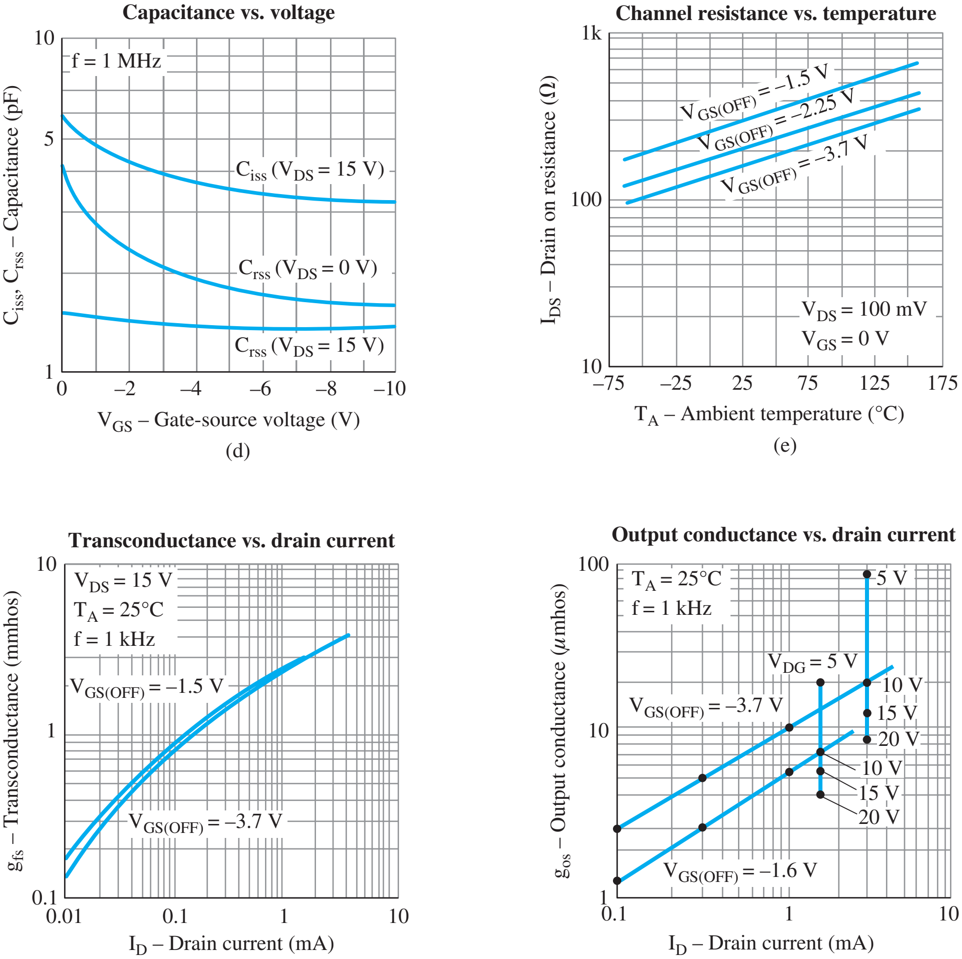
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10\ \mu A$, $V_{DS} = 0$	–25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$ $V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$			–1.0 –200	nA nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA 5457	–0.5		–6.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 100\ \mu A$ 5457		–2.5		V
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate Voltage Drain Current	$V_{DS} = 15$ V, $V_{GS} = 0$ 5457	1.0	3.0	5.0	mA
SMALL SIGNAL CHARACTERISTICS						
g_{fs}	Forward Transfer Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz 5457	1000		5000	μmhos
g_{os}	Output Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz		10	50	μmhos
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz		4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz		1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_G = 1.0$ megohm, BW = 1.0 Hz			3.0	dB

(a)



(b) (c)

FIG. 6.20
n-channel 2N5457 JFET Characteristic k.



(d) (e)

(f) (g)

FIG. 6.20
Continued

Maximum Ratings

The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device. The specified maximum levels for V_{DS}, V_{DG} and V_{GS} must not be exceeded at any point in the design operation of the device. Any good design will try to avoid these levels by a good margin of safety. Although normally designed to operate with $I_G = 0$ mA, if *forced* to accept a gate current, it could withstand 10 mA (I_{GF}) before damage would occur.

Thermal Characteristics

The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$\boxed{P_D = V_{DS} I_D} \qquad \textbf{(6.11)}$$

Note the similarity in format with the maximum power dissipation equation for the BJT transistor.

The derating factor is discussed in detail in Chapter 3, but for the moment recognize that the 5 mW/°C rating reveals that the dissipation rating *decreases* by 5 mW for each *increase* in temperature of 1°C above 25°C.

Electrical Characteristics

The electrical characteristics include the level of V_P in the "off" characteristics and I_{DSS} in the "on" characteristics. In this case $V_P = V_{GS(\text{off})}$ has a range from −0.5 V to −6.0 V and I_{DSS} from 1 mA to 5 mA. The fact that both will vary from device to device with the same nameplate identification must be considered in the design process. The small-signal characteristics will become important when we examine ac networks in Chapter 8.

Typical Characteristics

The Typical Characteristics listing will include a variety of curves demonstrating how important parameters vary with voltage, current, temperature, and frequency.

First note in Fig. 6.20a that the plot includes the negative region of V_{GS} on the normally positive side of the horizontal axis. Notice also that the plot is for a pinch-off voltage of −2.6 V, which is about halfway between the range of possible pinch-off voltages. If this is the only plot provided it acts like an average value between limits. The Common-Drain characteristics are provided in Fig. 6.20b for a pinch-off voltage of −1.8 V. Note how the drain current drops to 0 ampere when this pinch-off voltage is applied. Also note that the I_{DSS} level is only about 3.75 mA for this pinch-off voltage, whereas it was about 9.5 mA for a pinch-off of −2.6 V in Fig. 6.20a. The Power Dissipation versus Ambient temperature is plotted in Fig. 6.20c, clearly showing the dramatic drop in power handling capability with temperature. At the boiling point of water (100°C) it is only 250 mW compared with 650 mW at room temperature. Capacitive effects in Fig. 6.20d will become very important at high frequencies because of the resulting reactance and the effect on speed of operation. It is interesting to note that the more negative the gate-to-source voltage, the less the capacitive effects at a frequency of 1 MHz. The Channel Resistance plot of Fig. 6.20e demonstrates how the channel resistance changes with temperature at various levels of $V_{GS(\text{OFF})}$. At first glance the change may not appear that dramatic, but take note of the fact that the vertical axis is a log scale extending from 10 Ω to 1 kΩ. The plots of Transconductance (Fig. 6.20f) and Output Conductance (Fig. 6.20g) will become important when we consider JFET ac networks. They define the two parameters of the ac equivalent circuit. Each is certainly affected by the level of drain current with lesser sensitivity to the pinch-off voltage.

Operating Region

The specification sheet and the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in Fig. 6.21. The ohmic region defines the minimum permissible values of V_{DS} at each level of V_{GS}, and $V_{DS_{\max}}$ specifies the maximum value for this parameter. The saturation

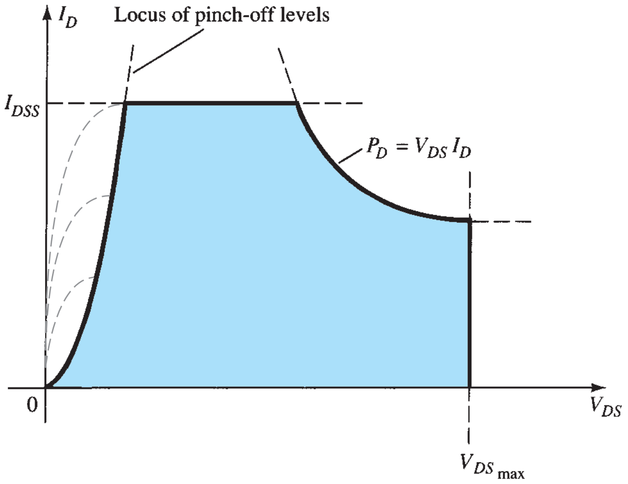


FIG. 6.21
Normal operating region for linear amplifier design.

current I_{DSS} is the maximum drain current, and the maximum power dissipation level defines the curve drawn in the same manner as described for BJT transistors. The resulting shaded region is the normal operating region for amplifier design.

6.5 INSTRUMENTATION

Recall from Chapter 3 that hand-held instruments are available to measure the level of β_{dc} for the BJT transistor. Similar instrumentation is not available to measure the levels of I_{DSS} and V_P. However, the curve tracer introduced for the BJT transistor can also display the drain characteristics of the JFET transistor through a proper setting of the various controls. The vertical scale (in milliamperes) and the horizontal scale (in volts) have been set to provide a full display of the characteristics, as shown in Fig. 6.22. For the JFET of Fig. 6.22, each vertical division (in centimeters) reflects a 1-mA change in I_D, whereas each horizontal division has a value of 1 V. The step voltage is 500 mV/step (0.5 V/step), revealing that the top curve is defined by $V_{GS} = 0$ V and the next curve down is -0.5 V for the n-channel device. Using the same step voltage, we see the next curve is -1 V, then -1.5 V, and finally -2 V. By drawing a line from the top curve over to the I_D axis, we can estimate the level of I_{DSS} to be about 9 mA. The level of V_P can be estimated by noting the V_{GS} value of the bottom curve and taking into account the shrinking distance between curves as V_{GS} becomes more and more negative. In this case, V_P is certainly more negative than -2 V, and perhaps V_P is close to -2.5 V. However, keep in mind that the V_{GS} curves contract very quickly as they approach the cutoff condition, and perhaps $V_P = -3$ V is a better choice. It should also be noted that the step control is set for a five-step display, limiting the displayed curves to $V_{GS} = 0, -0.5, -1, -1.5$, and -2 V. If the step control had been increased to 10, the voltage per step could be reduced to 250 mV $= 0.25$ V and the curve for $V_{GS} = -2.25$ V would have been included as well as an additional curve between each step of Fig. 6.22. The $V_{GS} = -2.25$ V curve would reveal how quickly the curves are closing in on each other for the same step voltage. Fortunately, the level of V_P can be estimated to a reasonable degree of accuracy simply by applying a condition appearing

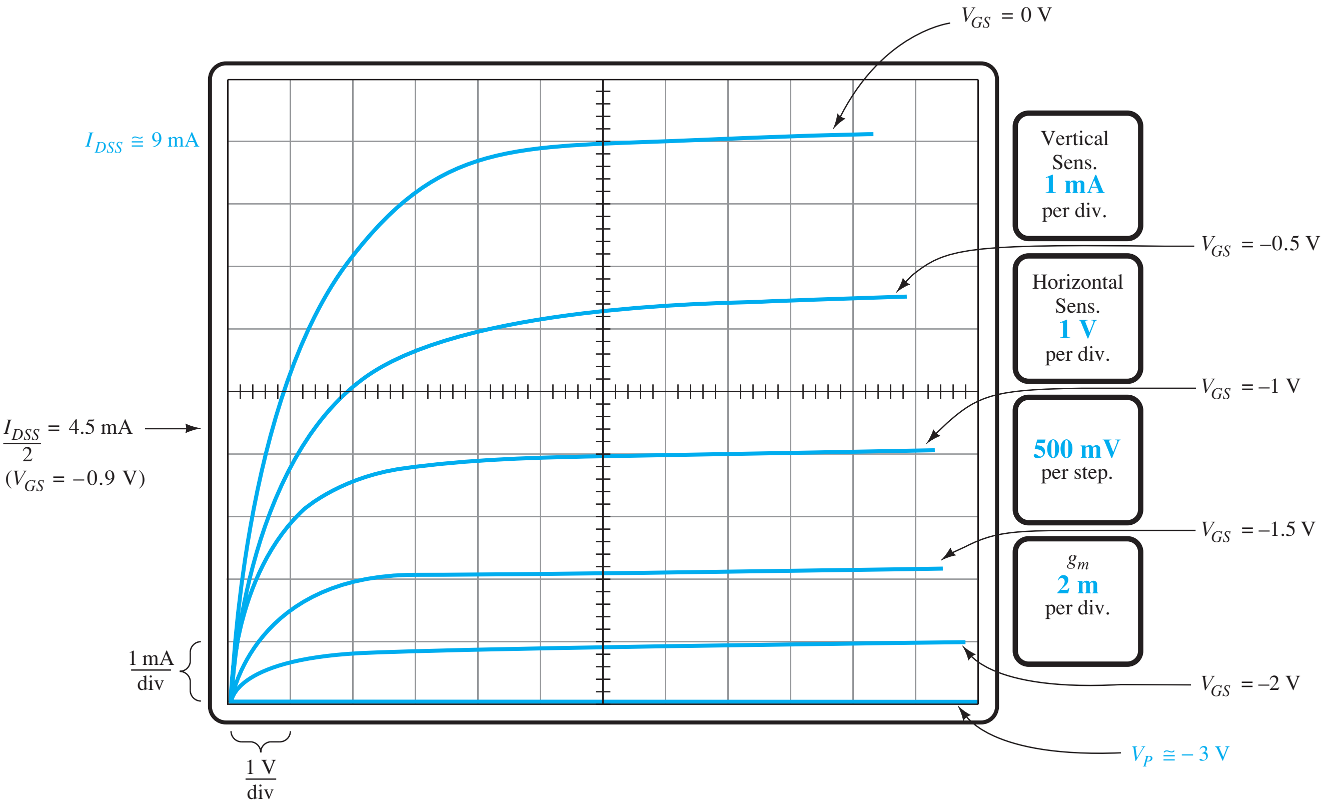


FIG. 6.22

Drain characteristics for a 2N4416 JFET transistor as displayed on a curve tracer.

in Table 6.1. That is, when $I_D = I_{DSS}/2$, then $V_{GS} = 0.3V_P$. For the characteristics of Fig. 6.22, $I_D = I_{DSS}/2 = 9\text{ mA}/2 = 4.5\text{ mA}$, and, as visible from Fig. 6.22, the corresponding level of V_{GS} is about -0.9 V. Using this information, we find that $V_P = V_{GS}/0.3 = -0.9\text{ V}/0.3 = -3\text{ V}$, which will be our choice for this device. Using this value, we find that at $V_{GS} = -2$ V,

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= 9\text{ mA}\left(1 - \frac{-2\text{ V}}{-3\text{ V}}\right)^2 \\ &\cong 1\text{ mA} \end{aligned}$$

as supported by Fig. 6.22.

At $V_{GS} = -2.5$ V, Shockley's equation results in $I_D = 0.25$ mA, with $V_P = -3$ V, clearly revealing how quickly the curves contract near V_P. The importance of the parameter g_m and how it is determined from the characteristics of Fig. 6.22 are described in Chapter 8 when small-signal ac conditions are examined.

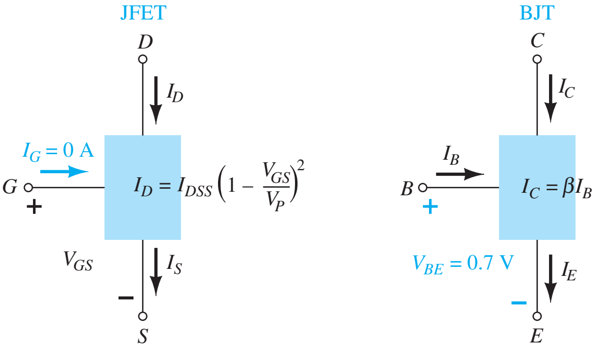
6.6 IMPORTANT RELATIONSHIPS

A number of important equations and operating characteristics for the JFET have been introduced that are of particular importance for the analysis of dc and ac configurations that will follow. To isolate and emphasize their importance, they are repeated in Table 6.2 next to corresponding equations for the BJT transistor. The JFET equations are defined for the configuration of Fig. 6.23a, whereas the BJT equations relate to Fig. 6.23b.

TABLE 6.2

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\text{ A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\text{ V}$

(6.12)



(a) (b)

FIG. 6.23
(a) JFET versus (b) BJT.

A clear understanding of the effect of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that $V_{BE} = 0.7$ V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}. The number of similarities between the analysis of BJT and JFET dc configurations will become quite apparent in Chapter 7.

6.7 DEPLETION-TYPE MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal–*o*xide–*s*emiconductor *f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at I_{DSS}, and also has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 6.24. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that in Fig. 6.24. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric*, which sets up opposing (as indicated by the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

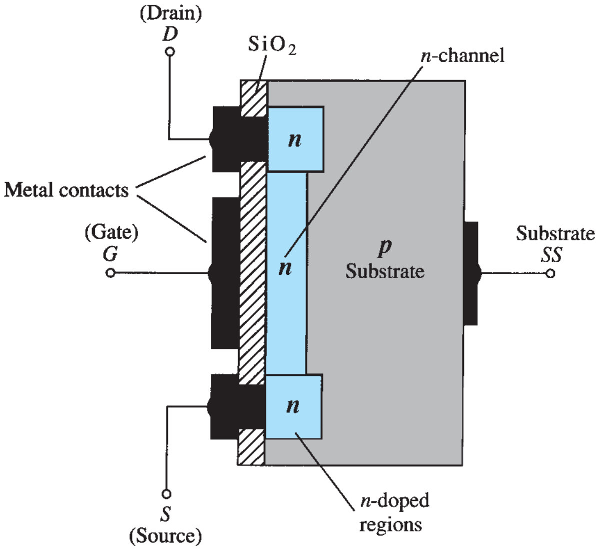


FIG. 6.24
n-Channel depletion-type MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is usually more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. Because of the very high input impedance, the gate current I_G is essentially 0 A for dc-biased configurations.

The reason for the label metal–oxide–semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections; *oxide* for the silicon dioxide insulating layer; and *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and the channel has resulted in another name for the device: *insulated-gate FET*, or *IGFET*, although this label is used less and less in the literature.

Basic Operation and Characteristics

In Fig. 6.25 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the *n*-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 6.26.

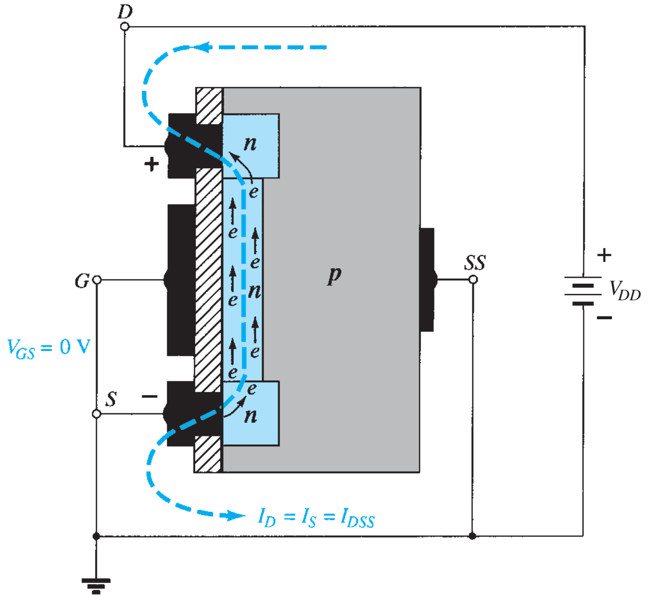


FIG. 6.25
n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

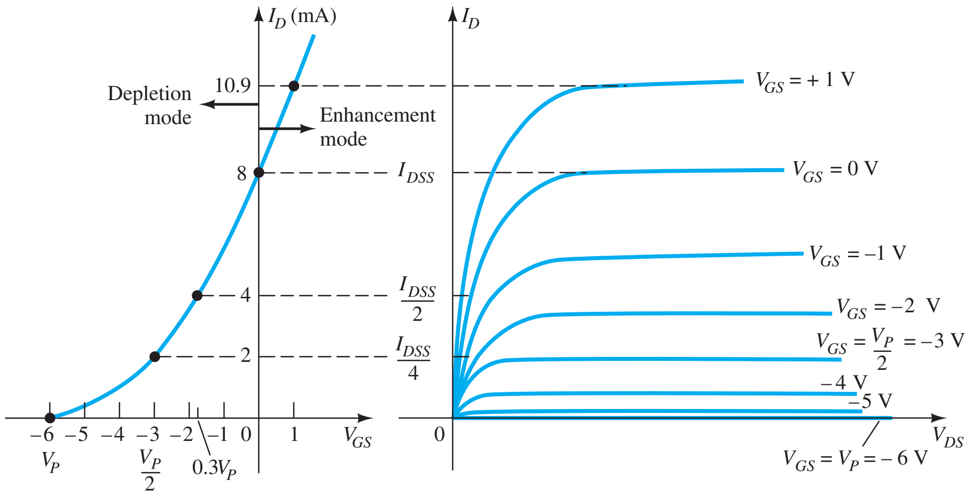


FIG. 6.26
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. 6.27, V_{GS} is set at a negative voltage such as −1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 6.27. Depending on the

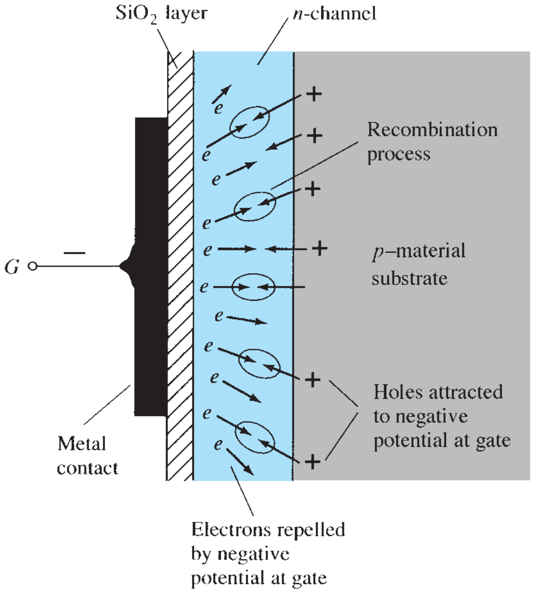

SiO_2 layer
n-channel
Recombination process
p–material substrate
Holes attracted to negative potential at gate
G
−
Metal contact
Electrons repelled by negative potential at gate
e
+

FIG. 6.27

Reduction in free carriers in a channel due to a negative potential at the gate terminal.

magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 6.26 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.26 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 6.26 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 6.26, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 6.3 Sketch the transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution:

$$\text{At } V_{GS} = 0\text{ V}, \qquad I_D = I_{DSS} = 10\text{ mA}$$

$$V_{GS} = V_P = -4\text{ V}, \qquad I_D = 0\text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \qquad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

all of which appear in Fig. 6.28.

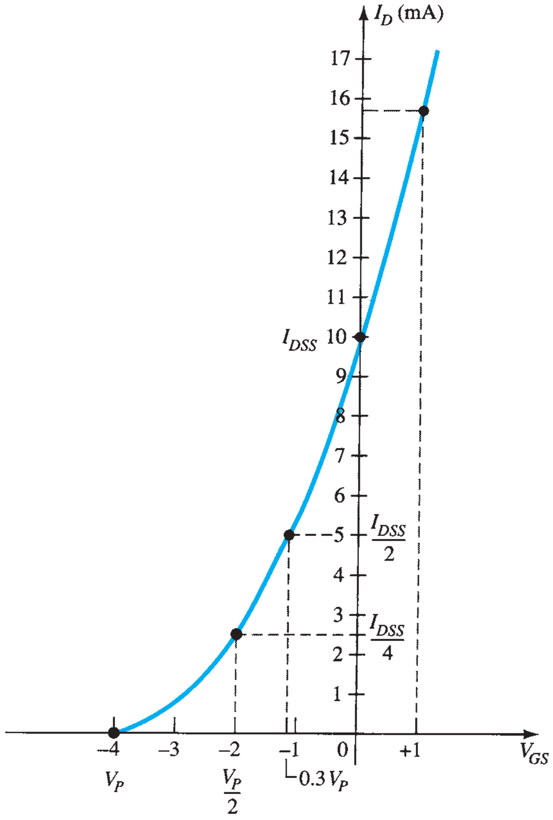


FIG. 6.28

Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625) \\ &\cong 15.63\text{ mA} \end{aligned}$$

which is sufficiently high to finish the plot.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 6.24. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 6.29a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 6.26, but with V_{DS} having negative values, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 6.29c. The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 6.29b. In other words,

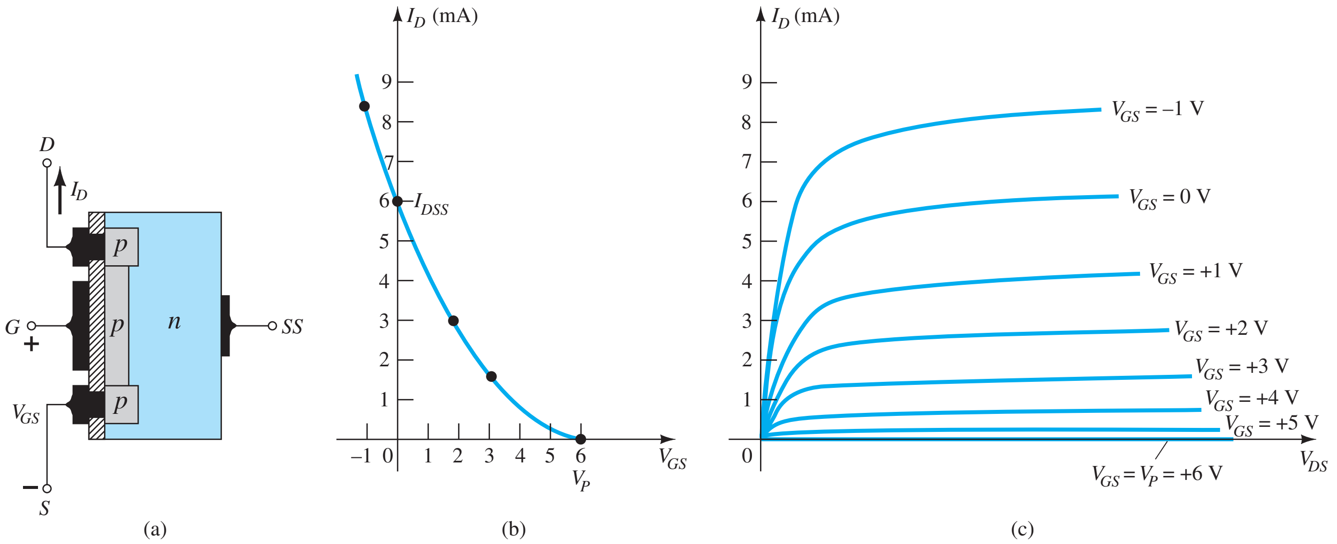


FIG. 6.29

p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

the drain current will increase from cutoff at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 6.30. Note how the symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and the source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not. For most of the analysis to follow in Chapter 7, the substrate and the source will be connected and the lower symbols will be employed.

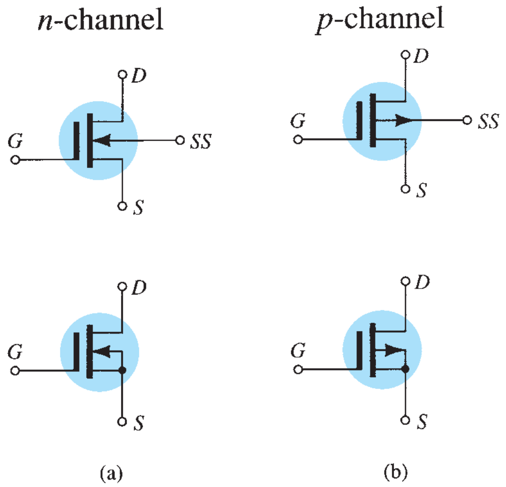
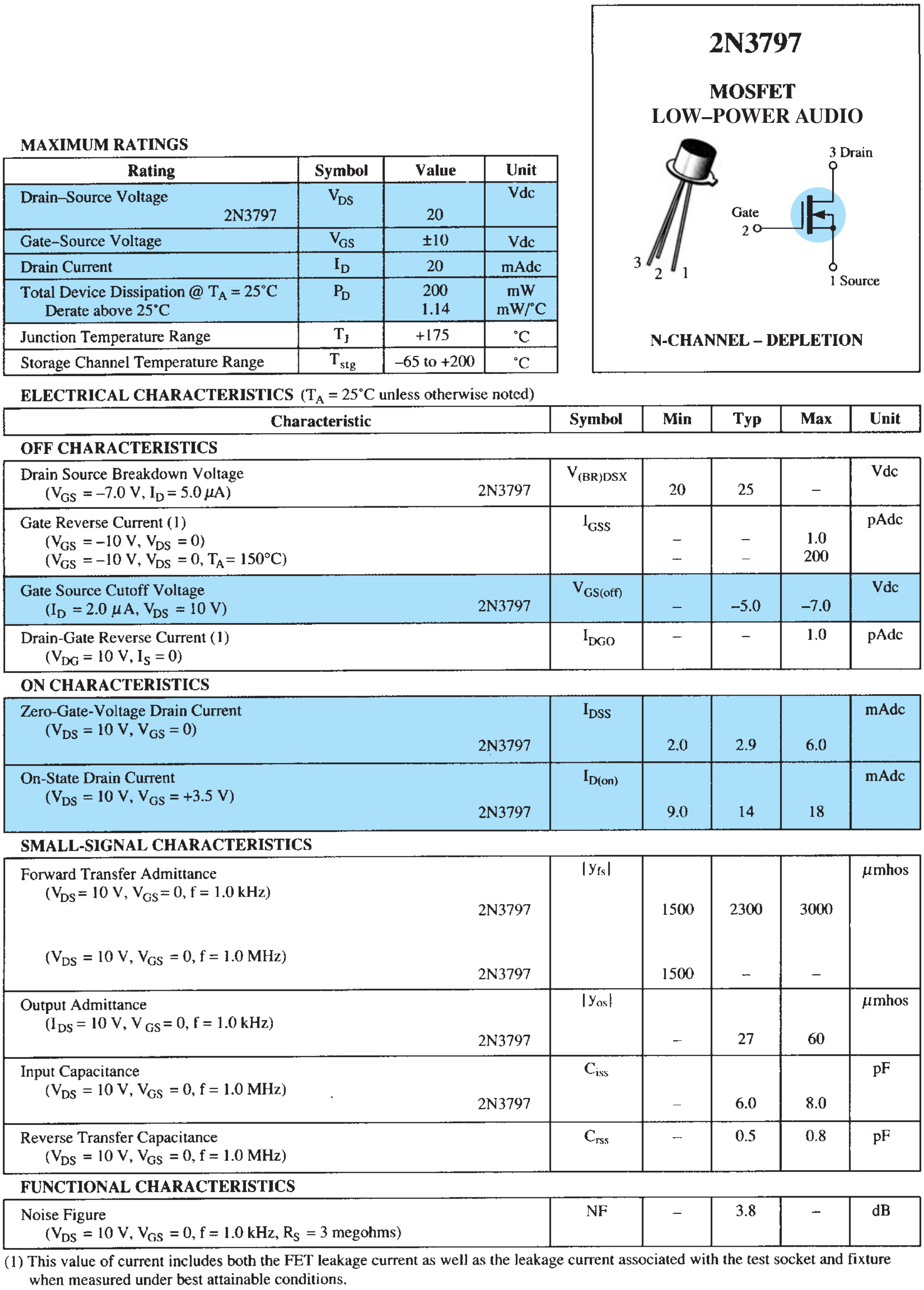


FIG. 6.30

Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

The device appearing in Fig. 6.31 has three terminals, with the terminal identification appearing in the same figure. The specification sheet for a depletion-type MOSFET is similar to that of a JFET. The levels of V_P and I_{DSS} are provided along with a list of maximum values and typical "on" and "off" characteristics. In addition, however, since I_D can extend beyond the I_{DSS} level, another point is normally provided that reflects a typical value of I_D for some positive voltage (for an *n*-channel device). For the unit of Fig. 6.31, I_D is specified as $I_{D(\text{on})} = 9$ mA dc, with $V_{DS} = 10$ V and $V_{GS} = 3.5$ V.


3 Drain
Gate
2
3
2
1
1 Source

2N3797

MOSFET
LOW–POWER AUDIO

N-CHANNEL – DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	–65 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain Source Breakdown Voltage ($V_{GS} = -7.0$ V, $I_D = 5.0\ \mu A$) 2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) ($V_{GS} = -10$ V, $V_{DS} = 0$) ($V_{GS} = -10$ V, $V_{DS} = 0$, $T_A = 150°C$)	I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0\ \mu A$, $V_{DS} = 10$ V) 2N3797	$V_{GS(off)}$	–	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10$ V, $I_S = 0$)	I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) 2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10$ V, $V_{GS} = +3.5$ V) 2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz) 2N3797 ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz) 2N3797	$\lvert y_{fs} \rvert$	1500 1500	2300 –	3000 –	µmhos
Output Admittance ($I_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz) 2N3797	$\lvert y_{os} \rvert$	–	27	60	µmhos
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz) 2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz, R_S = 3 megohms)	NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

FIG. 6.31

2N3797 Motorola n-channel depletion-type MOSFET.

6.8 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 6.32. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labeled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 6.32 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

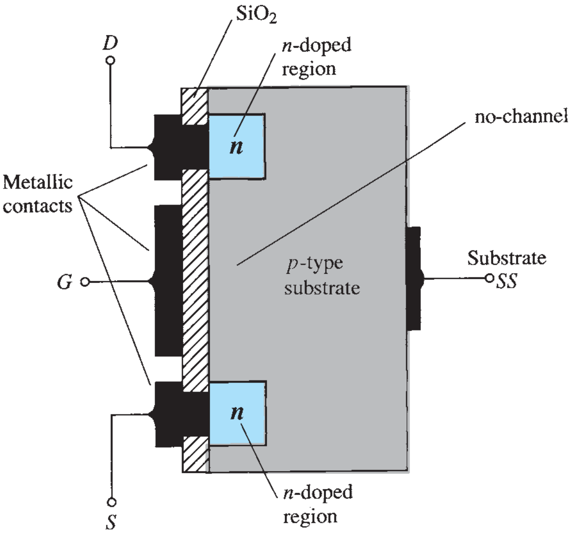


FIG. 6.32
n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of Fig. 6.32, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p–n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 6.33, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.

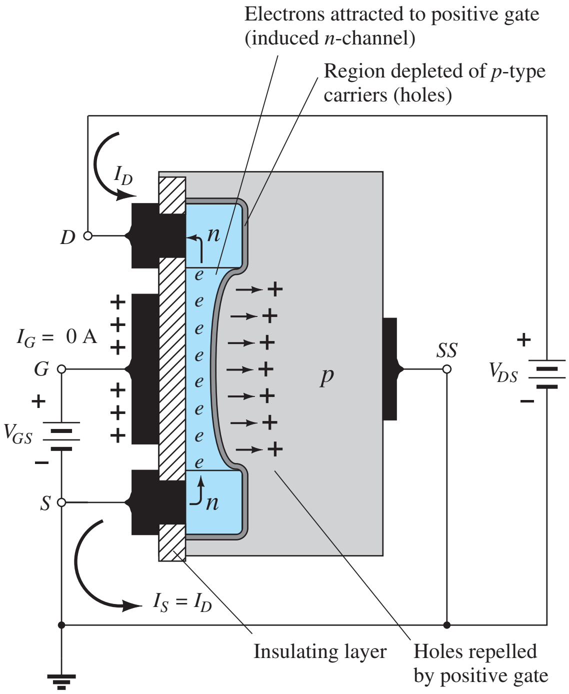

Electrons attracted to positive gate (induced n-channel)
Region depleted of p-type carriers (holes)
I_D
D
n
e
I_G = 0 A
G
V_{GS}
S
n
p
SS
V_{DS}
$I_S = I_D$
Insulating layer
Holes repelled by positive gate

FIG. 6.33
Channel formation in the n-channel enhancement-type MOSFET.

The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(\text{Th})}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.34. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 6.34, we find that

$$\boxed{V_{DG} = V_{DS} - V_{GS}} \tag{6.13}$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 V to 5 V, the voltage V_{DG} [by Eq. (6.13)] will increase from -6 V to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described

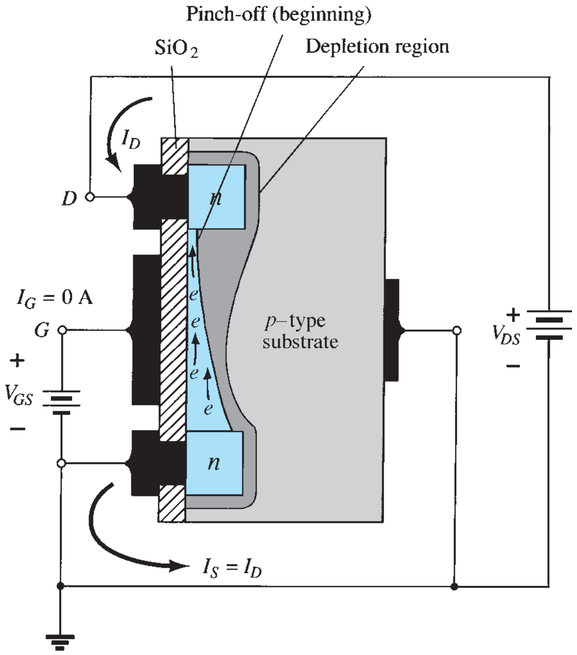


FIG. 6.34

Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

earlier for the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$\boxed{V_{DS_{\text{sat}}} = V_{GS} - V_T} \qquad \textbf{(6.14)}$$

Obviously, therefore, for a fixed value of V_T, the higher the level of V_{GS}, the greater is the saturation level for V_{DS}, as shown in Fig. 6.34 by the locus of saturation levels.

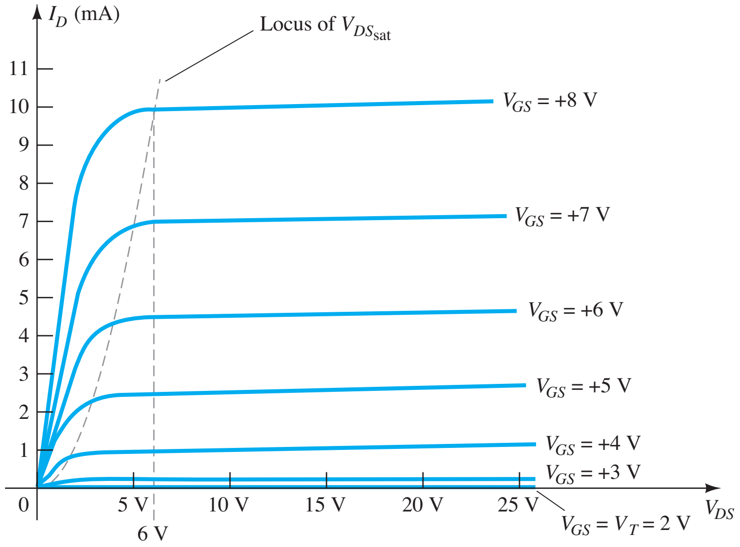


FIG. 6.35

Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V².

For the characteristics of Fig. 6.34, the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 6.35 clearly reveals that as the level of V_{GS} increases from V_T to 8 V, the resulting saturation level for I_D also increases from a level of 0 mA to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increases as the magnitude of V_{GS} increases, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{6.15}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (6.15)], where $I_{D(\text{on})}$ and $V_{GS(\text{on})}$ are the values for each at a particular point on the characteristics of the device.

$$\boxed{k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}} \tag{6.16}$$

Substituting $I_{D(\text{on})} = 10$ mA when $V_{GS(\text{on})} = 8$ V from the characteristics of Fig. 6.35 yields

$$\begin{aligned} k &= \frac{10\text{ mA}}{(8\text{ V} - 2\text{ V})^2} = \frac{10\text{ mA}}{(6\text{ V})^2} = \frac{10\text{ mA}}{36\text{ V}^2} \\ &= \mathbf{0.278 \times 10^{-3}\ A/V^2} \end{aligned}$$

and a general equation for I_D for the characteristics of Fig. 6.35 results in

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2\text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$\begin{aligned} I_D &= 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2 \\ &= 0.278 \times 10^{-3}(4) = \mathbf{1.11\ mA} \end{aligned}$$

as verified by Fig. 6.35. At $V_{GS} = V_T$, the squared term is 0, and $I_D = 0$ mA.

For the dc analysis of enhancement-type MOSFETs to appear in Chapter 7, the transfer characteristics will again be the characteristics to be employed in the graphical solution. In Fig. 6.36, the drain and transfer characteristics have been set side by side to describe the

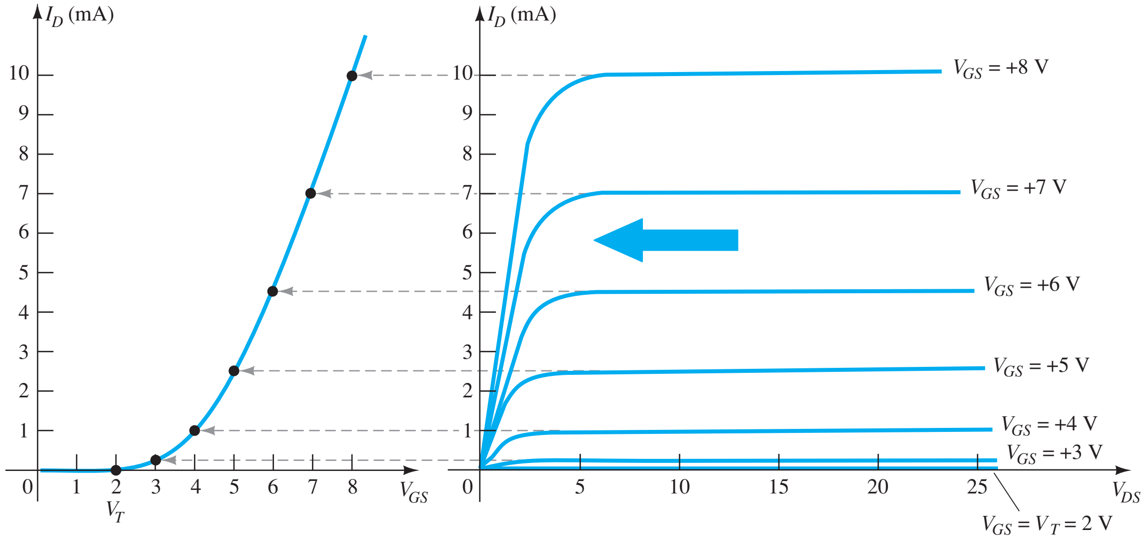


FIG. 6.36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. As V_{GS} is increased beyond V_T, the drain current I_D will begin to flow at an increasing rate in accordance with Eq. (6.15). Note that in defining the points on the transfer characteristics from the drain characteristics, only the saturation levels are employed, thereby limiting the region of operation to levels of V_{DS} greater than the saturation levels as defined by Eq. (6.14).

The transfer curve of Fig. 6.36 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive V_{GS} region and does not rise until $V_{GS} = V_T$. The question now surfaces as to how to plot the transfer characteristics given the levels of *k* and V_T as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$

First, a horizontal line is drawn at $I_D = 0$ mA from $V_{GS} = 0$ V to $V_{GS} = 4$ V as shown in Fig. 6.37a. Next, a level of V_{GS} greater than V_T such as 5 V is chosen and substituted into Eq. (6.15) to determine the resulting level of I_D as follows:

$$\begin{aligned} I_D &= 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2 \\ &= 0.5 \times 10^{-3}(5\text{ V} - 4\text{ V})^2 = 0.5 \times 10^{-3}(1)^2 \\ &= \mathbf{0.5\text{ mA}} \end{aligned}$$

and a point on the plot is obtained as shown in Fig. 6.37b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6$, 7, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 6.37c.

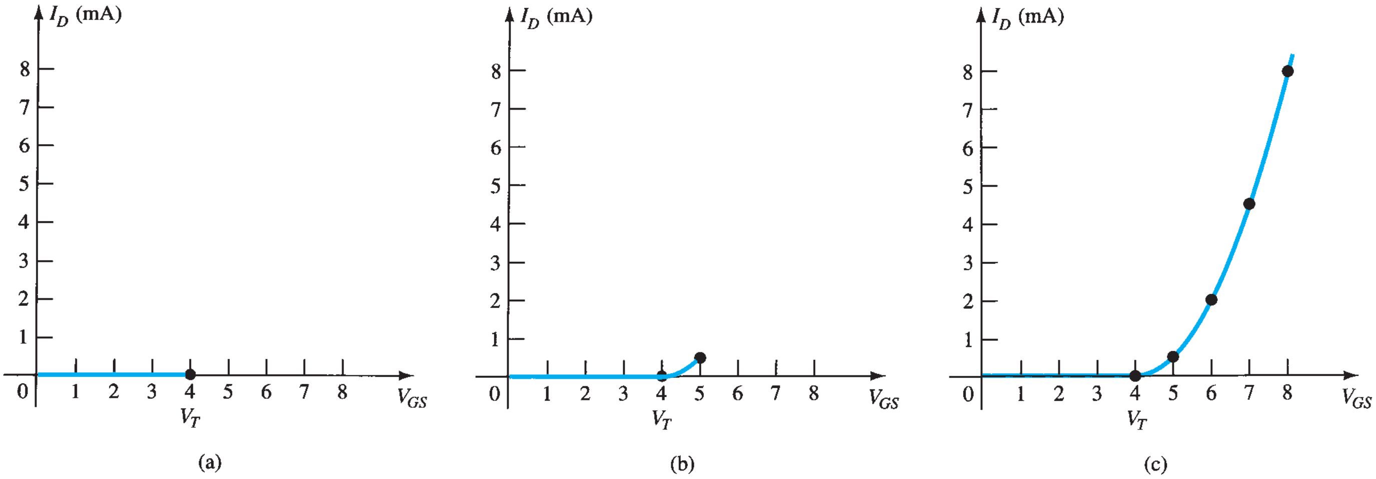


FIG. 6.37

Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}\text{ A/V}^2$ *and* $V_T = 4$ *V.*

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 6.32, as shown in Fig. 6.38a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 6.38c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics of Fig. 6.38b will be the mirror image (about the I_D axis) of the transfer curve of Fig. 6.36, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 6.38c. Equations (6.13) through (6.16) are equally applicable to *p*-channel devices.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 6.39. Again note how the symbols try to reflect the actual construction of

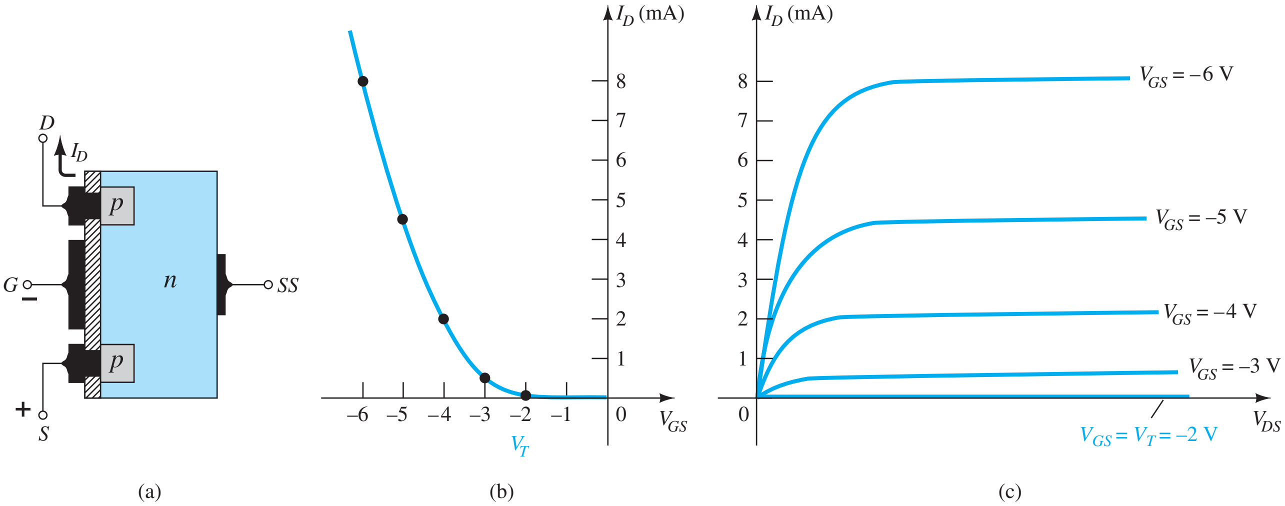


FIG. 6.38

p-Channel enhancement-type MOSFET with $V_T = 2$ V *and* $k = 0.5 \times 10^{-3}$ A/V^2.

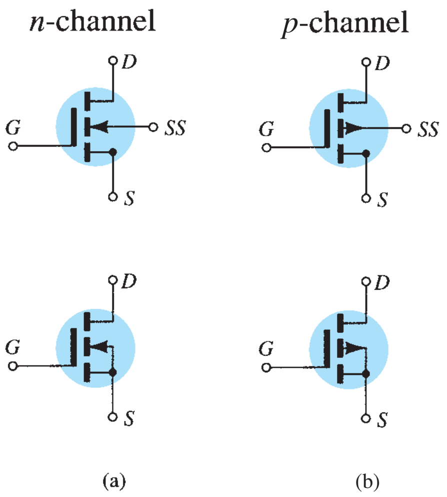
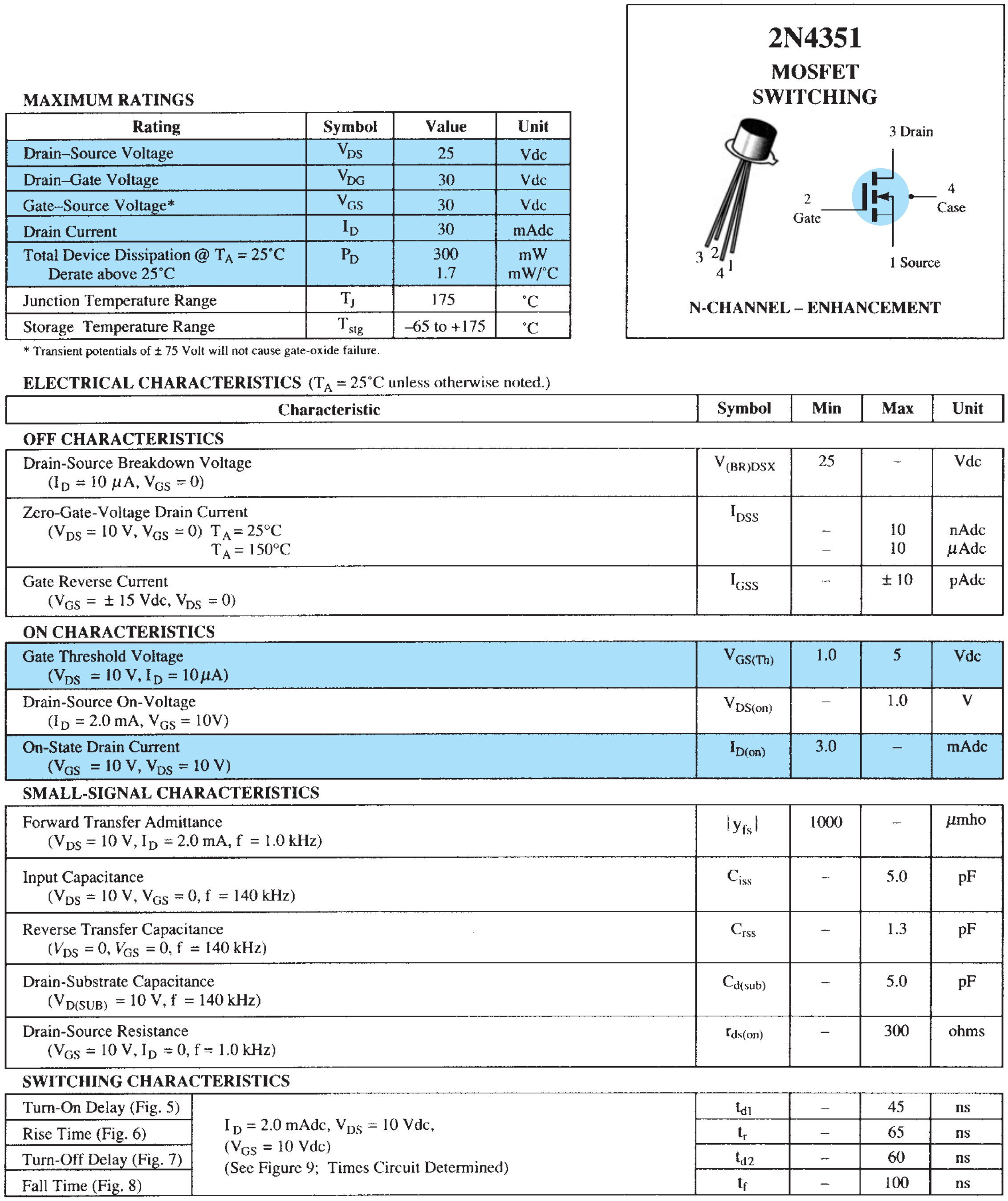


FIG. 6.39

Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

the device. The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 6.40. The case construction and the terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of I_{DSS} under “off” conditions, which is now simply 10 nA dc (at $V_{DS} = 10$ V and $V_{GS} = 0$ V), compared to the milliampere range for the JFET and the depletion-type MOSFET. The threshold voltage is specified as $V_{GS(\text{Th})}$ and has a range of 1 to 5 V dc, depending on the device employed. Rather than provide a range of *k* in Eq. (6.15), a typical level of $I_{D(\text{on})}$ (3 mA in this case) is specified at a particular level of $V_{GS(\text{on})}$ (10 V for the specified I_D level). In other words, when $V_{GS} = 10$ V, $I_D = 3$ mA. The given levels of $V_{GS(\text{Th})}$, $I_{D(\text{on})}$, and $V_{GS(\text{on})}$ permit a determination of *k* from Eq. (6.16) and a writing of the general equation for the transfer characteristics. The handling requirements of MOSFETs are reviewed in Section 6.9.


3 Drain
2
Gate
4
Case
1 Source
3
2
1
4

2N4351

MOSFET
SWITCHING

N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc µAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\ \mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	1000	–	µmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay (Fig. 5)	$I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined)	t_{d1}	–	45	ns
Rise Time (Fig. 6)		t_r	–	65	ns
Turn-Off Delay (Fig. 7)		t_{d2}	–	60	ns
Fall Time (Fig. 8)		t_f	–	100	ns

FIG. 6.40

2N4351 Motorola n-channel enhancement-type MOSFET.

EXAMPLE 6.4 Using the data provided on the specification sheet of Fig. 6.40 and an average threshold voltage of $V_{GS(\text{Th})} = 3$ V, determine:

a. The resulting value of k for the MOSFET.
b. The transfer characteristics.

Solution:

a. Eq. (6.16):

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{ A/V}^2$$
$$= \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

b. Eq. (6.15):

$$I_D = k(V_{GS} - V_T)^2$$
$$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$$

For $V_{GS} = 5$ V,

$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$
$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8$, 10, 12, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 6.41.

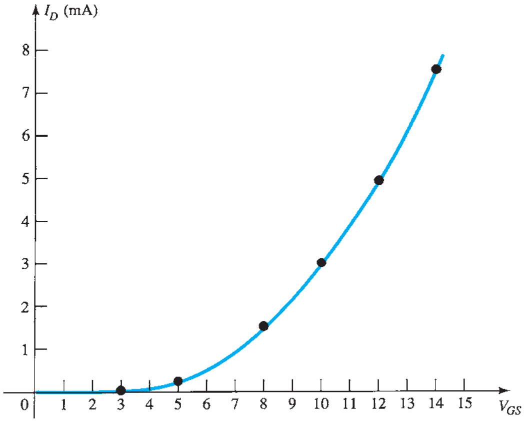


FIG. 6.41

Solution to Example 6.4.

6.9 MOSFET HANDLING

The thin SiO_2 layer between the gate and the channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors. There is often sufficient accumulation of static charge (picked up from the surroundings) to establish a potential difference across the thin layer that can break down the layer and establish conduction through it. It is therefore imperative to leave the shorting (or conduction) shipping foil (or ring) connecting the leads of the device together until the device is to be inserted in the system. The shorting ring prevents the possibility of applying a potential across any two terminals of the device. With the ring, the potential difference between any two terminals is maintained at 0 V. At the very least always touch ground to permit discharge of the accumulated static charge before handling the device, and always pick up the transistor by the casing.

There are often transients (sharp changes in voltage or current) in a network when elements are removed or inserted if the power is on. The transient levels can often be more than the device can handle, and therefore the power should always be off when network changes are made.

The maximum gate-to-source voltage is normally provided in the list of maximum ratings of the device. One method of ensuring that this voltage is not exceeded (perhaps by transient effects) for either polarity is to introduce two Zener diodes, as shown in Fig. 6.42. The Zeners are back to back to ensure protection for either polarity. If both are 30-V Zeners and a positive transient of 40 V appears, the lower Zener will "fire" at 30 V and the upper will turn on with a 0-V drop (ideally—for the positive "on" region of a semiconductor diode) across the other diode. The result is a maximum of 30 V for the gate-to-source voltage. One disadvantage introduced by the Zener protection is that the off resistance of a Zener diode is less than the input impedance established by the SiO_2 layer. The result is a reduction in input resistance, but even so, it is still high enough for most applications. So many of the discrete devices now have the Zener protection that some of the concerns listed above are not as troublesome. However, it is still best to be somewhat cautious when handling discrete MOSFET devices.

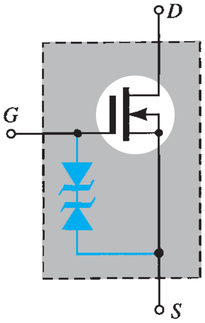


FIG. 6.42

Zener-protected MOSFET.

6.10 VMOS AND UMOS POWER MOSFETs

One of the disadvantages of the typical planar MOSFET is the reduced power handling (typically less than 1 W) and current levels compared with the broad range of bipolar transistors. However, through a vertical design such as shown for the VMOS MOSFET in Fig. 6.43a and the UMOS MOSFET in Fig. 6.43b, power and current levels have been increased along with higher switching speeds and reduced operating dissipation. All the elements of the planar MOSFET are present in the VMOS or UMOS MOSFETs—the metallic surface connection to the terminals of the device, the SiO_2 layer between the gate, and the *p*-type region between the drain and the source for the growth of the induced *n*-channel (enhancement-mode operation). The term *vertical* is due primarily to the fact that the channel is now formed in the *vertical* direction resulting in a vertical current direction rather than the horizontal direction for the planar device. However, the channel of Fig. 6.43a also has the appearance of a "V" cut in the semiconductor base, which often stands out as the reason for the name for the device. The construction of Fig. 6.43a is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

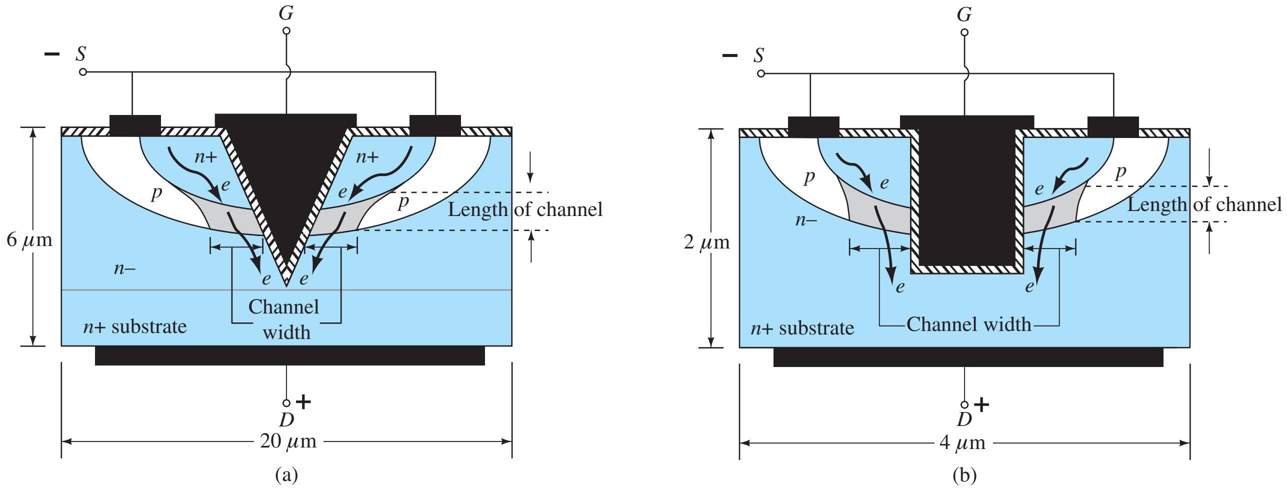


FIG. 6.43
(a) VMOS MOSFET; (b) UMOS MOSFET.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive "on" level as shown in Fig. 6.43a results in the induced *n*-channel in the narrow *p*-type region of the device. The length of the channel is now defined by the vertical height of the *p*-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 μm to 2 μm (1 $\mu m = 10^{-6}$ m). Diffusion layers (such as the *p*-region of Fig. 6.43) can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the n^+ region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers. There is also the existence of two conduction paths between drain and source, as shown in Fig. 6.43, to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

The VMOS MOSFET was the first in line of vertical MOSFETs designed primarily to be used as power switches to control the operation of power supplies, low-voltage motor controllers, DC- to DC-convertors, flat-panel displays, and a host of applications in today's automobiles. Fundamentally, a good power switch should work at relatively low voltages (less than 200 V), has excellent high-speed characteristics, and low levels of "on" resistance to ensure minimum power losses during operation. Over time, a variety of other vertical designs began to surface to improve on the "V" construction of Fig. 6.43a. The delicate etching required to establish the V groove resulted in difficulties establishing a consistent threshold voltage, and the sharp tip at the end of the channel created high electric fields, which affected the breakdown voltage of the MOSFET. The breakdown voltage is important because it is directly related to the "on" resistance. Increase the breakdown voltage and the "on" resistance begins to increase.

One improvement over the "V" design is the "U" groove or channel as appearing in Fig. 6.43b. The operation of this UMOS MOSFET (also called Trench MOSFET) is very similar to that of the VMOS MOSFET but with improved characteristics. First the fabrication process is preferred because the trench-etching process developed for memory cells in DRAMs can be utilized. The result is reduced widths in the neighborhood of 2–10 μm compared with the VMOS construction with widths in the 20–30 μm range. The channel width itself may be only 1 μm with a height of 2 μm. The "on" resistance is less using the trench approach because the channel length is decreased and the width of the current path is increased near the bottom of the trench. However, due to the large surface area required for the heavy current flow, there are capacitive effects that must be considered at frequencies beyond 100 kHz. The three that have to be considered are C_{GS}, C_{GD}, and C_{DS} (respectively referred to as C_{iss}, C_{rss}, and C_{oss} on specification sheets). For the UMOS MOSFET the gate-to-source capacitance at the input is the largest and typically thousands of pF.

The Toshiba line of UMOS-V MOSFETs has a drain current running from 11 A to 45 A with "on" resistances as low as 3.1–11.5 mΩ at 10 V. The maximum drain-to-source voltage for the units is 30 V, and the gate-to-source capacitance ranges from 1400 pF to 4600 pF. They are primarily used in flat-panel displays, desktop and mobile computers, and other portable electronic devices.

In general, therefore

Power MOSFETs have reduced "on" resistance levels and higher current and power ratings than planar MOSFETs.

An additional important characteristic of the vertical construction is:

Power MOSFETs have a positive temperature coefficient, which combats the possibility of thermal runaway.

If the temperature of a device should increase due to the surrounding medium or currents of the device, the resistance levels will increase, causing a reduction in drain current rather than an increase as encountered for a conventional device. Negative temperature coefficients result in decreased levels of resistance with increases in temperature, which fuel the growing current levels and result in further temperature instability and thermal runaway.

Another positive characteristic of the vertical configuration is:

The reduced charge storage levels result in faster switching times for vertical construction compared to those for conventional planar construction.

In fact, VMOS and UMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

6.11 CMOS

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 6.44. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS); it has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 6.45. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 6.45 that both gates are connected to the applied signal and both drain to the output V_o. The source of the *p*-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, whereas the source of the *n*-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V

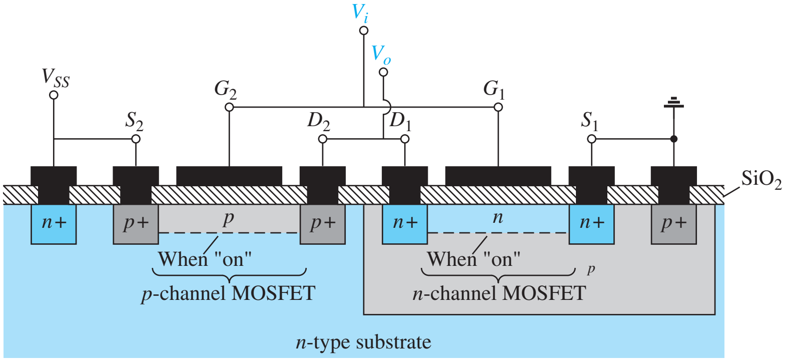

V_i
V_o
V_{SS}
G_2
G_1
S_2
D_2
D_1
S_1
SiO$_2$
$n+$
$p+$
p
$p+$
$n+$
n
$n+$
$p+$
When "on"
p-channel MOSFET
When "on"
p
n-channel MOSFET
n-type substrate

FIG. 6.44
CMOS with the connections indicated in Fig. 6.45.

at the output. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$, and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 6.46. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 6.46. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V, or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V, and Q_1 will be "off" with $V_{SS_2} = -5$ V, turning on the p-channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low. Additional comment on the application of CMOS logic is presented in Chapter 13.

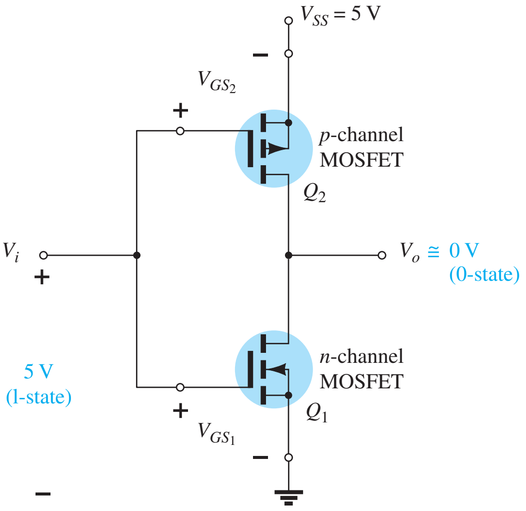

$V_{SS} = 5$ V
−
V_{GS_2}
+
p-channel MOSFET
Q_2
V_i
+
$V_o \cong 0$ V
(0-state)
5 V
(1-state)
n-channel MOSFET
Q_1
+
V_{GS_1}
−
−

FIG. 6.45
CMOS inverter.

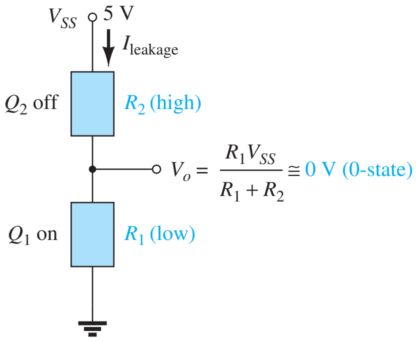

V_{SS} 5 V
I_{leakage}
Q_2 off
R_2 (high)
$V_o = \dfrac{R_1 V_{SS}}{R_1 + R_2} \cong 0$ V (0-state)
Q_1 on
R_1 (low)

FIG. 6.46
Relative resistance levels for $V_i = 5$ V (1-state).

6.12 MESFETs

As noted in earlier discussions, the use of GaAs in the construction of semiconductor devices has been around for quite a few decades. Unfortunately, however, the manufacturing costs, lower resulting density in ICs, and production problems have kept it from prominence in the industry until the last few years. The need for high-speed devices and improved production methods in recent years have established a strong demand for large-scale integrated circuits using GaAs.

Although the Si MOSFETs just described can be made using GaAs instead, it is a more difficult manufacturing process due to diffusion problems. However, the production of FETs using a Schottky barrier (discussed in detail in Chapter 16) at the gate can be done quite efficiently:

Schottky barriers are barriers established by depositing a metal such as tungsten on an n-type channel.

The use of a Schottky barrier at the gate is the major difference from the depletion- and enhancement-type MOSFETs, which employ an insulating barrier between the metal contact and the *n*-type channel. The absence of an insulating layer reduces the distance between the metal contact surface of the gate and the semiconductor layer, resulting in a lower level of stray capacitance between the two surfaces (recall the effect of distance between the plates of a capacitor and its terminal capacitance). The result of the lower capacitance level is a reduced sensitivity to high frequencies (forming a shorting effect), which further supports the high mobility of carriers in the GaAs material.

The presence of a metal–semiconductor junction is the reason such FETs are called *metal–semiconductor field-effect transistors* (MESFETs). The basic construction of a MESFET is provided in Fig. 6.47. Note in Fig. 6.47 that the gate terminal is connected directly to a metallic conductor lying directly against the *n*-channel between the source and drain terminals. The only difference from the depletion-type MOSFET construction is the absence of the insulator at the gate. When a negative voltage is applied to the gate, it will attract free negative carriers (electrons) in the channel to the metal surface, reducing the number of carriers in the channel. The result is a reduced drain current, as shown in Fig. 6.48, for increasing values of negative voltage at the gate terminal. For positive voltages at the gate, additional electrons will be attracted into the channel and the current will rise as shown by the drain characteristics of Fig. 6.48. The fact that the drain and transfer characteristics of the depletion-type MESFET are so similar to those of the depletion-type MOSFET results in analysis techniques similar to those applied to depletion-type MOSFETs. The defined polarities and current directions for the MESFET are provided in Fig. 6.49 along with the symbol for the device.

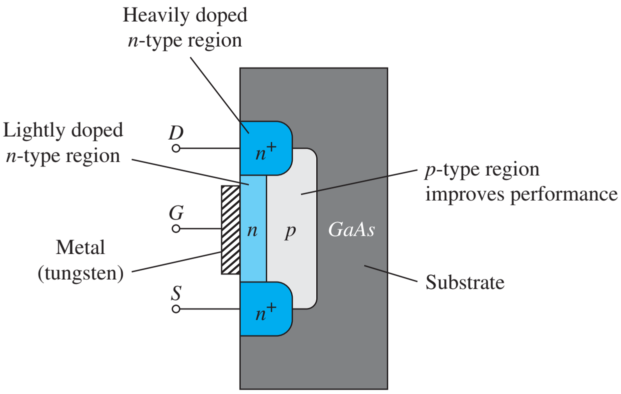


FIG. 6.47
Basic construction of an n-channel MESFET.

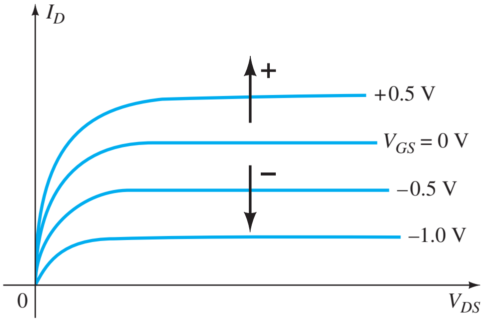


FIG. 6.48
Characteristics of an n-channel MESFET.

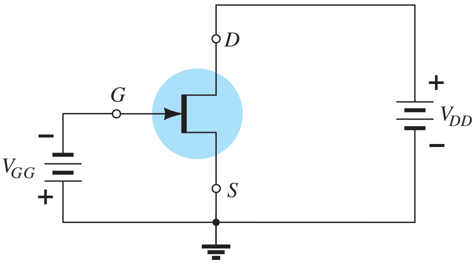


FIG. 6.49
Symbol and basic biasing arrangement for an n-channel MESFET.

There are also enhancement-type MESFETs with a construction the same as in Fig. 6.47 but without the initial channel, as shown in Fig. 6.50 along with its graphic symbol. The response and characteristics are essentially the same as for the enhancement-type MOSFET. However, due to the Schottky barrier at the gate, the positive threshold voltage is limited to 0 V to about 0.4 V because the "turn-on" voltage for a Schottky barrier diode is about 0.7 V. Again, the analysis techniques applied to enhancement-type MESFETs are similar to those employed for enhancement-type MOSFETs.

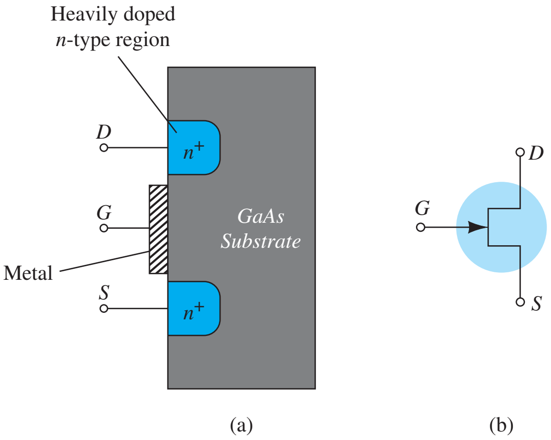


FIG. 6.50
Enhancement-type MESFET: (a) construction; (b) symbol.

It is important to realize, however, that the channel must be an *n*-type material in a MESFET. The mobility of holes in GaAs is relatively low compared to that of the negatively charged carriers, losing the advantage of using GaAs for high-speed applications. The result is:

Depletion-type and enhancement-type MESFETs are made with an n-channel between the drain and the source, and therefore only n-type MESFETs are commercially available.

For both types of MESFETs the channel length (identified in Figs. 6.47 and 6.50) should be made as short as possible for high-speed applications. The length is typically between 0.1 μm and 1 μm.

6.13 SUMMARY TABLE

Since the transfer curves and some important characteristics vary from one type of FET to another, Table 6.3 was developed to clearly display the differences from one device to the next. A clear understanding of all the curves and parameters of the table will provide a sufficient background for the dc and ac analyses to follow. Take a moment to ensure that each curve is recognizable and its derivation understood, and then establish a basis for comparison of the levels of the important parameters of R_i and C_i for each device.

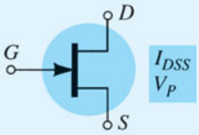
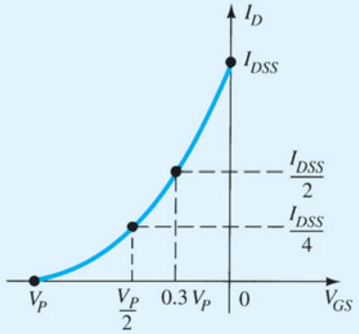
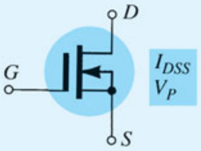
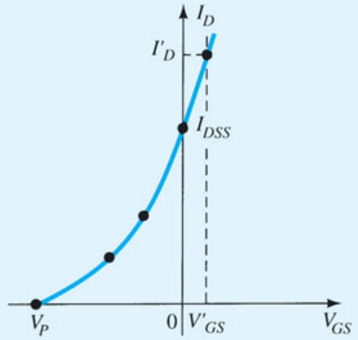
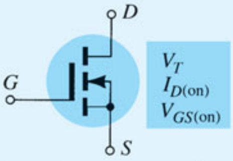
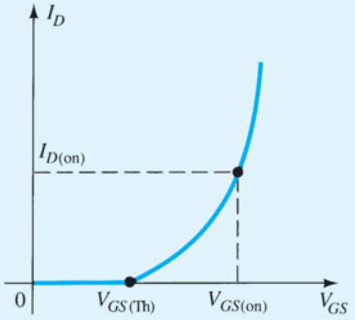
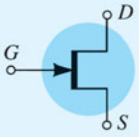
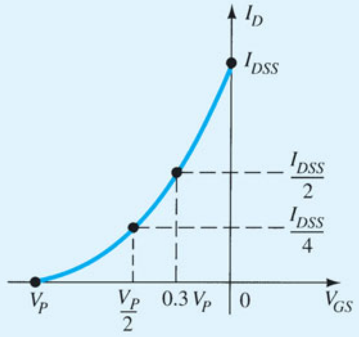
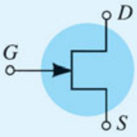
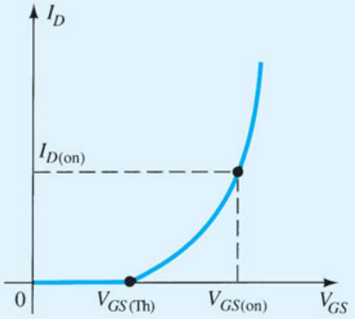
6.14 SUMMARY

Important Conclusions and Concepts

1. A **current-controlled device** is one in which a current defines the operating conditions of the device, whereas a **voltage-controlled device** is one in which a particular voltage defines the operating conditions.
2. The JFET can actually be used as a **voltage-controlled resistor** because of a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.
3. The **maximum current** for any JFET is labeled I_{DSS} and occurs when $V_{GS} = 0$ V.
4. The **minimum current** for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.
5. The relationship between the drain current and the gate-to-source voltage of a JFET is a **nonlinear one** defined by Shockley's equation. As the current level approaches I_{DSS}, the sensitivity of I_D to changes in V_{GS} increases significantly.

TABLE 6.3

Field Effect Transistors

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100\text{ M}\Omega$ C_i: $(1 - 10)$ pF
MOSFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}\ \Omega$ C_i: $(1 - 10)$ pF
MOSFET enhancement type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  D G S V_T $I_{D(\text{on})}$ $V_{GS(\text{on})}$ $I_D = k\,(V_{GS} - V_{GS\,(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS\,(\text{Th})})^2}$		$R_i > 10^{10}\ \Omega$ C_i: $(1 - 10)$ pF
MESFET depletion type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ $I_G = 0\text{ A}, I_D = I_S$		$R_i > 10^{12}\ \Omega$ C_i: $(1 - 5)$ pF
MESFET enhancement type (*n*-channel)	 $I_D = k\,(V_{GS} - V_{GS\,(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS\,(\text{Th})})^2}$		$R_i > 10^{12}\ \Omega$ C_i: $(1 - 5)$ pF

6. The transfer characteristics (I_D versus V_{GS}) are characteristics **of the device itself** and are not sensitive to the network in which the JFET is employed.
7. When $V_{GS} = V_P/2$, $I_D = I_{DSS}/4$; and at a point where $I_D = I_{DSS}/2$, $V_{GS} \cong 0.3$ V.
8. Maximum operating conditions are determined by the **product** of the drain-to-source voltage and the drain current.
9. MOSFETs are available in one of two types: **depletion and enhancement**.
10. The depletion-type MOSFET has the same transfer characteristics as a JFET for drain currents up to the I_{DSS} level. At this point the characteristics of a depletion-type MOSFET **continue to levels above** I_{DSS}, whereas those of the JFET will end.
11. The arrow in the symbol of *n*-channel JFETs or MOSFETs will **always point in to the center of the symbol**, whereas those of a *p*-channel device will always point out of the center of the symbol.
12. The transfer characteristics of an enhancement-type MOSFET are **not defined by Shockley's equation** but rather by a nonlinear equation controlled by the gate-to-source voltage, the threshold voltage, and a constant *k* defined by the device employed. The resulting plot of I_D versus V_{GS} **rises exponentially with incrseasing values of** V_{GS}.
13. Always handle MOSFETs with **additional care** due to the static electricity that exists in places we might least suspect. Do not remove any shorting mechanism between the leads of the device until it is installed.
14. A CMOS (complementary MOSFET) device employs a unique **combination of a *p*-channel and an *n*-channel MOSFET** with a single set of external leads. It has the advantages of a very high input impedance, fast switching speeds, and low operating power levels, all of which make it very useful in logic circuits.
15. A depletion-type MESFET includes a metal–semiconductor junction, resulting in characteristics that **match those of an *n*-channel depletion-type JFET**. Enhancement-type MESFETs have the same characteristics as enhancement-type MOSFETs. The result of this similarity is that the **same type of dc and ac analysis techniques can be applied to MESFETs as was applied to JFETs**.

Equations

JFET:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\big|_{V_{GS}=0\text{ V}}, \quad I_D = 0\text{ mA}\big|_{V_{GS}=V_P}, \quad I_D = \frac{I_{DSS}}{4}\bigg|_{V_{GS}=V_P/2}, \quad V_{GS} \cong 0.3V_P\big|_{I_D=I_{DSS}/2}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS}I_D$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

6.15 COMPUTER ANALYSIS

PSpice Windows

The characteristics of an *n*-channel JFET can be displayed using the same procedure employed for the transistor in Section 3.13. The series of curves across the characteristics plotted against various values of voltage requires a nested sweep within the sweep for the drain-to-source voltage. The required configuration of Fig. 6.51 is constructed using procedures described in the previous chapters. In particular, note the complete absence of resistors since the input impedance is assumed to be infinite, resulting in a gate current of 0 A.

The JFET is found under **Part** in the **Place Part** dialog box. It can be called up by simply typing in **JFET** in the provided space under the **Part** heading. Once in place, a single click on the symbol followed by **Edit-PSpice Model** will result in the **PSpice Model Editor Demo** dialog box. Note that **Beta** is equal to 1.304 mA/V^2 and **Vto** is −3 V. For the junction field effect transistor **Beta** is defined by

$$\boxed{\text{Beta} = \frac{I_{DSS}}{V_P{}^2}} \qquad (\text{A/V}^2) \tag{6.17}$$

The parameter **Vto** defines $V_{GS} = V_P = -3$ V as the pinch-off voltage. Using Eq. (6.17), one can solve for I_{DSS} and find that it is about 11.37 mA. Once the plots are obtained one can check whether both of these parameters are accurately defined by the characteristics. With the network established, select a **New Simulation** to obtain the **New Simulation** dialog box. Using **OrCAD 6-1** as the name followed by **Create** results in the **Simulation Settings** dialog box, in which **DC Sweep** is selected under the **Analysis type** heading. The **Sweep variable** is set as a **Voltage source** with the **Name VDD**. The **Start Value** is 0 V, the **End Value** is 10 V, and the **Increment** is 0.01 V. Now select **Secondary Sweep** and apply the **Name VGG** with a **Start Value** of 0 V, an **End Value** of −5 V, and an **Increment** of −1 V. Finally, the **Secondary Sweep** must be enabled by ensuring the check appears in the box to the left of the listing, followed by an **OK** to leave the dialog box. A **Simulation**, and the **SCHEMATIC** screen will appear with a horizontal axis labeled **VDD** extending from 0 V to 10 V. Continue with the sequence **Trace-Add Trace** to obtain the **Add Traces** dialog box, and select **ID(J1)** to obtain the characteristics of Fig. 6.52. Note in particular that I_{DSS} is very close to 11.7 mA as predicted based on the value of Beta. Also note that cutoff does occur at $V_{GS} = V_P = -3$ V.

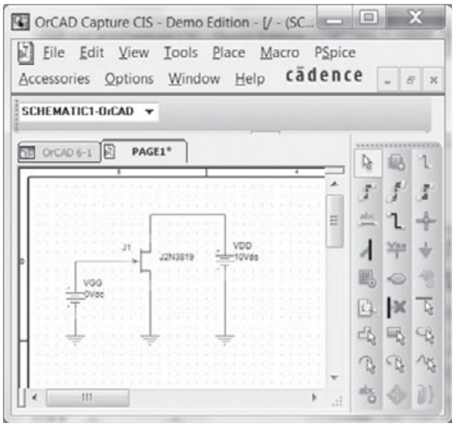

OrCAD Capture CIS - Demo Edition - [/ - (SC...
File Edit View Tools Place Macro PSpice
Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 6-1
PAGE1*
J1
J2N3819
VDD
10Vdc
VGG
0Vdc

FIG. 6.51
Network used to obtain the characteristics of the n-channel J2N3819 JFET.

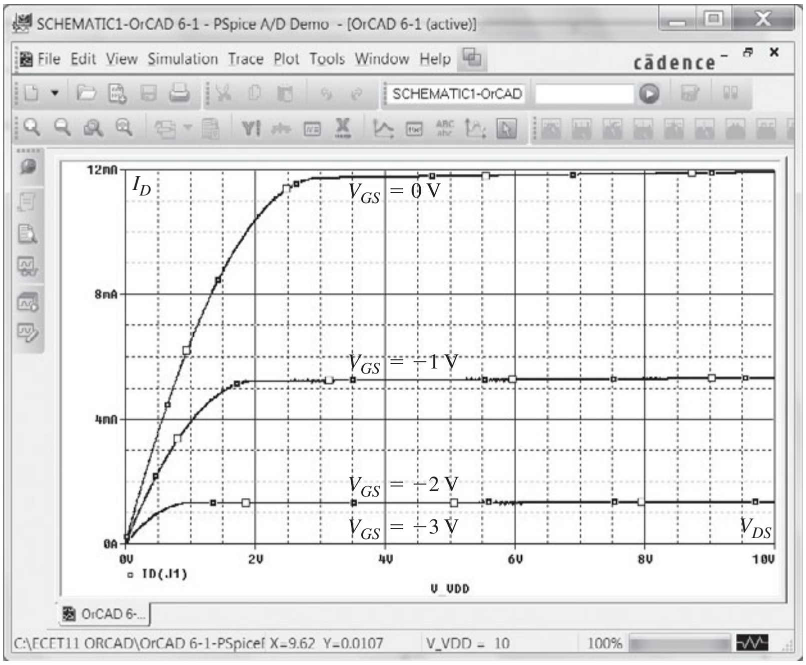

SCHEMATIC1-OrCAD 6-1 - PSpice A/D Demo - [OrCAD 6-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
12mA
8mA
4mA
0A
I_D
$V_{GS} = 0$ V
$V_{GS} = -1$ V
$V_{GS} = -2$ V
$V_{GS} = -3$ V
V_{DS}
0V
2V
4V
6V
8V
10V
ID(J1)
V_VDD
OrCAD 6-...
C:\ECET11 ORCAD\OrCAD 6-1-PSpiceF X=9.62 Y=0.0107
V_VDD = 10
100%

FIG. 6.52
Drain characteristics for the n-channel J2N3819 JFET of Fig. 6.51.

The transfer characteristics can be obtained by setting up a **New Simulation** that has a single sweep since there is only one curve to plot. Once **DC Sweep** is again selected, the **Name** is **VGG** with a **Start Value** of −3 V, an **End Value** of 0 V, and an **Increment** of 0.01 V. Since there is no need for a secondary nested sweep, select **OK**, and the simulation is performed. When the graph appears, select **Trace-Add Trace-ID(J1)** to obtain the transfer characteristics of Fig. 6.53. Note how the axis is set with the −3 V to the far left and the 0 V to the far right. Again, I_{DSS} is very close to the predicted 11.7 mA and $V_P = -3$ V.

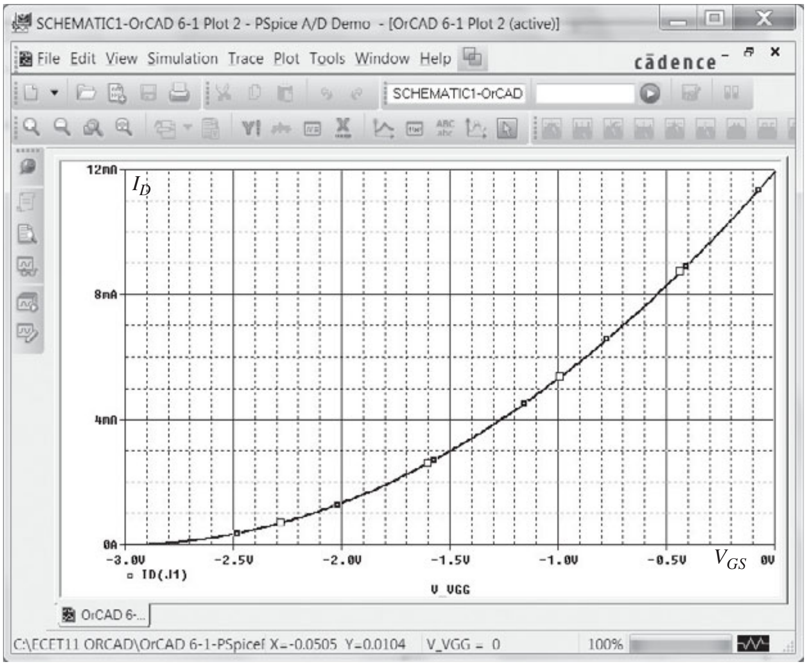

SCHEMATIC1-OrCAD 6-1 Plot 2 - PSpice A/D Demo - [OrCAD 6-1 Plot 2 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
12mA
I_D
8mA
4mA
0A
-3.0V
-2.5V
-2.0V
-1.5V
-1.0V
-0.5V
V_{GS}
0V
▫ ID(J1)
V_VGG
OrCAD 6-...
C:\ECET11 ORCAD\OrCAD 6-1-PSpice\ X=-0.0505 Y=0.0104
V_VGG = 0
100%

FIG. 6.53

Transfer characteristics for the n-channel J2N3819 JFET of Fig. 6.51.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

6.2 Construction and Characteristics of JFETs

1. **a.** Draw the basic construction of a *p*-channel JFET.
   b. Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.
2. Using the characteristics of Fig. 6.11, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$):
   a. $V_{GS} = 0$ V.
   b. $V_{GS} = -1$ V.
   c. $V_{GS} = -1.5$ V.
   d. $V_{GS} = -1.8$ V.
   e. $V_{GS} = -4$ V.
   f. $V_{GS} = -6$ V.
3. Using the results of problem 2 plot the transfer characteristics of I_D vs. V_{GS}.
4. **a.** Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 6.11.
   b. Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.
   c. Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.
   d. Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.
   e. Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.
   f. Using the results of part (e), calculate the resistance of the JFET for the region $I_D = 0$ to 1.5 mA for $V_{GS} = -2$ V.
   g. Defining the result of part (b) as r_o, determine the resistance for $V_{GS} = -1$ V using Eq. (6.1) and compare with the results of part (d).
   h. Repeat part (g) for $V_{GS} = -2$ V using the same equation, and compare the results with part (f).
   i. Based on the results of parts (g) and (h), does Eq. (6.1) appear to be a valid approximation?
5. Using the characteristics of Fig. 6.11:
   a. Determine the difference in drain current (for $V_{DS} > V_P$) between $V_{GS} = 0$ V and $V_{GS} = -1$ V.
   b. Repeat part (a) between $V_{GS} = -1$ and -2 V.
   c. Repeat part (a) between $V_{GS} = -2$ and -3 V.
   d. Repeat part (a) between $V_{GS} = -3$ and -4 V.
   e. Is there a marked change in the difference in current levels as V_{GS} becomes increasingly negative?

f. Is the relationship between the change in V_{GS} and the resulting change in I_D linear or nonlinear? Explain.

6. What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does I_C react to increasing levels of I_B versus changes in I_D to increasingly negative values of V_{GS}? How does the spacing between steps of I_B compare to the spacing between steps of V_{GS}? Compare $V_{C_{\text{sat}}}$ to V_P in defining the nonlinear region at low levels of output voltage.

7. **a.** Describe in your own words why I_G is effectively 0 A for a JFET transistor.
b. Why is the input impedance to a JFET so high?
c. Why is the terminology *field effect* appropriate for this important three-terminal device?

8. Given $I_{DSS} = 12$ mA and $|V_P| = 6$ V, sketch a probable distribution of characteristic curves for the JFET (similar to Fig. 6.11).

9. In general, comment on the polarity of the various voltages and direction of the currents for an *n*-channel JFET versus a *p*-channel JFET.

6.3 Transfer Characteristics

10. Given the characteristics of Fig. 6.54:
a. Sketch the transfer characteristics directly from the drain characteristics.
b. Using Fig. 6.54 to establish the values of I_{DSS} and V_P, sketch the transfer characteristics using Shockley's equation.
c. Compare the characteristics of parts (a) and (b). Are there any major differences?

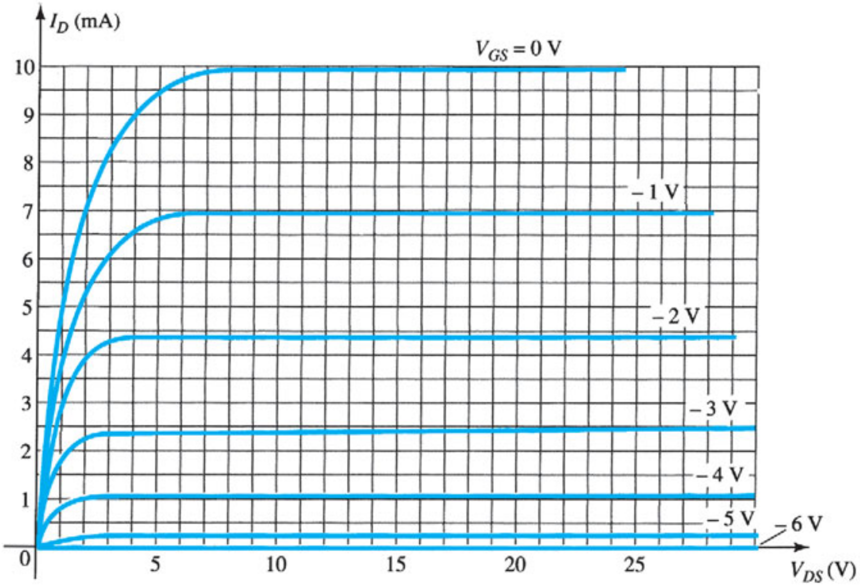


FIG. 6.54
Problems 10 and 20.

11. **a.** Given $I_{DSS} = 12$ mA and $V_P = -4$ V, sketch the transfer characteristics for the JFET transistor.
b. Sketch the drain characteristics for the device of part (a).

12. Given $I_{DSS} = 9$ mA and $V_P = -4$ V, determine I_D when:
a. $V_{GS} = 0$ V.
b. $V_{GS} = -2$ V.
c. $V_{GS} = -4$ V.
d. $V_{GS} = -6$ V.

13. Given $I_{DSS} = 16$ mA and $V_P = -5$ V, sketch the transfer characteristics using the data points of Table 6.1. Determine the value of I_D at $V_{GS} = -3$ V from the curve, and compare it to the value determined using Shockley's equation. Repeat the above for $V_{GS} = -1$ V.

14. For a particular JFET if $I_D = 4$ mA when $V_{GS} = -3$ V, determine V_P if $I_{DSS} = 12$ mA.

15. Given $I_{DSS} = 6$ mA and $V_P = -4.5$ V:
a. Determine I_D at $V_{GS} = -2$ and -3.6 V.
b. Determine V_{GS} at $I_D = 3$ and 5.5 mA.

16. Given a *Q*-point of $I_{D_Q} = 3$ mA and $V_{GS} = -3$ V, determine I_{DSS} if $V_P = -6$ V.

17. A *p*-channel JFET has device parameters of $I_{DSS} = 7.5$ mA and $V_P = 4$ V. Sketch the transfer characteristics.

6.4 Specification Sheets (JFETs)

18. Define the region of operation for the 2N5457 JFET of Fig. 6.20 using the range of I_{DSS} and V_P provided. That is, sketch the transfer curve defined by the maximum I_{DSS} and V_P and the transfer curve for the minimum I_{DSS} and V_P. Then, shade in the resulting area between the two curves.

19. For the 2N5457 JFET of Fig. 6.20, what is the power rating at a typical operating temperature of 45°C using the 5.0 mW/°C derating factor.

20. Define the region of operation for the JFET of Fig. 6.54 if $V_{DS_{\max}} = 30$ V and $P_{D_{\max}} = 100$ mW.

6.5 Instrumentation

21. Using the characteristics of Fig. 6.22, determine I_D at $V_{GS} = -0.7$ V and $V_{DS} = 10$ V.

22. Referring to Fig. 6.22, is the locus of pinch-off values defined by the region of $V_{DS} < |V_P| = 3$ V?

23. Determine V_P for the characteristics of Fig. 6.22 using I_{DSS} and I_D at some value of V_{GS}. That is, simply substitute into Shockley's equation and solve for V_P. Compare the result to the assumed value of -3 V from the characteristics.

24. Using $I_{DSS} = 9$ mA and $V_P = -3$ V for the characteristics of Fig. 6.22, calculate I_D at $V_{GS} = -1$ V using Shockley's equation and compare to the level in Fig. 6.22.

25. **a.** Calculate the resistance associated with the JFET of Fig. 6.22 for $V_{GS} = 0$ V from $I_D = 0$ mA to 4 mA.
b. Repeat part (a) for $V_{GS} = -0.5$ V from $I_D = 0$ to 3 mA.
c. Assigning the label r_o to the result of part (a) and r_d to that of part (b), use Eq. (6.1) to determine r_d and compare to the result of part (b).

6.7 Depletion-Type MOSFET

26. **a.** Sketch the basic construction of a *p*-channel depletion-type MOSFET.
b. Apply the proper drain-to-source voltage and sketch the flow of electrons for $V_{GS} = 0$ V.

27. In what ways is the construction of a depletion-type MOSFET similar to that of a JFET? In what ways is it different?

28. Explain in your own words why the application of a positive voltage to the gate of an *n*-channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.

29. Given a depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = -3$ V, determine the drain current at $V_{GS} = -1, 0, 1,$ and 2 V. Compare the difference in current levels between -1 V and 0 V with the difference between 1 V and 2 V. In the positive V_{GS} region, does the drain current increase at a significantly higher rate than for negative values? Does the I_D curve become more and more vertical with increasing positive values of V_{GS}? Is there a linear or a nonlinear relationship between I_D and V_{GS}? Explain.

30. Sketch the transfer and drain characteristics of an *n*-channel depletion-type MOSFET with $I_{DSS} = 12$ mA and $V_P = -8$ V for a range of $V_{GS} = -V_P$ to $V_{GS} = 1$ V.

31. Given $I_D = 14$ mA and $V_{GS} = 1$ V, determine V_P if $I_{DSS} = 9.5$ mA for a depletion-type MOSFET.

32. Given $I_D = 4$ mA at $V_{GS} = -2$ V, determine I_{DSS} if $V_P = -5$ V.

33. Using an average value of 2.9 mA for the I_{DSS} of the 2N3797 MOSFET of Fig. 6.31, determine the level of V_{GS} that will result in a maximum drain current of 20 mA if $V_P = -5$ V.

34. If the drain current for the 2N3797 MOSFET of Fig. 6.31 is 8 mA, what is the maximum permissible value of V_{DS} utilizing the maximum power rating?

6.8 Enhancement-Type MOSFET

35. **a.** What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET?
b. Sketch a *p*-channel enhancement-type MOSFET with the proper biasing applied ($V_{DS} > 0$ V, $V_{GS} > V_T$) and indicate the channel, the direction of electron flow, and the resulting depletion region.
c. In your own words, briefly describe the basic operation of an enhancement-type MOSFET.

36. **a.** Sketch the transfer and drain characteristics of an *n*-channel enhancement-type MOSFET if $V_T = 3.5$ V and $k = 0.4 \times 10^{-3}$ A/V^2.
b. Repeat part (a) for the transfer characteristics if V_T is maintained at 3.5 V but k is increased by 100% to 0.8×10^{-3} A/V^2.

37. **a.** Given $V_{GS(\text{Th})} = 4$ V and $I_{D(\text{on})} = 4$ mA at $V_{GS(\text{on})} = 6$ V, determine k and write the general expression for I_D in the format of Eq. (6.15).

b. Sketch the transfer characteristics for the device of part (a).

c. Determine I_D for the device of part (a) at $V_{GS} = 2$, 5, and 10 V.

38. Given the transfer characteristics of Fig. 6.55, determine V_T and k and write the general equation for I_D.

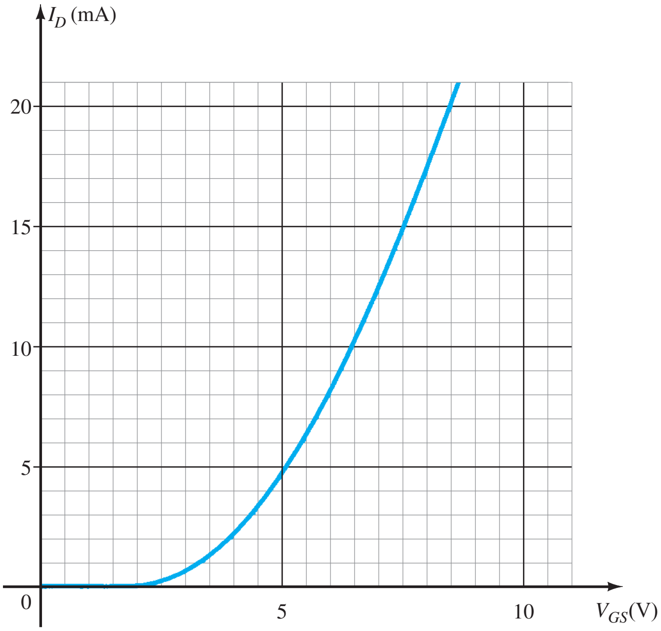


FIG. 6.55
Problem 38.

39. Given $k = 0.4 \times 10^{-3}$ A/V^2 and $I_{D(\text{on})} = 3$ mA with $V_{GS(\text{on})} = 4$ V, determine V_T.

40. The maximum drain current for the 2N4351 *n*-channel enhancement-type MOSFET is 30 mA. Determine V_{GS} at this current level if $k = 0.06 \times 10^{-3}$ A/V^2 and V_T is the maximum value.

41. Does the current of an enhancement-type MOSFET increase at about the same rate as a depletion-type MOSFET for the conduction region? Carefully review the general format of the equations, and if your mathematics background includes differential calculus, calculate dI_D/dV_{GS} and compare its magnitude.

42. Sketch the transfer characteristics of a *p*-channel enhancement-type MOSFET if $V_T = -5$ V and $k = 0.45 \times 10^{-3}$ A/V^2.

43. Sketch the curve of $I_D = 0.5 \times 10^{-3}(V_{GS}^2)$ and $I_D = 0.5 \times 10^{-3}(V_{GS} - 4)^2$ for V_{GS} from 0 V to 10 V. Does $V_T = 4$ V have a significant effect on the level of I_D for this region?

6.10 VMOS and UMOS Power MOSFETs

44. **a.** Describe in your own words why the VMOS FET can withstand a higher current and power rating than devices constructed with standard techniques.

b. Why do VMOS FETs have reduced channel resistance levels?

c. Why is a positive temperature coefficient desirable?

45. What are the relative advantages of the UMOS technology over the VMOS technology?

6.11 CMOS

***46.** **a.** Describe in your own words the operation of the network of Fig. 6.45 with $V_i = 0$ V.

b. If the "on" MOSFET of Fig. 6.45 (with $V_i = 0$ V) has a drain current of 4 mA with $V_{DS} = 0.1$ V, what is the approximate resistance level of the device? If $I_D = 0.5\ \mu$A for the "off" transistor, what is the approximate resistance of the device? Do the resulting resistance levels suggest that the desired output voltage level will result?

47. Research CMOS logic at your local or college library, and describe the range of applications and basic advantages of the approach.

7

FET Biasing

CHAPTER OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.

7.1 INTRODUCTION

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $V_{BE} = 0.7\text{ V}$, $I_C = \beta I_B$, and $I_C \cong I_E$. The link between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

Another distinct difference between the analysis of BJT and FET transistors is that:

The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$\boxed{I_G \cong 0\text{ A}} \tag{7.1}$$

and

$$\boxed{I_D = I_S} \tag{7.2}$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{7.3}$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{7.4}$$

It is particularly important to realize that all of the equations above are for the *field-effect transistor only*! They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.

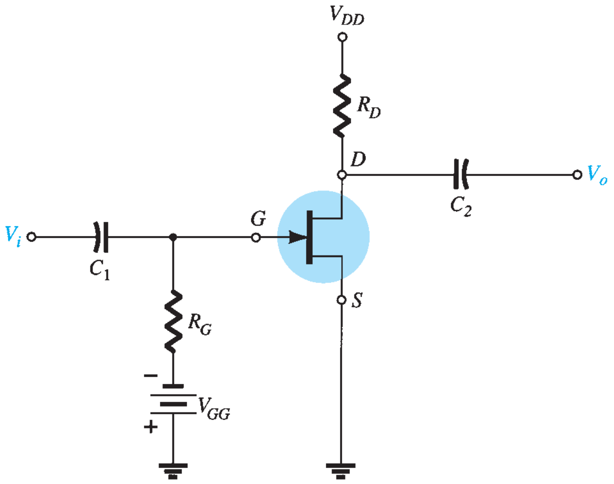


FIG. 7.1
Fixed-bias configuration.

The configuration of Fig. 7.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,

$$I_G \cong 0\text{ A}$$

and

$$V_{R_G} = I_G R_G = (0\text{ A})R_G = 0\text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

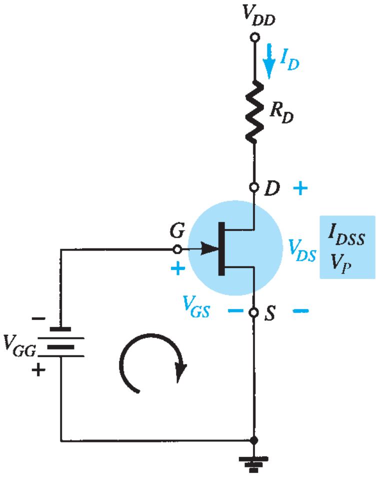


FIG. 7.2

Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \tag{7.5}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 7.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

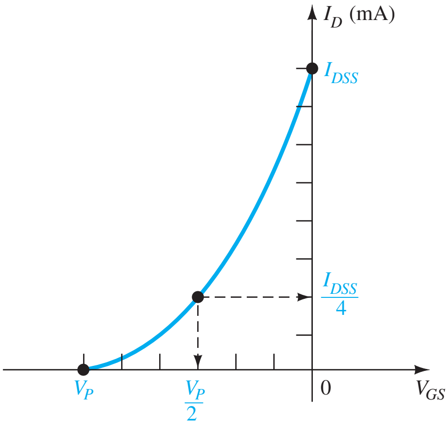


FIG. 7.3

Plotting Shockley's equation.

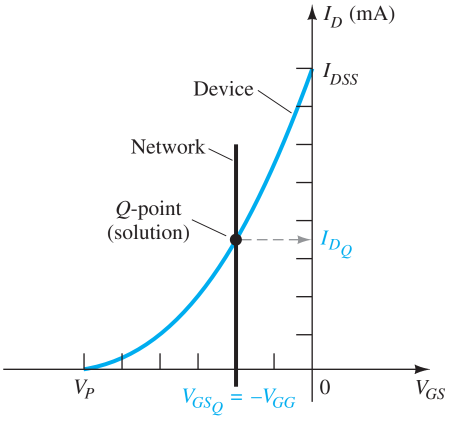


FIG. 7.4

Finding the solution for the fixed-bias configuration.

In Fig. 7.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.* The subscript Q will be applied to the drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 7.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis. It is important to realize that once the network of Fig. 7.1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 7.5 are the quiescent values defined by Fig. 7.4.

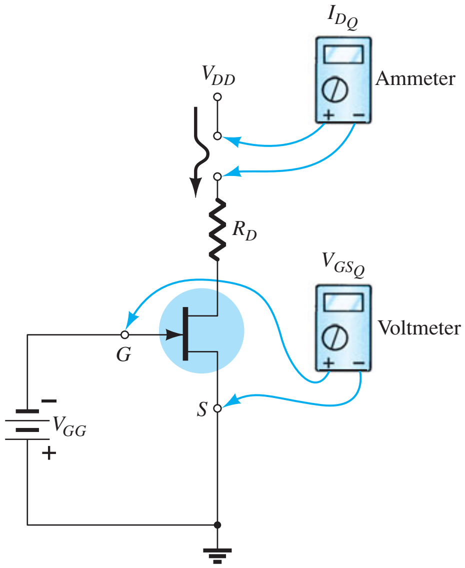


FIG. 7.5
Measuring the quiescent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \qquad \textbf{(7.6)}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$\boxed{V_S = 0\text{ V}} \qquad \textbf{(7.7)}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V}$$

and

$$\boxed{V_D = V_{DS}} \qquad \textbf{(7.8)}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V}$$

and

$$\boxed{V_G = V_{GS}} \qquad \textbf{(7.9)}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

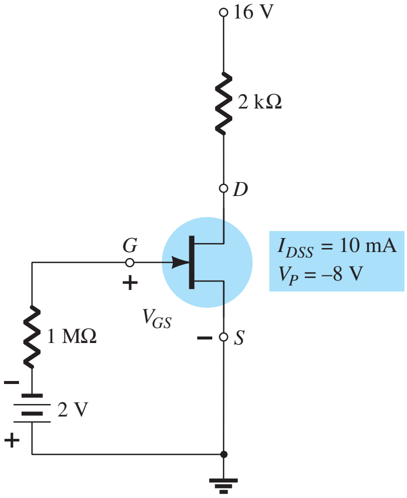


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without

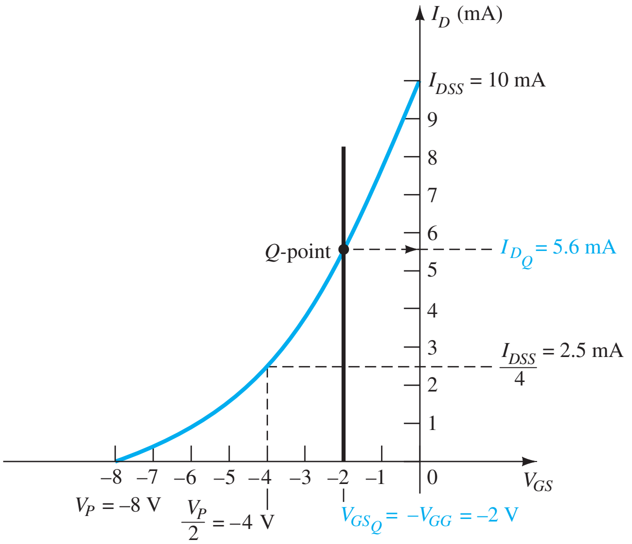


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 7.8.

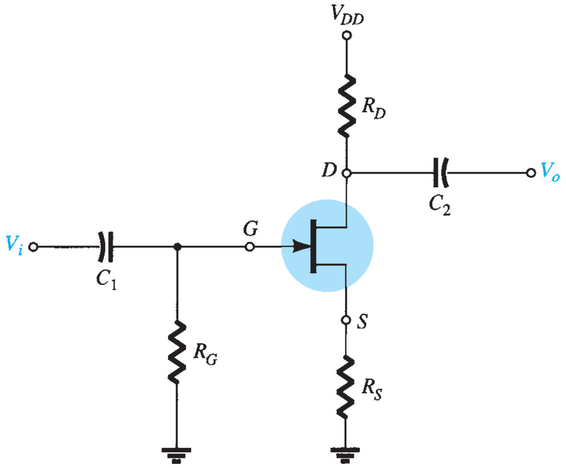


FIG. 7.8
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 7.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \tag{7.10}$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

Equation (7.10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, I_D and V_{GS}, permitting either a mathematical or a graphical solution.

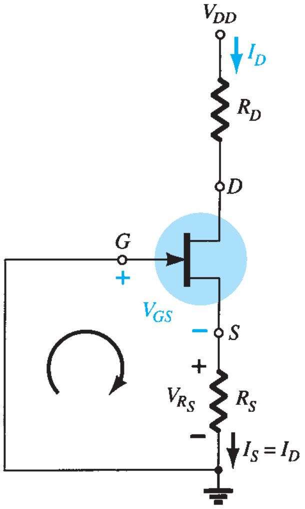


FIG. 7.9
DC analysis of the self-bias configuration.

A mathematical solution could be obtained simply by substituting Eq. (7.10) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or $$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 7.10. Since Eq. (7.10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0$ A since it results in $V_{GS} = -I_D R_S = (0\text{ A})R_S = 0$ V. For Eq. (7.10), therefore, one point on the straight line is defined by $I_D = 0$ A and $V_{GS} = 0$ V, as appearing on Fig. 7.10.

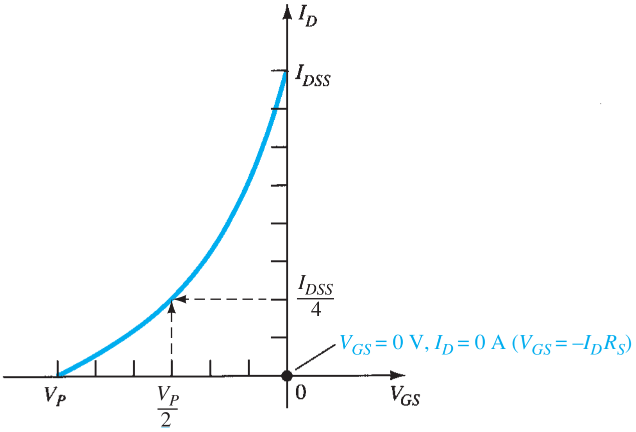


FIG. 7.10

Defining a point on the self-bias line.

The second point for Eq. (7.10) requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined using Eq. (7.10). The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit the drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

Then $$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 7.11. The straight line as defined by Eq. (7.10) is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and $$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

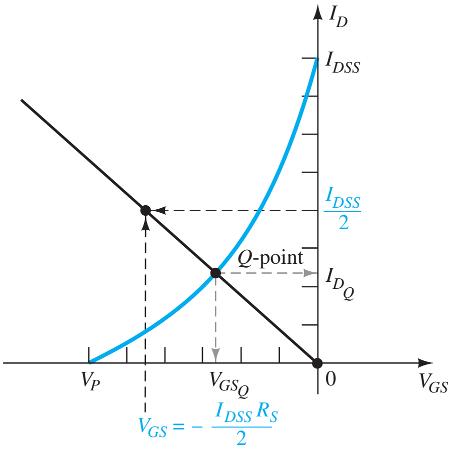


FIG. 7.11
Sketching the self-bias line.

but

$$I_D = I_S$$

and

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{7.11}$$

In addition,

$$\boxed{V_S = I_D R_S} \tag{7.12}$$

$$\boxed{V_G = 0\text{ V}} \tag{7.13}$$

and

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \tag{7.14}$$

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

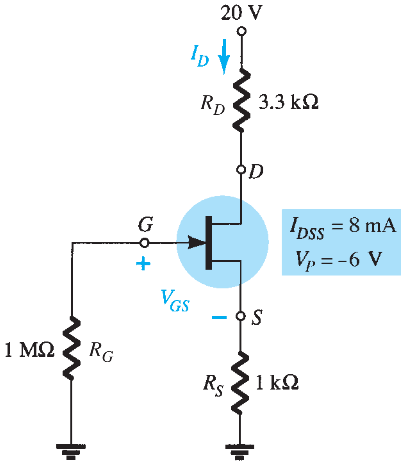


FIG. 7.12
Example 7.2.

Solution:

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

The result is the plot of Fig. 7.13 as defined by the network.

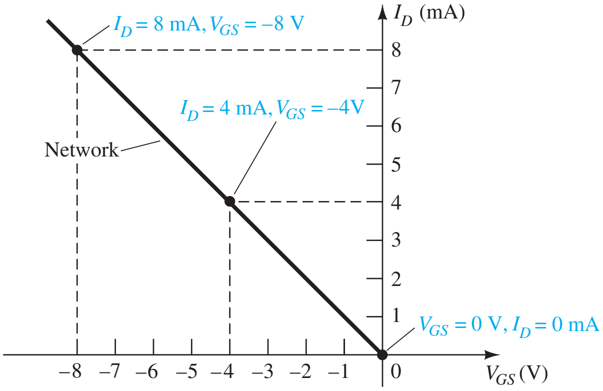


FIG. 7.13
Sketching the self-bias line for the network of Fig. 7.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (7.10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D determined graphically.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2$ mA, and the plot of Fig. 7.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 7.13 on the device characteristics of Fig. 7.14 and finding the point of intersection of the two as indicated on Fig. 7.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6\ V}$$

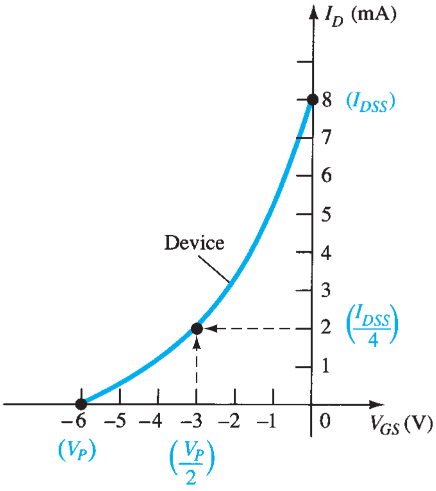


FIG. 7.14
Sketching the device characteristics for the JFET of Fig. 7.12.

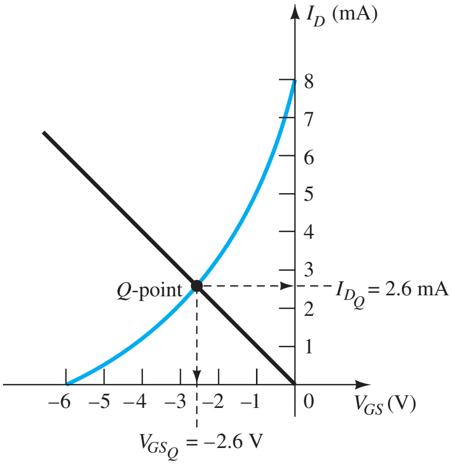


FIG. 7.15
Determining the Q-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. Eq. (7.11):
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega) \\ &= 20\text{ V} - 11.18\text{ V} \\ &= \mathbf{8.82\ V} \end{aligned}$$

d. Eq. (7.12): $V_S = I_D R_S$

$= (2.6\text{ mA})(1\text{ k}\Omega)$

$= \mathbf{2.6\ V}$

e. Eq. (7.13): $V_G = \mathbf{0\ V}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\ V}$

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\ \Omega$.
b. $R_S = 10\text{ k}\Omega$.

Solution: Both $R_S = 100\ \Omega$ and $R_S = 10\text{ k}\Omega$ are plotted on Fig. 7.16.

a. For $R_S = 100\ \Omega$:

$$I_{D_Q} \cong \mathbf{6.4\ mA}$$

and from Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

b. For $R_S = 10\text{ k}\Omega$

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

and from Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

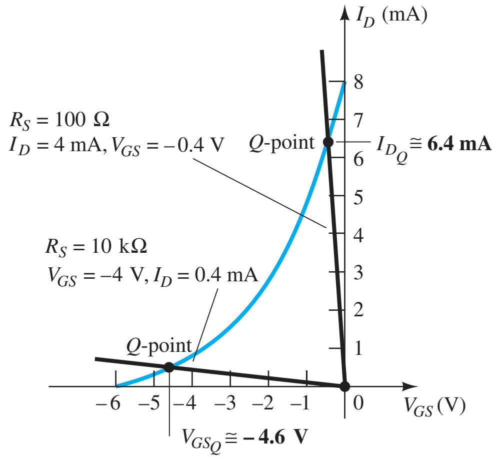


FIG. 7.16
Example 7.3.

7.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.17. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.

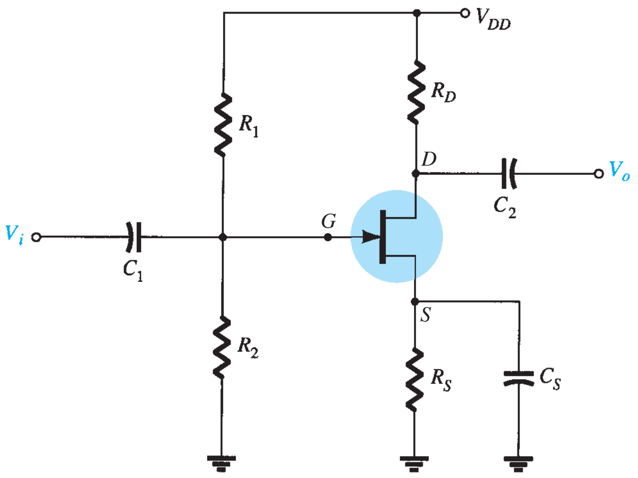


FIG. 7.17
Voltage-divider bias arrangement.

The network of Fig. 7.17 is redrawn as shown in Fig. 7.18 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent in Fig. 7.18b. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule and Fig. 7.18a as follows:

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \tag{7.15}$$

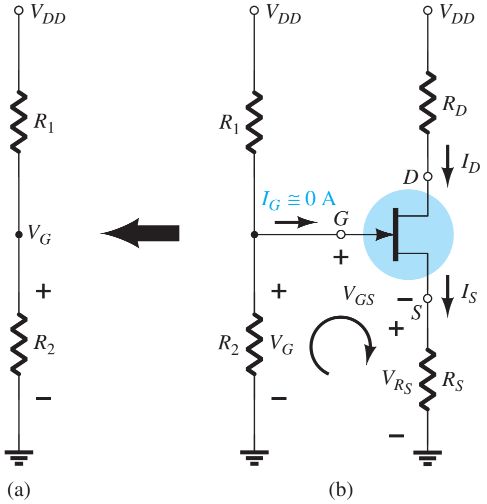


FIG. 7.18
Redrawn network of Fig. 7.17 for dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 7.18 results in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.19 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (7.16) and finding the resulting value of V_{GS} as follows:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= V_G - (0\text{ mA})R_S \end{aligned}$$

and

$$\boxed{V_{GS} = V_G\big|_{I_D = 0\text{ mA}}} \tag{7.17}$$

The result specifies that whenever we plot Eq. (7.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 7.19.

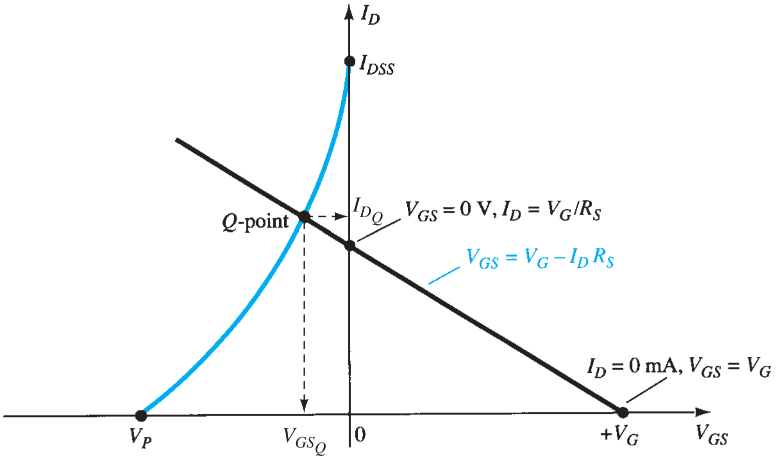


FIG. 7.19
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ 0\text{ V} &= V_G - I_D R_S \end{aligned}$$

and

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\text{ V}}} \tag{7.18}$$

The result specifies that whenever we plot Eq. (7.16), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (7.18). This intersection also appears on Fig. 7.19.

The two points defined above permit the drawing of a straight line to represent Eq. (7.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as

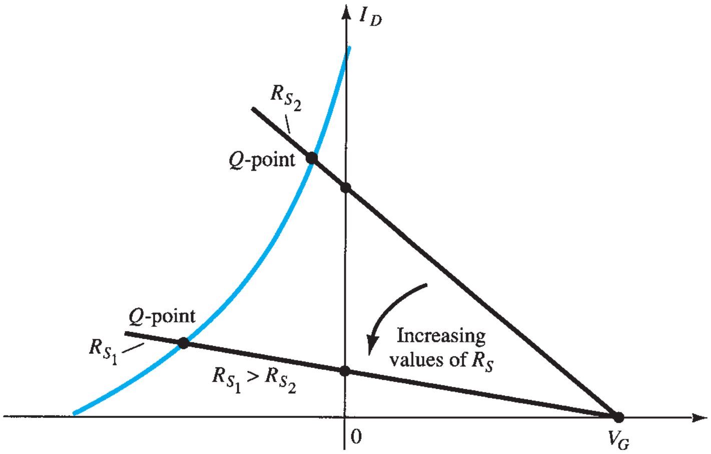


FIG. 7.20

Effect of R_S on the resulting Q-point.

shown in Fig. 7.20. It is fairly obvious from Fig. 7.20 that:

Increasing values of R_S result in lower quiescent values of I_D and declining values of V_{GS}.

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \tag{7.19}$$

$$\boxed{V_D = V_{DD} - I_DR_D} \tag{7.20}$$

$$\boxed{V_S = I_DR_S} \tag{7.21}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}} \tag{7.22}$$

EXAMPLE 7.4 Determine the following for the network of Fig. 7.21:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

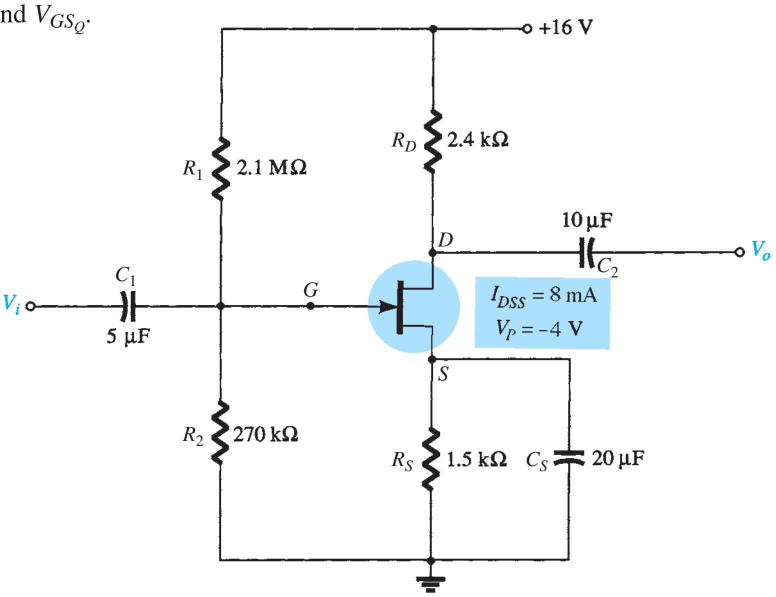

+16 V
R_D 2.4 kΩ
R_1 2.1 MΩ
10 μF
D
C_2
V_o
C_1
V_i
5 μF
G
I_{DSS} = 8 mA
V_P = −4 V
S
R_2 270 kΩ
R_S 1.5 kΩ
C_S 20 μF

FIG. 7.21

Example 7.4.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$V_G = \frac{R_2V_{DD}}{R_1 + R_2} = \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega} = 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_DR_S = 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

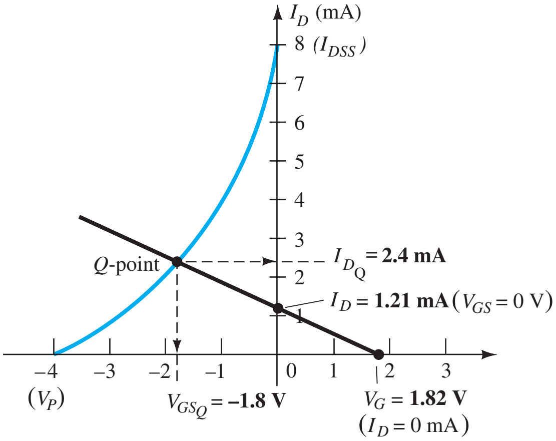


FIG. 7.22

Determining the Q-point for the network of Fig. 7.21.

When $I_D = 0\text{ mA}$,

$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0\text{ V}$,

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8\text{ V}}$$

b. $V_D = V_{DD} - I_DR_D$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$
$= \mathbf{10.24\text{ V}}$

c. $V_S = I_DR_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$
$= \mathbf{3.6\text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$
$= \mathbf{6.64\text{ V}}$

or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$
$= \mathbf{6.64\text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$\begin{aligned} V_{DG} &= V_D - V_G \\ &= 10.24\text{ V} - 1.82\text{ V} \\ &= \mathbf{8.42\text{ V}} \end{aligned}$$

7.5 COMMON-GATE CONFIGURATION

The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown in Fig. 7.23a. The network can also be drawn as shown in Fig. 7.23b.

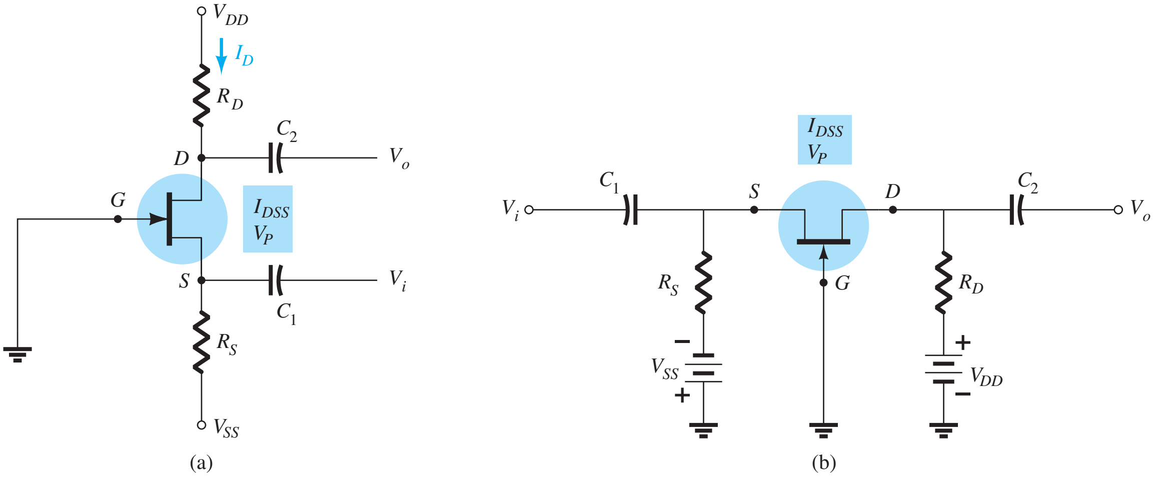


FIG. 7.23

Two versions of the common-gate configuration.

The network equation can be determined using Fig. 7.24.

Applying Kirchhoff's voltage law in the direction shown in Fig. 7.24 will result in

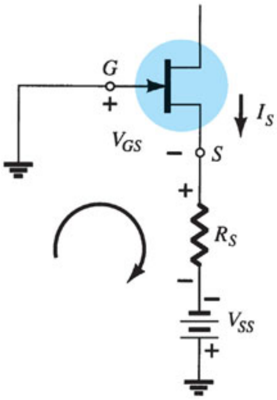


FIG. 7.24

Determining the network equation for the configuration of Fig. 7.23.

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

and
$$V_{GS} = V_{SS} - I_S R_S$$

but
$$I_S = I_D$$

so
$$\boxed{V_{GS} = V_{SS} - I_D R_S} \tag{7.23}$$

Applying the condition $I_D = 0$ mA to Eq. 7.23 will result in

$$V_{GS} = V_{SS} - (0)R_S$$

and
$$\boxed{V_{GS} = V_{SS}\big|_{I_D = 0\text{mA}}} \tag{7.24}$$

Applying the condition $V_{GS} = 0$ V to Eq. 7.23 will result in

$$0 = V_{SS} - I_D R_S$$

and
$$\boxed{I_D = \frac{V_{SS}}{R_S}\bigg|_{V_{GS}=0\text{ V}}} \tag{7.25}$$

The resulting load-line appears in Fig. 7.25 intersecting the transfer curve for the JFET as shown in the figure.

The resulting intersection defines the operating current I_{D_Q} and voltage V_{D_Q} for the network as also indicated in the network.

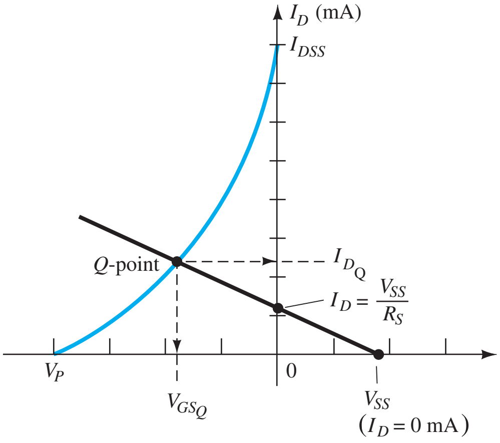


FIG. 7.25

Determining the Q-point for the network of Fig. 7.24.

Applying Kirchhoff's voltage law around the loop containing the two sources, the JFET and the resistors R_D and R_S in Fig. 7.23a and Fig. 7.23b will result in

$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting $I_S = I_D$ we have

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

so that

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \tag{7.26}$$

with

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{7.27}$$

and

$$\boxed{V_S = -V_{SS} + I_D R_S} \tag{7.28}$$

EXAMPLE 7.5 Determine the following for the common-gate configuration of Fig. 7.26:

a. V_{GS_Q}
b. I_{D_Q}
c. V_D
d. V_G
e. V_S
f. V_{DS}

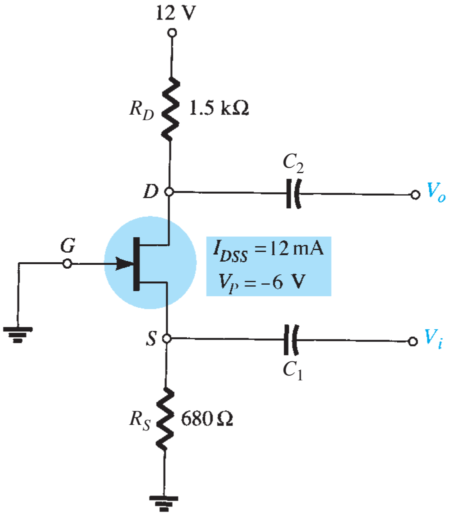


FIG. 7.26

Example 7.5.

Solution: Even though V_{SS} is not present in this common-gate configuration the equations derived above can still be used by simply substituting $V_{SS} = 0\text{ V}$ into each equation in which it appears.

a. For the transfer characteristics Eq. 7.23 becomes

$$V_{GS} = 0 - I_D R_S$$

and $$V_{GS} = -I_D R_S$$

For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing $I_D = 6\text{ mA}$ and solving for V_{GS} will result in the following:

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 7.27.

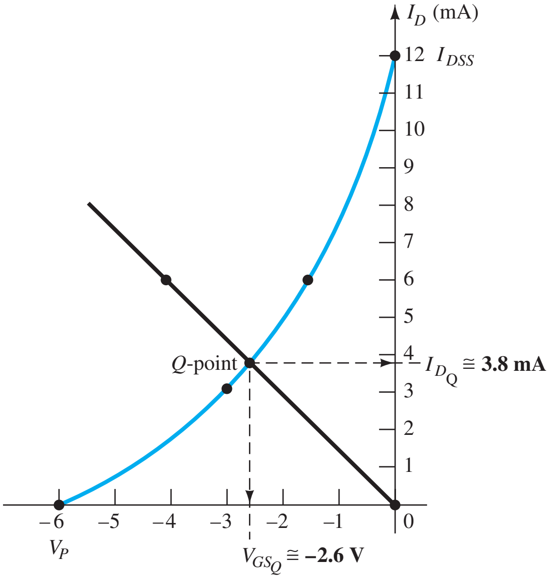


FIG. 7.27

Determining the Q-point for the network of Fig. 7.26.

The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}(\text{at } V_P/2)$$

and $$V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = -1.8\text{ V (at } I_D = I_{DSS}/2)$$

The resulting solution is:

$$V_{GS_Q} \cong \mathbf{-2.6\ V}$$

b. From Fig. 7.27,

$$I_{D_Q} \cong \mathbf{3.8\ mA}$$

c. $$\begin{aligned} V_D &= V_{DD} - I_D R_D \\ &= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V} \\ &= \mathbf{6.3\ V} \end{aligned}$$

d. $V_G = \mathbf{0\ V}$

e. $$\begin{aligned} V_S &= I_D R_S = (3.8\text{ mA})(680\ \Omega) \\ &= \mathbf{2.58\ V} \end{aligned}$$

f. $$\begin{aligned} V_{DS} &= V_D - V_S \\ &= 6.3\text{ V} - 2.58\text{ V} \\ &= \mathbf{3.72\ V} \end{aligned}$$

7.6 SPECIAL CASE: $V_{GS_Q} = 0$ V

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 7.28. Note that direct connection of the gate and source terminals to ground resulting in $V_{GS} = 0$ V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at $V_{GS_Q} = 0$ V as shown in Fig. 7.29.

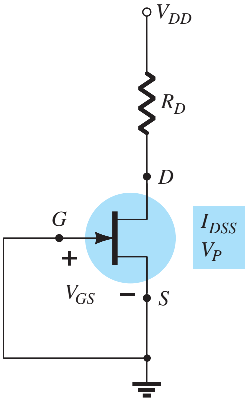


FIG. 7.28

Special case $V_{GS_Q} = 0$ V configuration.

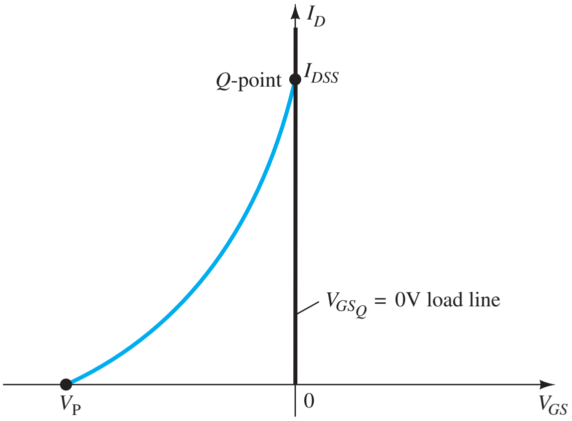


FIG. 7.29

Finding the Q-point for the network of Fig. 7.28.

Since the transfer curve of a JFET will cross the vertical axis at I_{DSS} the drain current for the network is set at that level.

Therefore,
$$\boxed{I_{D_Q} = I_{DSS}} \tag{7.29}$$

Applying Kirchhoff's voltage law:
$$V_{DD} - I_D R_D - V_{DS} = 0$$

and
$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{7.30}$$

with
$$\boxed{V_D = V_{DS}} \tag{7.31}$$

and
$$\boxed{V_S = 0 \text{ V}} \tag{7.32}$$

7.7 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

EXAMPLE 7.6 For the *n*-channel depletion-type MOSFET of Fig. 7.30, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

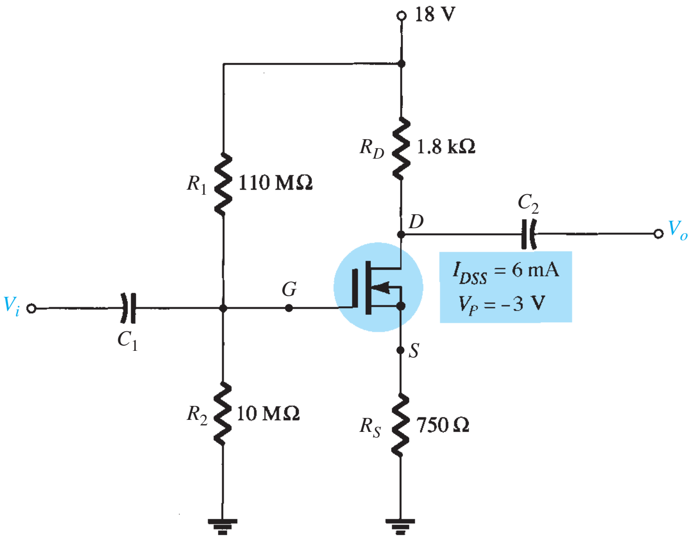


FIG. 7.30

Example 7.6.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778) \\ &= 10.67\text{ mA} \end{aligned}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (7.16):}\ V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

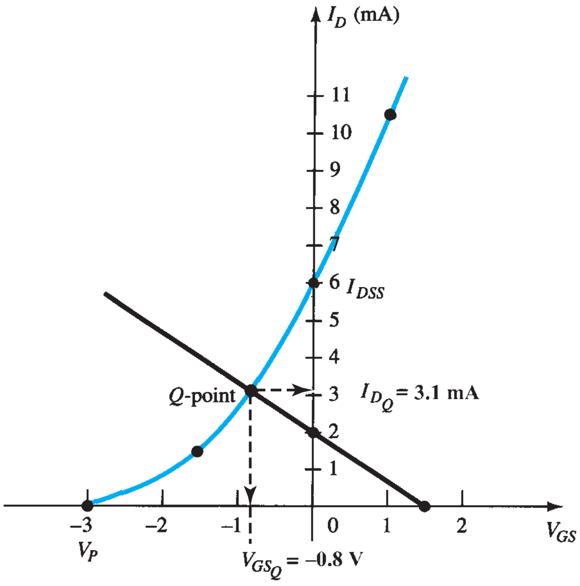


FIG. 7.31

Determining the Q-point for the network of Fig. 7.30.

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\ mA}$$
$$V_{GS_Q} = \mathbf{-0.8\ V}$$

b. Eq. (7.19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega) \\ &\cong \mathbf{10.1\ V} \end{aligned}$$

EXAMPLE 7.7 Repeat Example 7.6 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

$$V_{GS} = V_G - I_DR_S = 1.5\text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$

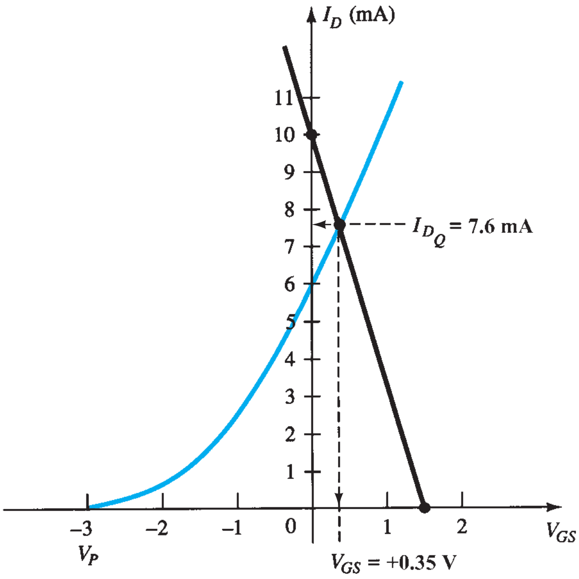


FIG. 7.32

Example 7.7.

The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\ mA}$$
$$V_{GS_Q} = \mathbf{+0.35\ V}$$

b. Eq. (7.19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega) \\ &= \mathbf{3.18\ V} \end{aligned}$$

EXAMPLE 7.8 Determine the following for the network of Fig. 7.33:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

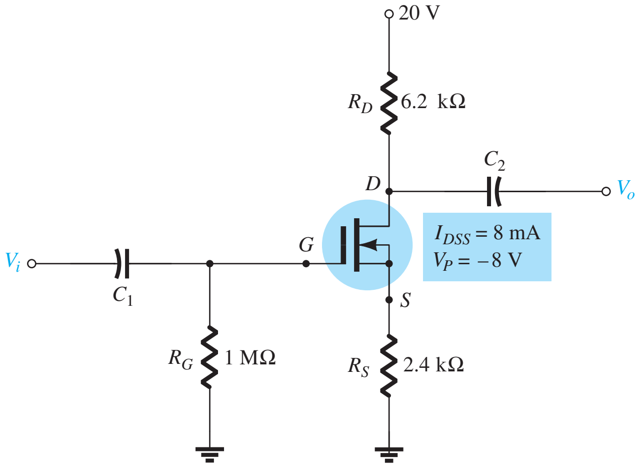


FIG. 7.33
Example 7.8.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and $$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$
$= \mathbf{9.46\text{ V}}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

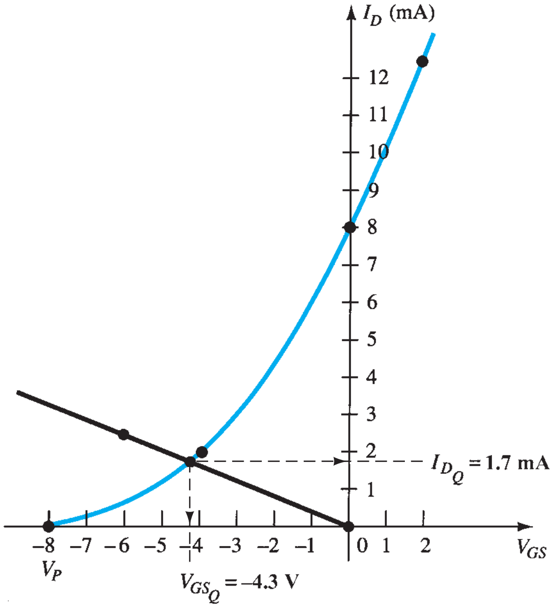


FIG. 7.34
Determining the Q-point for the network of Fig. 7.33.

EXAMPLE 7.9 Determine V_{DS} for the network of Fig. 7.35.

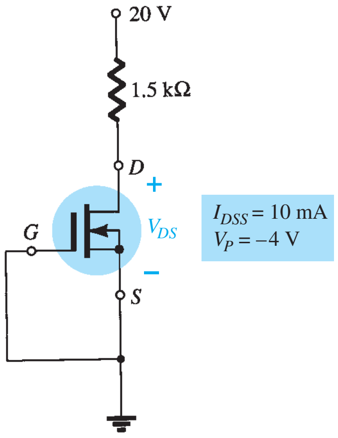


FIG. 7.35
Example 7.9.

Solution: The direct connection between the gate and source terminals requires that

$$V_{GS} = 0\text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0\ V}$$

and

$$I_{D_Q} = \mathbf{10\ mA}$$

There is therefore no need to draw the transfer curve, and

$$\begin{aligned} V_D &= V_{DD} - I_D R_D = 20\text{ V} - (10\text{ mA})(1.5\text{ k}\Omega) \\ &= 20\text{ V} - 15\text{ V} \\ &= \mathbf{5\ V} \end{aligned}$$

7.8 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(\text{Th})}$, as shown in Fig. 7.36. For levels of V_{GS} greater than $V_{GS(\text{Th})}$, the drain current is defined by

$$\boxed{I_D = k(V_{GS} - V_{GS(\text{Th})})^2} \qquad \textbf{(7.33)}$$

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(\text{on})}$) and its corresponding level of $V_{GS(\text{on})}$, two points are defined immediately as shown in Fig. 7.36. To complete the curve, the constant *k* of Eq. (7.33) must be determined from the specification sheet data by substituting into Eq. (7.33) and solving for *k* as follows:

$$\begin{aligned} I_D &= k(V_{GS} - V_{GS(\text{Th})})^2 \\ I_{D(\text{on})} &= k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2 \end{aligned}$$

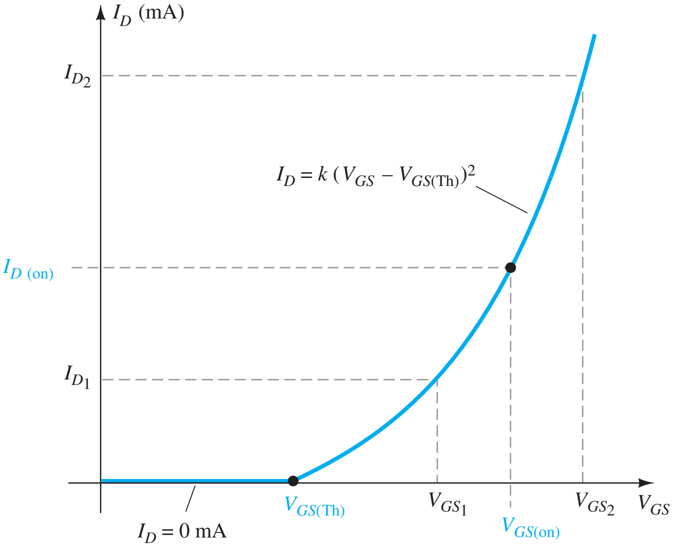


FIG. 7.36

Transfer characteristics of an n-channel enhancement-type MOSFET.

and

$$\boxed{k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}} \tag{7.34}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(\text{Th})}$ and $V_{GS(\text{on})}$ and one just greater than $V_{GS(\text{on})}$ will provide a sufficient number of points to plot Eq. (7.33) (note I_{D_1} and I_{D_2} on Fig. 7.36).

Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 7.37. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA, $V_{R_G} = 0$ V and the dc equivalent network appears as shown in Fig. 7.38.

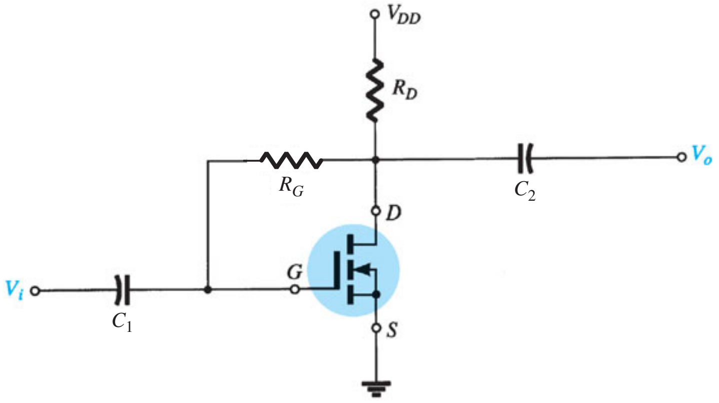


FIG. 7.37

Feedback biasing arrangement.

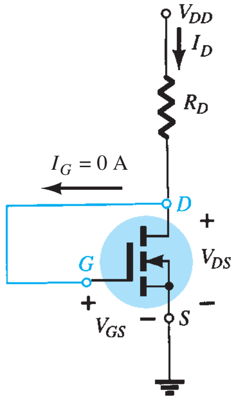


FIG. 7.38

DC equivalent of the network of Fig. 7.37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$\boxed{V_{DS} = V_{GS}} \tag{7.35}$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (7.27):

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \tag{7.36}$$

The result is an equation that relates I_D to V_{GS}, permitting the plot of both on the same set of axes.

Since Eq. (7.36) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0$ mA into Eq. (7.36) gives

$$\boxed{V_{GS} = V_{DD}\big|_{I_D = 0\text{ mA}}} \tag{7.37}$$

Substituting $V_{GS} = 0$ V into Eq. (7.36), we have

$$\boxed{I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\text{ V}}} \tag{7.38}$$

The plots defined by Eqs. (7.33) and (7.36) appear in Fig. 7.39 with the resulting operating point.

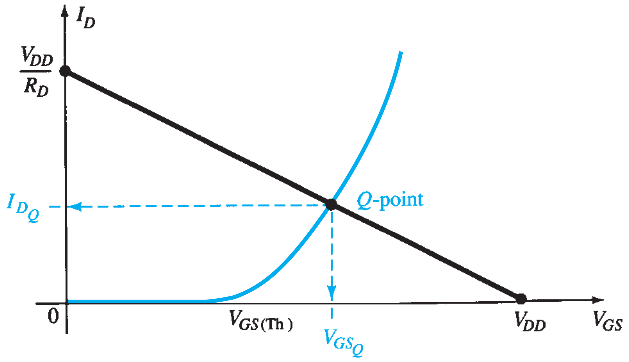


FIG. 7.39
Determining the Q-point for the network of Fig. 7.37.

EXAMPLE 7.10 Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 7.40.

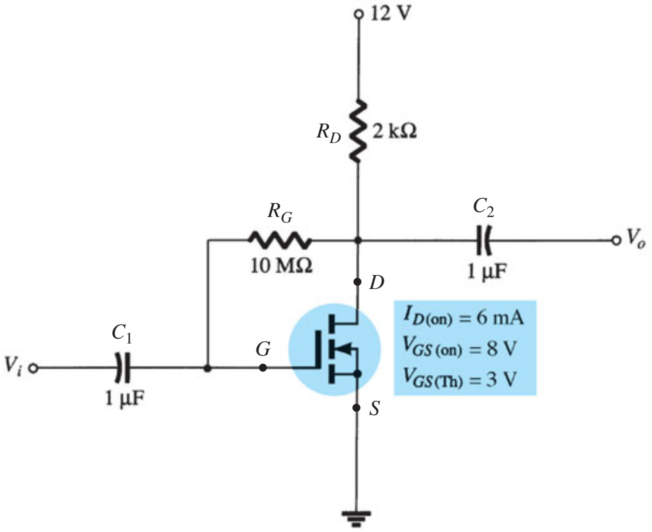

12 V
R_D
2 kΩ
R_G
10 MΩ
C_2
1 μF
V_o
D
C_1
1 μF
V_i
G
S
$I_{D(\text{on})} = 6$ mA
$V_{GS(\text{on})} = 8$ V
$V_{GS(\text{Th})} = 3$ V

FIG. 7.40
Example 7.10.

Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. 7.41. Solving for k, we obtain

$$\text{Eq. (7.34):}\quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$
$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$

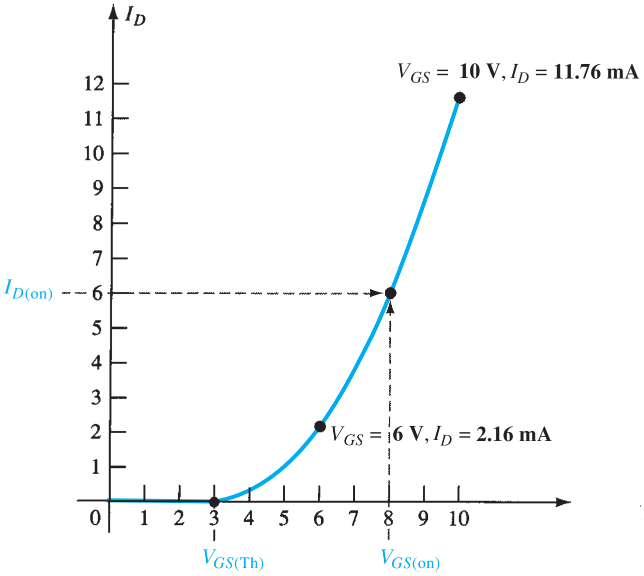


FIG. 7.41
Plotting the transfer curve for the MOSFET of Fig. 7.40.

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$
$$= 2.16\text{ mA}$$

as shown on Fig. 7.41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

as also appearing on Fig. 7.41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.41.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$
$$\text{Eq. (7.37):}\quad V_{GS} = V_{DD} = 12\text{ V}\big|_{I_D = 0\text{ mA}}$$
$$\text{Eq. (7.38):}\quad I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}\big|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 7.42.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\ mA}$$

and
$$V_{GS_Q} = 6.4\text{ V}$$

with
$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\ V}$$

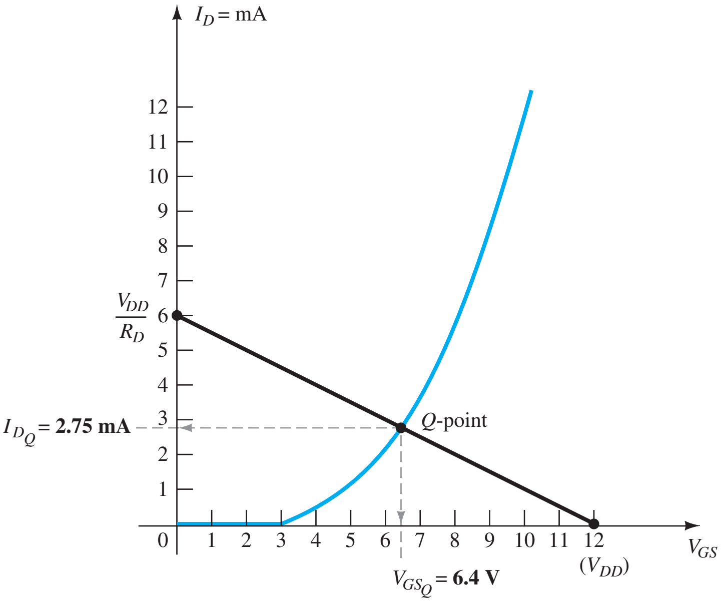


FIG. 7.42

Determining the Q-point for the network of Fig. 7.40.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.43. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \tag{7.39}$$

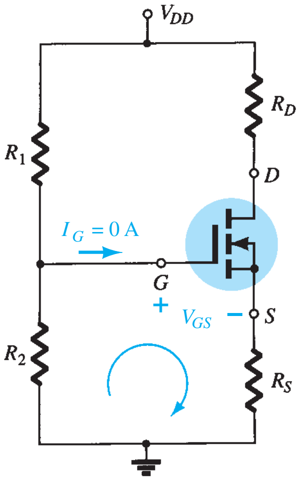


FIG. 7.43

Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.40}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{7.41}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (7.40) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

Solution:

Network

$$\text{Eq. (7.39):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$\text{Eq. (7.40):} \quad V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

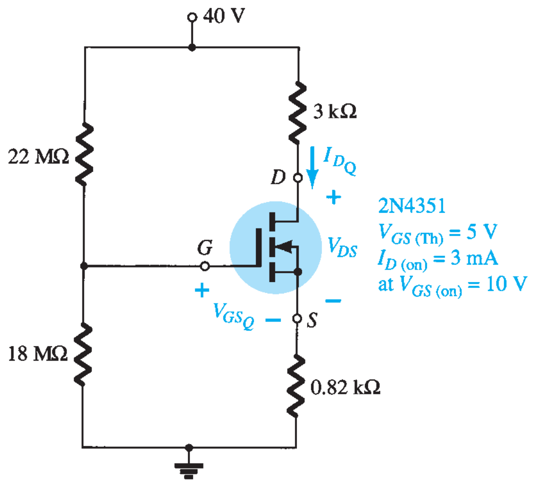

40 V
3 kΩ
22 MΩ
I_{D_Q}
D
+
2N4351
$V_{GS\,(\text{Th})} = 5$ V
$I_{D\,(\text{on})} = 3$ mA
at $V_{GS\,(\text{on})} = 10$ V
G
V_{DS}
+
V_{GS_Q} –
–
S
18 MΩ
0.82 kΩ

FIG. 7.44

Example 7.11.

When $I_D = 0$ mA,

$$V_{GS} = 18\text{ V} - (0\text{ mA})(0.82\text{ k}\Omega) = 18\text{ V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0$ V,

$$\begin{aligned} V_{GS} &= 18\text{ V} - I_D(0.82\text{ k}\Omega) \\ 0 &= 18\text{ V} - I_D(0.82\text{ k}\Omega) \\ I_D &= \frac{18\text{ V}}{0.82\text{ k}\Omega} = 21.95\text{ mA} \end{aligned}$$

as appearing on Fig. 7.45.

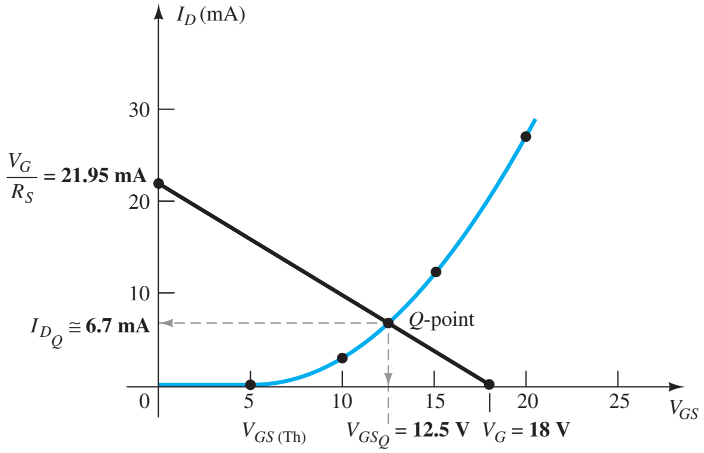


FIG. 7.45

Determining the Q-point for the network of Example 7.11.

Device

$$V_{GS(\text{Th})} = 5\text{ V}, \quad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

$$\text{Eq. (7.34):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} = \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and

$$\begin{aligned} I_D &= k(V_{GS} - V_{GS(\text{Th})})^2 \\ &= 0.12 \times 10^{-3}(V_{GS} - 5)^2 \end{aligned}$$

which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

Eq. (7.41):
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega) \\ &= 40\ \text{V} - 25.6\ \text{V} \\ &= \mathbf{14.4\ V} \end{aligned}$$

7.9 SUMMARY TABLE

Table 7.1 reviews the basic results and demonstrates the similarity in approach for a number of FET configurations. It also reveals that the analysis of dc configurations for FETs is fairly straightforward. Once the transfer characteristics are established, the network bias line can be drawn and the *Q*-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

7.10 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 4 to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

EXAMPLE 7.12 Determine the levels of V_D and V_C for the network of Fig. 7.46.

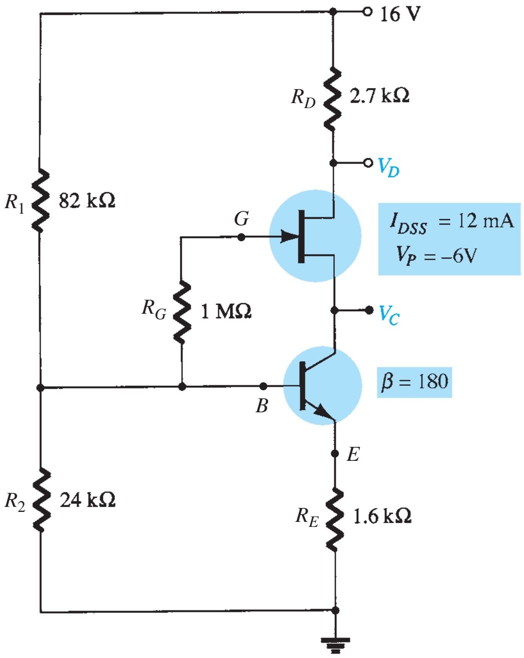
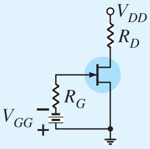
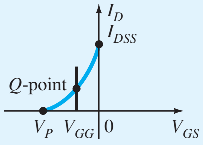
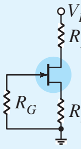
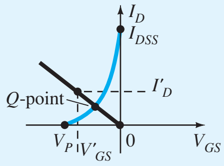
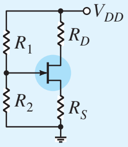
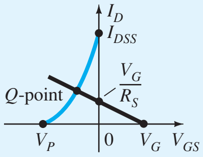
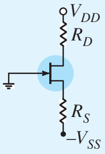
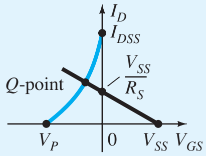
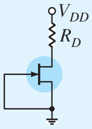
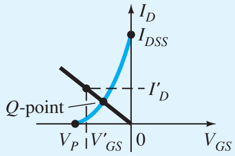
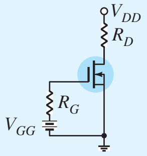
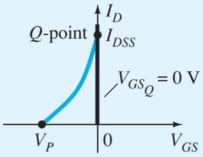
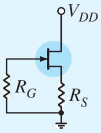
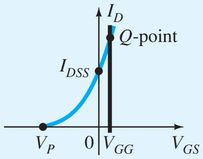
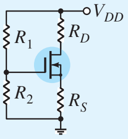
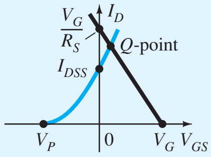
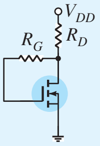
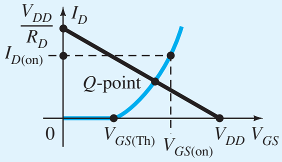
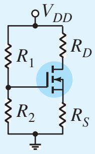
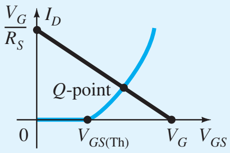


FIG. 7.46
Example 7.12.

TABLE 7.1

FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias	 V_{DD} R_D R_G V_{GG} – +	$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias	 V_{DD} R_1 R_D R_2 R_S	$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate	 V_{DD} R_D R_S $-V_{SS}$	$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GS_Q} = 0$ V)	 V_{DD} R_D R_G V_{GG}	$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)	 V_{DD} R_1 R_D R_2 R_S	$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)	 V_{DD} R_1 R_D R_2 R_S	$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Solution: From experience we now realize that V_{GS} is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since V_{GS} is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ($\beta R_E = 180 \times 1.6\,\text{k}\Omega = 288\,\text{k}\Omega > 10R_2 = 240\,\text{k}\Omega$), permitting a determination of V_B using the voltage-divider rule on the input circuit.

For V_B,

$$V_B = \frac{24\,\text{k}\Omega(16\,\text{V})}{82\,\text{k}\Omega + 24\,\text{k}\Omega} = 3.62\,\text{V}$$

Using the fact that $V_{BE} = 0.7$ V results in

$$\begin{aligned} V_E &= V_B - V_{BE} = 3.62\,\text{V} - 0.7\,\text{V} \\ &= 2.92\,\text{V} \end{aligned}$$

and

$$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92\,\text{V}}{1.6\,\text{k}\Omega} = 1.825\,\text{mA}$$

with

$$I_C \cong I_E = 1.825\,\text{mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and

$$\begin{aligned} V_D &= 16\,\text{V} - I_D(2.7\,\text{k}\Omega) \\ &= 16\,\text{V} - (1.825\,\text{mA})(2.7\,\text{k}\Omega) = 16\,\text{V} - 4.93\,\text{V} \\ &= \mathbf{11.07\,V} \end{aligned}$$

The question of how to determine V_C is not as obvious. Both V_{CE} and V_{DS} are unknown quantities, preventing us from establishing a link between V_D and V_C or from V_E to V_D. A more careful examination of Fig. 7.46 reveals that V_C is linked to V_B by V_{GS} (assuming that $V_{R_G} = 0$ V). Since we know V_B if we can find V_{GS}, V_C can be determined from

$$V_C = V_B - V_{GS}$$

The question then arises as to how to find the level of V_{GS_Q} from the quiescent value of I_D. The two are related by Shockley's equation:

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

and V_{GS_Q} could be found mathematically by solving for V_{GS_Q} and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 7.47. The level of $I_{D_Q} = I_{S_Q} = I_{C_Q} = I_{E_Q}$ is then established by a horizontal line as shown in the same figure. V_{GS_Q} is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GS_Q} = \mathbf{-3.7\,V}$$

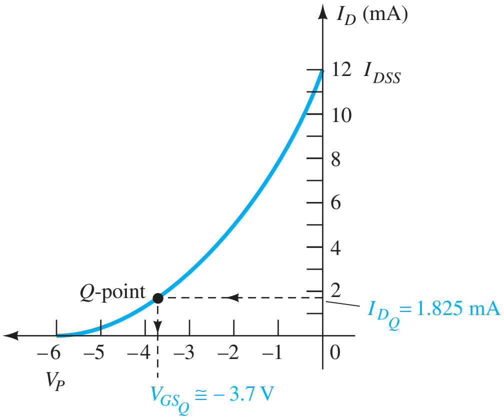


FIG. 7.47

Determining the Q-point for the network of Fig. 7.46.

The level of V_C is given by

$$V_C = V_B - V_{GS_Q} = 3.62\text{ V} - (-3.7\text{ V})$$
$$= \mathbf{7.32\text{ V}}$$

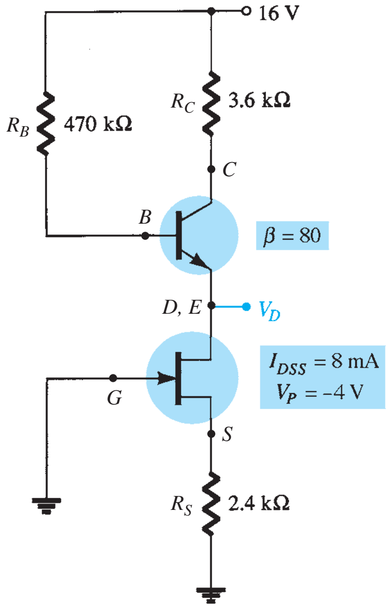


FIG. 7.48
Example 7.13.

EXAMPLE 7.13 Determine V_D for the network of Fig. 7.48.

Solution: In this case, there is no obvious path for determining a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, we can derive an equation for V_{GS} and determine the resulting quiescent point using graphical techniques. That is,

$$V_{GS} = -I_DR_S = -I_D(2.4\text{ k}\Omega)$$

resulting in the self-bias line appearing in Fig. 7.49, which establishes a quiescent point at

$$V_{GS_Q} = -2.4\text{ V}$$
$$I_{D_Q} = 1\text{ mA}$$

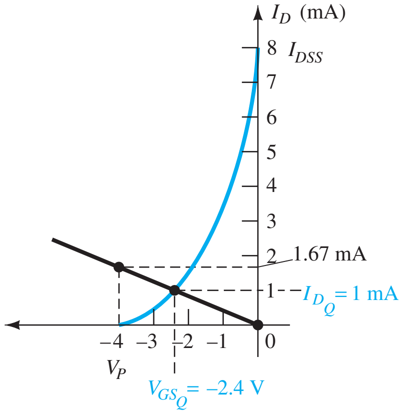


FIG. 7.49
Determining the Q-point for the network of Fig. 7.48.

For the transistor,

$$I_E \cong I_C = I_D = 1\text{ mA}$$

and
$$I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{80} = 12.5\ \mu\text{A}$$

$$V_B = 16\text{ V} - I_B(470\text{ k}\Omega)$$
$$= 16\text{ V} - (12.5\ \mu\text{A})(470\text{ k}\Omega) = 16\text{ V} - 5.88\text{ V}$$
$$= 10.12\text{ V}$$

and
$$V_E = V_D = V_B - V_{BE}$$
$$= 10.12\text{ V} - 0.7\text{ V}$$
$$= \mathbf{9.42\text{ V}}$$

7.11 DESIGN

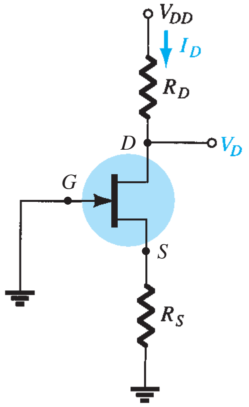


FIG. 7.50
Self-bias configuration to be designed.

The design process is a function of the area of application, level of amplification desired, signal strength, and operating conditions. The first step is normally to establish the proper dc levels of operation.

For example, if the levels of V_D and I_D are specified for the network of Fig. 7.50, the level of V_{GS_Q} can be determined from a plot of the transfer curve and R_S can then be determined from $V_{GS} = -I_DR_S$. If V_{DD} is specified, the level of R_D can then be calculated from $R_D = (V_{DD} - V_D)/I_D$. Of course, the values of R_S and R_D may not be standard commercial values, requiring that the nearest commercial values be employed. However, with the tolerance (range of values) normally specified for the parameters of a network, the slight variation due to the choice of standard values will seldom cause a real concern in the design process.

The above is only one possibility for the design phase involving the network of Fig. 7.50. It is possible that only V_{DD} and R_D are specified together with the level of V_{DS}. The device to be employed may have to be specified along with the level of R_S. It appears logical that the device chosen should have a maximum V_{DS} greater than the specified value by a safe margin.

In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cutoff (V_P) regions. Levels of V_{GS_Q} close to $V_P/2$ or levels of I_{D_Q} near $I_{DSS}/2$ are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of I_D and V_{DS} as appearing on the specification sheet must not be exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as R_D, R_S, V_{DD}, and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$\boxed{R_{\text{unknown}} = \frac{V_R}{I_R}} \tag{7.42}$$

where V_R and I_R are often parameters that can be found directly from the specified voltage and current levels.

EXAMPLE 7.14 For the network of Fig. 7.51, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

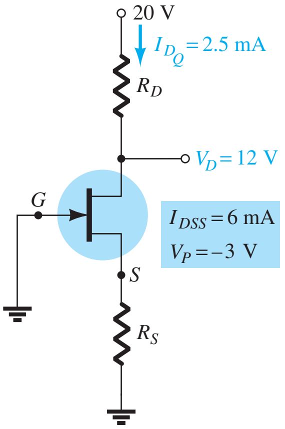


FIG. 7.51
Example 7.14.

Solution: As defined by Eq. (7.42),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\text{ V} - 12\text{ V}}{2.5\text{ mA}} = \frac{8\text{ V}}{2.5\text{ mA}} = \mathbf{3.2\ k\Omega}$$

Plotting the transfer curve in Fig. 7.52 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA results in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_DR_S$ establishes the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\text{ V})}{2.5\text{ mA}} = \mathbf{0.4\ k\Omega}$$

The nearest standard commercial values are

$$R_D = 3.2\text{ k}\Omega \Rightarrow \mathbf{3.3\ k\Omega}$$
$$R_S = 0.4\text{ k}\Omega \Rightarrow \mathbf{0.39\ k\Omega}$$

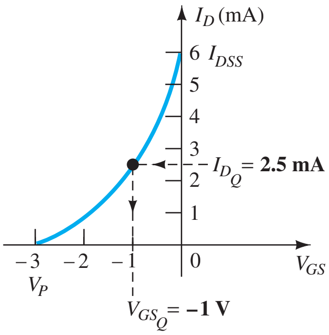


FIG. 7.52
Determining V_{GS_Q} for the network of Fig. 7.51.

EXAMPLE 7.15 For the voltage-divider bias configuration of Fig. 7.53, if $V_D = 12$ V and $V_{GS_Q} = -2$ V, determine the value of R_S.

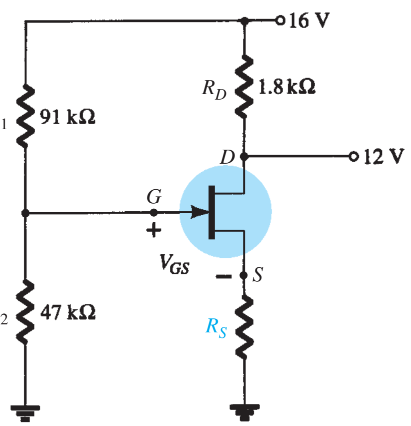


FIG. 7.53
Example 7.15.

Solution: The level of V_G is determined as follows:

$$V_G = \frac{47\text{ k}\Omega(16\text{ V})}{47\text{ k}\Omega + 91\text{ k}\Omega} = 5.44\text{ V}$$

with

$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$= \frac{16\text{ V} - 12\text{ V}}{1.8\text{ k}\Omega} = 2.22\text{ mA}$$

The equation for V_{GS} is then written and the known values substituted:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ -2\text{ V} &= 5.44\text{ V} - (2.22\text{ mA})R_S \\ -7.44\text{ V} &= -(2.22\text{ mA})R_S \end{aligned}$$

and

$$R_S = \frac{7.44\text{ V}}{2.22\text{ mA}} = \mathbf{3.35\text{ k}\Omega}$$

The nearest standard commercial value is 3.3 kΩ.

EXAMPLE 7.16 The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(\text{on})}$ for the network of Fig. 7.54. Determine the levels of V_{DD} and R_D.

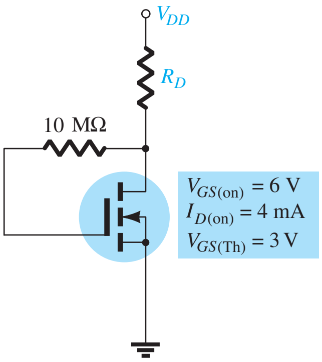

V_{DD}
R_D
10 MΩ
$V_{GS(\text{on})} = 6$ V
$I_{D(\text{on})} = 4$ mA
$V_{GS(\text{Th})} = 3$ V

FIG. 7.54
Example 7.16.

Solution: Given $I_D = I_{D(\text{on})} = 4$ mA and $V_{GS} = V_{GS(\text{on})} = 6$ V, for this configuration,

$$V_{DS} = V_{GS} = \tfrac{1}{2}V_{DD}$$

and

$$6\text{ V} = \tfrac{1}{2}V_{DD}$$

so that

$$V_{DD} = \mathbf{12\text{ V}}$$

Applying Eq. (7.42) yields

$$R_D = \frac{V_{R_D}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(\text{on})}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(\text{on})}} = \frac{\frac{1}{2}V_{DD}}{I_{D(\text{on})}}$$

and

$$R_D = \frac{6\text{ V}}{4\text{ mA}} = \mathbf{1.5\text{ k}\Omega}$$

which is a standard commercial value.

7.12 TROUBLESHOOTING

How often has a network been carefully constructed only to find that when the power is applied, the response is totally unexpected and fails to match the theoretical calculations? What is the next step? Is it a bad connection? A misreading of the color code for a resistive element? An error in the construction process? The range of possibilities seems vast and often frustrating. The troubleshooting process first described in the analysis of BJT transistor configurations should narrow down the list of possibilities and isolate the problem area following a definite plan of attack. In general, the process begins with a rechecking of the network construction and the terminal connections. This is usually followed by the checking of voltage levels between specific terminals and ground or between terminals of the network. Seldom are current levels measured since such maneuvers require disturbing the network structure to insert the meter. Of course, once the voltage levels are obtained, current levels can be calculated using Ohm's law. In any case, some idea of the expected voltage or current level must be known for the measurement to have any importance. In total, therefore, the troubleshooting process can begin with some hope of success only if the basic operation of the network is understood along with some expected levels of voltage or current. For the n-channel JFET amplifier, it is clearly understood that the quiescent value of V_{GS_Q} is limited to 0 V or a negative voltage. For the network of Fig. 7.55, V_{GS_Q} is limited to negative values in the range 0 V to V_P. If a meter is hooked up as shown in Fig. 7.55, with the positive lead (normally red) to the gate and the negative lead (usually black) to the source, the resulting reading should have a negative sign and a magnitude of a few volts. Any other response should be considered suspicious and needs to be investigated.

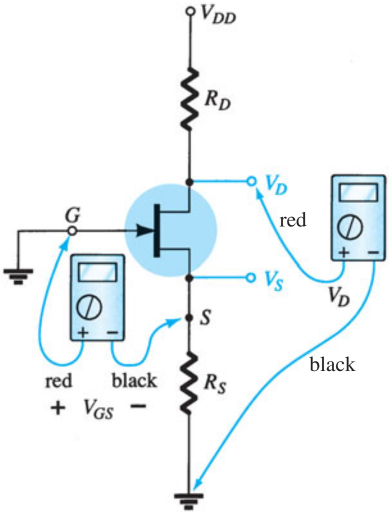


FIG. 7.55
Checking the dc operation of the JFET self-bias configuration.

The level of V_{DS} is typically between 25% and 75% of V_{DD}. A reading of 0 V for V_{DS} clearly indicates that either the output circuit has an "open" or the JFET is internally short-circuited between drain and source. If V_D is V_{DD} volts, there is obviously no drop across R_D, due to the lack of current through R_D, and the connections should be checked for continuity.

If the level of V_{DS} seems inappropriate, the continuity of the output circuit can easily be checked by grounding the negative lead of the voltmeter and measuring the voltage levels from V_{DD} to ground using the positive lead. If $V_D = V_{DD}$, the current through R_D may be zero, but there is continuity between V_D and V_{DD}. If $V_S = V_{DD}$, the device is not open between drain and source, but it is also not "on." The continuity through to V_S is confirmed, however. In this case, it is possible that there is a poor ground connection between R_S and ground that may not be obvious. The internal connection between the wire of the lead and the terminal connector may have separated. Other possibilities also exist, such as a shorted device from drain to source, but the troubleshooter will simply have to narrow down the possible causes for the malfunction.

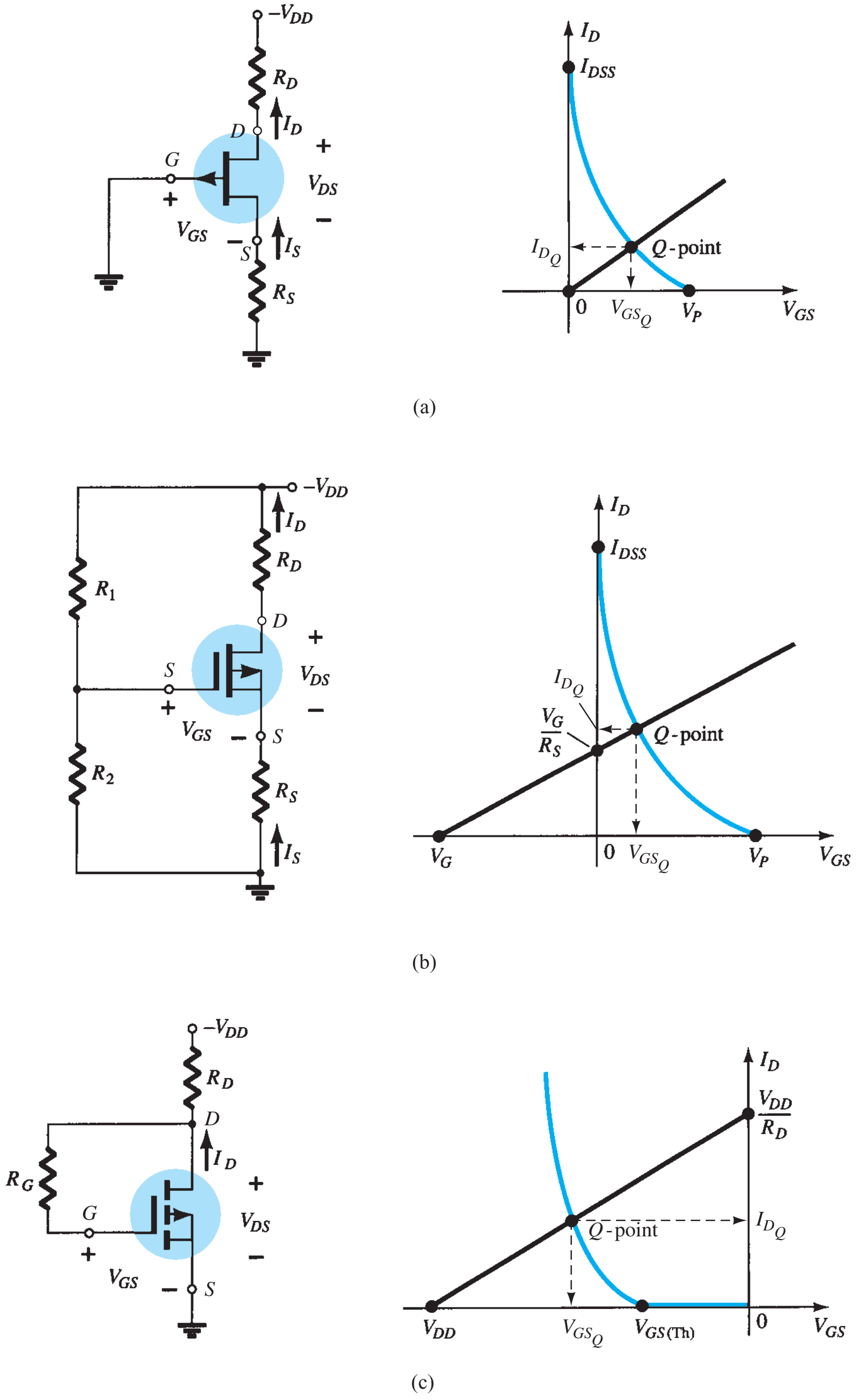
The continuity of a network can also be checked simply by measuring the voltage across any resistor of the network (except for R_G in the JFET configuration). An indication of 0 V immediately reveals the lack of current through the element due to an open circuit in the network.

The most sensitive element in the BJT and JFET configurations is the amplifier itself. The application of excessive voltage during the construction or testing phase or the use of incorrect resistor values resulting in high current levels can destroy the device. If you question the condition of the amplifier, the best test for the FET is the curve tracer since it not only reveals whether the device is operable, but also its range of current and voltage levels. Some testers may reveal that the device is still fundamentally sound but do not reveal whether its range of operation has been severely reduced.

The development of good troubleshooting techniques comes primarily from experience and a level of confidence in what to expect and why. There are, of course, times when the reasons for a strange response seem to disappear mysteriously when you check a network. In such cases, it is best not to breathe a sigh of relief and continue with the construction. The cause for such a sensitive "make or break" situation should be found and corrected, or it may reoccur at the most inopportune moment.

7.13 *p*-CHANNEL FETs

The analysis thus far has been limited solely to n-channel FETs. For p-channel FETs, a mirror image of the transfer curves is employed, and the defined current directions are reversed as shown in Fig. 7.56 for the various types of FETs.


$-V_{DD}$
R_D
I_D
D
G
$+$
V_{DS}
$-$
V_{GS}
S
I_S
R_S
I_D
I_{DSS}
I_{D_Q}
Q-point
0
V_{GS_Q}
V_P
V_{GS}
R_1
R_2
$\frac{V_G}{R_S}$
V_G
R_G
$\frac{V_{DD}}{R_D}$
V_{DD}
$V_{GS(\text{Th})}$

(a)

(b)

(c)

FIG. 7.56

p-Channel configurations: (a) JFET; (b) depletion-type MOSFET; (c) enhancement-type MOSFET.

Note for each configuration of Fig. 7.56 that each supply voltage is now a negative voltage drawing current in the indicated direction. In particular, note that the double-subscript notation for voltages continues as defined for the *n*-channel device: V_{GS}, V_{DS}, and so on. In this case, however, V_{GS} is positive (positive or negative for the depletion-type MOSFET) and V_{DS} negative.

Due to the similarities between the analysis of *n*-channel and *p*-channel devices, one can assume an *n*-channel device and reverse the supply voltage and perform the entire analysis. When the results are obtained, the magnitude of each quantity will be correct, although the current direction and voltage polarities will have to be reversed. However, the next example will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.

EXAMPLE 7.17 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the *p*-channel JFET of Fig. 7.57.

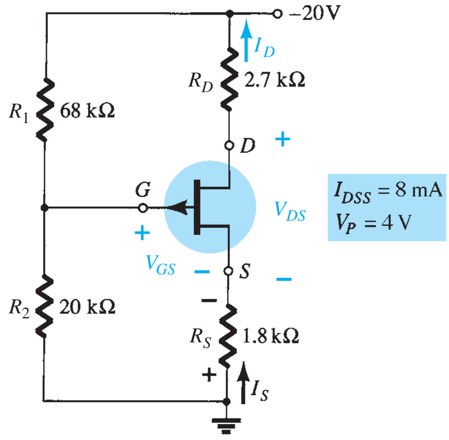


FIG. 7.57
Example 7.17.

Solution: We have

$$V_G = \frac{20\text{ k}\Omega(-20\text{ V})}{20\text{ k}\Omega + 68\text{ k}\Omega} = -4.55\text{ V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0$ mA yields

$$V_{GS} = V_G = -4.55\text{ V}$$

as appearing in Fig. 7.58.

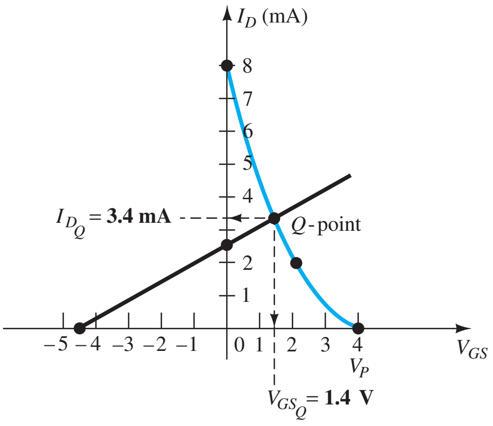


FIG. 7.58
Determining the Q-point for the JFET configuration of Fig. 7.57.

Choosing $V_{GS} = 0$ V, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\text{ V}}{1.8\text{ k}\Omega} = 2.53\text{ mA}$$

as also appearing in Fig. 7.58.

The resulting quiescent point from Fig. 7.58 is given by

$$I_{D_Q} = \mathbf{3.4\ mA}$$
$$V_{GS_Q} = \mathbf{1.4\ V}$$

For V_{DS}, Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\ \text{V} + (3.4\ \text{mA})(2.7\ \text{k}\Omega + 1.8\ \text{k}\Omega) \\ &= -20\ \text{V} + 15.3\ \text{V} \\ &= \mathbf{-4.7\ V} \end{aligned}$$

7.14 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GS_Q}) is provided in Fig. 7.59. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled *m* can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled *M*, is employed along with the *m* scale to find the

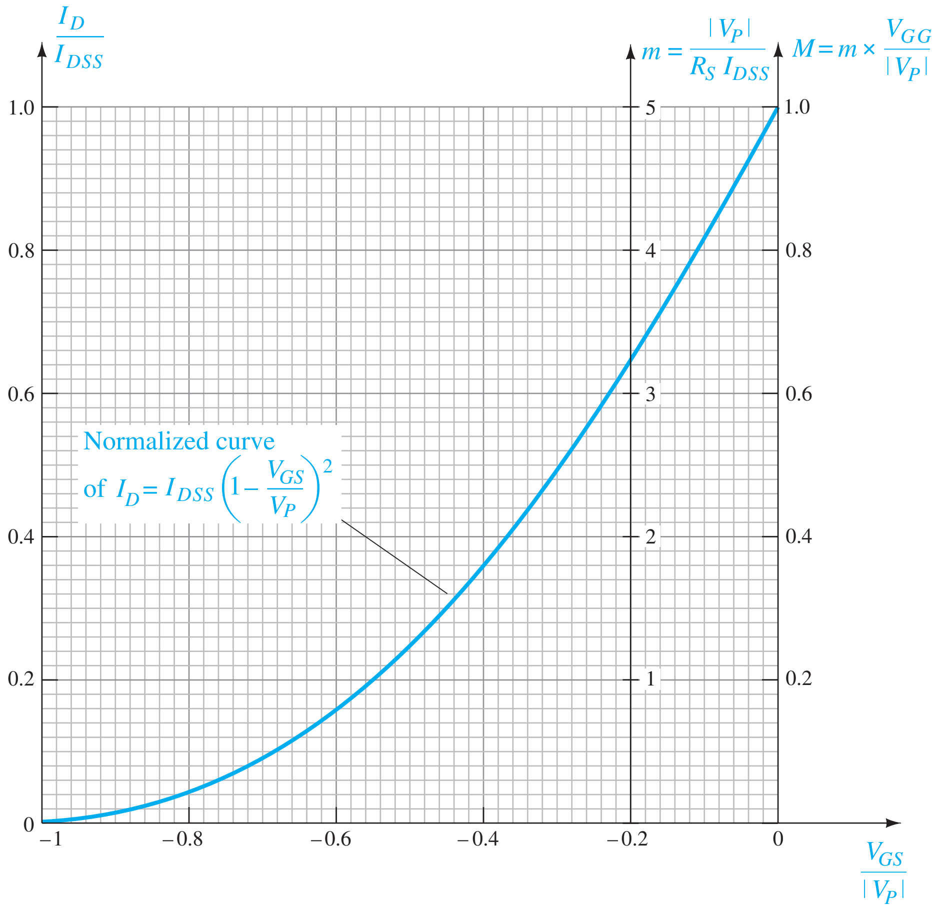


FIG. 7.59

Universal JFET bias curve.

solution to voltage-divider configurations. The scaling for m and M come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the m scale extends from 0 to 5 at $V_{GS}/|V_P| = -0.2$ and the M scale ranges from 0 to 1 at $V_{GS}/|V_P| = 0$, but rather on how to use the resulting scales to obtain a solution for the configurations. The equations for m and M are the following, with V_G as defined by Eq. (7.15):

$$\boxed{m = \frac{|V_P|}{I_{DSS}R_S}} \tag{7.43}$$

$$\boxed{M = m \times \frac{V_G}{|V_P|}} \tag{7.44}$$

with $$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the m and M axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

EXAMPLE 7.18 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.60.

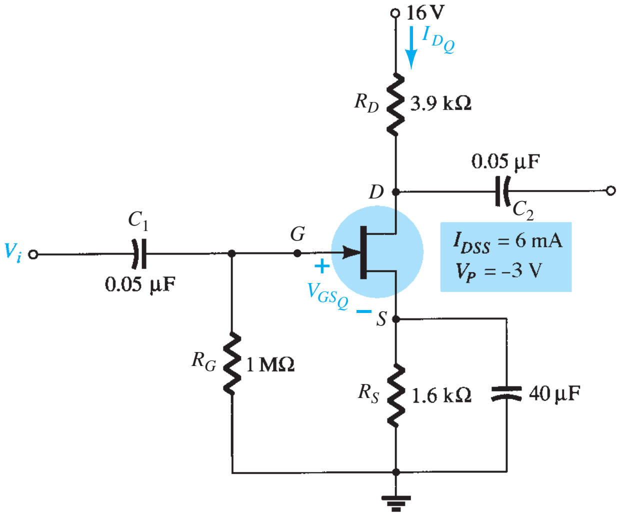


FIG. 7.60
Example 7.18.

Solution: Calculating the value of m, we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3\text{ V}|}{(6\text{ mA})(1.6\text{ k}\Omega)} = 0.31$$

The self-bias line defined by R_S is plotted by drawing a straight line from the origin through a point defined by $m = 0.31$, as shown in Fig. 7.61.

The resulting Q-point:

$$\frac{I_D}{I_{DSS}} = 0.18 \qquad \text{and} \qquad \frac{V_{GS}}{|V_P|} = -0.575$$

The quiescent values of I_D and V_{GS} can then be determined as follows:

$$I_{D_Q} = 0.18 I_{DSS} = 0.18(6\text{ mA}) = \mathbf{1.08\text{ mA}}$$

and $$V_{GS_Q} = -0.575|V_P| = -0.575(3\text{ V}) = \mathbf{-1.73\text{ V}}$$

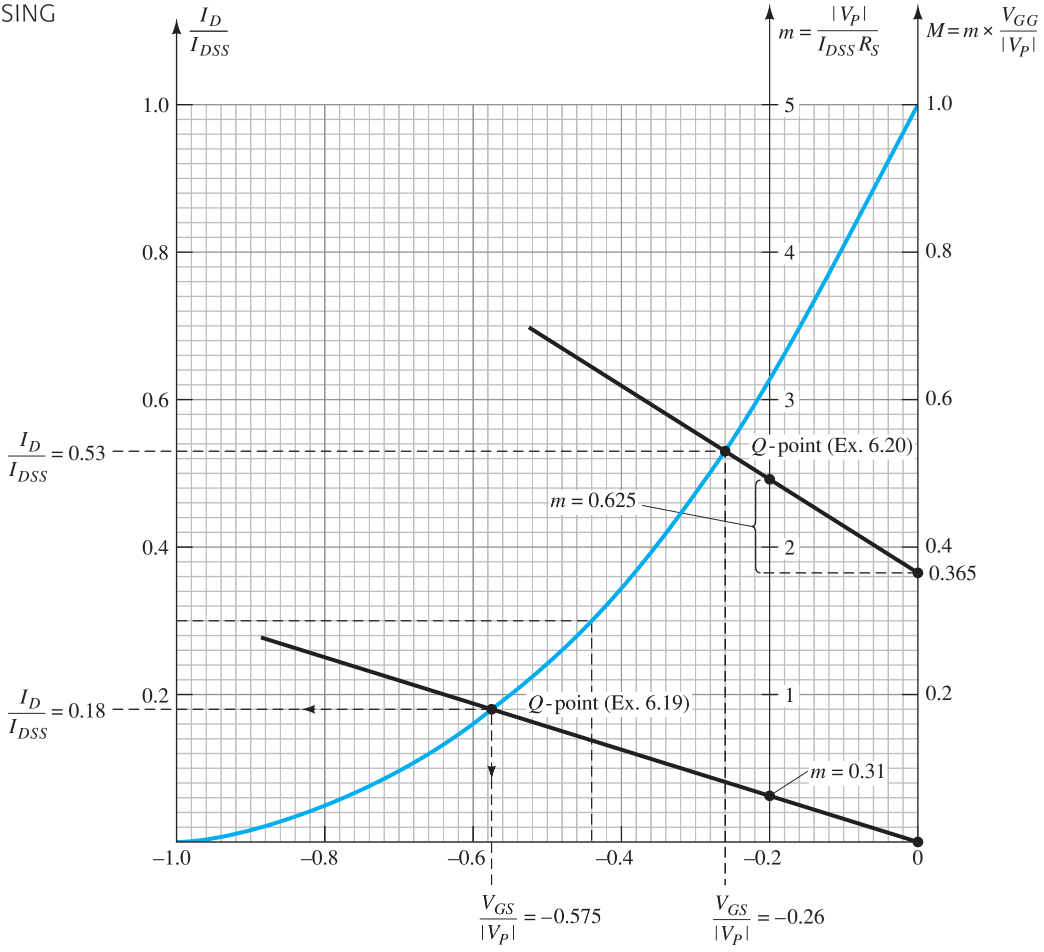


FIG. 7.61

Universal curve for Examples 7.18 and 7.19.

EXAMPLE 7.19 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.62.

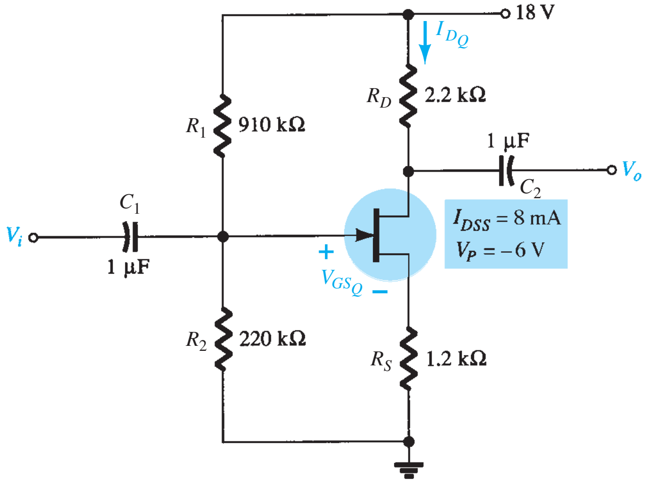

18 V
I_{D_Q}
R_D
2.2 kΩ
R_1
910 kΩ
1 μF
C_2
V_o
C_1
V_i
1 μF
$I_{DSS} = 8$ mA
$V_P = -6$ V
+
V_{GS_Q}
–
R_2
220 kΩ
R_S
1.2 kΩ

FIG. 7.62

Example 7.19.

Solution: Calculating m gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining V_G yields

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(220\text{ k}\Omega)(18\text{ V})}{910\text{ k}\Omega + 220\text{ k}\Omega} = 3.5\text{ V}$$

Finding M, we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625\left(\frac{3.5\text{ V}}{6\text{ V}}\right) = 0.365$$

Now that m and M are known, the bias line can be drawn on Fig. 7.61. In particular, note that even though the levels of I_{DSS} and V_P are different for the two networks, the same universal curve can be employed. First find M on the M axis as shown in Fig. 7.61. Then draw a horizontal line over to the m axis and, at the point of intersection, add the magnitude of m as shown in the figure. Using the resulting point on the m axis and the M intersection, draw the straight line to intersect with the transfer curve and define the Q-point. That is,

$$\frac{I_D}{I_{DSS}} = 0.53 \qquad \text{and} \qquad \frac{V_{GS}}{|V_P|} = -0.26$$

and $$I_{D_Q} = 0.53 I_{DSS} = 0.53(8\text{ mA}) = \mathbf{4.24\text{ mA}}$$

with $$V_{GS_Q} = -0.26|V_P| = -0.26(6\text{ V}) = \mathbf{-1.56\text{ V}}$$

7.15 PRACTICAL APPLICATIONS

The applications described here take full advantage of the high input impedance of field-effect transistors, the isolation that exists between the gate and drain circuits, and the linear region of JFET characteristics that permit approximating the device by a resistive element between the drain and source terminals.

Voltage-Controlled Resistor (Noninverting Amplifier)

One of the most common applications of the JFET is as a variable resistor whose resistance value is controlled by the applied dc voltage at the gate terminal. In Fig. 7.63a, the linear region of a JFET transistor has been clearly indicated. Note that in this region the various curves all start at the origin and follow a fairly straight path as the drain-to-source voltage and drain current increase. Recall from your basic dc courses that **the plot of a fixed resistor is nothing more than a straight line with its origin at the intersection of the axes**.

In Fig. 7.63b, the linear region has been expanded to a maximum drain-to-source voltage of about 0.5 V. Note that even though the curves do have some curvature to them, they can easily be approximated by fairly straight lines, all having their origin at the intersection of the axes and a slope determined by the gate-to-source dc voltage. Recall from earlier discussions that **for an *I–V* plot where the current is the vertical axis and the voltage the horizontal axis, the steeper the slope, the less is the resistance; and the more horizontal the curve, the greater is the resistance**. The result is that a vertical line has 0 Ω resistance and a horizontal line has infinite resistance. At $V_{GS} = 0$ V, the slope is the steepest and the resistance the least. As the gate-to-source voltage becomes increasingly negative, the slope decreases until it is almost horizontal near the pinch-off voltage.

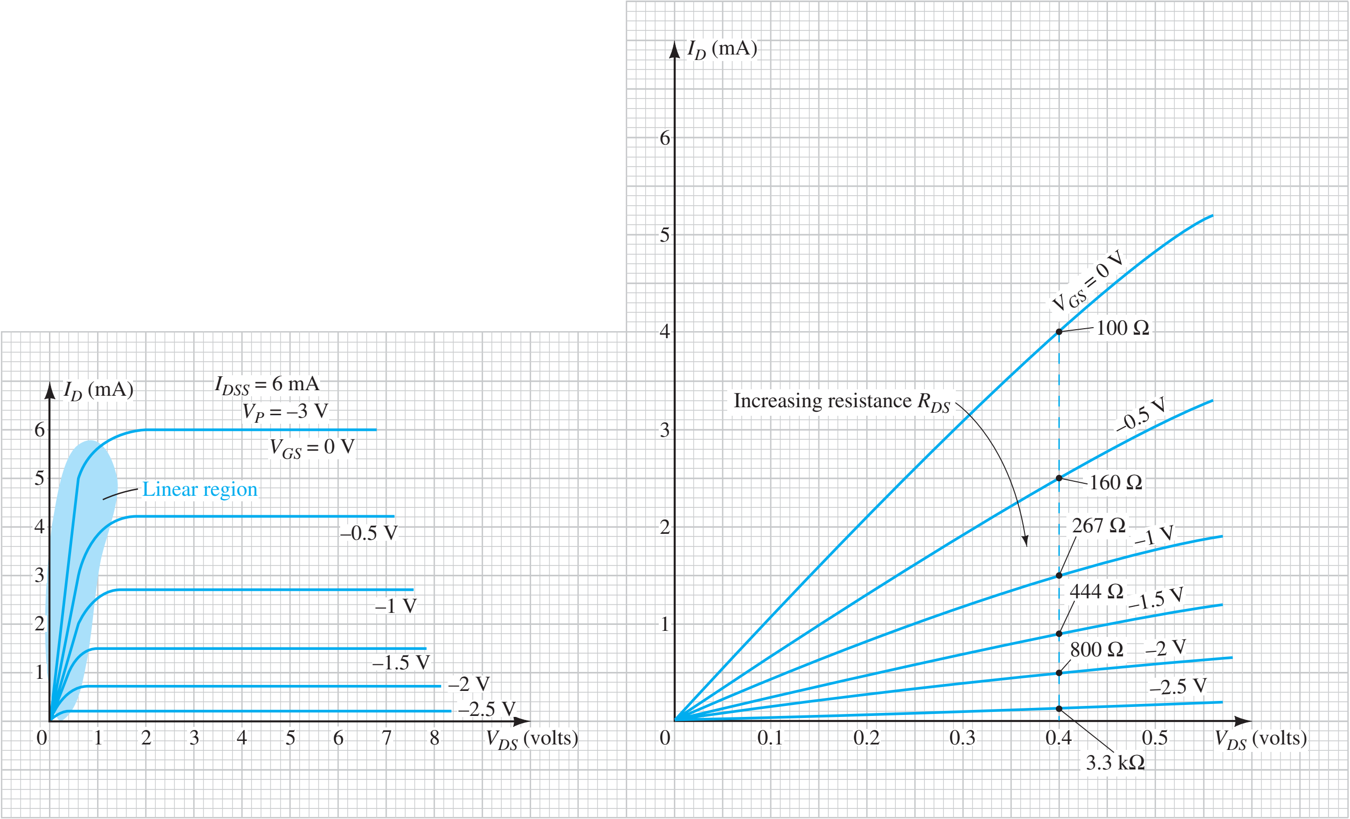
It is important to remember that this linear region is limited to levels of V_{DS} that are relatively small compared to the pinch-off voltage. In general, **the linear region of a JFET is defined by $V_{DS} \ll V_{DS_{\max}}$ and $|V_{GS}| \ll |V_P|$**.

Using Ohm's law, let us calculate the resistance associated with each curve of Fig. 7.63b using the current that results at a drain-to-source voltage of 0.4 V.

$$V_{GS} = 0\text{ V:} \qquad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{4\text{ mA}} = \mathbf{100\ \Omega}$$

$$V_{GS} = -0.5\text{ V:} \qquad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{2.5\text{ mA}} = \mathbf{160\ \Omega}$$

$$V_{GS} = -1\text{ V:} \qquad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{1.5\text{ mA}} = \mathbf{267\ \Omega}$$



(a) (b)

FIG. 7.63

JFET characteristics: (a) defining the linear region; (b) expanding the linear region.

$$V_{GS} = -1.5\text{ V:}\quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.9\text{ mA}} = \mathbf{444\ \Omega}$$

$$V_{GS} = -2\text{ V:}\quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.5\text{ mA}} = \mathbf{800\ \Omega}$$

$$V_{GS} = -2.5\text{ V:}\quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.12\text{ mA}} = \mathbf{3.3\ k\Omega}$$

In particular, note how **the drain-to-source resistance increases as the gate-to-source voltage approaches the pinch-off value**.

The results just obtained can be verified by Eq. (6.1) using the pinch-off voltage of -3 V and $R_o = 100\ \Omega$ at $V_{GS} = 0$ V. We have

$$R_{DS} = \frac{R_o}{\left(1 - \dfrac{V_{GS}}{V_P}\right)^2} = \frac{100\ \Omega}{\left(1 - \dfrac{V_{GS}}{-3\text{ V}}\right)^2}$$

$$V_{GS} = -0.5\text{ V:}\quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-0.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{144\ \Omega}\quad \text{(versus 160 }\Omega\text{ above)}$$

$$V_{GS} = -1\text{ V:}\quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-1\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{225\ \Omega}\quad \text{(versus 267 }\Omega\text{ above)}$$

$$V_{GS} = -1.5\text{ V:}\quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-1.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{400\ \Omega}\quad \text{(versus 444 }\Omega\text{ above)}$$

$$V_{GS} = -2\text{ V}: \quad R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-2\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{900\ \Omega} \quad \text{(versus 800 } \Omega \text{ above)}$$

$$V_{GS} = -2.5\text{ V}: R_{DS} = \frac{100\ \Omega}{\left(1 - \dfrac{-2.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{3.6\ k\Omega} \quad \text{(versus 3.3 k}\Omega \text{ above)}$$

Although the results are not an exact match, for most applications Equation (6.1) provides an excellent approximation to the actual resistance level for R_{DS}.

Keep in mind that **the possible levels of V_{GS} between 0 V and pinch-off are infinite**, resulting in the full range of resistor values between 100 Ω and 3.3 kΩ. In general, therefore, the above discussion is summarized by Fig. 7.64a. For $V_{GS} = 0$ V, the equivalence of Fig. 7.64b would result; for $V_{GS} = -1.5$ V, the equivalence of Fig. 7.64c; and so on.

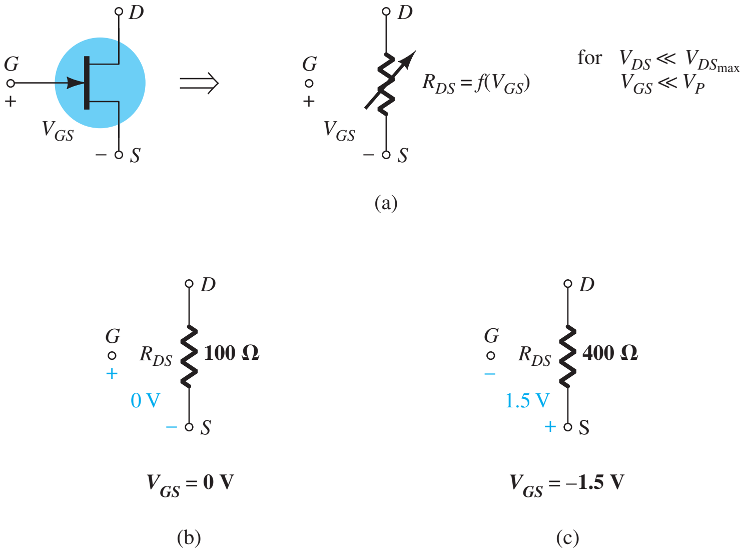
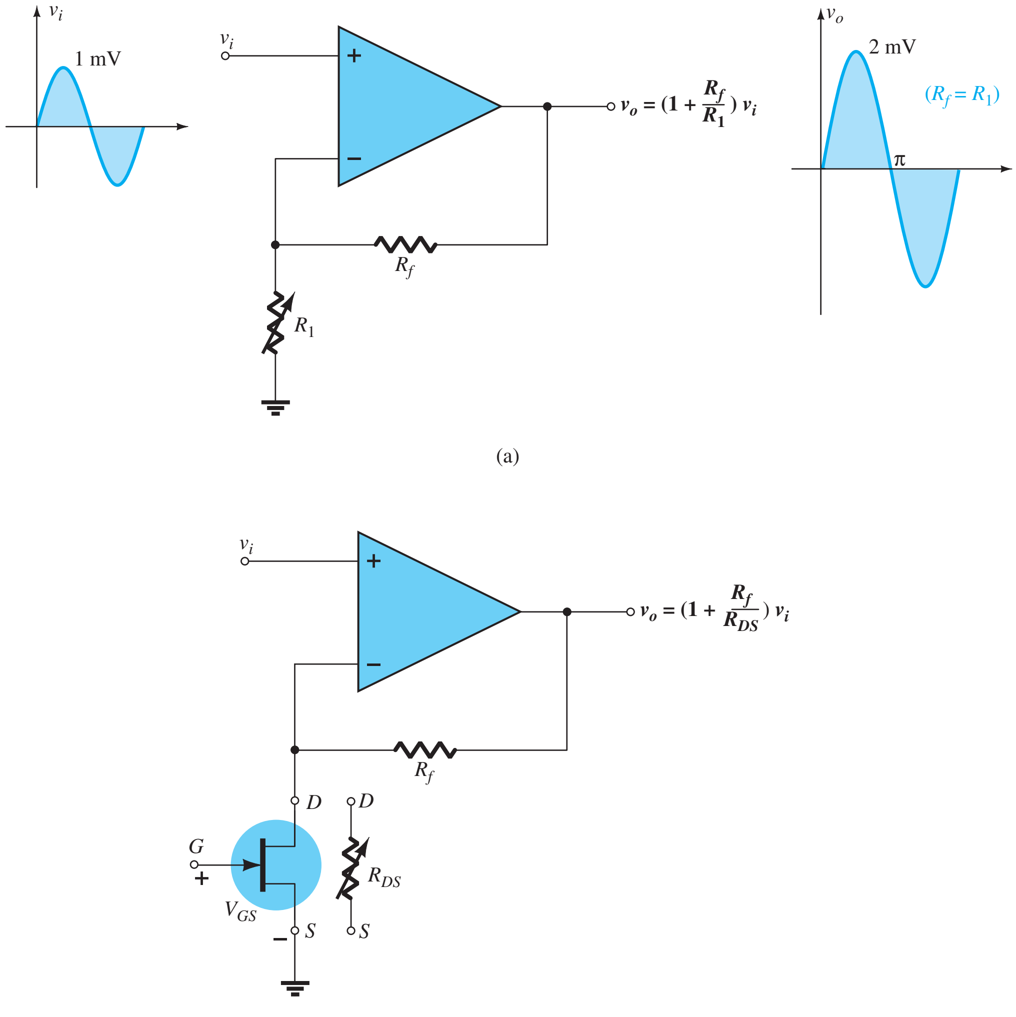


FIG. 7.64

JFET voltage-controlled drain resistance: (a) general equivalence; (b) with $V_{GS} = 0$ V; (c) with $V_{GS} = -1.5$ V.

Let us now investigate the use of this voltage-controlled drain resistance in the noninverting amplifier of Fig. 7.65a—**noninverting indicates that the input and output signals are in phase**. The op-amp of Fig. 7.65a is discussed in detail in Chapter 10, and the equation for the gain is derived in Section 10.4.

If $R_f = R_1$, the resulting gain is 2, as shown by the in-phase sinusoidal signals of Fig. 7.65a. In Fig. 7.65b, the variable resistor has been replaced by an *n*-channel JFET. If $R_f = 3.3\text{ k}\Omega$ and the transistor of Fig. 7.63 were employed, the gain could extend from $1 + 3.3\text{ k}\Omega/3.3\text{ k}\Omega = 2$ to $1 + 3.3\text{ k}\Omega/100\ \Omega = 34$ for V_{GS} varying from −2.5 V to 0 V, respectively. In general, therefore, the gain of the amplifier can be set at any value between 2 and 34 by simply controlling the applied dc biasing voltage. The effect of this type of control can be extended to an extensive variety of applications. For instance, if the battery voltage of a radio should start to drop due to extended use, the dc level at the gate of the controlling JFET will drop, and the level of R_{DS} will decrease also. A drop in R_{DS} will result in an increase in gain for the same value of R_f, and the output volume of the radio can be maintained. A number of oscillators (networks designed to generate sinusoidal signals of specific frequencies) have a resistance factor in the equation for the frequency generated. If the frequency generated should start to drift, a feedback network can be designed that changes the dc level at the gate of a JFET and therefore its drain resistance. If that drain resistance is part of the resistance factor in the frequency equation, the frequency generated can be stabilized or maintained.



(a)

(b)

FIG. 7.65

(a) Noninverting op-amp configuration; (b) using the voltage-controlled drain-to-source resistance of a JFET in the noninverting amplifier.

One of the most important factors that affect the stability of a system is temperature variation. As a system heats up, the usual tendency is for the gain to increase, which in turn will usually cause additional heating and may eventually result in a condition referred to as "thermal runaway." Through proper design, a thermistor can be introduced that will affect the biasing level of a voltage-controlled variable JFET resistor. As the resistance of the thermistor drops with increase in heat, the biasing control of the JFET can be such that the drain resistance changes in the amplifier design to reduce the gain—establishing a balancing effect.

Before leaving the subject of thermal problems, note that some design specifications (often military type) require that systems that are overly sensitive to temperature variations be placed in a "chamber" or "oven" to establish a constant heat level. For instance, a 1-W resistor may be placed in an enclosed area with an oscillator network to establish a constant ambient heat level in the region. The design then centers on this heat level, which would be so high compared to the heat normally generated by the components that the variations in temperature levels of the elements could be ignored and a steady output frequency assured.

Other areas of application include any form of volume control, musical effects, meters, attenuators, filters, stability designs, and so on. One general advantage of this type of stability is that it avoids the need for expensive regulators (Chapter 15) in the overall design, although it should be understood that the purpose of this type of control mechanism is to "fine-tune" rather than to provide the primary source of stability.

For the noninverting amplifier, **one of the most important advantages associated with using a JFET for control is the fact that it is dc rather than ac control**. For most systems, dc control not only results in a reduced chance of adding unwanted noise to the system, but also lends itself well to remote control. For example, in Fig. 7.66a, a remote control panel controls the amplifier gain for the speaker by an ac line connected to the variable resistor.

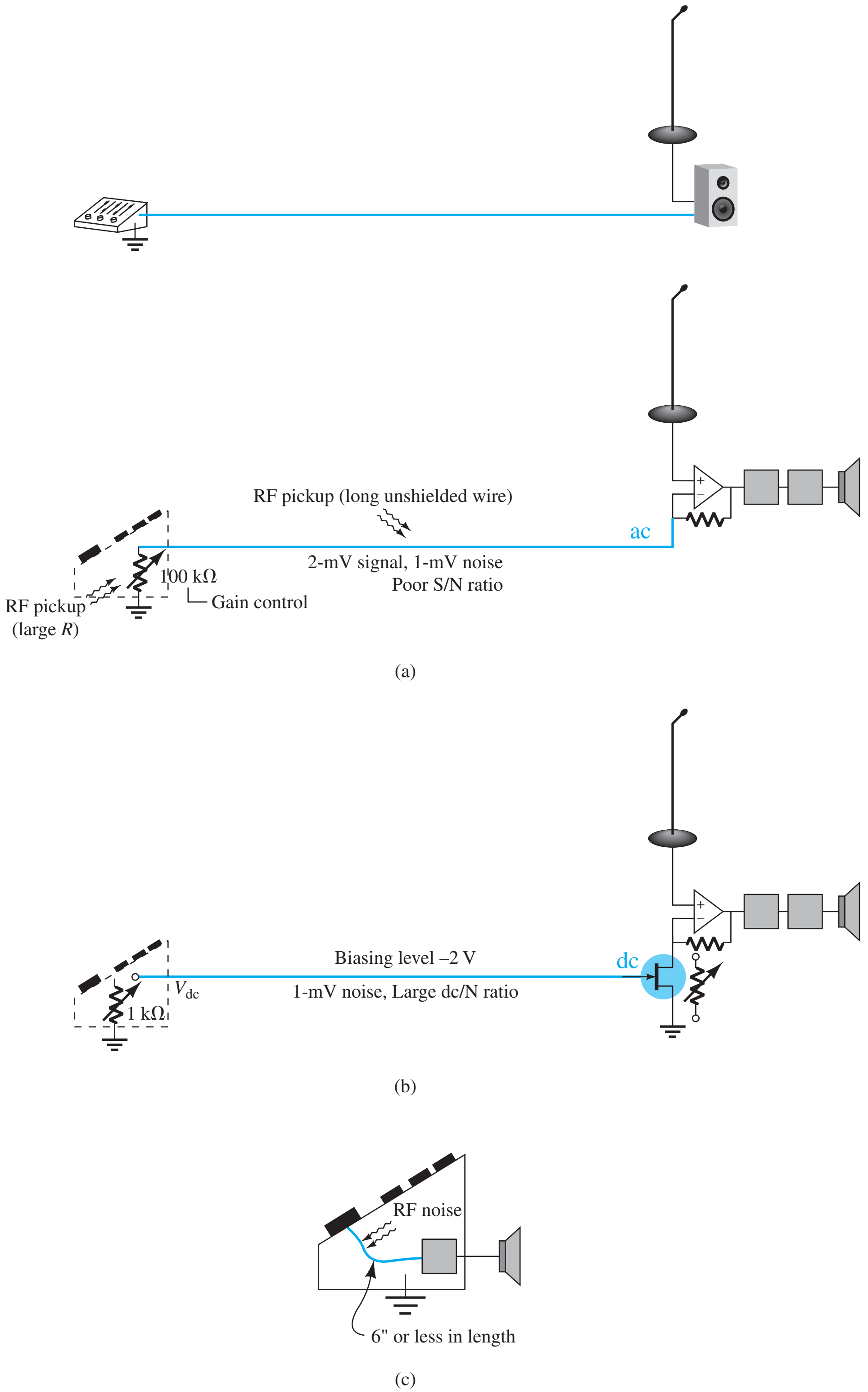

RF pickup (long unshielded wire)
ac
2-mV signal, 1-mV noise
Poor S/N ratio
100 kΩ
Gain control
RF pickup
(large R)
(a)
Biasing level –2 V
dc
V_{dc}
1-mV noise, Large dc/N ratio
1 kΩ
(b)
RF noise
6" or less in length
(c)

FIG. 7.66

Demonstrating the benefits of dc control: system with (a) ac control; (b) dc control; (c) RF noise pickup.

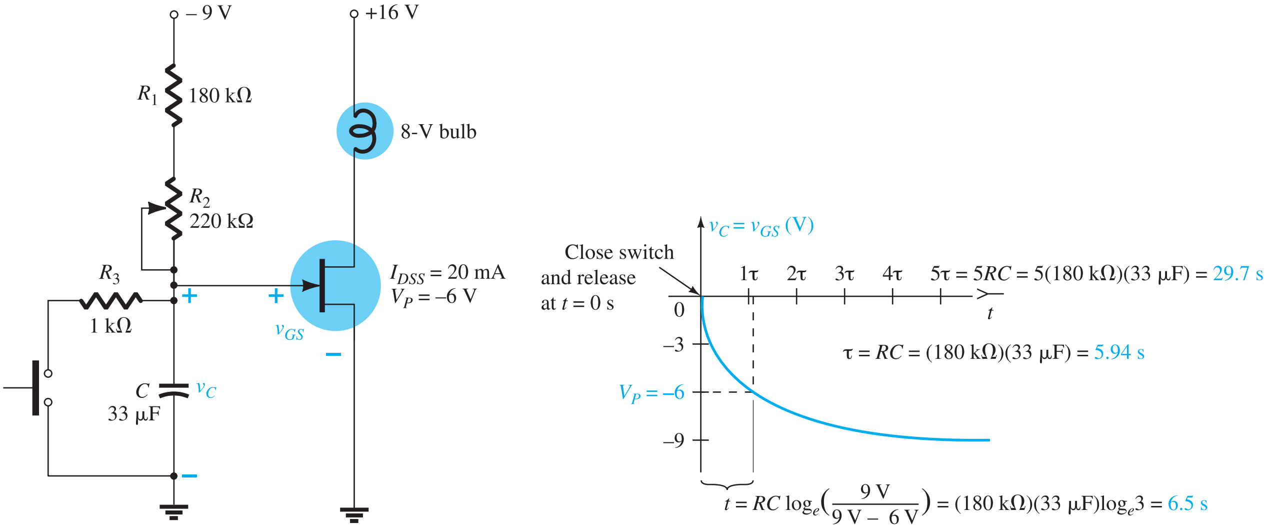
The long line from the amplifier can easily pick up noise from the surrounding air as generated by fluorescent lights, local radio stations, operating equipment (even computers), motors, generators, and so on. The result may be a 2-mV signal on the line with a 1-mV noise level—a terrible signal-to-noise ratio, which would only contribute to further deterioration of the signal coming in from the microphone due to the loop gain of the amplifier. In Fig. 7.66b, a dc line controls the gate voltage of the JFET and the variable resistance of the noninverting amplifier. Even though the dc line voltage on the line may be only −2 V, a ripple of 1 mV picked up by the long line will result in a very large signal-to-noise ratio, which could essentially be ignored in the distortion process. In other words, the noise on the dc line would simply move the dc operating point slightly on the device characteristics and would have almost no effect on the resulting drain resistance—isolation between the noise on the line and the amplifier response would be almost ideal.

Even though Figures 7.66a and 7.66b have a relatively long control line, the control line may only be 6″ long, as shown in the control panel of Fig. 7.66c, where all the elements of the amplifier are housed in the same container. Consider, however, **that just 1″ is enough to pick up RF noise**, so dc control is a favorable characteristic for almost any system. Furthermore, since the control resistance in Fig. 7.66a is usually quite large (hundreds of kilohms), whereas the dc voltage control resistors of the dc system of Fig. 7.66b are usually quite small (a few kilohms), the volume control resistor for the ac system will absorb a great deal more ac noise than the dc design. This phenomenon is a result of the fact that **RF noise signals in the air have a very high internal resistance, and therefore the larger the pickup resistance, the greater is the RF noise absorbed by the receiver**. Recall Thévenin's theorem, which states that for maximum power transfer, the load resistance should equal the internal resistance of the source.

As noted above, **dc control lends itself to computer and remote control systems** since they operate off specific fixed dc levels. For instance, when an infrared (IR) signal is sent out by a remote control to the receiver in a TV or VCR, the signal is passed through a decoder–counter sequence to define a particular dc voltage level on a staircase of voltage levels that can be fed into the gate of the JFET. For a volume control, that gate voltage may control the drain resistance of a noninverting amplifier controlling the volume of the system.

Timer Network

The high isolation between gate and drain circuits permits the design of a relatively simple timer such as shown in Fig. 7.67. The switch is a normally open (NO) switch, which, when closed, will short out the capacitor and cause its terminal voltage to quickly drop to 0 V. The switching network can handle the rapid discharge of voltage across the capacitor



−9 V
+16 V
R_1
180 kΩ
8-V bulb
R_2
220 kΩ
R_3
1 kΩ
+
+
v_{GS}
−
$I_{DSS} = 20$ mA
$V_P = -6$ V
C
33 μF
v_C
−
Close switch and release at $t = 0$ s
$v_C = v_{GS}$ (V)
1τ
2τ
3τ
4τ
$5\tau = 5RC = 5(180\text{ k}\Omega)(33\ \mu\text{F}) = 29.7$ s
t
0
−3
$V_P = -6$
−9
$\tau = RC = (180\text{ k}\Omega)(33\ \mu\text{F}) = 5.94$ s
$t = RC\log_e\left(\frac{9\text{ V}}{9\text{ V} - 6\text{ V}}\right) = (180\text{ k}\Omega)(33\ \mu\text{F})\log_e 3 = 6.5$ s

FIG. 7.67
JFET timer network.

because the working voltages are relatively low and the discharge time is extremely short. Some would say it is a poor design, but in the practical world it is frequently used and not looked on as a terrible crime.

When power is first applied, the capacitor will respond with its short-circuit equivalence since the **voltage across the capacitor cannot change instantaneously**. The result is that the gate-to-source voltage of the JFET will immediately be set to 0 V, the drain current I_D will equal I_{DSS}, and the bulb will turn on. However, with the switch in the normally open position, the capacitor will begin to charge to -9 V. **Because of the parallel high input impedance of the JFET, it has essentially no effect on the charging time constant of the capacitor**. Eventually, when the capacitor reaches the pinch-off level, the JFET and bulb will turn off. In general, therefore, when the system is first turned on, the bulb will light for a very short period of time and then turn off. It is now ready to perform its timing function.

When the switch is closed, it will short out the capacitor ($R_3 \ll R_1, R_2$) and will set the voltage at the gate to 0 V. The resulting drain current is I_{DSS}, and the bulb will burn brightly. When the switch is released, the capacitor will charge toward -9 V, and eventually when it reaches the pinch-off level, the JFET and bulb will turn off. The period during which the bulb is on will be determined by the time constant of the charging network, determined by $\tau = (R_1 + R_2)C$ and the level of the pinch-off voltage. The more negative the pinch-off level, the longer the bulb will be on. Resistor R_1 is included to be sure that there is some resistance in the charging circuit when the power is turned on. Otherwise, a very heavy current could result that might damage the network. Resistor R_2 is a variable resistor, so the "on" time can be controlled. Resistor R_3 was added to limit the discharge current when the switch is closed. When the switch across the capacitor is closed, the discharge time of the capacitor will be only $5\tau = 5RC = 5(1\text{ k}\Omega)(33\ \mu\text{F}) = 165\ \mu\text{s} = 0.165\text{ ms} = 0.000165\text{ s}$. In summary, therefore, when the switch is pressed and released, the bulb will come on brightly, and then, as time goes on, it will become dimmer until it shuts off after a period of time determined by the network time constant.

One of the most obvious applications of such a timing system is in a hallway or travel corridor where you want light for a short period of time so that you can pass safely but then want the system to turn off on its own. When you enter or leave a car, you may want a light on for a short period of time but don't want to worry about turning it off. There are endless possibilities for a timing network such as just described. Just consider the variety of other electrical or electronic systems that you would like to turn on for specific periods of time, and the list of uses grows exponentially.

One might ask why a BJT would not be a good alternative to the JFET for the same application. First, the input resistance of the BJT may be only a few kilohms. That would affect not only the time constant of the charging network, but also the maximum voltage to which the capacitor could charge. Just draw an equivalent network with the transistor replaced by a 1-kΩ resistor, and the above will immediately become clear. In addition, the control levels will have to be designed with a great deal more care since the BJT transistor turns on at about 0.7 V. The voltage swing from off to on is only 0.7 V rather than 4 V for the JFET configuration. One final note: You might have noticed the absence of a series resistor in the drain circuit for the situation when the bulb is first turned on and the resistance of the bulb is very low. The resulting current could be quite high until the bulb reaches its rated intensity. However, again, as described above for the switch across the capacitor, if the energy levels are small and the duration of stress minimal, such designs are often accepted. If there were any concern, adding a resistor of 0.1 to 1 Ω in series with the bulb would provide some security.

Fiber Optic Systems

The introduction of fiber optic technology has had a dramatic effect on the communications industry. The information-carrying capacity of fiber optic cable is significantly greater than that provided by conventional methods with individual pairs of wire. In addition, the cable size is reduced, the cable is less expensive, crosstalk due to electromagnetic effects between current-carrying conductors is eliminated, and noise pickup due to external disturbances such as lightning are eliminated.

The fiber optic industry is based on the fact that information can be transmitted on a beam of light. Although the speed of light through free space is 3×10^8 meters per second, or approximately 186,000 miles per second, its speed will be reduced by encounters with other media, causing reflection and refraction. When light information is passed through a fiber optic cable, it is expected to bounce off the walls of the cable. However, the angle at which the light is injected into the cable is critical, as is the actual design of the cable. In Fig. 7.68, the basic elements of a fiber optic cable are defined. The glass or plastic core of the cable can be as small as 8 μm, which is close to 1/10 the diameter of a human hair. The core is surrounded by an outer layer called the *cladding*, which is also made of glass or plastic, but has a different refractive index to ensure that the light in the core that hits the outer surface of the core is reflected back into the core. A protective coating is then added to protect the two layers from outside environmental effects.

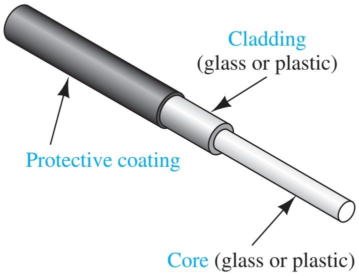


FIG. 7.68
Basic elements of a fiber optic cable.

Most optical communication systems work in the infrared frequency range, which extends from 3×10^{11} Hz to 5×10^{14} Hz. This spectrum is just below the visible light spectrum, which extends from 5×10^{14} Hz to 7.7×10^{14} Hz. For most optical systems the frequency range of 1.87×10^{14} Hz to 3.75×10^{14} Hz is used. Because of the very high frequencies, each carrier can be modulated by hundreds or thousands of voice channels simultaneously. In addition, very high speed computer transmission is a possibility, although one must be sure that the electronic components of the modulators can also operate successfully at the same frequency. For distances over 30 nautical miles, repeaters (a combination receiver, amplifier, and transmitter) must be used, which require an additional electrical conductor in the cable that carries a current of about 1.5 A at 2500 V.

The basic components of an optical communication system are shown in Fig. 7.69. The input signal is applied to a light modulator whose sole purpose is to convert the input signal to one of corresponding levels of light intensity to be directed down the length of fiber optic cable. The information is then carried through the cable to the receiving station, where a light demodulator converts the varying light intensities back to voltage levels that match those of the original signal.

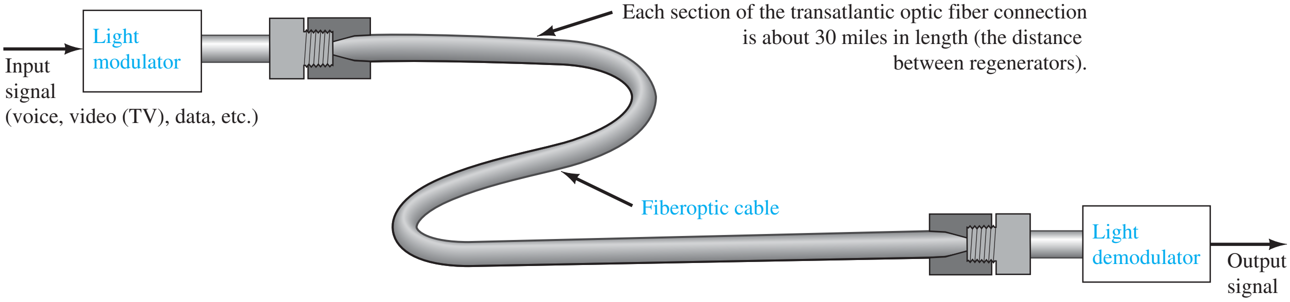

Light
modulator
Input
signal
(voice, video (TV), data, etc.)
Each section of the transatlantic optic fiber connection
is about 30 miles in length (the distance
between regenerators).
Fiberoptic cable
Light
demodulator
Output
signal

FIG. 7.69
Basic components of an optical communication system.

An electronic equivalent for the transmission of computer transistor-transistor-logic (TTL) information is provided in Fig. 7.70a. With the Enable control in the "on" or 1-state, the TTL information at the input to the AND gate can pass through to the gate of the JFET configuration. The design is such that the discrete levels of voltage associated with the TTL logic will turn the JFET on and off (perhaps 0 V and −5 V, respectively, for a JFET with $V_P = -4$ V). The resulting change in current levels will result in two distinct levels of light intensity from the LED (Section 1.16) in the drain circuit. That emitted light will then be directed through the cable to the receiving station, where a photodiode (Section 16.6) will react to the incident light and permit different levels of current to pass through as established by V and R. The current for photodiodes is a reverse current having the direction shown in Fig. 7.70a, but in the ac equivalent the photodiode and the resistor R are in parallel as shown in Fig. 7.70b, establishing the desired signal with the polarity shown at the gate of the JFET. Capacitor C is simply an open circuit to dc to isolate the biasing arrangement for the photodiode from the JFET and a short circuit as shown for the signal v_s. The incoming signal will then be amplified and will appear at the drain terminal of the output JFET.

As mentioned above, all the elements of the design, including the JFETs, LED, photodiode, capacitors, and so on, must be carefully chosen to ensure that they function properly

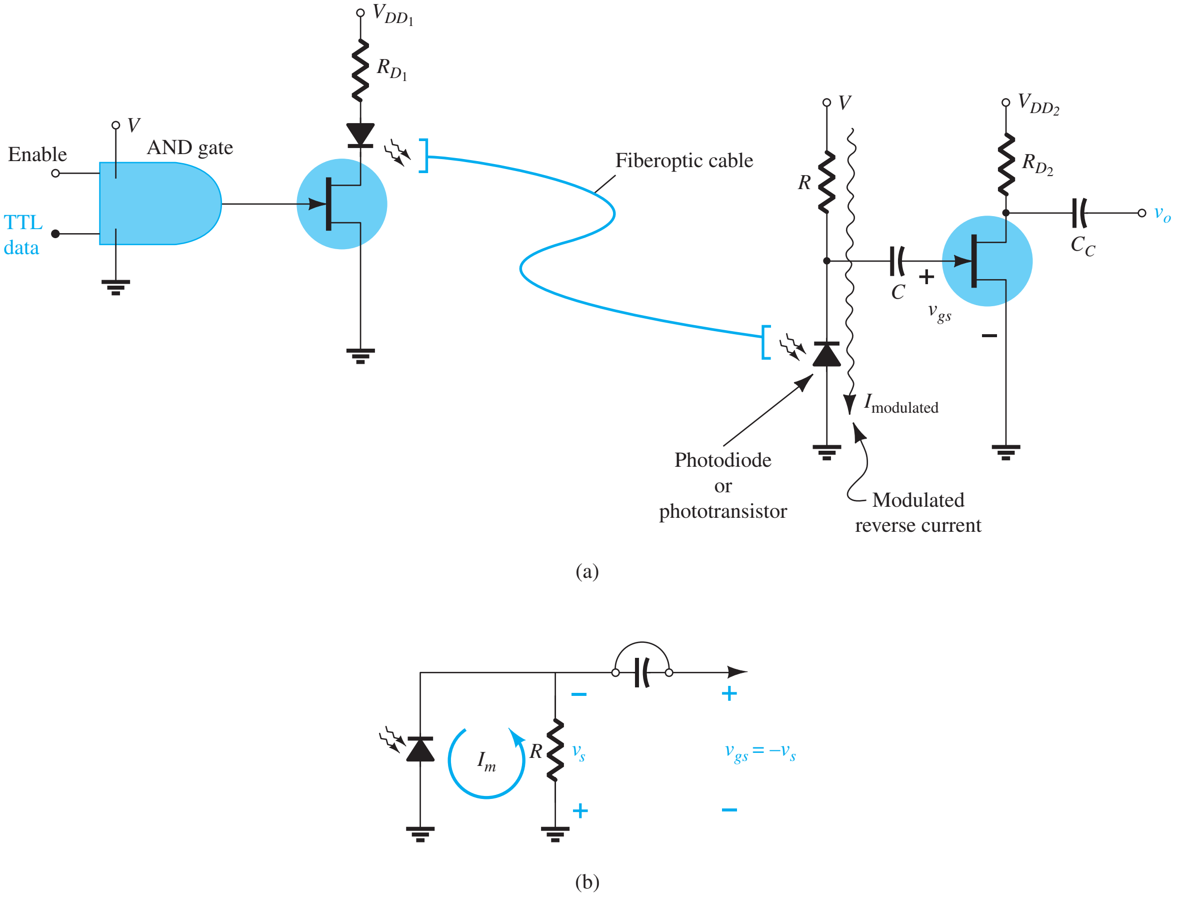


FIG. 7.70

TTL fiber optic communication channel: (a) JFET design; (b) passing on the signal generated across the photodiode.

at the high frequency of transmission. In fact, laser diodes are frequently used instead of LEDs in the modulator because they work at higher information rates and higher powers and have lower coupling and transmission losses. However, laser diodes are a great deal more expensive and more temperature sensitive, and they typically have a shorter lifetime than LEDs. For the demodulator side, the photodiodes are either of the pin photodiode or the avalanche photodiode variety. The *pin* abbreviation comes from the *p*-*i*ntrinsic-*n* construction process, and the term *avalanche* from the rapidly growing ionization process that develops during operation.

In general, the JFET is excellent for this application because of its high isolation at the input side and its ability to quickly "snap" from one state to the other due to the TTL input. At the output side the isolation blocks any effect of the demodulator sensing circuit from affecting the ac response, and it provides some gain for the signal before it is passed on to the next stage.

MOSFET Relay Driver

The MOSFET relay driver to be described in this section is an excellent example of how the FETs can be used to **drive high-current/high-voltage networks without drawing current or power from the driving circuit. The high input impedance of FETs essentially isolates the two parts of the network without the need for optical or electromagnetic linkages**. The network to be described can be used for a variety of applications, but our application will be limited to an alarm system activated when someone or something passes the plane of the transmitted light.

The IR (infrared—not visible) LED of Fig. 7.71 is directing its light through a directional funnel to hit the face of a photoconductive cell (Section 16.7) of the controlling network. The photoconductive cell has a range of resistance from about 200 kΩ as its dark

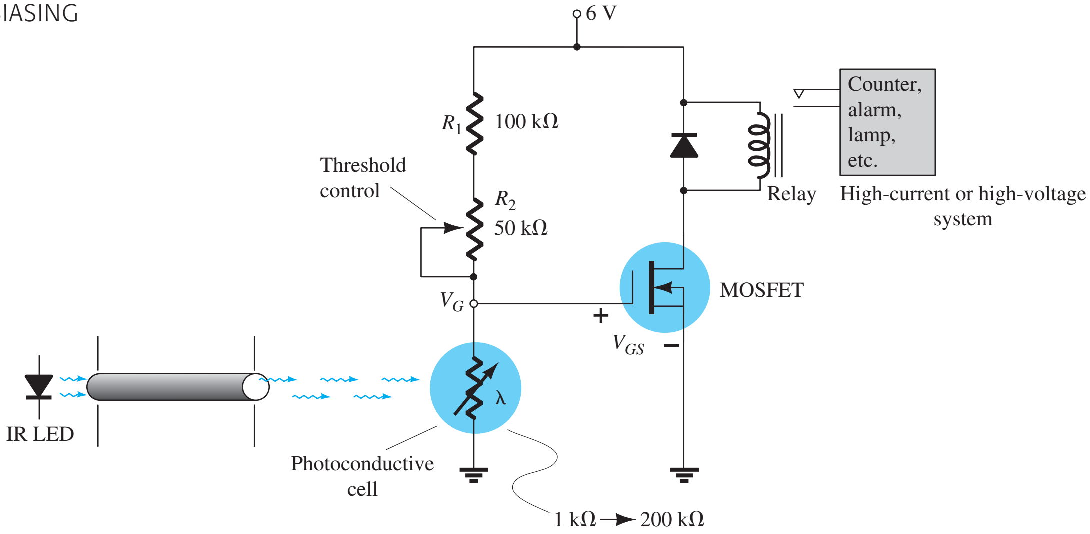


FIG. 7.71
MOSFET relay driver.

resistance level down to less than 1 kΩ at high illumination levels. Resistor R_1 is a variable resistance that can be used to set the threshold level of the depletion-type MOSFET. A medium-power MOSFET was employed because of the high level of drain current through the magnetizing coil. The diode is included as a protective device for reasons discussed in detail in Section 2.11.

When the system is on and the light consistently hitting the photoconductive cell, the resistance of the cell may drop to 10 kΩ. At this level an application of the voltage-divider rule will result in a voltage of about 0.54 V at the gate terminal (with the 50-kΩ potentiometer set to 0 kΩ). The MOSFET will be on, but not at a drain current level that will cause the relay to change state. When someone passes by, the light source will be cut off, and the resistance of the cell may quickly (in a few microseconds) rise to 100 kΩ. The voltage at the gate will then rise to 3 V, turning on the MOSFET and activating the relay and turning on the system under control. An alarm circuit has its own control design to ensure that it will not turn off when light returns to the photoconductive cell.

In essence, therefore, we have controlled a high-current network with a relatively small dc voltage level and a rather inexpensive design. The only obvious flaw in the design is the fact that the MOSFET will be on even when there is no intrusion. This can be remedied through the use of a more sophisticated design, but keep in mind that **MOSFETs are typically low-power-consumption devices**, so the power loss, even over time, is not that great.

7.16 SUMMARY

Important Conclusions and Concepts

1. A fixed-bias configuration has, as the label implies, a **fixed** dc voltage applied from gate to source to establish the operating point.
2. The **nonlinear** relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution (involving the solution of two simultaneous equations) be used to determine the quiescent point of operation.
3. All voltages with a single subscript define a voltage from a specified point to **ground**.
4. The self-bias configuration is determined by an equation for V_{GS} that will *always* pass through the origin. Any other point determined by the biasing equation will establish a **straight** line to represent the biasing network.
5. For the voltage-divider biasing configuration, one can always assume that the gate current is 0 A to permit an **isolation** of the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be **positive for an *n*-channel JFET** and **negative for a *p*-channel JFET. Increasing values of** R_S result in **lower quiescent values of** I_D and more **negative values of** V_{GS} **for an *n*-channel JFET**.

6. The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an I_D level **above** the I_{DSS} value.
7. The characteristics and method of analysis applied to enhancement-type MOSFETs are **entirely different** from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current is 0 A.
8. When analyzing networks with a variety of devices, first work with the region of the network that will provide a **voltage or current level** using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.
9. The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind, remember that a resistance level is defined by the **voltage across the resistor divided by the current** through the resistor. In the design process, both of these quantities are often available for a particular resistive element.
10. The ability to troubleshoot a network requires a **clear**, **firm understanding** of the terminal behavior of each of the devices in the network. That knowledge will provide an **estimate** of the working voltage levels of specific points of the network, which can be checked with a voltmeter. The ohmmeter section of a multimeter is particularly helpful in ensuring that there is a **true connection** between all the elements of the network.
11. The analysis of p-channel FETs is the same as that applied to n-channel FETs except for the fact that all the voltages will have the **opposite polarity** and the currents the **opposite direction**.

Equations

JFETs/depletion-type MOSFETs:

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$

$$V_{GS} = V_G - I_D R_S$$

Enhancement-type MOSFETs:

Feedback biasing: $V_{DS} = V_{GS}$

$$V_{GS} = V_{DD} - I_D R_D$$

Voltage-divider biasing: $V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$

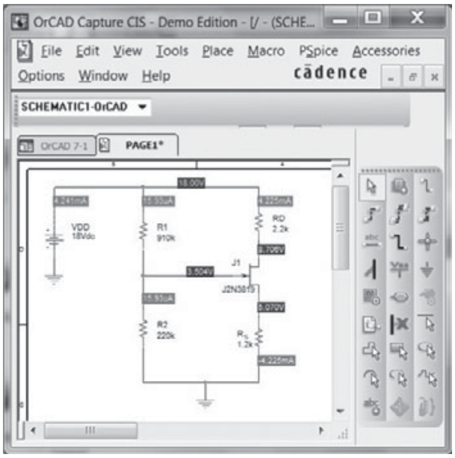
$$V_{GS} = V_G - I_D R_S$$

7.17 COMPUTER ANALYSIS

PSpice Windows

JFET Voltage-Divider Configuration The results of Example 7.19 will now be verified using PSpice Windows. The network of Fig. 7.72 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL** library, and **Edit-PSpice model** is used to set **Beta** to 0.222 mA/V^2 and **Vto** to −6 V. The **Beta** value is determined using beta = I_{DSS}/V_P^2 Eq. (6.17) and the provided I_{DSS} and V_P. The results of the **Simulation** appear in Fig. 7.73 with the dc bias voltage and current levels. The resulting drain current is 4.225 mA, compared to the calculated level of 4.24 mA—an excellent match. The voltage V_{GS} is 3.504 V − 5.070 V = −1.57 V versus the calculated level of −1.56 V in Example 7.19—another excellent match.

Combination Network Next, the result of Example 7.12 with both a transistor and JFET will be verified. For the transistor **Bf** is set to 180, whereas for the JFET, **Beta** is set to 0.333 mA/V^2 and **Vto** to −6 V as called for in the example. The results for all the dc levels appear in Fig. 7.73. Note again the excellent comparison with the calculator solution, with V_D at 11.44 V compared to 11.07 V, $V_S = V_C$ at 7.138 V compared to 7.32 V, and V_{GS} at 3.380 V − 7.138 V = −3.76 V compared to −3.7 V.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File Edit View Tools Place Macro PSpice Accessories
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SCHEMATIC1-OrCAD
OrCAD 7-1
PAGE1*
18.00V
4.241mA
15.53uA
4.225mA
VDD
18Vdc
R1
910k
RD
2.2k
8.706V
J1
3.504V
J2N3819
15.53uA
5.070V
R2
220k
R_S
1.2k
4.225mA

FIG. 7.72

JFET voltage-divider configuration with PSpice Windows results for current and voltage levels.

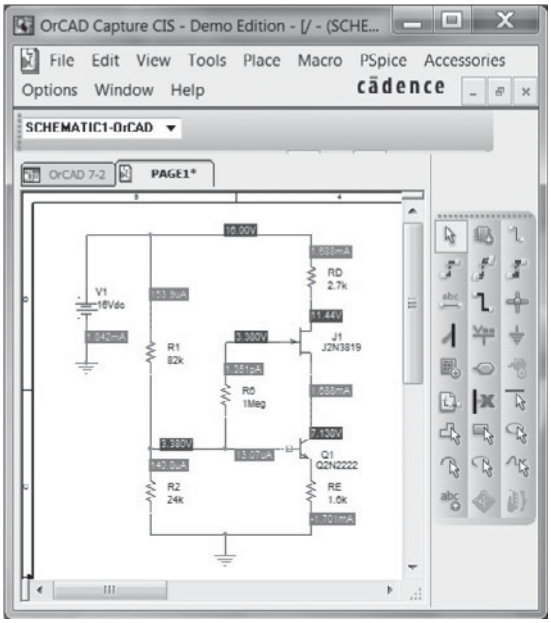

OrCAD Capture CIS - Demo Edition - [/ - (SCHE...
File Edit View Tools Place Macro PSpice Accessories
Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 7-2
PAGE1*
16.00V
1.688mA
RD
2.7k
V1
16Vdc
153.9uA
11.44V
1.042mA
3.300V
J1
J2N3819
R1
82k
1.351pA
R6
1Meg
1.688mA
7.130V
3.380V
13.07uA
Q1
Q2N2222
140.0uA
R2
24k
RE
1.6k
-1.701mA

FIG. 7.73

Verifying the hand-calculated solution of Example 7.12 using PSpice Windows.

Multisim

The results of Example 7.2 will now be verified using Multisim. The construction of the network of Fig. 7.74 is essentially the same as applied in the BJT chapters. The JFET is obtained by selecting **Transistor**, the fourth key down on the first vertical toolbar. A **Select a Component** dialog box will appear, in which **JFET_N** can be selected under the **Family** listing. A long **Component** list appears, in which **2N3821** is selected for this application. An **OK**, and it can be placed on the screen. After double-clicking the symbol on the screen, a **JFET_N** dialog box will appear in which **Value** can be selected, followed

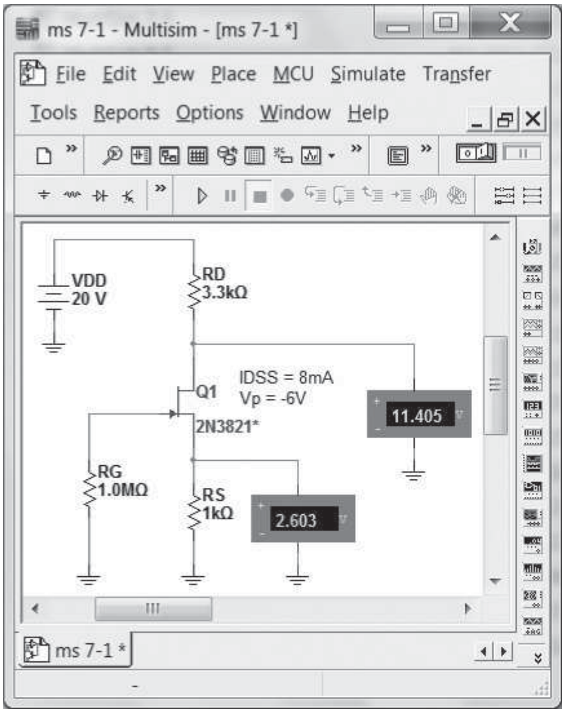

ms 7-1 - Multisim - [ms 7-1 *]
File Edit View Place MCU Simulate Transfer
Tools Reports Options Window Help
VDD
20 V
RD
3.3kΩ
IDSS = 8mA
Vp = -6V
Q1
2N3821*
11.405
RG
1.0MΩ
RS
1kΩ
2.603
ms 7-1 *

FIG. 7.74

Verifying the results of Example 7.2 using Multisim.

by **Edit Model**. An **Edit Model** dialog box will appear in which **Beta** and **Vto** can be set to **0.222 mA/V^2** and **−6 V**, respectively. The value of **Beta** is determined using Eq. (6.17) and the parameters of the network as follows:

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{8\text{ mA}}{|-6\text{ V}|^2} = \frac{8\text{ mA}}{36\text{ V}^2} = 0.222\text{ mA}/\text{V}^2$$

Once the change is made, be sure to select **Change Part Model** before leaving the dialog box. The **JFET_N** dialog box will appear again, but an **OK**, and the changes will be made. The labels **IDSS = 8 mA** and **Vp = −6 V** are added using **Place-Text**. A blinking vertical bar will appear marking the place where the label can be entered. Once entered, it can easily be moved by simply clicking the area and dragging it to the desired position while holding the clicker down.

Using the **Indicator** option on the first vertical toolbar displays the drain and source voltages as shown in Fig. 7.74. In both cases the **VOLTMETER_V** option was chosen in the **Select a Component** dialog box.

Selecting **Simulate-Run** or moving the switch to the **1** position results in the display of Fig. 7.74. Note that V_{GS} at −2.603 V is an exact match with the hand-calculated solution of −2.6 V. Although the indicator is connected from source to ground, be aware that this is also the gate-to-source voltage because the voltage drop across the 1-MΩ resistor is assumed to be 0 V. The level of 11.405 V at the drain is very close to the hand-calculated solution of 11.42 V—in all, a complete verification of the results of Example 7.2.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.75:
   a. Sketch the transfer characteristics of the device.
   b. Superimpose the network equation on the same graph.
   c. Determine I_{D_Q} and V_{DS_Q}.
   d. Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

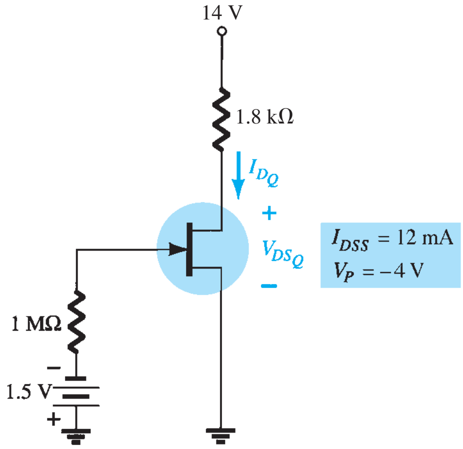


FIG. 7.75
Problems 1 and 37.

2. For the fixed-bias configuration of Fig. 7.76, determine:
   a. I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
   b. Repeat part (a) using a graphical approach and compare results.
   c. Find V_{DS}, V_D, V_G, and V_S using the results of part (a).
3. Given the measured value of V_D in Fig. 7.77, determine:
   a. I_D.
   b. V_{DS}.
   c. V_{GG}.

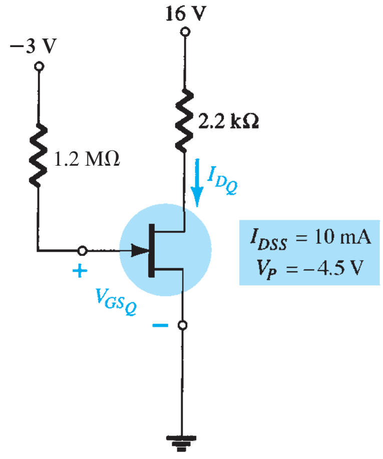

16 V
−3 V
2.2 kΩ
1.2 MΩ
I_{D_Q}
I_{DSS} = 10 mA
V_P = −4.5 V
+
V_{GS_Q}
−

FIG. 7.76
Problem 2.

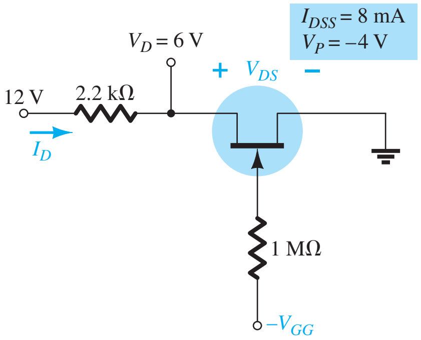

I_{DSS} = 8 mA
V_P = −4 V
V_D = 6 V
+ V_{DS} −
12 V
2.2 kΩ
I_D
1 MΩ
$-V_{GG}$

FIG. 7.77
Problem 3.

4. Determine V_D and V_{GS} for the fixed-bias configuration of Fig. 7.78.
5. Determine V_D and V_{GS} for the fixed-bias configuration of Fig. 7.79.

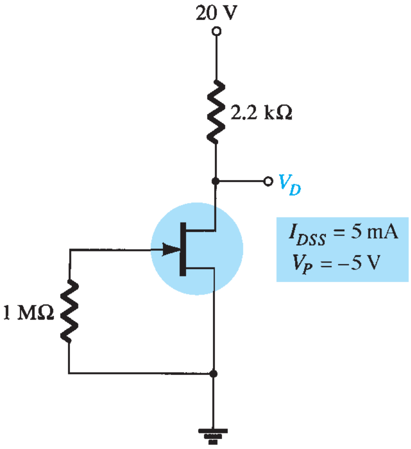

20 V
2.2 kΩ
V_D
I_{DSS} = 5 mA
V_P = −5 V
1 MΩ

FIG. 7.78
Problem 4.

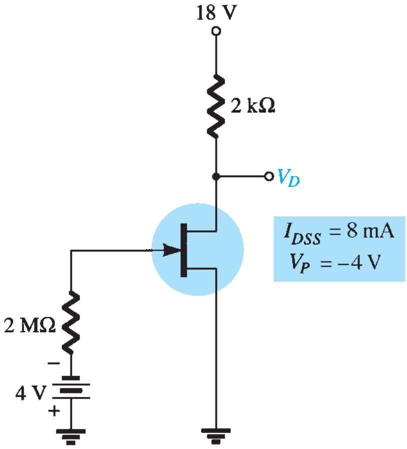

18 V
2 kΩ
V_D
I_{DSS} = 8 mA
V_P = −4 V
2 MΩ
−
4 V
+

FIG. 7.79
Problem 5.

7.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 7.80:
   - **a.** Sketch the transfer curve for the device.
   - **b.** Superimpose the network equation on the same graph.
   - **c.** Determine I_{D_Q} and V_{GS_Q}.
   - **d.** Calculate V_{DS}, V_D, V_G, and V_S.

*7. Determine I_{D_Q} for the network of Fig. 7.80 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 7.81, determine:
   - **a.** V_{GS_Q} and I_{D_Q}.
   - **b.** V_{DS}, V_D, V_G, and V_S.

9. Given the measurement $V_S = 1.7$ V for the network of Fig. 7.82, determine:
   - **a.** I_{D_Q}.
   - **b.** V_{GS_Q}.
   - **c.** I_{DSS}.
   - **d.** V_D.
   - **e.** V_{DS}.

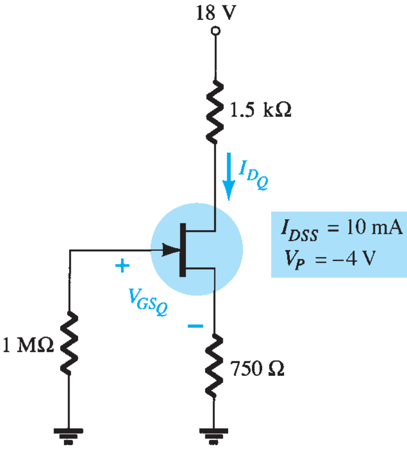

18 V
1.5 kΩ
I_{D_Q}
I_{DSS} = 10 mA
V_P = −4 V
+
V_{GS_Q}
−
1 MΩ
750 Ω

FIG. 7.80
Problems 6, 7, and 38.

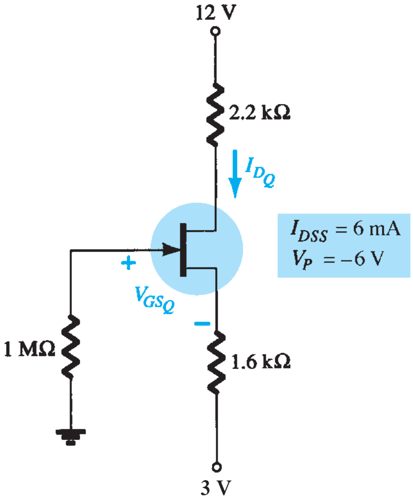

12 V
2.2 kΩ
I_{D_Q}
I_{DSS} = 6 mA
V_P = −6 V
+
V_{GS_Q}
−
1 MΩ
1.6 kΩ
3 V

FIG. 7.81
Problem 8.

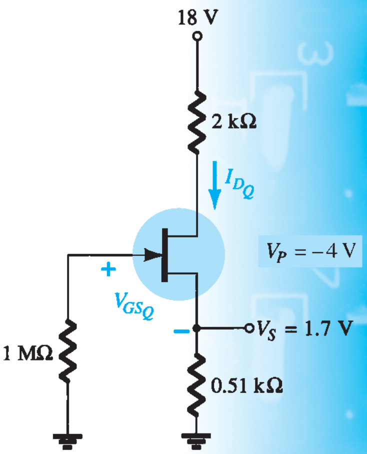
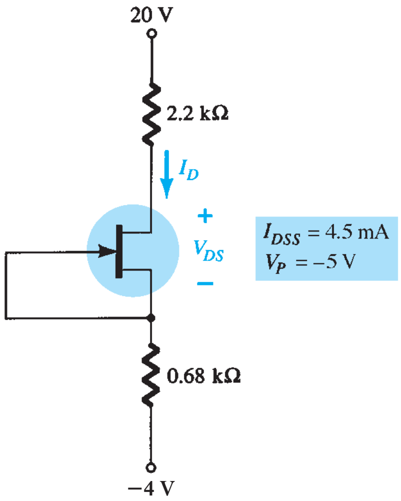

18 V
2 kΩ
I_{D_Q}
V_P = −4 V
+
V_{GS_Q}
−
V_S = 1.7 V
1 MΩ
0.51 kΩ

FIG. 7.82
Problem 9.

***10.** For the network of Fig. 7.83, determine:

a. I_D.
b. V_{DS}.
c. V_D.
d. V_S.

***11.** Find V_S for the network of Fig. 7.84.


20 V
2.2 kΩ
I_D
+
V_{DS}
−
I_{DSS} = 4.5 mA
V_P = −5 V
0.68 kΩ
−4 V

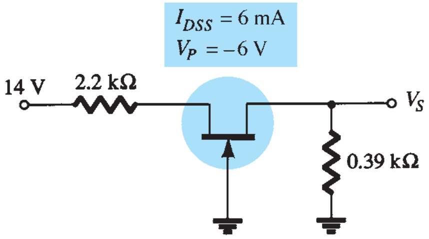

I_{DSS} = 6 mA
V_P = −6 V
14 V
2.2 kΩ
V_S
0.39 kΩ

FIG. 7.83
Problem 10.

FIG. 7.84
Problem 11.

7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.85, determine:

a. V_G.
b. I_{D_Q} and V_{GS_Q}.
c. V_D and V_S.
d. V_{DS_Q}.

13. a. Repeat Problem 12 with $R_S = 0.51\text{ k}\Omega$ (about 50% of the value of that of Problem 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
b. What is the minimum possible value of R_S for the network of Fig. 7.85?

14. For the network of Fig. 7.86, $V_D = 12$ V. Determine:

a. I_D.
b. V_S and V_{DS}.
c. V_G and V_{GS}.
d. V_P.

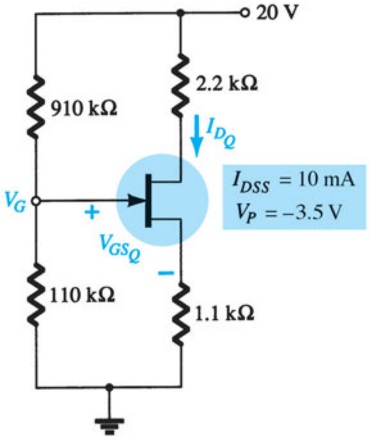

20 V
910 kΩ
2.2 kΩ
I_{D_Q}
I_{DSS} = 10 mA
V_P = −3.5 V
V_G
+
V_{GS_Q}
−
110 kΩ
1.1 kΩ

FIG. 7.85
Problems 12 and 13.

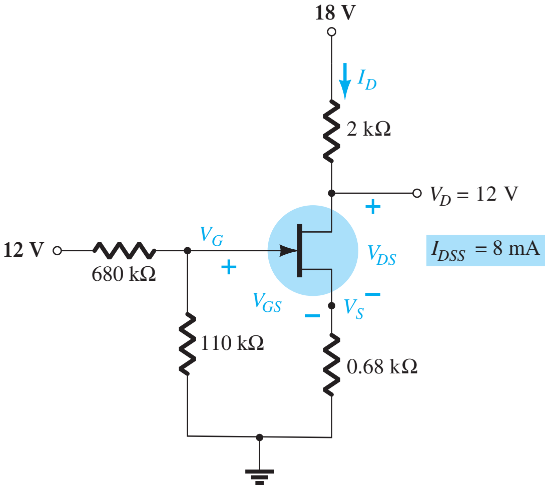

18 V
I_D
2 kΩ
V_D = 12 V
+
12 V
680 kΩ
V_G
+
V_{DS}
I_{DSS} = 8 mA
V_{GS}
−
V_S
−
110 kΩ
0.68 kΩ

FIG. 7.86
Problem 14.

15. Determine the value of R_S for the network of Fig. 7.87 to establish $V_D = 10$ V.

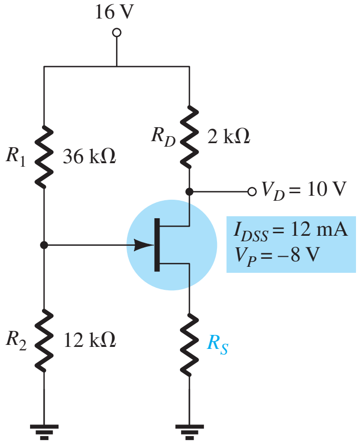

16 V
R_1
36 kΩ
R_D
2 kΩ
V_D = 10 V
I_{DSS} = 12 mA
V_P = −8 V
R_2
12 kΩ
R_S

FIG. 7.87
Problem 15.

7.5 Common-Gate Configuration

***16.** For the network of Fig. 7.88, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS} and V_S.

***17.** Given $V_{DS} = 4$ V for the network of Fig. 7.89, determine:

a. I_D.
b. V_D and V_S.
c. V_{GS}.

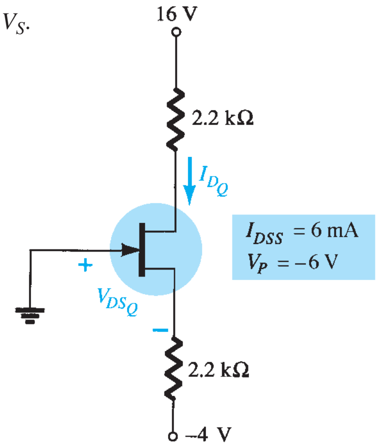

16 V
2.2 kΩ
I_{D_Q}
I_{DSS} = 6 mA
V_P = −6 V
+
V_{DS_Q}
−
2.2 kΩ
−4 V

FIG. 7.88
Problems 16 and 39.

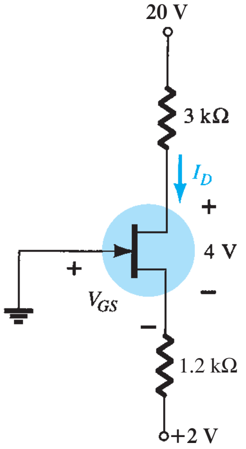

20 V
3 kΩ
I_D
+
4 V
−
+
V_{GS}
−
1.2 kΩ
+2 V

FIG. 7.89
Problem 17.

7.6 Special Case: $V_{GS_Q} = 0$ V

18. For the network of Fig. 7.90.

- **a.** Find I_{D_Q}.
- **b.** Determine V_{D_Q} and V_{DS_Q}.
- **c.** Find the power supplied by the source and dissipated by the device.

19. Determine V_D and V_{GS} for the network of Fig. 7.91 using the provided information.

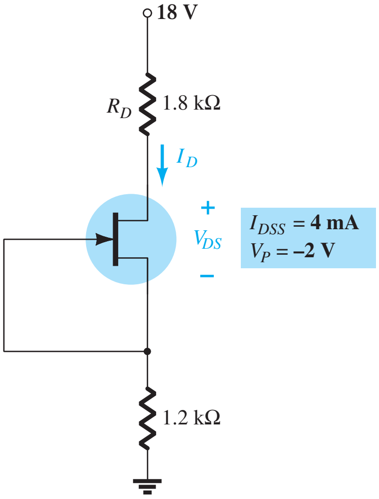

18 V
R_D
1.8 kΩ
I_D
+
V_{DS}
−
I_{DSS} = 4 mA
V_P = −2 V
1.2 kΩ

FIG. 7.90
Problem 18.

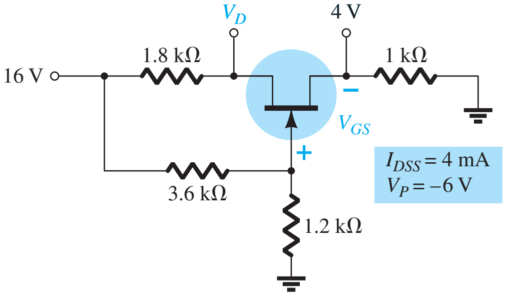

V_D
4 V
1.8 kΩ
1 kΩ
16 V
−
V_{GS}
+
3.6 kΩ
I_{DSS} = 4 mA
V_P = −6 V
1.2 kΩ

FIG. 7.91
Problem 19.

7.7 Depletion-Type MOSFETs

20. For the self-bias configuration of Fig. 7.92, determine:

- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS} and V_D.

***21.** For the network of Fig. 7.93, determine:

- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS} and V_S.

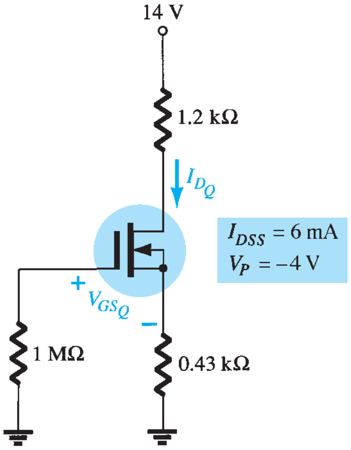

14 V
1.2 kΩ
I_{D_Q}
I_{DSS} = 6 mA
V_P = −4 V
+
V_{GS_Q}
−
1 MΩ
0.43 kΩ

FIG. 7.92
Problem 20.

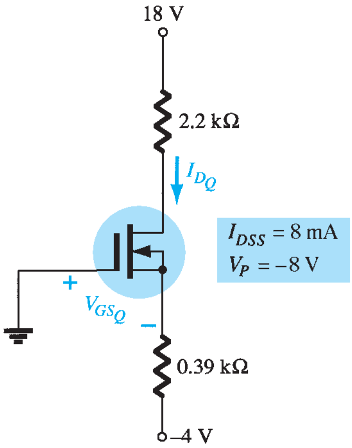

18 V
2.2 kΩ
I_{D_Q}
I_{DSS} = 8 mA
V_P = −8 V
+
V_{GS_Q}
−
0.39 kΩ
−4 V

FIG. 7.93
Problem 21.

7.8 Enhancement-Type MOSFETs

22. For the network of Fig. 7.94, determine:

- **a.** I_{D_Q}.
- **b.** V_{GS_Q} and V_{DS_Q}.
- **c.** V_D and V_S.
- **d.** V_{DS}.

23. For the voltage-divider configuration of Fig. 7.95, determine:

- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_D and V_S.

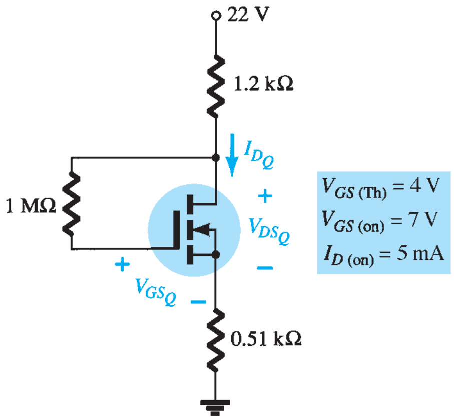

22 V
1.2 kΩ
I_{D_Q}
1 MΩ
+
V_{DS_Q}
−
+
V_{GS_Q}
−
0.51 kΩ
$V_{GS\,(\text{Th})} = 4$ V
$V_{GS\,(\text{on})} = 7$ V
$I_{D\,(\text{on})} = 5$ mA

FIG. 7.94
Problem 22.

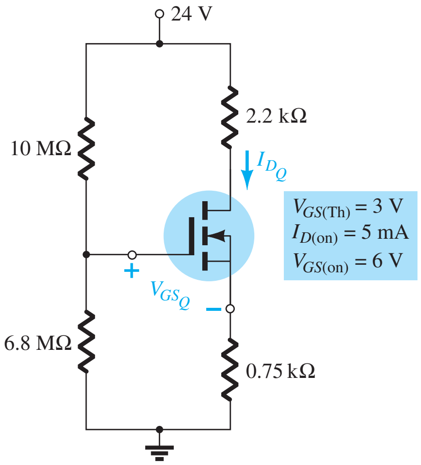

24 V
2.2 kΩ
10 MΩ
I_{D_Q}
$V_{GS(\text{Th})} = 3$ V
$I_{D(\text{on})} = 5$ mA
$V_{GS(\text{on})} = 6$ V
+
V_{GS_Q}
−
6.8 MΩ
0.75 kΩ

FIG. 7.95
Problem 23.

7.10 Combination Networks

***24.** For the network of Fig. 7.96, determine:

a. V_G.
b. V_{GS_Q} and I_{D_Q}.
c. I_E.
d. I_B.
e. V_D.
f. V_C.

***25.** For the combination network of Fig. 7.97, determine:

a. V_B and V_G.
b. V_E.
c. I_E, I_C, and I_D.
d. I_B.
e. V_C, V_S, and V_D.
f. V_{CE}.
g. V_{DS}.

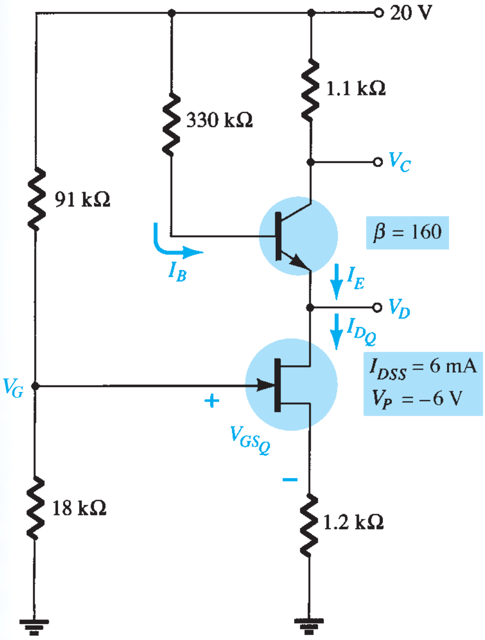

20 V
1.1 kΩ
330 kΩ
V_C
91 kΩ
$\beta = 160$
I_B
I_E
V_D
I_{D_Q}
$I_{DSS} = 6$ mA
$V_P = -6$ V
V_G
+
V_{GS_Q}
−
18 kΩ
1.2 kΩ

FIG. 7.96
Problem 24.

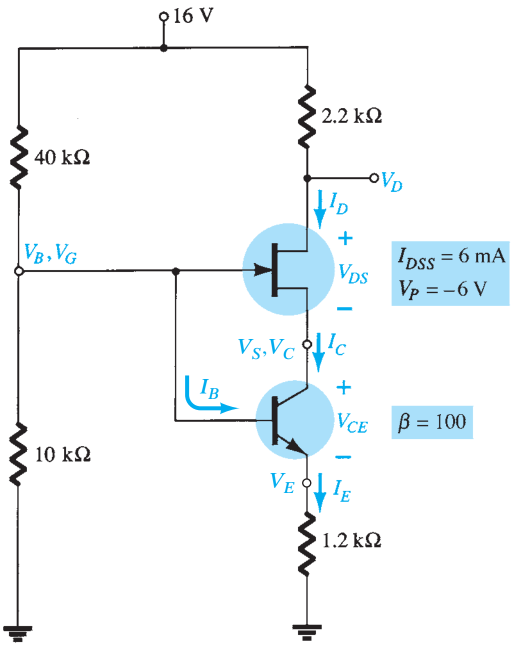

16 V
2.2 kΩ
40 kΩ
V_D
I_D
+
V_{DS}
−
V_B, V_G
$I_{DSS} = 6$ mA
$V_P = -6$ V
V_S, V_C
I_C
I_B
+
V_{CE}
−
$\beta = 100$
10 kΩ
V_E
I_E
1.2 kΩ

FIG. 7.97
Problem 25.

7.11 Design

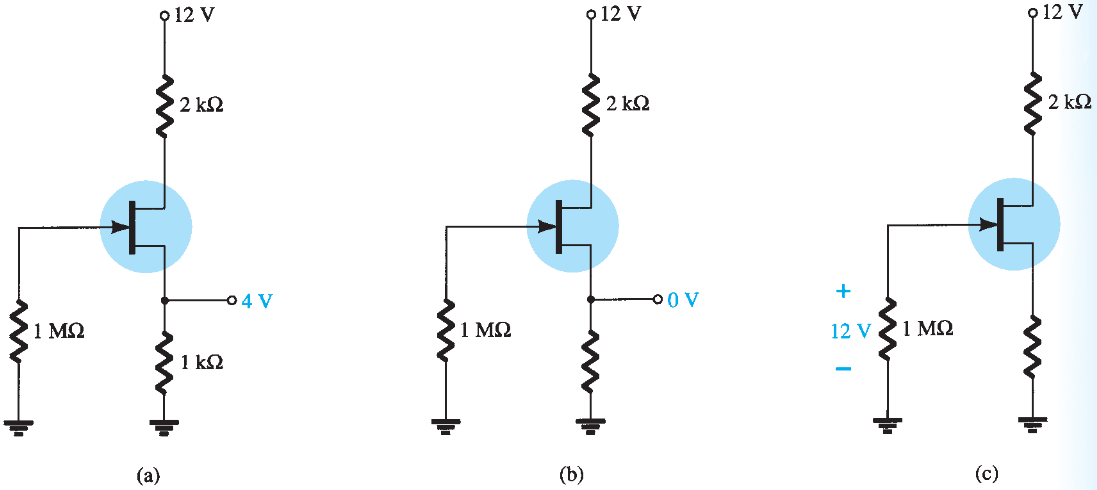
***26.** Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

***27.** Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22\ \text{M}\Omega$. Use standard values.

28. Design a network such as appears in Fig. 7.39 using an enhancement-type MOSFET with $V_{GS(\text{Th})} = 4$ V and $k = 0.5 \times 10^{-3}\ \text{A/V}^2$ to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

7.12 Troubleshooting

***29.** What do the readings for each configuration of Fig. 7.98 suggest about the operation of the network?


12 V
2 kΩ
4 V
1 MΩ
1 kΩ
12 V
2 kΩ
0 V
1 MΩ
12 V
2 kΩ
+
12 V
−
1 MΩ

(a) (b) (c)

FIG. 7.98
Problem 29.

***30.** Although the readings of Fig. 7.99 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

***31.** The network of Fig. 7.100 is not operating properly. What is the specific cause for its failure?

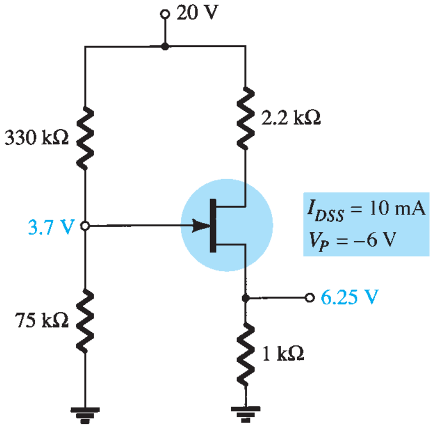

20 V
330 kΩ
2.2 kΩ
3.7 V
I_{DSS} = 10 mA
V_P = −6 V
6.25 V
75 kΩ
1 kΩ

FIG. 7.99
Problem 30.

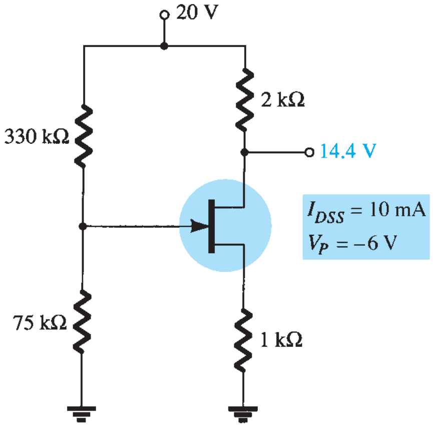

20 V
330 kΩ
2 kΩ
14.4 V
I_{DSS} = 10 mA
V_P = −6 V
75 kΩ
1 kΩ

FIG. 7.100
Problem 31.

7.13 *p*-Channel FETs

32. For the network of Fig. 7.101, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS}.
- **c.** V_D.

33. For the network of Fig. 7.102, determine:
- **a.** I_{D_Q} and V_{GS_Q}.
- **b.** V_{DS}.
- **c.** V_D.

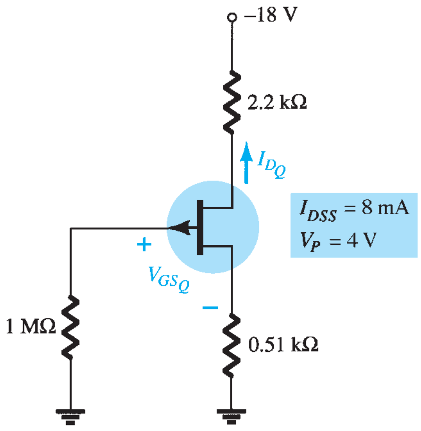

–18 V
2.2 kΩ
I_{D_Q}
I_{DSS} = 8 mA
V_P = 4 V
+
V_{GS_Q}
–
1 MΩ
0.51 kΩ

FIG. 7.101
Problem 32.

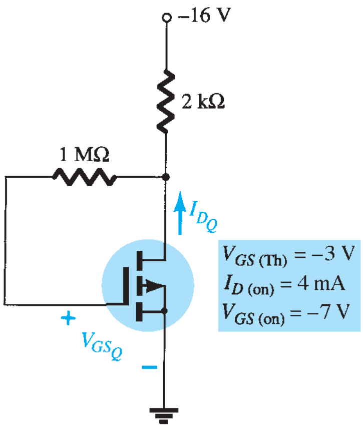

–16 V
2 kΩ
1 MΩ
I_{D_Q}
$V_{GS\,(\text{Th})}$ = –3 V
$I_{D\,(\text{on})}$ = 4 mA
$V_{GS\,(\text{on})}$ = –7 V
+
V_{GS_Q}
–

FIG. 7.102
Problem 33.

7.14 Universal JFET Bias Curve

34. Repeat Problem 1 using the universal JFET bias curve.

35. Repeat Problem 6 using the universal JFET bias curve.

36. Repeat Problem 12 using the universal JFET bias curve.

37. Repeat Problem 16 using the universal JFET bias curve.

7.15 Computer Analysis

38. Perform a PSpice Windows analysis of the network of Problem 1.

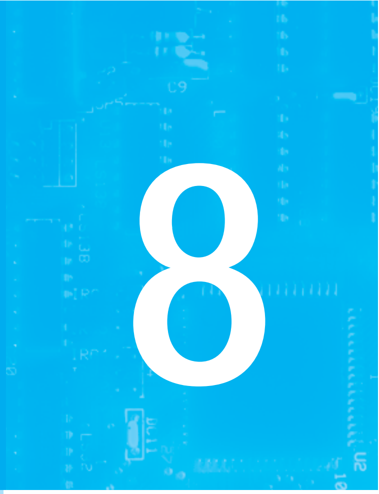
39. Perform a PSpice Windows analysis of the network of Problem 6.

40. Perform a Multisim analysis of the network of Problem 16.

41. Perform a Multisim analysis of the network of Problem 33.

8

FET Amplifiers



CHAPTER OBJECTIVES

- Become acquainted with the small-signal ac model for a JFET and MOSFET.
- Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
- Begin to appreciate the design sequence applied to FET configurations.
- Understand the effects of a source resistor and load resistor on the input impedance, output impedance and overall gain.
- Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.

8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13 provides a summary of FET small-signal amplifier circuits and related formulas.

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity.

Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice or Multisim, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models, one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as C++ that can perform both the dc and ac analyses and provide the results in a very special format.

8.2 JFET SMALL-SIGNAL MODEL

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\boxed{\Delta I_D = g_m \, \Delta V_{GS}} \tag{8.1}$$

The prefix *trans*- in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because g_m is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.

Solving for g_m in Eq. (8.1), we have

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 8.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$\boxed{g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.3}$$

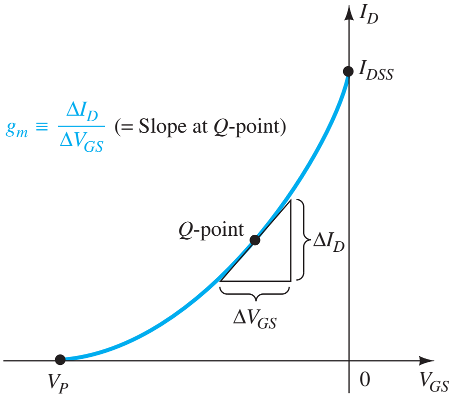


FIG. 8.1

Definition of g_m using transfer characteristic.

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. In other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

Equation (8.2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (8.2) to determine g_m.

EXAMPLE 8.1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ Vat the following dc bias points:

a. $V_{GS} = -0.5$ V.
b. $V_{GS} = -1.5$ V.
c. $V_{GS} = -2.5$ V.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\ mS}$

b. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\ mS}$

c. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\ mS}$

Note the decrease in g_m as V_{GS} approaches V_P.

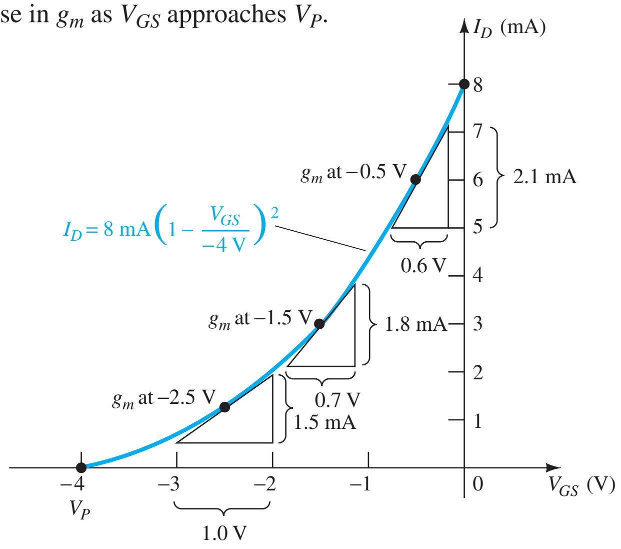


FIG. 8.2
Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$
\begin{aligned}
g_m &= \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2\right] \\
&= I_{DSS}\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right) \\
&= 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1)-\frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\left[0-\frac{1}{V_P}\right]
\end{aligned}
$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1-\frac{V_{GS}}{V_P}\right]} \qquad \textbf{(8.4)}$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (8.4) results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1-\frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \qquad \textbf{(8.5)}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (8.4) then becomes

$$\boxed{g_m = g_{m0}\left[1-\frac{V_{GS}}{V_P}\right]} \qquad \textbf{(8.6)}$$

EXAMPLE 8.2 For the JFET having the transfer characteristics of Example 8.1:

a. Find the maximum value of g_m.
b. Find the value of g_m at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\ mS}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1-\frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1-\frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\ mS}$$ (vs. 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1-\frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1-\frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\ mS}$$ (vs. 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1-\frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1-\frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\ mS}$$ (vs. 1.5 mS graphically)

The results of Example 8.2 are certainly sufficiently close to validate Eq. (8.4) through (8.6) for future use when g_m is required.

On specification sheets, g_m is often provided as g_{fs} or y_{fs}, where y indicates it is part of an admittance equivalent circuit. The *f* signifies *f*orward transfer conductance, and the *s* indicates that it is connected to the *s*ource terminal.

In equation form,

$$\boxed{g_m = g_{fs} = y_{fs}} \tag{8.7}$$

For the JFET of Fig. 6.20, g_{fs} ranges from 1000 μS to 5000 μS, or 1 mS to 5 mS.

Plotting g_m versus V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (8.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of g_m, as shown by the plot of Fig. 8.3.

In general, therefore

the maximum value of g_m occurs where $V_{GS} = 0$ V and the minimum value at $V_{GS} = V_P$. The more negative the value of V_{GS} the less the value of g_m.

Figure 8.3 also shows that when V_{GS} is one-half the pinch-off value, g_m is one-half the maximum value.

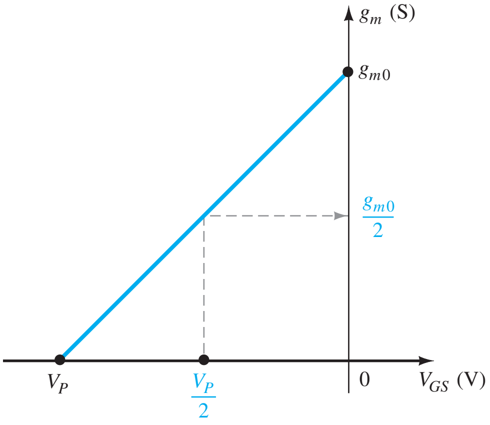


FIG. 8.3
Plot of g_m versus V_{GS}.

EXAMPLE 8.3 Plot g_m versus V_{GS} for the JFET of Examples 8.1 and 8.2.

Solution: Note Fig. 8.4.

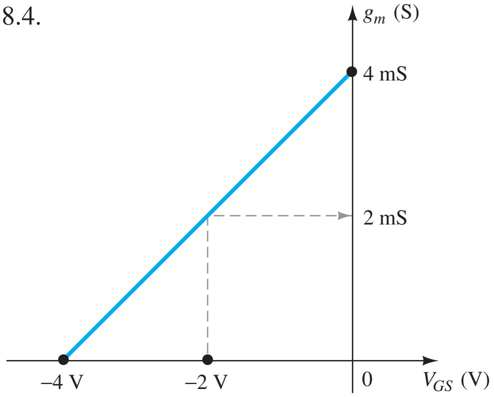


FIG. 8.4
Plot of g_m versus V_{GS} for a JFET with I_{DSS} = 8 mA and $V_P = -4$ V.

Effect of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$\boxed{1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}} \qquad \textbf{(8.8)}$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}} \qquad \textbf{(8.9)}$$

Using Eq. (8.9) to determine g_m for a few specific values of I_D, we obtain the following results:

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \mathbf{g_{m0}}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707}\mathbf{g_{m0}}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5}\mathbf{g_{m0}}$$

EXAMPLE 8.4 Plot g_m versus I_D for the JFET of Examples 8.1 through 8.3.

Solution: See Fig. 8.5.

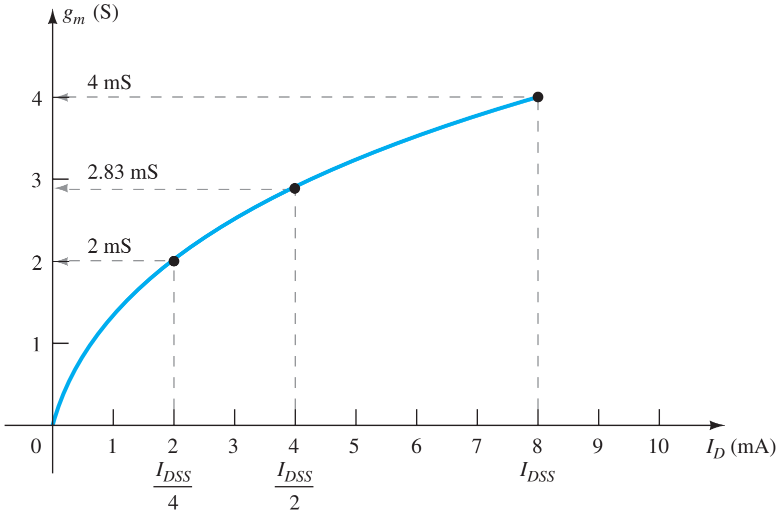


FIG. 8.5

Plot of g_m versus I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of Examples 8.3 and 8.4 clearly reveal that

the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

JFET Input Impedance Z_i

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$\boxed{Z_i\,(\text{JFET}) = \infty\,\Omega} \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

JFET Output Impedance Z_o

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as g_{os} or y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.20, g_{os} has a range of 10 μS to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$\boxed{Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}} \tag{8.11}$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$\boxed{r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}} \tag{8.12}$$

Note the requirement when applying Eq. (8.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

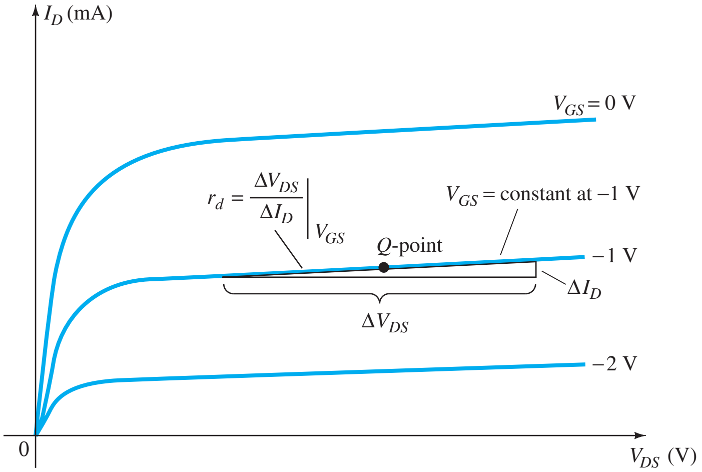


FIG. 8.6

Definition of r_d using JFET drain characteristics.

EXAMPLE 8.5 Determine the output impedance for the JFET of Fig. 8.7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

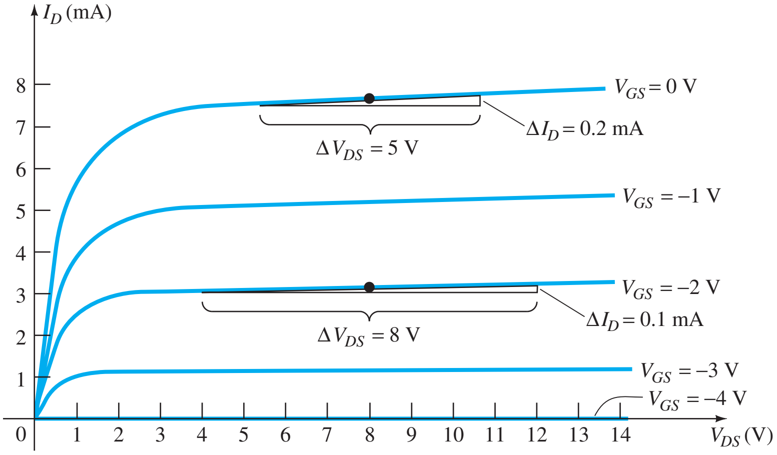


FIG. 8.7

Drain characteristics used to calculate r_d in Example 8.5.

Solution: For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$

which shows that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source g_mV_{gs} connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

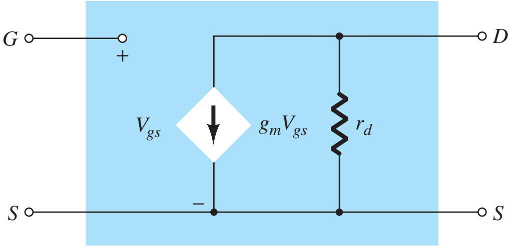


FIG. 8.8

JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source g_mV_{gs}.

In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled current source.

EXAMPLE 8.6 Given $g_{fs} = 3.8$ mS and $g_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution:

$$g_m = g_{fs} = 3.8\text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

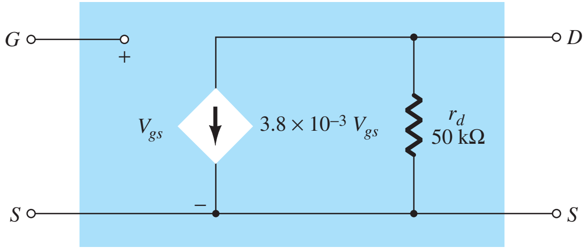


FIG. 8.9
JFET ac equivalent model for Example 8.6.

8.3 FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors C_1 and C_2, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

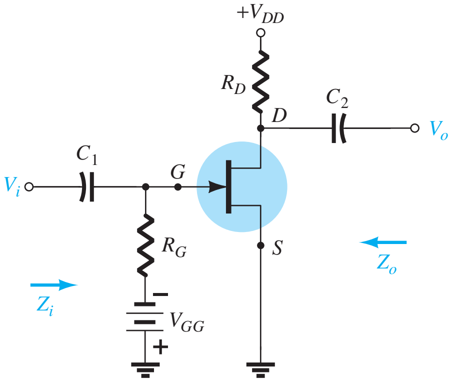


FIG. 8.10
JFET fixed-bias configuration.

Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across $R_D \| r_d$ by V_o.

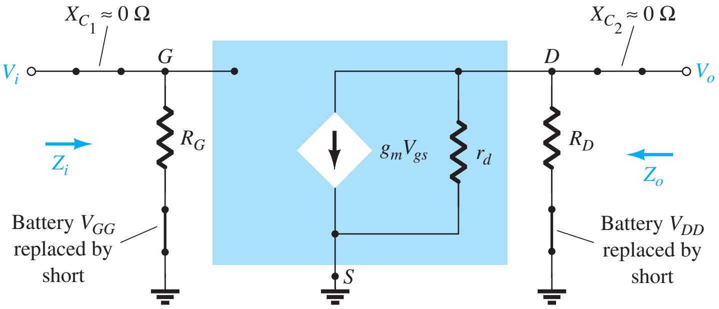

$X_{C_1} \approx 0\,\Omega$
$X_{C_2} \approx 0\,\Omega$
V_i
G
D
V_o
R_G
$g_m V_{gs}$
r_d
R_D
Z_i
Z_o
Battery V_{GG} replaced by short
Battery V_{DD} replaced by short
S

FIG. 8.11

Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.

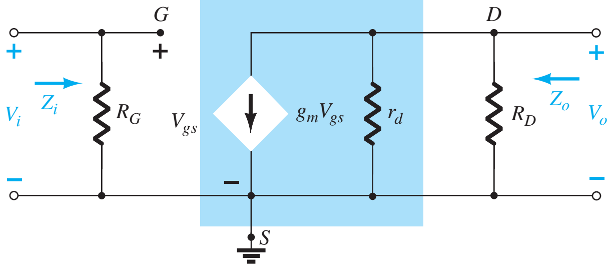

G
D
+
+
+
V_i
Z_i
R_G
V_{gs}
$g_m V_{gs}$
r_d
R_D
Z_o
V_o
–
–
–
S

FIG. 8.12

Redrawn network of Fig. 8.11.

Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G} \tag{8.13}$$

because of the infinite input impedance at the input terminals of the JFET.

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{8.14}$$

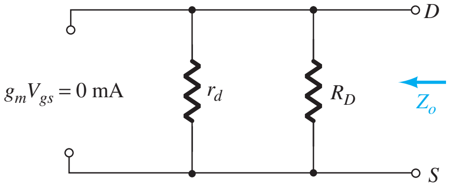

D
$g_m V_{gs} = 0$ mA
r_d
R_D
Z_o
S

FIG. 8.13

Determining Z_o.

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \qquad \textbf{(8.16)}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.17)}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

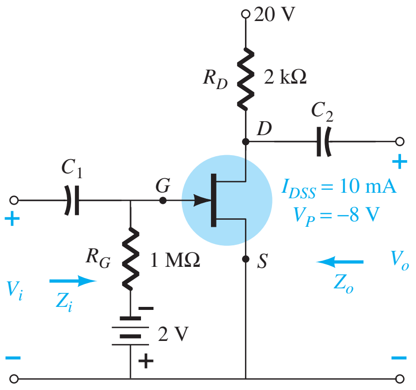


FIG. 8.14
JFET configuration for Example 8.7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\text{ k}\Omega}$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\text{ k}\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$

$\quad = \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

8.4 SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

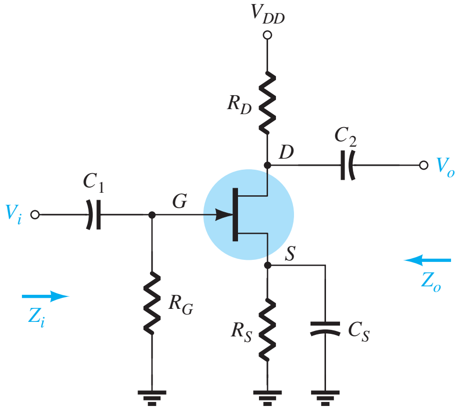

V_{DD}
R_D
D
C_2
V_o
C_1
G
V_i
S
Z_o
Z_i
R_G
R_S
C_S

FIG. 8.15
Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its open-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17. Since the resulting configuration is the same as appearing in Fig. 8.12, the resulting equations for Z_i, Z_o, and A_v will be the same.

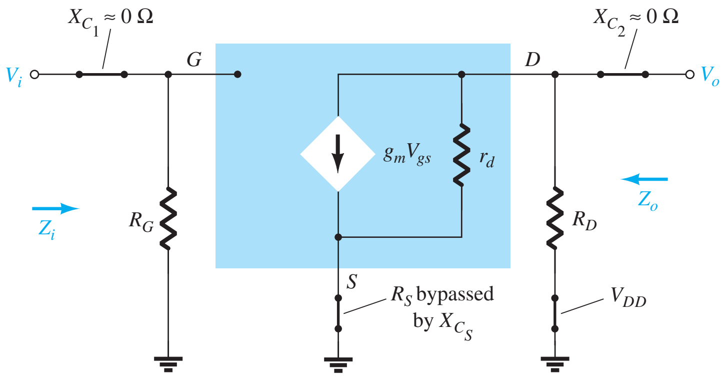

$X_{C_1} \approx 0\ \Omega$
$X_{C_2} \approx 0\ \Omega$
V_i
G
D
V_o
g_mV_{gs}
r_d
Z_o
Z_i
R_G
R_D
S
R_S bypassed by X_{C_S}
V_{DD}

FIG. 8.16
Network of Fig. 8.15 following the substitution of the JFET ac equivalent circuit.

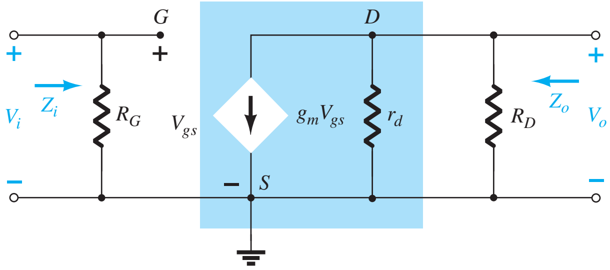

G
D
+
+
+
V_i
Z_i
R_G
V_{gs}
g_mV_{gs}
r_d
R_D
Z_o
V_o
–
–
–
S

FIG. 8.17
Redrawn network of Fig. 8.16.

Z_i

$$\boxed{Z_i = R_G} \tag{8.18}$$

Z_o

$$\boxed{Z_o = r_d \| R_D} \tag{8.19}$$

If $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.20}$$

A_v

$$\boxed{A_v = -g_m(r_d \| R_D)} \tag{8.21}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = -g_m R_D}_{r_d \geq 10R_D} \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 8.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

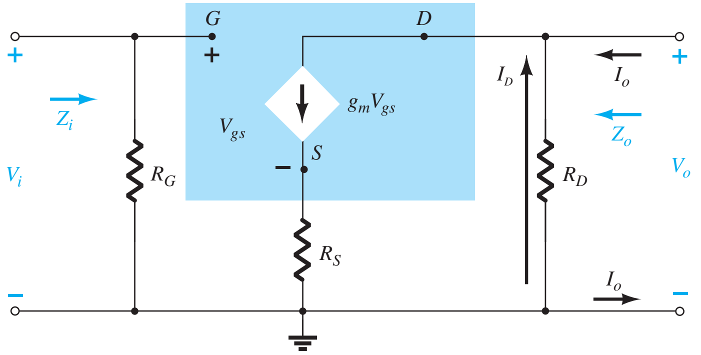


FIG. 8.18

Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$\boxed{Z_i = R_G} \tag{8.23}$$

Z_o The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$

Setting $V_i = 0$ V in Fig. 8.18 results in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

with

$$V_{gs} = -(I_o + I_D)R_S$$

so that
$$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$
or
$$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$
and
$$I_o = -I_D \quad \text{(the controlled current source } g_m V_{gs} = 0\text{ A for the applied conditions)}$$
Since
$$V_o = -I_D R_D$$
then
$$V_o = -(-I_o)R_D = I_o R_D$$
and
$$\boxed{Z_o = \frac{V_o}{I_o} = R_D}_{r_d = \infty\,\Omega} \tag{8.24}$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 8.19.

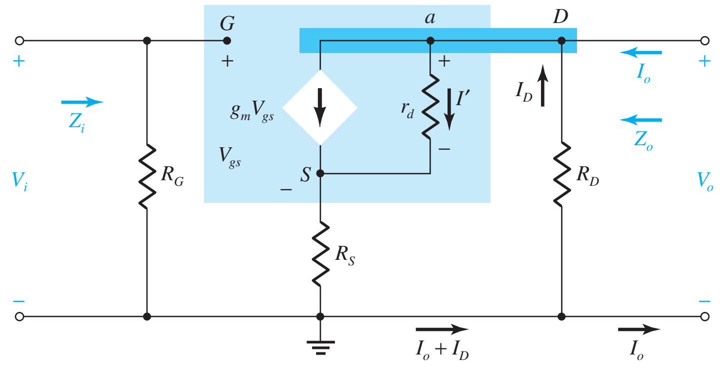


FIG. 8.19

Including the effects of r_d in the self-bias JFET configuration.

Since
$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$
we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law, we have
$$I_o = g_m V_{gs} + I_{r_d} - I_D$$
but
$$V_{r_d} = V_o + V_{gs}$$
and
$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$
or
$$I_o = \left(g_m + \frac{1}{r_d}\right)V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$
Now,
$$V_{gs} = -(I_D + I_o)R_S$$
so that
$$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)R_S - \frac{I_D R_D}{r_d} - I_D$$
with the result that
$$I_o\left[1 + g_m R_S + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$
or
$$I_o = \frac{-I_D\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}{1 + g_m R_S + \dfrac{R_S}{r_d}}$$
and
$$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right)}{1 + g_m R_S + \dfrac{R_S}{r_d}}}$$

and finally,

$$\boxed{Z_o = \frac{\left[1 + g_mR_S + \dfrac{R_S}{r_d}\right]}{\left[1 + g_mR_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}R_D} \qquad \textbf{(8.25a)}$$

For $r_d \geq 10R_D$,

$$\left(1 + g_mR_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$$

and

$$1 + g_mR_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_mR_S + \frac{R_S}{r_d}$$

resulting in

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \qquad \textbf{(8.25b)}$$

A_v For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{R_S} = 0$$
$$V_{gs} = V_i - I_DR_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_{r_d} = V_o - V_{R_S}$$

and

$$I' = \frac{V_{r_d}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_mV_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S}, we have

$$I_D = g_m[V_i - I_DR_S] + \frac{(-I_DR_D) - (I_DR_S)}{r_d}$$

so that

$$I_D\left[1 + g_mR_S + \frac{R_D + R_S}{r_d}\right] = g_mV_i$$

or

$$I_D = \frac{g_mV_i}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_DR_D = -\frac{g_mR_DV_i}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_mR_D}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}}} \qquad \textbf{(8.26)}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{g_mR_D}{1 + g_mR_S}}_{r_d \geq 10(R_D + R_S)} \qquad \textbf{(8.27)}$$

Phase Relationship The negative sign in Eq. (8.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

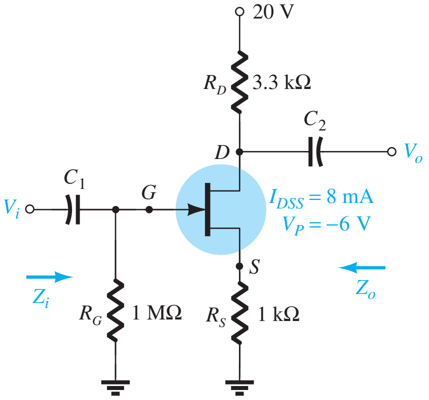


FIG. 8.20
Network for Example 8.8.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\text{ k}\Omega}$$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. With r_d,

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\text{ k}\Omega}$$

If $r_d = \infty\,\Omega$,

$$Z_o = R_D = \mathbf{3.3\text{ k}\Omega}$$

e. With r_d,

$$A_v = \frac{-g_mR_D}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

With $r_d = \infty\,\Omega$ (open-circuit equivalence),

$$A_v = \frac{-g_mR_D}{1 + g_mR_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d is minimal because the condition $r_d \geq 10(R_D + R_S)$ is satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

8.5 VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.21.

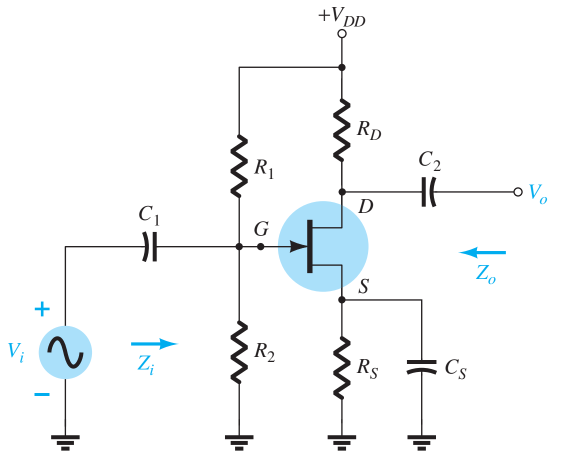


FIG. 8.21
JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 8.23. R_D can also be brought down to ground, but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$\boxed{Z_i = R_1 \| R_2} \tag{8.28}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$\boxed{Z_o = r_d \| R_D} \tag{8.29}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{\,r_d \geq 10R_D} \tag{8.30}$$

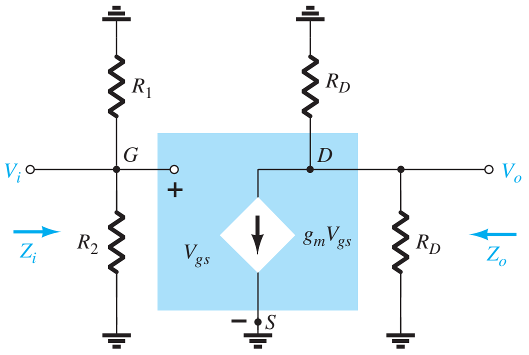


FIG. 8.22
Network of Fig. 8.21 under ac conditions.

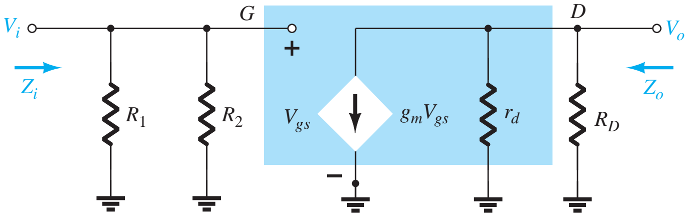


FIG. 8.23
Redrawn network of Fig. 8.22.

A_v

$$V_{gs} = V_i$$

and
$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that
$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.31}$$

If $r_d \geq 10R_D$,
$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{\,r_d \geq 10R_D} \tag{8.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

8.6 COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 8.24, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit results in Fig. 8.25. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network and the controlled current source is connected directly from drain to source. In addition, the resistor connected between input terminals is no longer R_G, but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

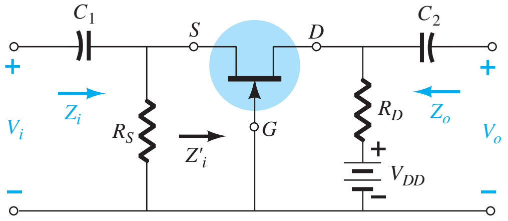


FIG. 8.24
JFET common-gate configuration.

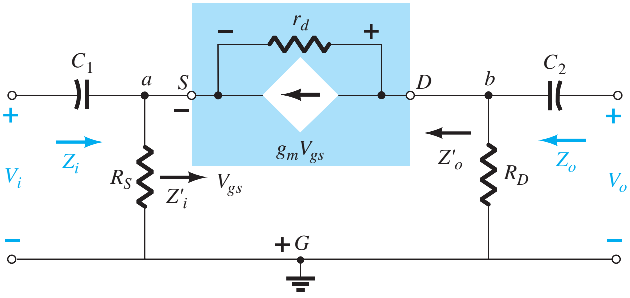


FIG. 8.25
Network of Fig. 8.24 following substitution of JFET ac equivalent model.

Z_i The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 8.24, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 8.26. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and
$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

Applying Kirchhoff's current law at node a results in

$$I' + g_m V_{gs} = I_{r_d}$$

and
$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or
$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

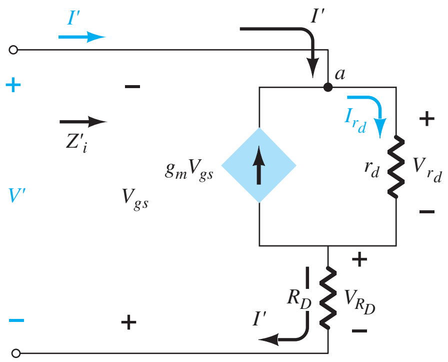


FIG. 8.26
Determining Z'_i for the network of Fig. 8.24.

so that
$$I'\left[1+\frac{R_D}{r_d}\right]=V'\left[\frac{1}{r_d}+g_m\right]$$

and
$$\boxed{Z'_i=\frac{V'}{I'}=\frac{\left[1+\dfrac{R_D}{r_d}\right]}{\left[g_m+\dfrac{1}{r_d}\right]}}\qquad\textbf{(8.33)}$$

or
$$Z'_i=\frac{V'}{I'}=\frac{r_d+R_D}{1+g_mr_d}$$

and
$$Z_i=R_S\|Z'_i$$

which results in
$$\boxed{Z_i=R_S\|\left[\frac{r_d+R_D}{1+g_mr_d}\right]}\qquad\textbf{(8.34)}$$

If $r_d \geq 10R_D$, Eq. (8.33) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z'_i=\frac{\left[1+\dfrac{R_D}{r_d}\right]}{\left[g_m+\dfrac{1}{r_d}\right]}\cong\frac{1}{g_m}$$

and
$$\boxed{Z_i\cong R_S\|1/g_m}_{r_d\geq 10R_D}\qquad\textbf{(8.35)}$$

Z_o Substituting $V_i = 0$ V in Fig. 8.25 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_mV_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o=R_D\|r_d}\qquad\textbf{(8.36)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o\cong R_D}_{r_d\geq 10R_D}\qquad\textbf{(8.37)}$$

A_v Figure 8.25 reveals that

$$V_i=-V_{gs}$$

and
$$V_o=I_DR_D$$

The voltage across r_d is

$$V_{r_d}=V_o-V_i$$

and
$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node *b* in Fig. 8.25 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and
$$I_D = -I_{r_d} - g_m V_{gs}$$
$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$
$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that
$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$
$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and
$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}} \qquad \textbf{(8.38)}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (8.38) can be dropped as a good approximation, and

$$\boxed{A_v \cong g_m R_D}_{r_d \geq 10R_D} \qquad \textbf{(8.39)}$$

Phase Relationship The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 8.9 Although the network of Fig. 8.27 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.24. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Determine V_o with and without r_d. Compare results.

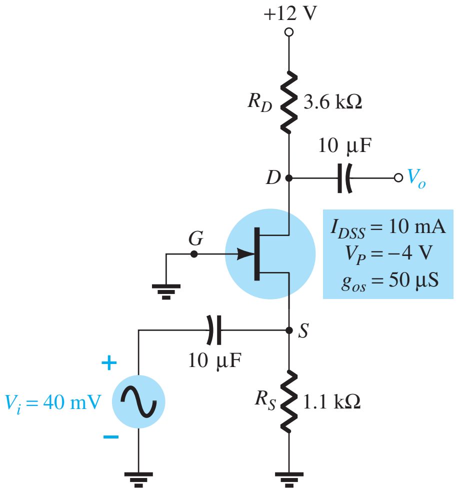


FIG. 8.27
Network for Example 8.9.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\text{ mS}}$$

b. $$r_d = \frac{1}{g_{os}} = \frac{1}{50\ \mu\text{S}} = \mathbf{20\text{ k}\Omega}$$

c. With r_d,

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ mS})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\text{ k}\Omega}$$

Without r_d,

$$Z_i = R_S \| 1/g_m = 1.1\text{ k}\Omega \| 1/2.25\text{ ms} = 1.1\text{ k}\Omega \| 0.44\text{ k}\Omega$$
$$= \mathbf{0.31\text{ k}\Omega}$$

Even though the condition $r_d \geq 10R_D$ is not satisfied with $r_d = 20\text{ k}\Omega$ and $10R_D = 36\text{ k}\Omega$, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

d. With r_d,

$$Z_o = R_D \| r_d = 3.6\text{ k}\Omega \| 20\text{ k}\Omega = \mathbf{3.05\text{ k}\Omega}$$

Without r_d,

$$Z_o = R_D = \mathbf{3.6\text{ k}\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

e. With r_d,

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\text{ mS})(3.6\text{ k}\Omega) + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}{\left[1 + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}$$

$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $$A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\text{ mV}) = \mathbf{280.8\text{ mV}}$$

Without r_d,

$$A_v = g_m R_D = (2.25\text{ mS})(3.6\text{ k}\Omega) = \mathbf{8.1}$$

with $$V_o = A_v V_i = (8.1)(40\text{ mV}) = \mathbf{324\text{ mV}}$$

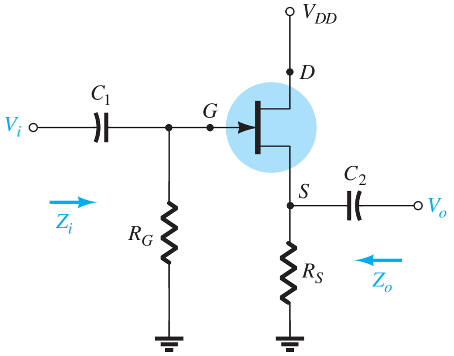
In this case, the difference is a little more noticeable, but not dramatically so.

Example 8.9 demonstrates that even though the condition $r_d \geq 10R_D$ was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

8.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 8.28. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology *common-drain*).

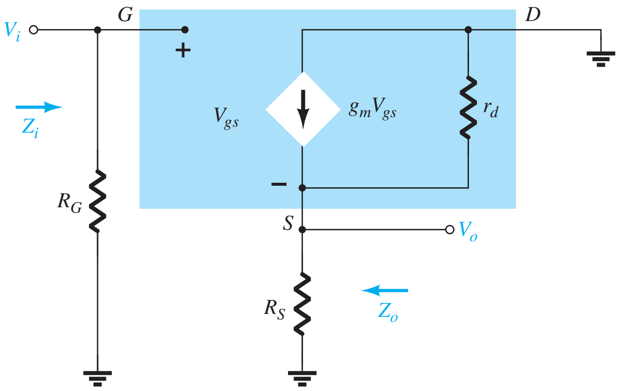
Substituting the JFET equivalent circuit results in the configuration of Fig. 8.29. The controlled source and the internal output impedance of the JFET are tied to ground at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to



V_{DD}
D
C_1
V_i
G
C_2
S
V_o
Z_i
R_G
R_S
Z_o

FIG. 8.28

JFET source-follower configuration.

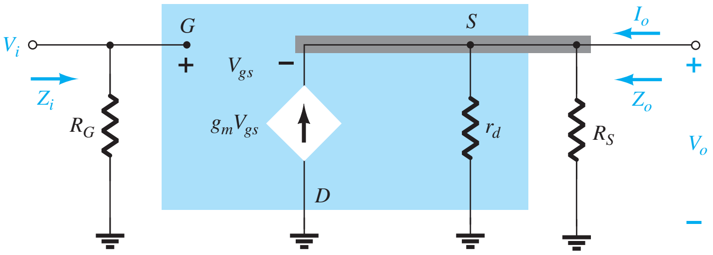


V_i
G
D
$+$
Z_i
V_{gs}
g_mV_{gs}
r_d
R_G
$-$
S
V_o
R_S
Z_o

FIG. 8.29

Network of Fig. 8.28 following the substitution of the JFET ac equivalent model.

the same terminal and ground, they can all be placed in parallel as shown in Fig. 8.30. The current source reversed direction, but V_{gs} is still defined between the gate and source terminals.



V_i
G
S
I_o
$+$
V_{gs}
$-$
$+$
Z_i
Z_o
R_G
g_mV_{gs}
r_d
R_S
V_o
D
$-$

FIG. 8.30

Network of Fig. 8.29 redrawn.

Z_i Figure 8.30 clearly reveals that Z_i is defined by

$$\boxed{Z_i = R_G} \tag{8.40}$$

Z_o Setting $V_i = 0$ V results in the gate terminal being connected directly to the ground as shown in Fig. 8.31.

The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

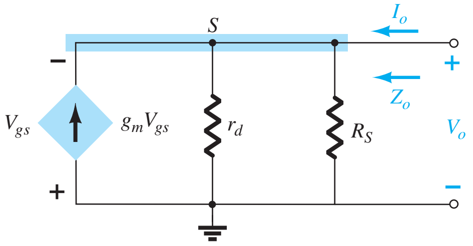


FIG. 8.31
Determining Z_o for the network of Fig. 8.30.

Applying Kirchhoff's current law at node *S*, we obtain

$$I_o + g_mV_{gs} = I_{r_d} + I_{R_s}$$
$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is
$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_mV_{gs}$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and
$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{8.41}$$

For $r_d \geq 10\,R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{r_d \geq 10R_S} \tag{8.42}$$

A_v The output voltage V_o is determined by

$$V_o = g_mV_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 8.30 results in

$$V_i = V_{gs} + V_o$$

and
$$V_{gs} = V_i - V_o$$

so that
$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or
$$V_o = g_mV_i(r_d \| R_S) - g_mV_o(r_d \| R_S)$$

and
$$V_o[1 + g_m(r_d \| R_S)] = g_mV_i(r_d \| R_S)$$

so that
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{8.43}$$

In the absence of r_d or if $r_d \geq 10\,R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_mR_S}{1 + g_mR_S}}_{r_d \geq 10R_S} \tag{8.44}$$

Since the denominator of Eq. (8.43) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).

Phase Relationship Since A_v of Eq. (8.43) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

EXAMPLE 8.10 A dc analysis of the source-follower network of Fig. 8.32 results in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o with and without r_d. Compare results.
e. Determine A_v with and without r_d. Compare results.

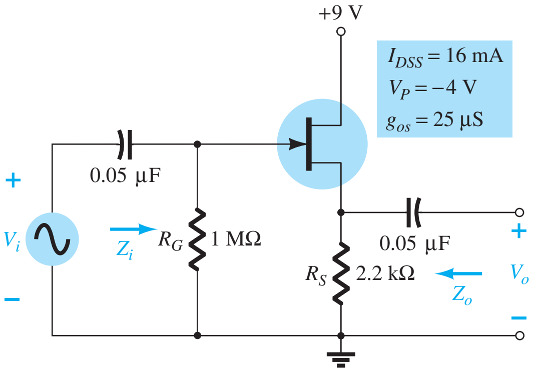


FIG. 8.32
Network to be analyzed in Example 8.10.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\text{ mS}}$$

b. $$r_d = \frac{1}{g_{os}} = \frac{1}{25\ \mu\text{S}} = \mathbf{40\text{ k}\Omega}$$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. With r_d,

$$\begin{aligned} Z_o &= r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS} \\ &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega \\ &= \mathbf{362.52\ \Omega} \end{aligned}$$

which shows that Z_o is often relatively small and determined primarily by $1/g_m$.
Without r_d,

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

which shows that r_d typically has little effect on Z_o.

e. With r_d,

$$\begin{aligned} A_v &= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)} \\ &= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83} \end{aligned}$$

which is less than 1, as predicted above.

Without r_d,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28 \text{ mS})(2.2 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(2.2 \text{ k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that r_d usually has little effect on the gain of the configuration.

8.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs shown in Fig. 8.33 is exactly the same as that employed for JFETs, as shown in Fig. 8.8.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for *n*-channel devices and negative for *p*-channel units. The result is that g_m can be greater than g_{m0}, as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

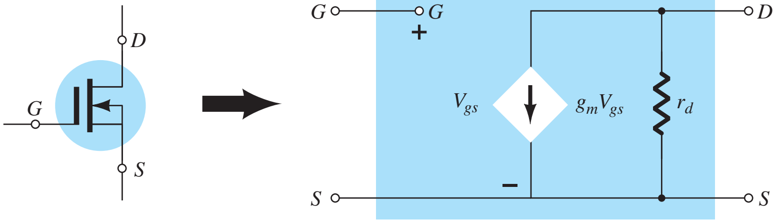


FIG. 8.33

D-MOSFET ac equivalent model.

EXAMPLE 8.11 The network of Fig. 8.34 was analyzed as Example 7.7, resulting in $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

a. Determine g_m and compare to g_{m0}.
b. Find r_d.
c. Sketch the ac equivalent network for Fig. 8.34.
d. Find Z_i.
e. Calculate Z_o.
f. Find A_v.

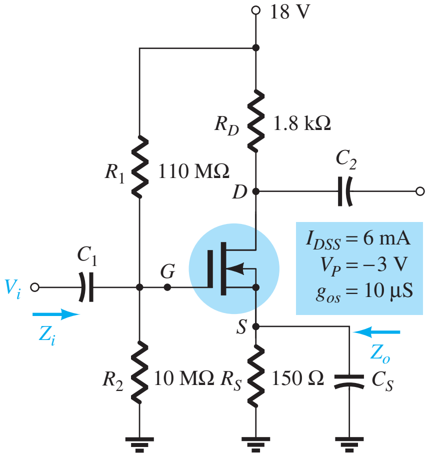


FIG. 8.34

Network for Example 8.11.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{10\ \mu\text{S}} = \mathbf{100\text{ k}\Omega}$$

c. See Fig. 8.35. Note the similarities with the network of Fig. 8.23. Equations (8.28) through (8.32) are therefore applicable.

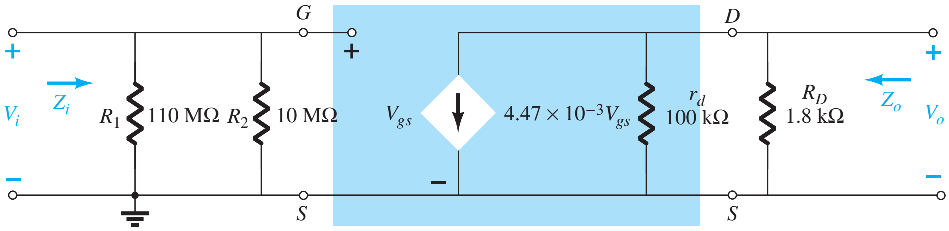


FIG. 8.35

AC equivalent circuit for Fig. 8.34.

d. Eq. (8.28): $Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\text{ M}\Omega}$

e. Eq. (8.29): $Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\text{ k}\Omega} \cong R_D = \mathbf{1.8\text{ k}\Omega}$

f. $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

Eq. (8.32): $A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$

8.9 ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET (E-MOSFET) can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 8.36. The ac small-signal equivalent circuit of either device is shown in Fig. 8.36, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as a conductance g_{os} or admittance y_{os}. The device transconductance g_m is provided on specification sheets as the forward transfer admittance y_{fs}.

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

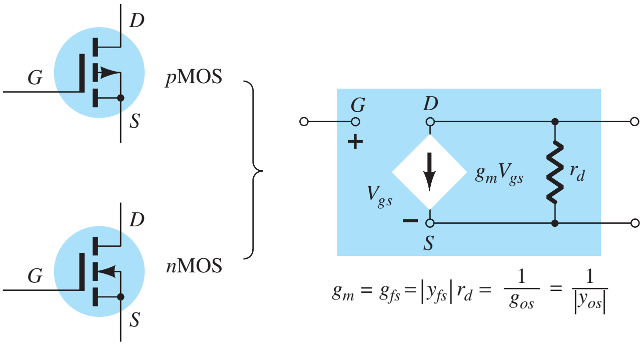

D
G
S
pMOS
D
G
S
nMOS
G
D
+
V_{gs}
−
S
$g_m V_{gs}$
r_d
$g_m = g_{fs} = |y_{fs}|$ $r_d = \frac{1}{g_{os}} = \frac{1}{|y_{os}|}$

FIG. 8.36

Enhancement MOSFET ac small-signal model.

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}}k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2 \\ &= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0) \end{aligned}$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \qquad \textbf{(8.45)}$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

8.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.37. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore $V_{R_G} = 0$ V. However, for ac situations it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

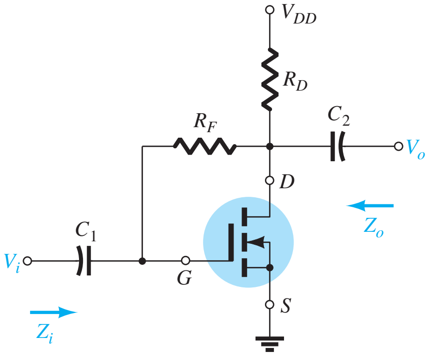


FIG. 8.37
E-MOSFET drain-feedback configuration.

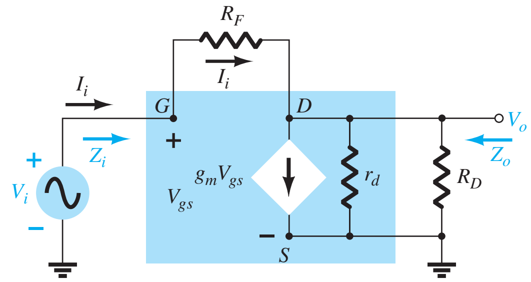


FIG. 8.38
AC equivalent of the network of Fig. 8.37.

Substituting the ac equivalent model for the device results in the network of Fig. 8.38. Note that R_F is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

Z_i Applying Kirchhoff's current law to the output circuit (at node D in Fig. 8.38) results in

$$I_i = g_mV_{gs} + \frac{V_o}{r_d \| R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_mV_i + \frac{V_o}{r_d \| R_D}$$

or

$$I_i - g_mV_i = \frac{V_o}{r_d \| R_D}$$

Therefore,

$$V_o = (r_d \| R_D)(I_i - g_mV_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_mV_i)}{R_F}$$

and
$$I_iR_F = V_i - (r_d \| R_D)I_i + (r_d \| R_D)g_mV_i$$
so that
$$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$
and finally,
$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}} \tag{8.46}$$

Typically, $R_F \gg r_d \| R_D$, so that
$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$
For $r_d \geq 10R_D$,
$$\boxed{Z_i \cong \frac{R_F}{1 + g_mR_D}} \quad {\scriptstyle R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{8.47}$$

Z_o Substituting $V_i = 0$ V results in $V_{gs} = 0$ V and $g_mV_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 8.39. R_F, r_d, and R_D are then in parallel and
$$\boxed{Z_o = R_F \| r_d \| R_D} \tag{8.48}$$

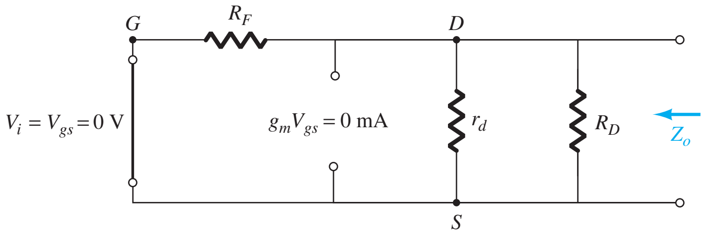


FIG. 8.39
Determining Z_o for the network of Fig. 8.37.

Normally, R_F is so much larger than $r_d \| R_D$ that
$$Z_o \cong r_d \| R_D$$
and with $r_d \geq 10R_D$,
$$\boxed{Z_o \cong R_D} \quad {\scriptstyle R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{8.49}$$

A_v Applying Kirchhoff's current law at node *D* of Fig. 8.38 results in
$$I_i = g_mV_{gs} + \frac{V_o}{r_d \| R_D}$$
but
$$V_{gs} = V_i \qquad \text{and} \qquad I_i = \frac{V_i - V_o}{R_F}$$
so that
$$\frac{V_i - V_o}{R_F} = g_mV_i + \frac{V_o}{r_d \| R_D}$$
and
$$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_mV_i + \frac{V_o}{r_d \| R_D}$$
so that
$$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$
and
$$A_v = \frac{V_o}{V_i} = \frac{\left[\dfrac{1}{R_F} - g_m\right]}{\left[\dfrac{1}{r_d \| R_D} + \dfrac{1}{R_F}\right]}$$
but
$$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and $$g_m \gg \frac{1}{R_F}$$

so that $$\boxed{A_v = -g_m(R_F \| r_d \| R_D)} \tag{8.50}$$

Since R_F is usually $\gg r_d \| R_D$ and if $r_d \geq 10R_D$,

$$\boxed{A_v \cong -g_m R_D}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{8.51}$$

Phase Relationship The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

EXAMPLE 8.12 The E-MOSFET of Fig. 8.40 was analyzed in Example 7.10, with the result that $k = 0.24 \times 10^{-3}\ \text{A/V}^2$, $V_{GS_Q} = 6.4\ \text{V}$, and $I_{D_Q} = 2.75\ \text{mA}$.

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Find A_v with and without r_d. Compare results.

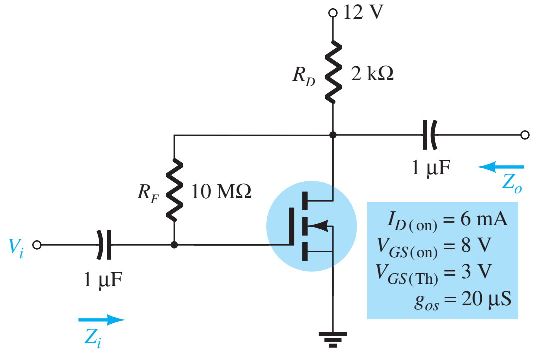

12 V
R_D
2 kΩ
V_o
1 µF
Z_o
R_F
10 MΩ
V_i
1 µF
Z_i
$I_{D(\text{on})} = 6\ \text{mA}$
$V_{GS(\text{on})} = 8\ \text{V}$
$V_{GS(\text{Th})} = 3\ \text{V}$
$g_{os} = 20\ \mu\text{S}$

FIG. 8.40
Drain-feedback amplifier from Example 8.11.

Solution:

a. $$\begin{aligned} g_m &= 2k(V_{GS_Q} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V}) \\ &= \mathbf{1.63\ mS} \end{aligned}$$

b. $$r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

c. With r_d,

$$\begin{aligned} Z_i &= \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)} \\ &= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega} \end{aligned}$$

Without r_d,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

which shows that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

d. With r_d,

$$\begin{aligned} Z_o &= R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega \\ &= \mathbf{1.92\ k\Omega} \end{aligned}$$

Without r_d,

$$Z_o \cong R_D = \mathbf{2\,k\Omega}$$

again providing very close results.

e. With r_d,

$$\begin{aligned} A_v &= -g_m(R_F \| r_d \| R_D) \\ &= -(1.63\text{ mS})(10\text{ M}\Omega \| 50\text{ k}\Omega \| 2\text{ k}\Omega) \\ &= -(1.63\text{ mS})(1.92\text{ k}\Omega) \\ &= \mathbf{-3.21} \end{aligned}$$

Without r_d,

$$\begin{aligned} A_v &= -g_m R_D = -(1.63\text{ mS})(2\text{ k}\Omega) \\ &= \mathbf{-3.26} \end{aligned}$$

which is very close to the above result.

8.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.42, which is exactly the same as Fig. 8.23. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

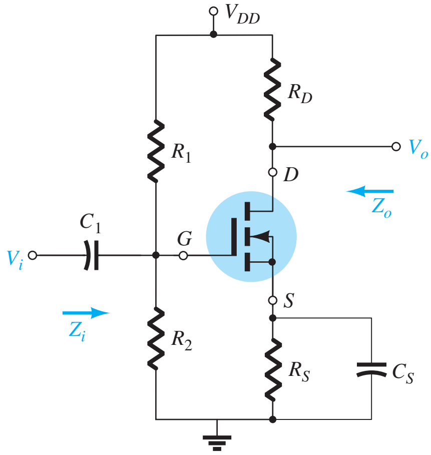


FIG. 8.41
E-MOSFET voltage-divider configuration.

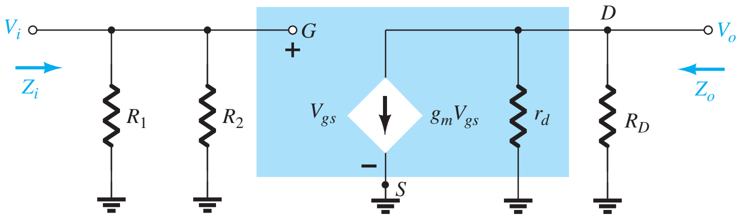


FIG. 8.42
AC equivalent network for the configuration of Fig. 8.41.

Z_i

$$\boxed{Z_i = R_1 \| R_2} \tag{8.52}$$

Z_o

$$\boxed{Z_o = r_d \| R_D} \tag{8.53}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_d}_{\,r_d \geq 10R_D} \tag{8.54}$$

A_v

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.55}$$

and if $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D} \tag{8.56}$$

8.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used "in reverse" to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance R_G could be replaced by a short-circuit equivalent in the feedback configuration because $I_G \cong 0$ A for dc conditions, but for the ac analysis, it presents an important high-impedance path between V_o and V_i. In addition, recall that g_m is larger for operating points closer to the I_D axis ($V_{GS} = 0$ V), requiring that R_S be relatively small. In the unbypassed R_S network, a small R_S will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its effect on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples determine the required parameters for a specific gain.

EXAMPLE 8.13 Design the fixed-bias network of Fig. 8.43 to have an ac gain of 10. That is, determine the value of R_D.

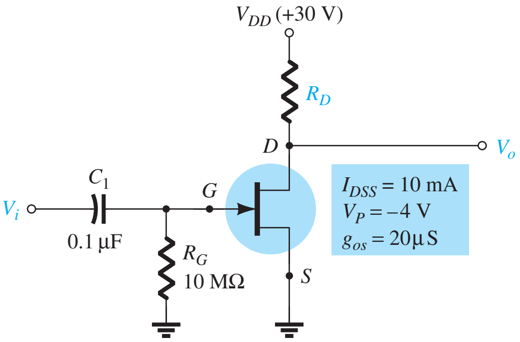


FIG. 8.43

Circuit for desired voltage gain in Example 8.13.

Solution: Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{g_{os}} = \frac{1}{20 \times 10^{-6}\,\text{S}} = 50\,\text{k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50\,\text{k}\Omega = 2\,\text{k}\Omega$$

and
$$\frac{R_D(50\,\text{k}\Omega)}{R_D + 50\,\text{k}\Omega} = 2\,\text{k}\Omega$$

or
$$50R_D = 2(R_D + 50\,\text{k}\Omega) = 2R_D + 100\,\text{k}\Omega$$

with
$$48R_D = 100\,\text{k}\Omega$$

and
$$R_D = \frac{100\,\text{k}\Omega}{48} \cong 2.08\,\text{k}\Omega$$

The closest standard value is **2 kΩ** (Appendix D), which would be employed for this design.

The resulting level of V_{DS_Q} is then determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\,\text{V} - (10\,\text{mA})(2\,\text{k}\Omega) = \mathbf{10\,V}$$

The levels of Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10\,M\Omega}$$

$$Z_o = R_D \| r_d = 2\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{1.92\,k\Omega} \cong R_D = 2\,\text{k}\Omega$$

EXAMPLE 8.14 Choose the values of R_D and R_S for the network of Fig. 8.44 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

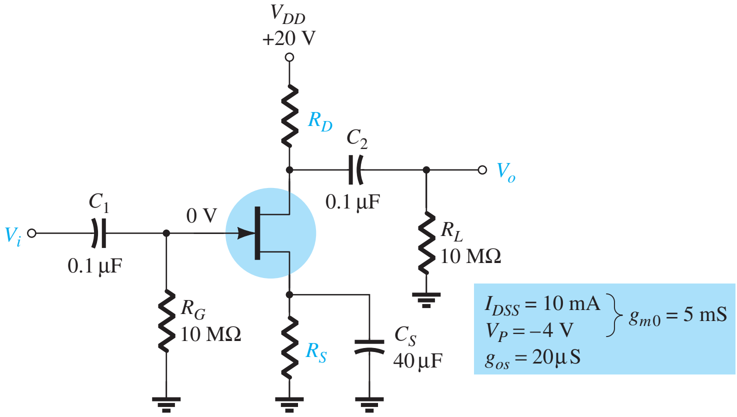


FIG. 8.44
Network for desired voltage gain in Example 8.14.

Solution: The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\,\text{V}) = -1\,\text{V}$$

and
$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\,\text{mA}\left(1 - \frac{(-1\,\text{V})}{(-4\,\text{V})}\right)^2 = 5.625\,\text{mA}$$

Determining g_m, we obtain

$$\begin{aligned} g_m &= g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) \\ &= 5\,\text{mS}\left(1 - \frac{(-1\,\text{V})}{(-4\,\text{V})}\right) = 3.75\,\text{mS} \end{aligned}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

so that
$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

and
$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\text{ k}\Omega}$$

which is a standard value.

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$
$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and
$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is **180 Ω**. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

In the next example, R_S is unbypassed and the design becomes a bit more complicated.

EXAMPLE 8.15 Determine R_D and R_S for the network of Fig. 8.44 to establish a gain of 8 if the bypass capacitor C_S is removed.

Solution: V_{GS_Q} and I_{D_Q} are still -1 V and 5.625 mA, respectively, and since the equation $V_{GS} = -I_D R_S$ has not changed, R_S continues to equal the standard value of **180 Ω** obtained in Example 8.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that $r_d \geq 10(R_D + R_S)$. Using the full equation for A_v at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain), we obtain

$$|8| = \left|\frac{-(3.75\text{ mS})R_D}{1 + (3.75\text{ mS})(180\ \Omega)}\right| = \frac{(3.75\text{ mS})R_D}{1 + 0.675}$$

and
$$8(1 + 0.675) = (3.75\text{ mS})R_D$$

so that
$$R_D = \frac{13.4}{3.75\text{ mS}} = 3.573\text{ k}\Omega$$

with the closest standard value at **3.6 kΩ**.

We can now test the condition

$$r_d \geq 10(R_D + R_S)$$

We have
$$50\text{ k}\Omega \geq 10(3.6\text{ k}\Omega + 0.18\text{ k}\Omega) = 10(3.78\text{ k}\Omega)$$

and
$$50\text{ k}\Omega \geq 37.8\text{ k}\Omega$$

which is satisfied—the solution stands!

8.13 SUMMARY TABLE

To provide a quick comparison between configurations and offer a listing that can be helpful for a variety of reasons, Table 8.1 was developed. The exact and approximate equations for each important parameter are provided with a typical range of values for each. Although

TABLE 8.1

Z_i, Z_o, and A_v for various FET configurations

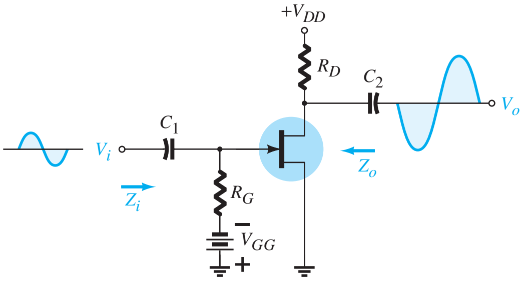
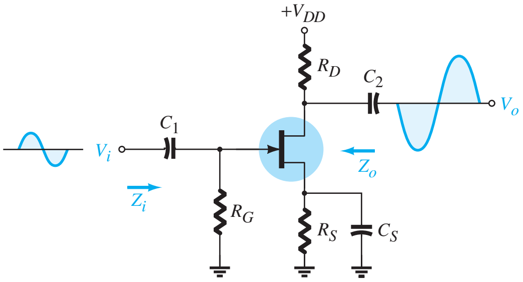
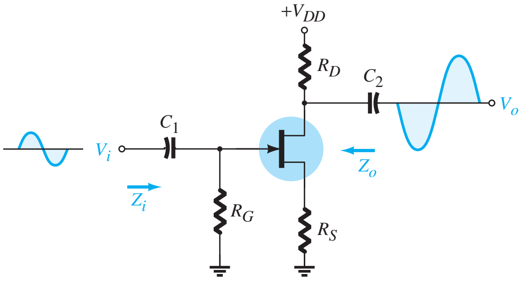
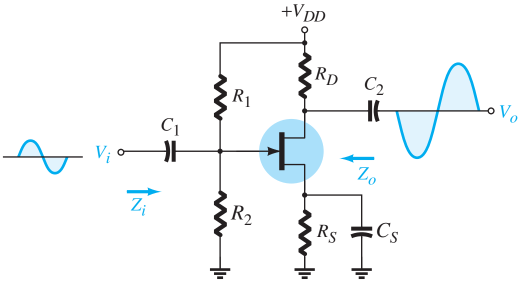
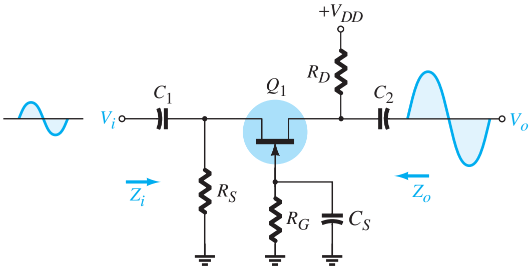
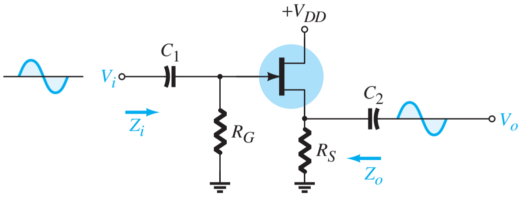
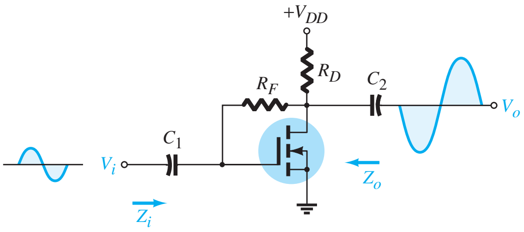
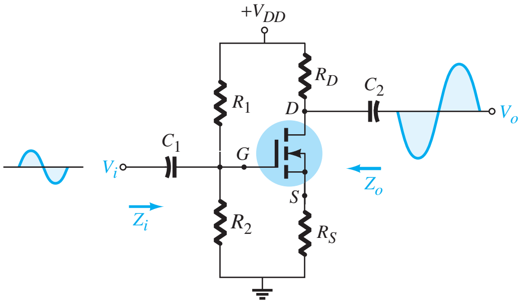
Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]  $+V_{DD}$ R_D C_2 V_o C_1 V_i Z_o Z_i R_G $-$ V_{GG} $+$	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\,R_D)$	Medium (−10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET]  $+V_{DD}$ R_D C_2 V_o C_1 V_i Z_o Z_i R_G R_S C_S	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\,R_D)$	Medium (−10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\,R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET]  $+V_{DD}$ R_D C_2 V_o C_1 V_i Z_o Z_i R_G R_S	High (10 MΩ) $= \boxed{R_G}$	$= \boxed{\dfrac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}}$ $= \boxed{R_D}$ $r_d \geq 10\,R_D$ or $r_d = \infty\,\Omega$	Low (−2) $= \boxed{\dfrac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}}$ $\cong \boxed{-\dfrac{g_m R_D}{1 + g_m R_S}}$ $[r_d \geq 10\,(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET]  $+V_{DD}$ R_1 R_D C_2 V_o C_1 V_i Z_o Z_i R_2 R_S C_S	High (10 MΩ) $= \boxed{R_1 \| R_2}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\,R_D)$	Medium (−10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\,R_D)$

TABLE 8.1

(Continued)

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET]  $+V_{DD}$ R_D Q_1 C_1 C_2 V_i V_o Z_i Z_o R_S R_G C_S	Low (1 kΩ) $= \boxed{R_S \Big\Vert \left[\frac{r_d + R_D}{1 + g_m r_d}\right]}$ $\cong \boxed{R_S \Big\Vert \frac{1}{g_m}}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $(R_d \geq 10\, R_D)$	Medium (+10) $= \boxed{\frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}}$ $\cong \boxed{g_m R_D}$ $(r_d \geq 10\, RD)$
Source-follower [JFET or D-MOSFET]  $+V_{DD}$ C_1 C_2 V_i V_o Z_i Z_o R_G R_S	High (10 MΩ) $= \boxed{R_G}$	Low (100 kΩ) $= \boxed{r_d \Vert R_S \Vert 1/g_m}$ $\cong \boxed{R_S \Vert 1/g_m}$ $(r_d \geq 10\, R_S)$	Low (<1) $= \boxed{\frac{g_m(r_d \Vert R_S)}{1 + g_m(r_d \Vert R_S)}}$ $\cong \boxed{\frac{g_m R_S}{1 + g_m R_S}}$ $(r_d \geq 10\, R_S)$
Drain-feedback bias E-MOSFET  $+V_{DD}$ R_D R_F C_2 C_1 V_i V_o Z_i Z_o	Medium (1 MΩ) $= \boxed{\frac{R_F + r_d \Vert R_D}{1 + g_m(r_d \Vert R_D)}}$ $\cong \boxed{\frac{R_F}{1 + g_m R_D}}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= \boxed{R_F \Vert r_d \Vert R_D}$ $\cong \boxed{R_D}$ $(R_F, r_d \geq 10 R_D)$	Medium (−10) $= \boxed{-g_m(R_F \Vert r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $(R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET  $+V_{DD}$ R_1 R_D D C_2 C_1 G V_i V_o S Z_i Z_o R_2 R_S	Medium (1 MΩ) $= \boxed{R_1 \Vert R_2}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\, R_D)$	Medium (–10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\, R_D)$

all the possible configurations are not present, the majority of the most frequently encountered are included. In fact, any configuration not listed will probably be some variation of those appearing in the table, so at the very least, the listing will provide some insight as to what expected levels should be and which path will probably generate the desired equations. The format chosen was designed to permit a duplication of the entire table on the front and back of one $8\frac{1}{2}$ by 11 inch page.

8.14 EFFECT OF R_L AND R_{sig}

This section will parallel Sections 5.16 and 5.17 of the BJT small-signal ac analysis chapter dealing with the effect of the source resistance and load resistance on the ac gain of an amplifier. There are again two approaches to the analysis. One can simply substitute the ac model for the FET of interest and perform a detailed analysis similar to the unloaded situation, or apply the two-port equations introduced in Section 5.17.

All of the two-port equations developed for the BJT transistor apply to FET networks also because the quantities of interest are defined at the input and output terminals and not the components of the system.

A few of the most important equations are repeated below to provide an easy reference for the analysis of this chapter and to refresh your memory about the conclusions:

$$\boxed{A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}} \tag{8.57}$$

$$\boxed{A_i = -A_{v_L}\frac{Z_i}{R_L}} \tag{8.58}$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = \left(\frac{R_i}{R_i + R_{\text{sig}}}\right)\left(\frac{R_L}{R_L + R_o}\right) A_{v_{\text{NL}}}} \tag{8.59}$$

Some of the important conclusions about the gain of BJT transistor configurations are also applicable to FET networks. They include the following facts:

The greatest gain of an amplifier is the no-load gain.

The loaded gain is always less than the no-load gain.

A source impedance will always reduce the overall gain below the no-load or loaded level.

In general, therefore,

$$\boxed{A_{v_{\text{NL}}} > A_{v_L} > A_{v_S}} \tag{8.60}$$

Recall from Chapter 5 that some BJT configurations are such that the output impedance is sensitive to the source impedance or the input impedance is sensitive to the applied load. For FET networks, however:

Due to the high impedance between the gate terminal and the channel, one can generally assume that the input impedance is unaffected by the load resistor and the output impedance is unaffected by the source resistance.

One must always be aware, however, that there are special situations where the above may not be totally true. Take, for instance, the feedback configuration that results in a direct connection between input and output networks. Although the feedback resistor is usually many times that of the source resistance, permitting the approximation that the source resistance is essentially 0 Ω, it does present a situation where the source resistance could possibly affect the output resistance or the load resistance could affect the input impedance. In general, however, due to the high isolation provided between the gate and the drain or source terminals, the general equations for the loaded gain are less complex than those encountered for BJT transistors. Recall that the base current provided a direct link between input and output circuits of any BJT transistor configuration.

To demonstrate each approach, let us examine the self-bias configuration of Fig. 8.45 with a bypassed source resistance. Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.46.

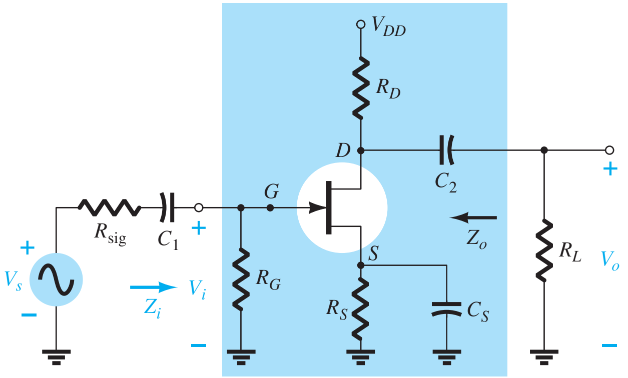


FIG. 8.45
JFET amplifier with R_{sig} and R_L.

Note that the load resistance appears in parallel with the drain resistance and the source resistance R_{sig} appears in series with the gate resistance R. For the overall voltage gain the result is a modified form of Eq. (8.21):

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L)} \qquad \textbf{(8.61)}$$

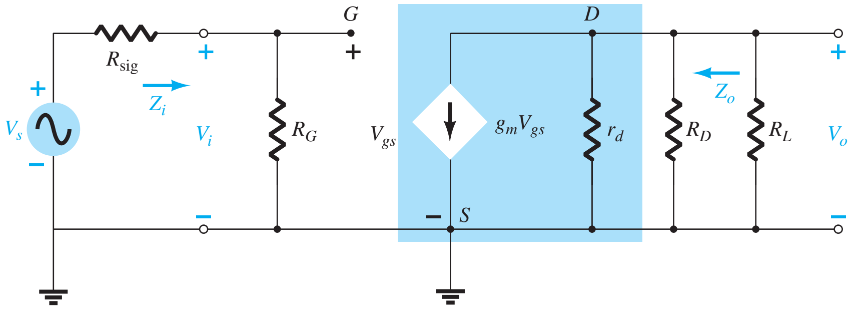


FIG. 8.46
Network of Fig. 8.45 following the substitution of the ac equivalent circuit for the JFET.

The output impedance is the same as obtained for the unloaded situation without a source resistance:

$$\boxed{Z_o = r_d \| R_D} \qquad \textbf{(8.62)}$$

The input impedance remains as

$$\boxed{Z_i = R_G} \qquad \textbf{(8.63)}$$

For the overall gain A_{v_S},

$$V_i = \frac{R_G V_S}{R_G + R_{\text{sig}}}$$

and

$$\boxed{A_{v_S} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = \left[\frac{R_G}{R_G + R_{\text{sig}}}\right][-g_m(r_d \| R_D \| R_L)]} \tag{8.64}$$

which for most applications where $R_G \gg R_{\text{sig}}$ and $R_D \| R_L \ll r_d$ results in

$$\boxed{A_{v_S} \cong -g_m(R_D \| R_L)} \tag{8.65}$$

If we now turn to the two-port approach for the same network, the equation for the overall gain becomes

$$A_{v_L} = \frac{R_L}{R_L + R_o}A_{v\text{NL}} = \frac{R_L}{R_L + R_o}[-g_m(r_d \| R_D)]$$

but
$$R_o = R_D \| r_d,$$

so that
$$A_{v_L} = \frac{R_L}{R_L + R_D \| r_d}[-g_m(r_d \| R_D] = -g_m\frac{(r_d \| R_D)(R_L)}{(r_d + R_D) + R_L}$$

and
$$A_{v_L} = -g_m(r_d \| R_D \| R_L)$$

matching the previous result.

The above derivation was included to demonstrate that the same result will be obtained using either approach. If numerical values for R_i, R_o, and $A_{v_{\text{NL}}}$ were available, it would simply be a matter of substituting the values into Eq. (8.57).

Continuing in the same manner for the most common configurations results in the equations of Table 8.2.

8.15 CASCADE CONFIGURATION

The cascade configuration introduced in Chapter 5 for BJTs can also be used with JFETs or MOSFETs, as shown for JFETs in Fig. 8.47. Recall that the output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

The total gain is the product of the gain of each stage including the loading effects of the following stage.

Too often, the no-load gain is employed and the overall gain is an unrealistic result. For each stage the loading effect of the following stage must be included in the gain calculations. Using the results of the previous sections of this chapter results in the following equation for the overall gain of the configuration of Fig. 8.47:

$$\boxed{A_v = A_{v_1}A_{v_2} = (-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2}) = g_{m_1}g_{m_2}R_{D_1}R_{D_2}} \tag{8.66}$$

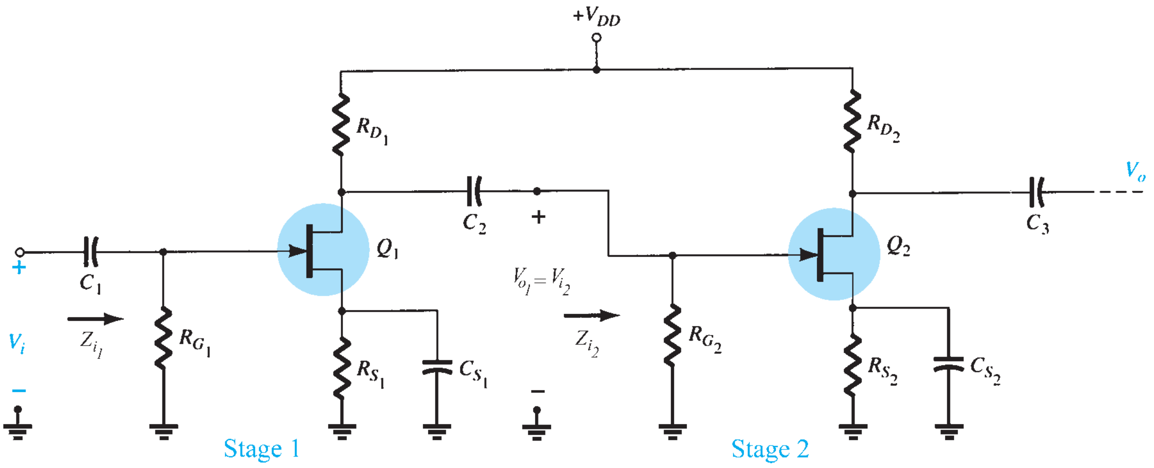
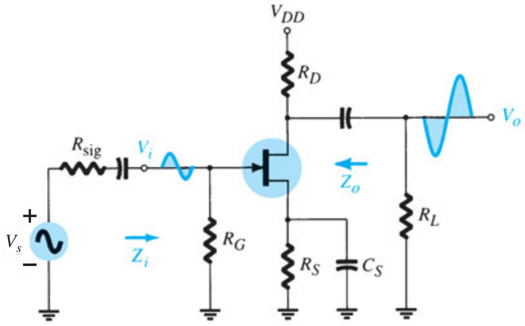
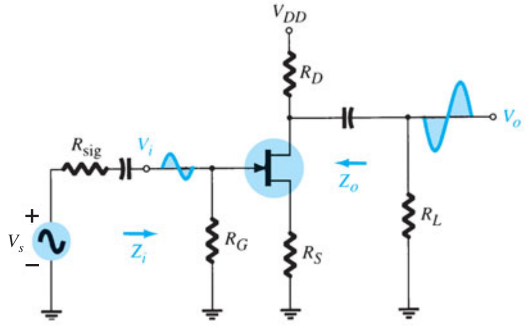
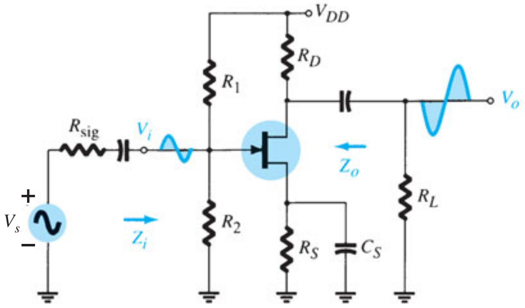
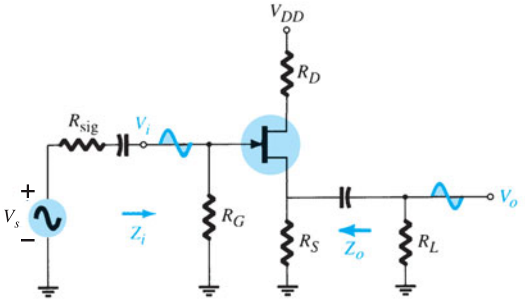
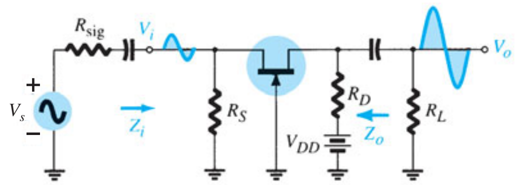


FIG. 8.47
Cascaded FET amplifier.

TABLE 8.2

Configuration	$A_{v_L} = V_o \| V_i$	Z_i	Z_o
 V_{DD} R_D V_o R_{sig} V_i Z_o R_L + V_s − Z_i R_G R_S C_S	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	R_G R_G	R_D $R_D \| r_d$
 V_{DD} R_D V_o R_{sig} V_i Z_o R_L + V_s − Z_i R_G R_S	$\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S}$ Including r_d: $\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1 + g_m R_S}$ $\cong \dfrac{R_D}{1 + g_m R_S}$
 V_{DD} R_D R_1 V_o R_{sig} V_i Z_o R_L + V_s − Z_i R_2 R_S C_S	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	$R_1 \| R_2$ $R_1 \| R_2$	R_D $R_D \| r_d$;
 V_{DD} R_D R_{sig} V_i + V_s − Z_i R_G V_o R_S Z_o R_L	$\dfrac{g_m(R_S \| R_L)}{1 + g_m(R_S \| R_L)}$ Including r_d: $= \dfrac{g_m r_d(R_S \| R_L)}{r_d + R_D + g_m r_d(R_S \| R_L)}$	R_G R_G	$R_S \| 1/g_m$ $\dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D}}$
 R_{sig} V_i V_o + V_s − Z_i R_S R_D V_{DD} Z_o R_L	$g_m(R_D \| R_L)$ Including r_d: $\cong g_m(R_D \| R_L)$	$\dfrac{R_S}{1 + g_m R_S}$ $Z_i = \dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D \| R_L}}$	R_D $R_D \| r_d$

The input impedance of the cascade amplifier is that of stage 1,

$$\boxed{Z_i = R_{G_1}} \tag{8.67}$$

and the output impedance is that of stage 2,

$$\boxed{Z_o = R_{D_2}} \tag{8.68}$$

The main function of cascading stages is the larger overall gain achieved. Since dc bias and ac calculations for a cascade amplifier follow those derived for the individual stages, an example will demonstrate the various calculations to determine dc bias and ac operation.

EXAMPLE 8.16 Calculate the dc bias, voltage gain, input impedance, output impedance, and resulting output voltage for the cascade amplifier shown in Fig. 8.48.

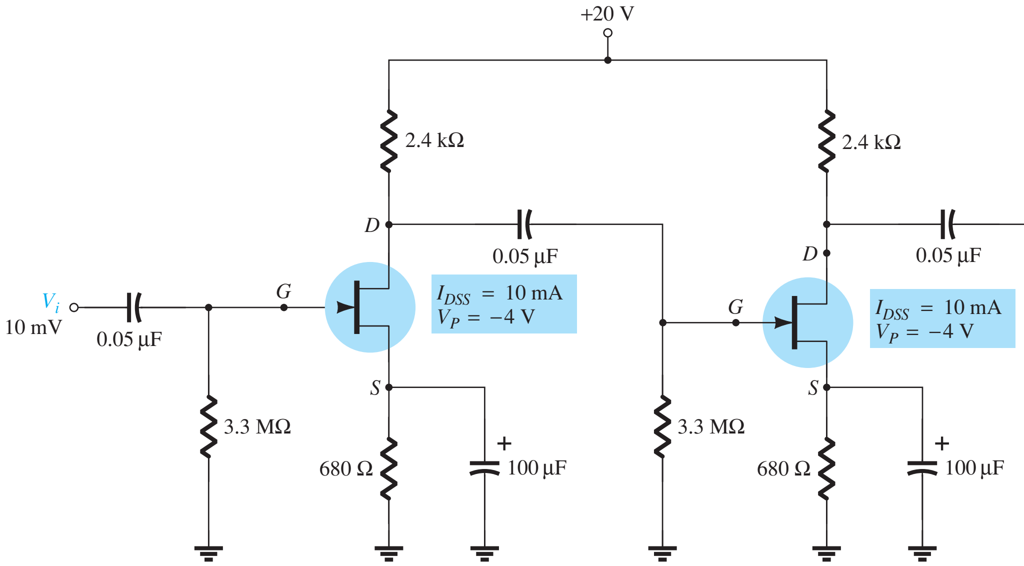


FIG. 8.48

Cascade amplifier circuit for Example 8.16.

Solution: Both amplifier stages have the same dc bias. Using dc bias techniques from Chapter 7 results in

$$V_{GS_Q} = -1.9\text{ V}, \qquad I_{D_Q} = 2.8\text{ mA} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{|-4\text{ V}|} = \mathbf{5\ mS}$$

and at the dc bias point,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = (5\text{ mS})\left(1 - \frac{-1.9\text{ V}}{-4\text{ V}}\right) = \mathbf{2.6\ mS}$$

Since the second stage is unloaded

$$A_{v_2} = -g_m R_D = -(2.6\text{ mS})(2.4\text{ k}\Omega) = \mathbf{-6.24}$$

For the first stage $2.4\text{ k}\Omega \| 3.3\text{ M}\Omega \cong 2.4\text{ k}\Omega$ resulting in the same gain.
The cascade amplifier voltage gain is

$$\text{Eq. (8.66):} \quad A_v = A_{v_1}A_{v_2} = (-6.2)(-6.2) = \mathbf{38.4}$$

Take special note of the fact that the total gain is positive.
The output voltage is then

$$V_o = A_v V_i = (38.4)(10\text{ mV}) = \mathbf{384\ mV}$$

The cascade amplifier input impedance is

$$Z_i = R_G = \mathbf{3.3\ M\Omega}$$

The cascade amplifier output impedance (assuming that $r_d = \infty\Omega$) is

$$Z_o = R_D = \mathbf{2.4\ k\Omega}$$

A combination of FET and BJT stages can also be used to provide high voltage gain and high input impedance, as demonstrated by the next example.

EXAMPLE 8.17 For the cascade amplifier of Fig. 8.49, use the dc bias calculated in Examples 5.15 and 8.16 to calculate input impedance, output impedance, voltage gain, and resulting output voltage.

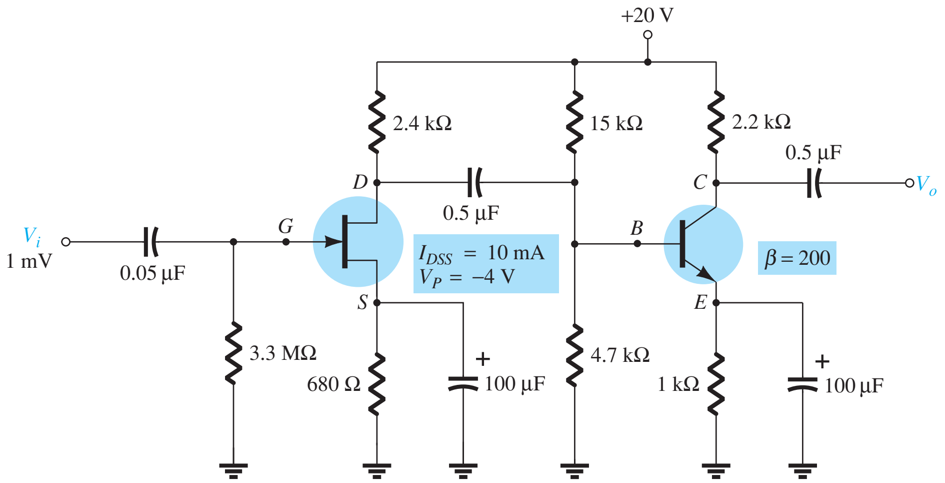


FIG. 8.49

Cascaded JFET-BJT amplifier for Example 8.17.

Solution: Since R_i (stage 2) $= 15\ \text{k}\Omega \| 4.7\ \text{k}\Omega \| 200(6.5\ \Omega) = 953.6\ \Omega$, the gain of stage 1 (when loaded by stage 2) is

$$\begin{aligned} A_{v_1} &= -g_m[R_D \| R_i\ (\text{stage }2)] \\ &= -2.6\ \text{mS}(2.4\ \text{k}\Omega \| 953.6\ \Omega) = -1.77 \end{aligned}$$

From Example 5.18, the voltage gain of stage 2 is $A_{v_2} = -338.46$. The overall voltage gain is then

$$A_v = A_{v_1}A_{v_2} = (-1.77)(-338.46) = \mathbf{599.1}$$

The output voltage is then

$$V_o = A_v V_i = (599.1)(1\ \text{mV}) \approx \mathbf{0.6\ V}$$

The input impedance of the amplifier is that of stage 1,

$$Z_i = \mathbf{3.3\ M\Omega}$$

and the output impedance is that of stage 2,

$$Z_o = R_D = \mathbf{2.2\ k\Omega}$$

8.16 TROUBLESHOOTING

As mentioned before, troubleshooting a circuit is a combination of knowing the theory and having experience using meters and an oscilloscope to check the operation of the circuit. A good troubleshooter has a sense for what to check based on the behavior of the networks. This ability is developed through building, testing, and repairing a wide variety of configurations. For any small-signal amplifier one might consider the following steps:

1. Look at the circuit board to see if any obvious problems can be seen: an area charred by excess heating of a component; a component that feels or seems too hot to touch; what appears to be a poor solder joint; any connection that appears to have come loose.
2. Use a dc meter: make some measurements as marked in a repair manual containing the circuit schematic diagram and a listing of test dc voltages.
3. Apply a test ac signal: measure the ac voltages starting at the input and work along toward the output.
4. If the problem is identified at a particular stage, the ac signal at various points should be checked using an oscilloscope to see the waveform, its polarity, amplitude, and frequency, as well as any unusual waveform "glitches" that may be present. In particular, observe that the signal is present for the full signal cycle.

Possible Symptoms and Actions

In the absence of an output ac voltage:

1. Check whether the supply voltage is properly connected.
2. Check whether the output voltage at V_D is in the midrange between 0 V and V_{DD}.
3. Check whether there is any input ac signal at the gate terminal.
4. Check the ac voltage at each side of the coupling capacitor terminals.

When building and testing an FET amplifier circuit in the laboratory:

1. Check the color code of resistor values to be sure that they are correct. Even better, measure the resistor values because components used repeatedly may get overheated when used incorrectly, causing the nominal value to change.
2. Check that all dc voltages are present at the component terminals. Be sure that all ground connections are made common.
3. Measure the ac input signal to be sure the expected value is provided to the circuit.

8.17 PRACTICAL APPLICATIONS

Three-Channel Audio Mixer

The basic components of a three-channel JFET audio mixer are shown in Fig. 8.50. The three input signals can come from different sources such as a microphone, a musical instrument, background sound generators, and so on. All signals can be applied to the same gate terminal because the input impedance of the JFET is so high that it can be approximated by

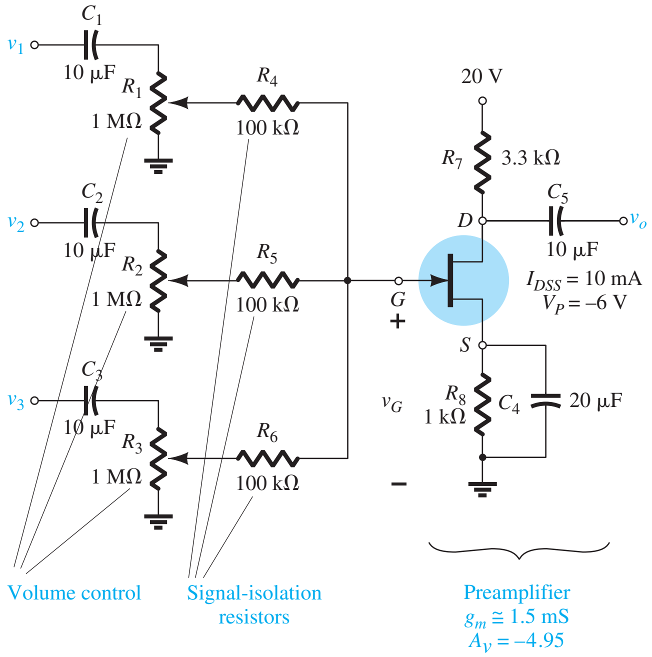


FIG. 8.50

Basic components of a three-channel JFET audio mixer.

an open circuit. **In general, the input impedance is 1000 MΩ (10^9 Ω) or better for JFETs and 100 million MΩ (10^{14} Ω) or better for MOSFETs**. If BJTs were employed instead of JFETs, the lower input impedance would require a transistor amplifier for each channel or at least an emitter-follower as the first stage to provide a higher input impedance.

The 10-μF capacitors are there to prevent any dc biasing levels on the input signal from appearing at the gate of the JFET, and the 1-MΩ potentiometers are the volume controls for each channel. The need for the 100-kΩ resistors for each channel is less obvious. Their purpose is to ensure that one channel does not load down the other channels and severely reduce or distort the signal at the gate. For instance, in Fig. 8.51a, one channel has a high-impedance (10-kΩ) microphone, whereas another channel has a low-impedance (0.5-kΩ) guitar amplifier. Channel 3 is left open, and the 100-kΩ isolation resistors have been removed for the moment. Replacing the capacitors by their short-circuit equivalent for the frequency range of interest and ignoring the effects of the parallel 1-MΩ potentiometers (set at their maximum value) result in the equivalent circuit of Fig. 8.51b at the gate of the JFET amplifier. Using the superposition theorem, we determine the voltage at the gate of the JFET by

$$\begin{aligned} v_G &= \frac{0.5\text{ k}\Omega(v_{\text{mic}})}{10.5\text{ k}\Omega} + \frac{10\text{ k}\Omega(v_{\text{guitar}})}{10.5\text{ k}\Omega} \\ &= 0.047v_{\text{mic}} + 0.95v_{\text{guitar}} \cong v_{\text{guitar}} \end{aligned}$$

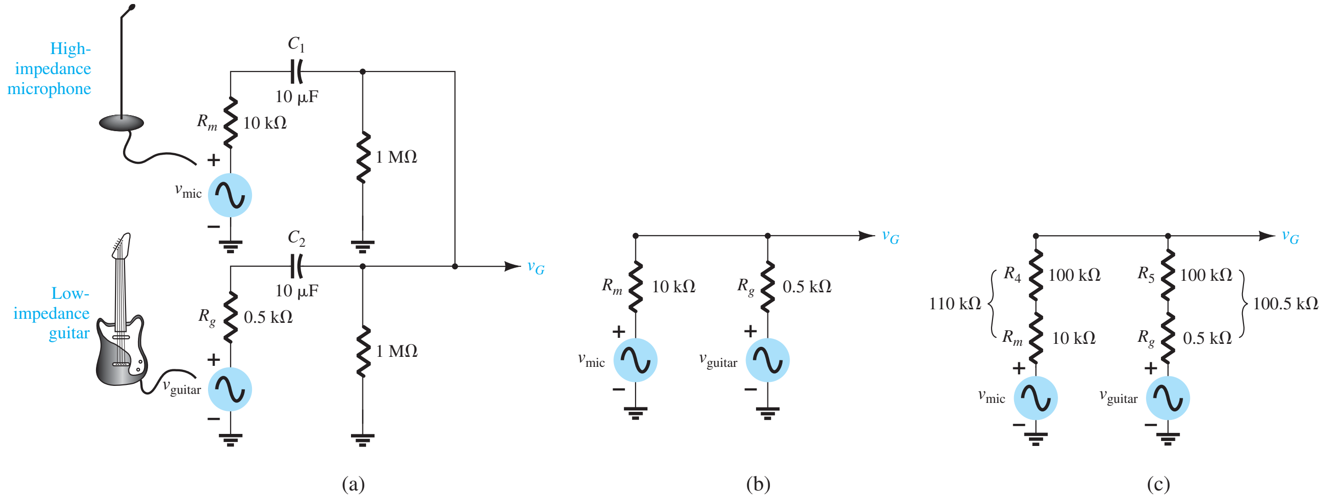


FIG. 8.51

(a) Application of a high- and a low-impedance source to the mixer of Fig. 8.50; (b) reduced equivalent without the 100-kΩ isolation resistors; (c) reduced equivalent with the 100-kΩ resistors.

clearly showing that the guitar has swamped the signal of the microphone. The only response of the amplifier of Fig. 8.51 will be to the guitar. Now, with the 100-kΩ resistors in place, the situation of Fig. 8.51c results. Using the superposition theorem again, we obtain the following equation for the voltage at the gate:

$$\begin{aligned} v_G &= \frac{101\text{ k}\Omega(v_{\text{mic}})}{211\text{ k}\Omega} + \frac{110\text{ k}\Omega(v_{\text{guitar}})}{211\text{ k}\Omega} \\ &\cong 0.48v_{\text{mic}} + 0.52v_{\text{guitar}} \end{aligned}$$

showing an even balance in the signals at the gate of the JFET. **In general, therefore, the 100-kΩ resistors compensate for any difference in signal impedance to ensure that one does not load down the other and develop a mixed level of signals at the amplifier. Technically, they are often called "signal isolation resistors."**

An interesting consequence of a situation such as described in Fig. 8.51b is depicted in Fig. 8.52, where a guitar of low impedance has a signal level of about 150 mV, whereas the microphone, having a larger internal impedance, has a signal strength of only 50 mV. As pointed out above, the major part of the signal at the "feed" point (v_G) is that of the guitar. The resulting direction of current and power flow is unquestionably from the guitar to the microphone. **Furthermore, since the basic construction of a microphone and a speaker is quite similar, the microphone may be forced to act like a speaker and broadcast the guitar signal**. New acoustic bands often face this problem as they learn the rudiments of

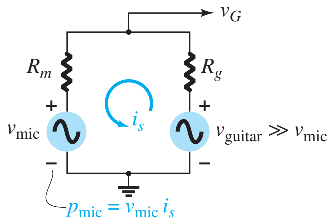

v_G
R_m
R_g
v_{mic}
i_s
$v_{\text{guitar}} \gg v_{\text{mic}}$
$p_{\text{mic}} = v_{\text{mic}}\, i_s$

FIG. 8.52

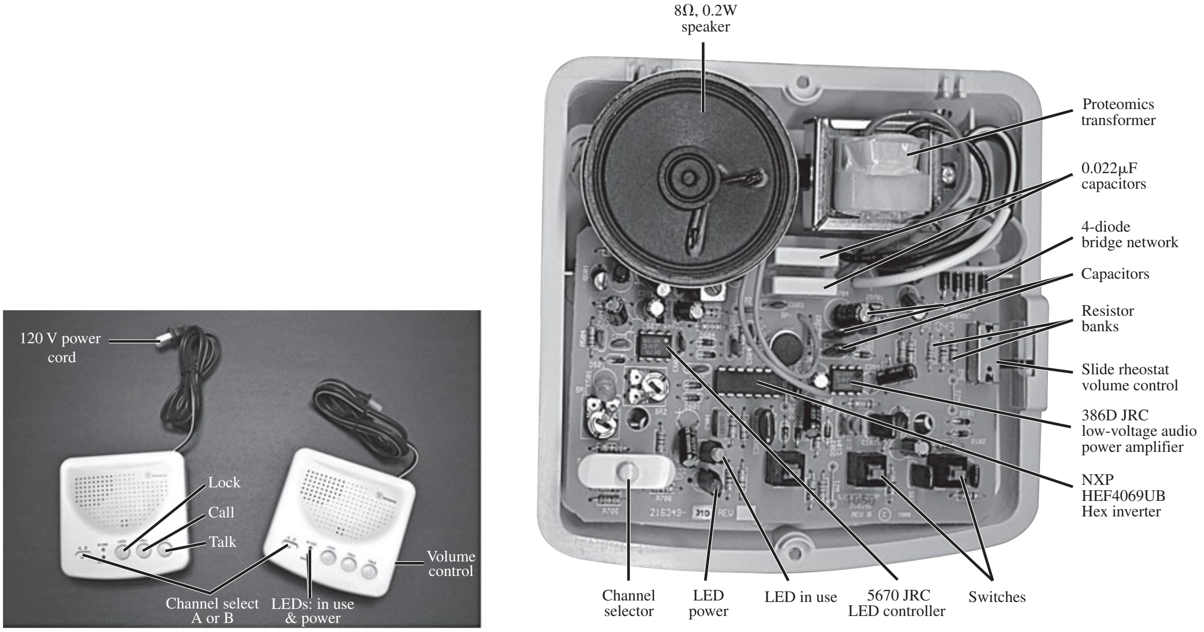
Demonstrating that for parallel signals, the channel with the least internal impedance and most power controls the situation.

good amplifier basics. **In general, for parallel signals, the channel with the least internal impedance controls the situation**.

In Fig. 8.50, the gain of the self-biased JFET is determined by $-g_m R_D$, which for this situation is

$$-g_m R_D = (-1.5\text{ mS})(3.3\text{ k}\Omega) = \mathbf{-4.95}$$

For some it may come as quite a surprise that a microphone can actually behave like a speaker. However, the classical example of the use of one voice cone to act as a microphone and a speaker is in the typical intercom system such as appearing in Fig. 8.53a. The 8 Ω, 0.2 W speaker of Fig. 8.53b can be used as a microphone or a speaker, depending on the position of the activation switch. It is important to note, however, as in the microphone–guitar example above, that most speakers are designed to handle reasonable power levels, but most microphones are designed to simply accept the voice-activated input, and they cannot handle the power levels normally associated with speakers. Just compare the size of each in any audio system. In general, a situation such as described above, where the guitar signal is heard over the microphone, will ultimately damage the microphone. For an intercom system the speaker is designed to handle both types of excitation without difficulty.


120 V power cord
Lock
Call
Talk
Volume control
Channel select A or B
LEDs: in use & power
8Ω, 0.2W speaker
Proteomics transformer
0.022µF capacitors
4-diode bridge network
Capacitors
Resistor banks
Slide rheostat volume control
386D JRC low-voltage audio power amplifier
NXP HEF4069UB Hex inverter
Channel selector
LED power
LED in use
5670 JRC LED controller
Switches

(a) (b)

FIG. 8.53

Two-station, two channel intercom: (a) external appearance; (b) internal construction.
(Photos by Dan Trudden/Pearson).

Silent Switching

Any electronic system that incorporates mechanical switching such as shown in Fig. 8.54 is prone to developing noise on the line that will reduce the signal-to-noise ratio. When the switch of Fig. 8.54 is opened and closed, one often gets an annoying "pfft, pfft" sound as part of the output signal. In addition, the longer wires normally associated with

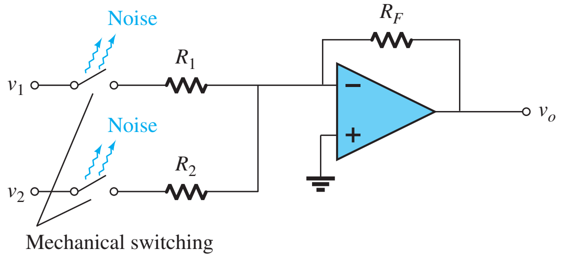

Noise
Noise
R_F
R_1
R_2
v_1
v_2
v_o
−
+
Mechanical switching

FIG. 8.54

Noise development due to mechanical switching.

mechanical switches will require that the switch be as close to the amplifier as possible to reduce the noise pickup on the line.

One effective method to essentially eliminate this source of noise is to use electronic switching such as shown in Fig. 8.55a for a two-channel mixing network. Recall from Chapter 7 that the drain to source of a JFET for low values of V_{DS} can be looked on as a

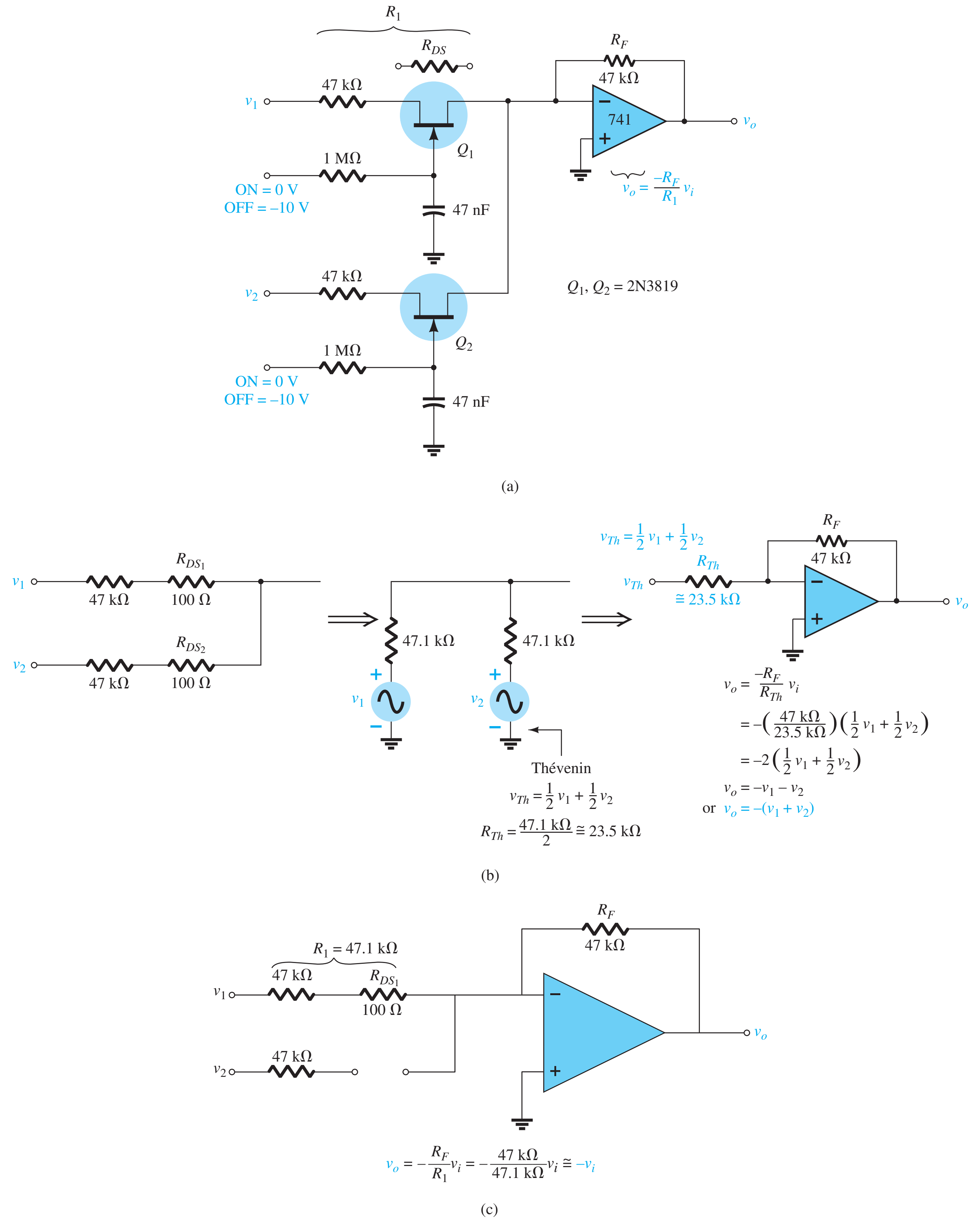

R_1
R_{DS}
R_F
47 kΩ
v_1
47 kΩ
741
v_o
Q_1
1 MΩ
ON = 0 V
OFF = –10 V
47 nF
$v_o = \frac{-R_F}{R_1} v_i$
v_2
47 kΩ
Q_2
1 MΩ
ON = 0 V
OFF = –10 V
47 nF
Q_1, Q_2 = 2N3819
(a)
v_1
R_{DS_1}
47 kΩ
100 Ω
v_2
R_{DS_2}
47 kΩ
100 Ω
47.1 kΩ
47.1 kΩ
v_1
v_2
Thévenin
$v_{Th} = \frac{1}{2}v_1 + \frac{1}{2}v_2$
$R_{Th} = \frac{47.1\text{ k}\Omega}{2} \cong 23.5\text{ k}\Omega$
$v_{Th} = \frac{1}{2}v_1 + \frac{1}{2}v_2$
R_F
47 kΩ
v_{Th}
R_{Th}
≅ 23.5 kΩ
v_o
$v_o = \frac{-R_F}{R_{Th}} v_i$
$= -\left(\frac{47\text{ k}\Omega}{23.5\text{ k}\Omega}\right)\left(\frac{1}{2}v_1 + \frac{1}{2}v_2\right)$
$= -2\left(\frac{1}{2}v_1 + \frac{1}{2}v_2\right)$
$v_o = -v_1 - v_2$
or $v_o = -(v_1 + v_2)$
(b)
R_1 = 47.1 kΩ
v_1
47 kΩ
R_{DS_1}
100 Ω
R_F
47 kΩ
v_o
v_2
47 kΩ
$v_o = -\frac{R_F}{R_1}v_i = -\frac{47\text{ k}\Omega}{47.1\text{ k}\Omega}v_i \cong -v_i$
(c)

FIG. 8.55

Silent switching audio network: (a) JFET configuration; (b) with both signals present; (c) with one signal on.

resistance whose value is determined by the applied gate-to-source voltage as described in detail in Section 7.13. In addition, recall that the resistance is the least at $V_{GS} = 0$ V and the highest near pinch-off. In Fig. 8.55a, the signals to be mixed are applied to the drain side of each JFET, and the dc control is connected directly to the gate terminal of each JFET. With 0 V at each control terminal, both JFETs are heavily "on," and the resistance from D_1 to S_1 and from D_2 to S_2 is relatively small, say, 100 Ω for this discussion. Although 100 Ω is not the 0 Ω assumed with an ideal switch, it is so small compared to the series 47-kΩ resistor that it can often be ignored. Both switches are therefore in the "on" position, and both input signals can make their way to the input of the inverting amplifier (to be introduced in Chapter 10) as shown in Fig. 8.55b. In particular, note that the chosen resistor values result in an output signal that is simply an inversion of the sum of the two signals. The amplifier stage to follow will then raise the summation to audio levels.

Both electronic switches can be put in the "off" state by applying a voltage that is more negative than the pinch-off level as indicated by the 10 V in Fig. 8.55a. The level of "off" resistance can approach 10,000 MΩ, which certainly can be approximated by an open circuit for most applications. Since both channels are isolated, one can be "on" while the other is "off." The speed of operation of a JFET switch is controlled by the substrate (those due to the device construction) and stray capacitance levels and the low "on" resistance of the JFET. **Maximum speeds for JFETs are about 100 MHz, with 10 MHz being more typical**. However, this speed is critically reduced by the input resistance and capacitance of the design. In Fig. 8.55a, the 1-MΩ resistor and the 47-nF capacitors have a time constant of $\tau = RC = 47$ ms $= 0.047$ s for the dc charging network that is controlling the voltage at the gate. If we assume two time constants to charge to the pinch-off level, the total time is 0.094 s, or a switching speed of $1/0.094 \text{ s} \cong 10.6$ per second. Compared to the typical switching speed of the JFET at 10 million times in 1 s, this number is extremely small. Keep in mind, however, that the application is the important consideration, and for a typical mixer, switching is not going to occur at speeds greater than 10.6 per second unless we have some radical input signals. One might ask why it is necessary to have the *RC* time constant at the gate at all. Why not let the applied dc level at the gate simply control the state of the JFET? In general, the *RC* time constant ensures that the control signal is not a spurious one generated by noise or "ringing" due to the sharply rising and falling applied pulses at the gate. By using a charging network, we ensure that the dc level must be present for a period of time before the pinch-off level is reached. Any spike on the line will not be present long enough to charge the capacitor and switch the state of the JFET.

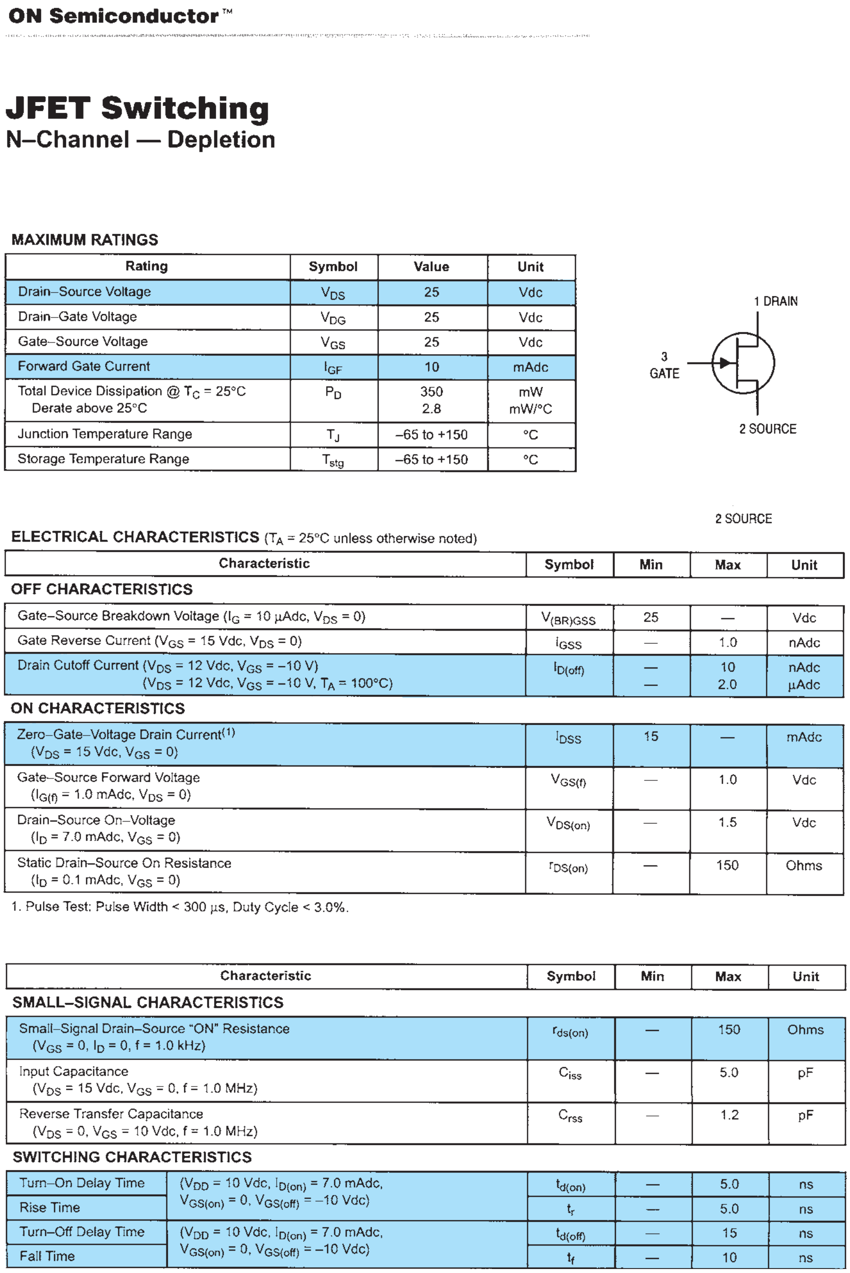
It is important to realize **that the JFET switch is a bilateral switch**. That is, signals in the "on" state can pass through the drain–source region in either direction. This, of course, is the way ordinary mechanical switches work, which makes it that much easier to replace mechanical switch designs with electronic switches. Remember that the diode is not a bilateral switch because it can conduct current at low voltages in only one direction.

It should be noted that **because the state of the JFETs can be controlled by a dc level, the design of Fig. 8.55a lends itself to remote and computer control** for the same reasons described in Chapter 7 when dc control was discussed.

The data sheet for a low-cost JFET analog switch is provided in Fig. 8.56. Note under the heading Drain Cutoff Current that the pinch-off voltage $V_{GS} = V_P$ is typically about -10 V at a drain-to-source voltage of 12 V. In addition, a current level of 10 nA is used to define the pinch-off level. The level of I_{DSS} is 15 mA, whereas the drain-to-source resistance is quite low at 150 Ω with $V_{GS} = 0$ V. The turn-on time is quite small at 10 ns ($t_d + t_r$), whereas the turn-off time is 25 ns.

Phase-Shift Networks

Using the voltage-controlled drain-to-source resistance characteristic of a JFET, we can control the phase angle of a signal using the configurations of Fig. 8.57. The network of Fig. 8.57a is a phase-advance network, which adds an angle to the applied signal, whereas the network of Fig. 8.57b is a phase-retard configuration, which creates a negative phase shift.


1 DRAIN
3 GATE
2 SOURCE
2 SOURCE

ON Semiconductor™

JFET Switching

N–Channel — Depletion

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage ($I_G = 10\ \mu Adc$, $V_{DS} = 0$)	$V_{(BR)GSS}$	25	—	Vdc
Gate Reverse Current ($V_{GS} = 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	1.0	nAdc
Drain Cutoff Current ($V_{DS} = 12$ Vdc, $V_{GS} = -10$ V) ($V_{DS} = 12$ Vdc, $V_{GS} = -10$ V, $T_A = 100°C$)	$I_{D(off)}$	— —	10 2.0	nAdc µAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current[1] ($V_{DS} = 15$ Vdc, $V_{GS} = 0$)	I_{DSS}	15	—	mAdc
Gate–Source Forward Voltage ($I_{G(f)} = 1.0$ mAdc, $V_{DS} = 0$)	$V_{GS(f)}$	—	1.0	Vdc
Drain–Source On–Voltage ($I_D = 7.0$ mAdc, $V_{GS} = 0$)	$V_{DS(on)}$	—	1.5	Vdc
Static Drain–Source On Resistance ($I_D = 0.1$ mAdc, $V_{GS} = 0$)	$r_{DS(on)}$	—	150	Ohms

1. Pulse Test: Pulse Width < 300 µs, Duty Cycle < 3.0%.

Characteristic		Symbol	Min	Max	Unit
SMALL–SIGNAL CHARACTERISTICS					
Small–Signal Drain–Source "ON" Resistance ($V_{GS} = 0$, $I_D = 0$, f = 1.0 kHz)		$r_{ds(on)}$	—	150	Ohms
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz)		C_{iss}	—	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 10$ Vdc, f = 1.0 MHz)		C_{rss}	—	1.2	pF
SWITCHING CHARACTERISTICS					
Turn–On Delay Time	($V_{DD} = 10$ Vdc, $I_{D(on)} = 7.0$ mAdc, $V_{GS(on)} = 0$, $V_{GS(off)} = -10$ Vdc)	$t_{d(on)}$	—	5.0	ns
Rise Time		t_r	—	5.0	ns
Turn–Off Delay Time	($V_{DD} = 10$ Vdc, $I_{D(on)} = 7.0$ mAdc, $V_{GS(on)} = 0$, $V_{GS(off)} = -10$ Vdc)	$t_{d(off)}$	—	15	ns
Fall Time		t_f	—	10	ns

FIG. 8.56

Specification sheet for a low-cost analog JFET current switch.

(Copyright of Semiconductor Components Industries, LLC. Used by permission.)

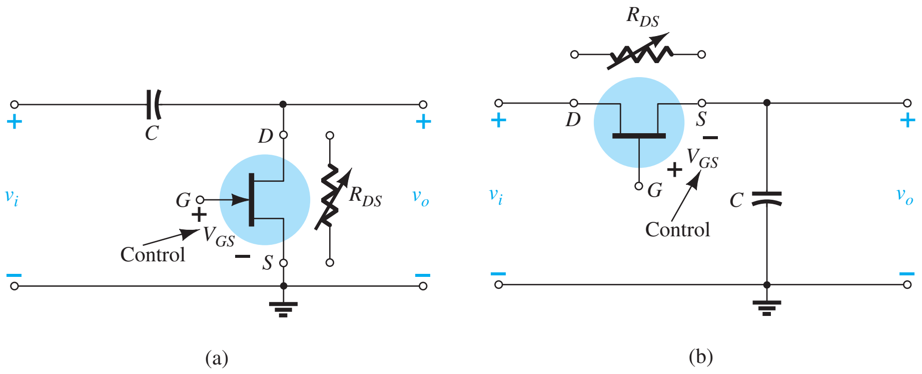


FIG. 8.57

Phase-shift networks: (a) advance; (b) retard.

For example, let us consider the effect of R_{DS} on an input signal having a frequency such as 10 kHz if we apply it to the network of Fig. 8.57a. For discussion, let us assume that the drain-to-source resistance is 2 kΩ due to an applied gate-to-source voltage of −3 V. Drawing the equivalent network results in the general configuration of Fig. 8.58. Solving for the output voltage results in

$$\mathbf{V}_o = \frac{R_{DS}\angle 0^\circ\, V_i\angle 0^\circ}{R_{DS} - jX_C} = \frac{R_{DS}V_i\angle 0^\circ}{\sqrt{R_{DS}^2 + X_C^2}\angle -\tan^{-1}\dfrac{X_C}{R_{DS}}}$$

$$= \frac{R_{DS}V_i}{\sqrt{R_{DS}^2 + X_C^2}}\angle \tan^{-1}\frac{X_C}{R_{DS}} = \left(\frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}}\right)V_i \angle \tan^{-1}\frac{X_C}{R_{DS}}$$

so that

$$\mathbf{V}_o = k_1 V_i \angle \theta_1$$

where

$$\boxed{k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_1 = \tan^{-1}\frac{X_C}{R_{DS}}} \tag{8.69}$$

Substituting the numerical values from above results in

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(10\text{ kHz})(0.01\ \mu\text{F})} = 1.592\text{ k}\Omega$$

and
$$k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} = \frac{2\text{ k}\Omega}{\sqrt{(2\text{ k}\Omega)^2 + (1.592\text{ k}\Omega)^2}} = 0.782$$

with
$$\theta_1 = \tan^{-1}\frac{X_C}{R_{DS}} = \tan^{-1}\frac{1.592\text{ k}\Omega}{2\text{ k}\Omega} = \tan^{-1} 0.796 = 38.52^\circ$$

so that
$$\mathbf{V}_o = 0.782V_i \angle 38.52^\circ$$

and an output signal that is 78.2% of its applied signal but with a phase shift of 38.52°.

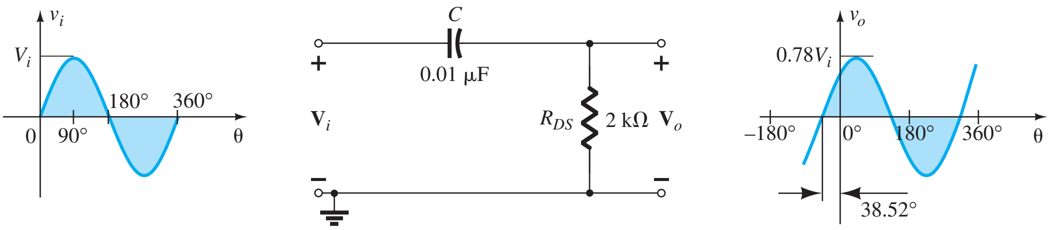


FIG. 8.58
RC phase-advance network.

In general, therefore, the network of Fig. 8.57a can introduce a positive phase shift extending from a few degrees (with X_C relatively small compared to R_{DS}) to almost 90° (with X_C relatively large compared to R_{DS}). Keep in mind, however, that for fixed values of R_{DS}, as the frequency increases, X_C will decrease and the phase shift will approach 0°. For decreasing frequencies and a fixed R_{DS}, the phase shift will approach 90°. It is also important to realize that for a fixed R_{DS}, an increasing level of X_C results in diminishing magnitude for V_o. For such a network, a balance between gain and desired phase shift will have to be made.

For the network of Fig. 8.57b, the resulting equation is

$$\boxed{\mathbf{V}_o = k_2 V_i \angle \theta_2} \tag{8.70}$$

where

$$k_2 = \frac{X_C}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_2 = -\tan^{-1}\frac{R_{DS}}{X_C}$$

Motion-Detection System

The basic components of a passive infrared (PIR) motion-detection system are shown in Fig. 8.59. The heart of the system is **the pyroelectric detector, which generates a voltage that varies with the amount of incident heat**. It filters out all but the infrared radiation from a particular area and focuses the energy onto a temperature-sensing element. Recall from Chapter 7, Section 7.13, that the infrared band is a nonvisible band just below the visible light spectrum. **Passive detectors do not emit a signal of any kind but simply respond to the energy flow of the environment**.

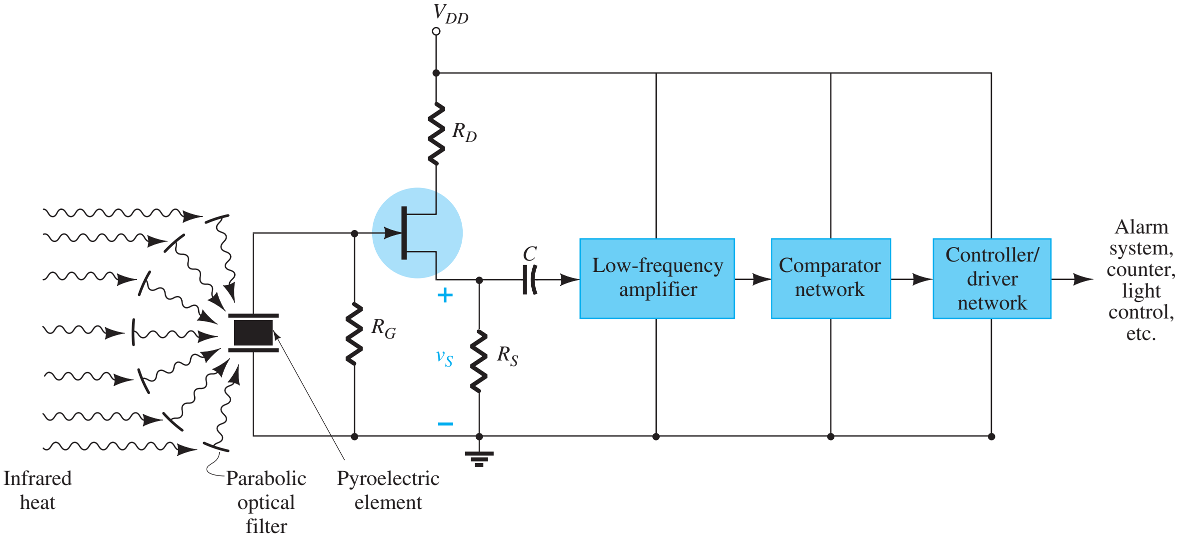


FIG. 8.59

Passive infrared (PIR) motion-detection system.

An external and an internal view of a commercially available unit are provided in Fig. 8.60a and b, respectively. Four interchangeable lens are provided for different coverage areas. For our purposes the "pet" option was selected with the coverage indicated in Fig. 8.60c. The unit is mounted at a height of 7′6″ and operates at a dc voltage of 8.5 V to 15.4 V, drawing a current of 17 mA at 12 V dc. The range of coverage is 35′ perpendicular to the sensor and 20′ to each side. In the lowest sensitivity setting the combined weight of the animals cannot exceed 80 lbs.

To focus the incident ambient heat on the pyroelectric detector, the unit of Fig. 8.60 uses a parabolic deflector. As a person walks past a sensor, he or she will cut the various fields appearing in Fig. 8.60c, and the detector will sense the **rapid changes** in heat level. **The result is a changing dc level akin to a low-frequency ac signal of relatively high internal impedance appearing at the gate of the JFET**. One might then ask why turning a heating system on or turning on a lamp doesn't generate an alarm signal since heat will be generated. The answer is that both will generate a voltage at the detector that grows steadily with increasing heat level from the heating system or the burning bulb. Remember that for the lamp, the detector is heat sensitive and not light sensitive. The resulting voltage is not oscillating between levels, but simply climbing in level and will not set off the alarm—a varying ac voltage will not be generated by the pyroelectric detector!

Note in Fig. 8.59 that a JFET source-follower configuration was employed to ensure a very high input impedance to capture most of the pyroelectric signal. It is then passed through a low-frequency amplifier, followed by a peak-detecting network and a comparator to determine whether the alarm should be set off. The dc voltage comparator is a network that "captures" the peak value of the generated ac voltage and compares it to a known dc voltage level. The output processor determines whether the difference between the two levels is sufficient to tell the driver to energize the alarm.

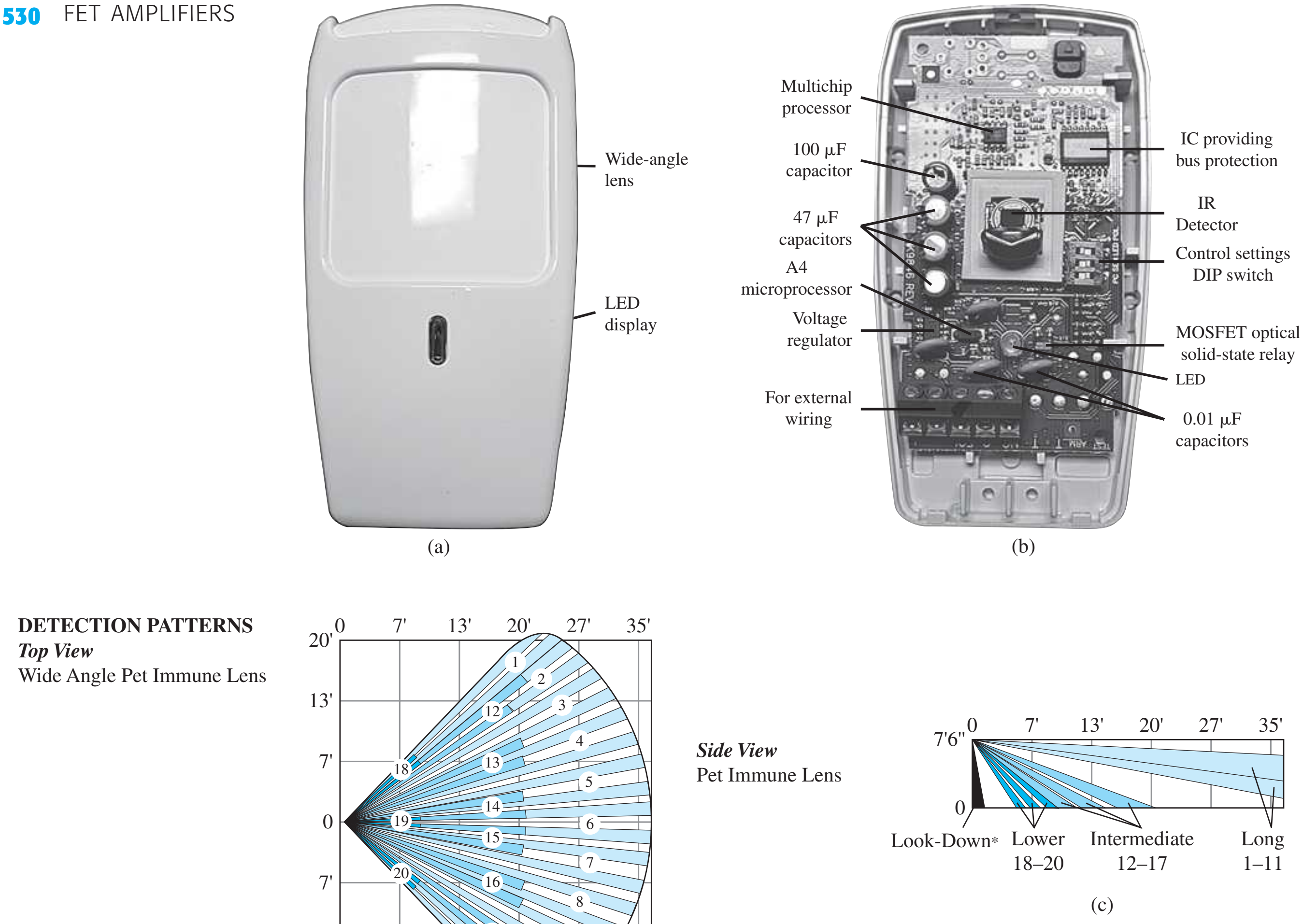

Wide-angle lens
LED display
(a)
Multichip processor
100 µF capacitor
47 µF capacitors
A4 microprocessor
Voltage regulator
For external wiring
IC providing bus protection
IR Detector
Control settings DIP switch
MOSFET optical solid-state relay
LED
0.01 µF capacitors
(b)
DETECTION PATTERNS
Top View
Wide Angle Pet Immune Lens
0
7'
13'
20'
27'
35'
20'
13'
7'
0
7'
13'
20'
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
Side View
Pet Immune Lens
7'6"
0
Look-Down*
Lower 18–20
Intermediate 12–17
Long 1–11
(c)

FIG. 8.60

Commercially available PIR motion-detection unit: (a) external appearance; (b) internal construction; (c) pet option coverage.
[Photos (a) and (b) by Dan Trudden/Pearson.]

8.18 SUMMARY

Important Conclusions and Concepts

1. **The transconductance parameter** g_m is determined by the **ratio of the change in drain current** associated with a particular **change in gate-to-source voltage** in the region of interest. The **steeper the slope** of the I_D-versus-V_{GS} curve, the **greater** is the level of g_m. In addition, the **closer the point or region of interest to the saturation current** I_{DSS}, the **greater** is the transconductance parameter.
2. On specification sheets, g_m is provided as y_{fs}.
3. When V_{GS} is **one-half the pinch-off value**, g_m is **one-half the maximum value**.
4. When I_D is **one-fourth the saturation level of** I_{DSS}, g_m **is one-half the value at saturation**.
5. The **output impedance** of FETs is **similar in magnitude** to that of **conventional BJTs**.
6. On specification sheets the **output impedance** r_d **is provided as** $1/y_{os}$. The **more horizontal** the characteristic curves on the drain characteristics, the **greater is the output impedance**.

7. The **voltage gain** for the fixed-bias and self-bias JFET configurations (with a bypassed source capacitance) **is the same**.
8. The **ac analysis** of JFETs and depletion-type MOSFETs **is the same**.
9. The **ac equivalent network** for an enhancement-type MOSFET **is the same** as that employed for JFETs and depletion-type MOSFETs. The only difference is the equation for g_m.
10. The **magnitude of the gain** of FET networks is typically **between 2 and 20**. The **self-bias configuration** (without a bypass source capacitance) and the **source-follower** are **low-gain configurations**.
11. There is **no phase shift** between input and output for the **source-follower** and **common-gate configurations**. Most others have a 180° phase shift.
12. The **output impedance** for most FET configurations is **determined primarily by R_D**. For the **source-follower** configuration it is determined by R_S and g_m.
13. The **input impedance** for most FET configurations is **quite high**. However, it is **quite low** for the **common-gate configuration**.
14. When **troubleshooting any electronic or mechanical system**, always check the **most obvious causes first**.

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

For JFET and depletion-type MOSFET configurations, see Tables 8.1 and 8.2.

8.19 COMPUTER ANALYSIS

PSpice Windows

JFET Fixed-Bias Configuration The first JFET configuration to be analyzed in the ac domain will be the fixed-bias configuration of Fig. 8.61, using a JFET with $V_P = -4$ V and $I_{DSS} = 10$ mA. The 10-MΩ resistor was added to act as a path to ground for the capacitor but is essentially an open circuit for the ac analysis. The **J2N3819** *n*-channel JFET from the **EVAL** library was used, and the ac voltage is to be determined at four different points for comparison and review.

The constant **Beta** is determined by

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{10\text{ mA}}{4^2\text{V}^2} = 0.625\text{ mA/V}^2$$

and is inserted in the **Edit Model** dialog box obtained by the sequence **EDIT-PROPERTIES**. **Vto** is also changed to -4 V. The remaining elements of the network are set as described for the transistor in Chapter 5.

An analysis of the network results in the printout of Fig. 8.62. The **CIRCUIT DESCRIPTION** includes all the elements of the network along with their assigned nodes. In particular, note that **Vi** is set at **10 mV** at a frequency of **10 kHz** and a phase angle of **0**

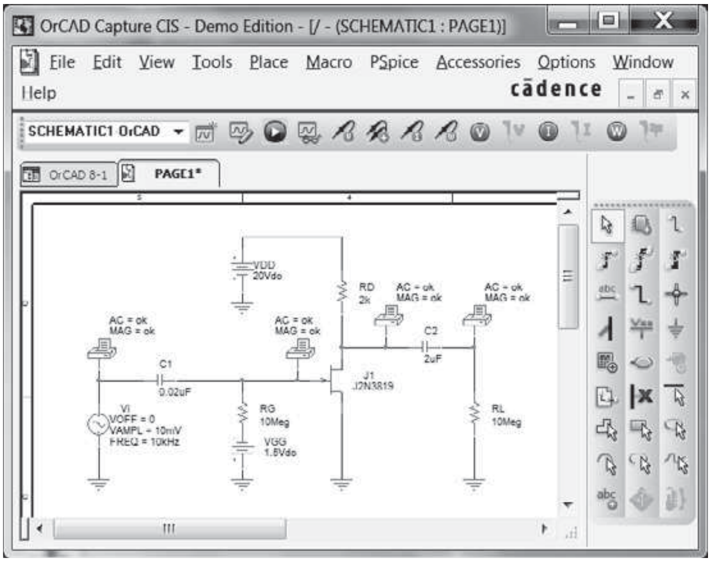
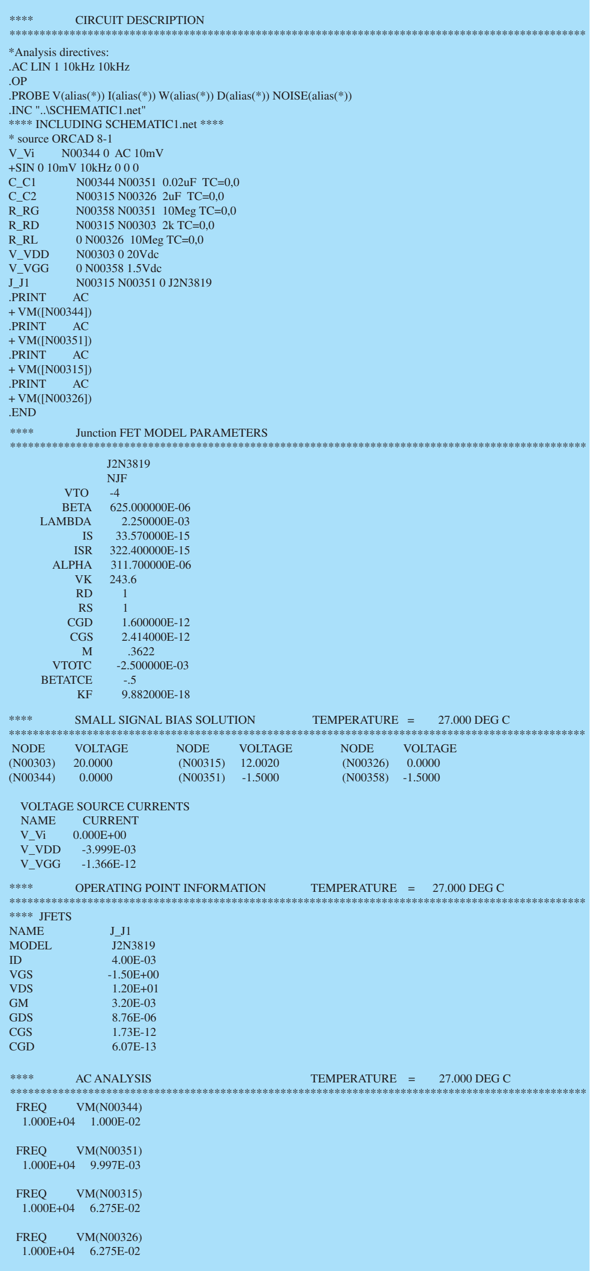

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window
Help
cādence
SCHEMATIC1 OrCAD
OrCAD 8-1
PAGE1*
VDD
20Vdc
RD
2k
AC = ok
MAG = ok
AC = ok
MAG = ok
AC = ok
MAG = ok
AC = ok
MAG = ok
C2
2uF
C1
0.02uF
J1
J2N3819
Vi
VOFF = 0
VAMPL = 10mV
FREQ = 10KHz
RG
10Meg
VGG
1.5Vdc
RL
10Meg

FIG. 8.61

Fixed-bias JFET configuration with an ac source.



```
****          CIRCUIT DESCRIPTION
**********************************************************************************************
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"
**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-1
V_Vi        N00344 0  AC 10mV
+SIN 0 10mV 10kHz 0 0 0
C_C1          N00344 N00351  0.02uF  TC=0,0
C_C2          N00315 N00326  2uF  TC=0,0
R_RG          N00358 N00351  10Meg TC=0,0
R_RD          N00315 N00303  2k TC=0,0
R_RL          0 N00326  10Meg TC=0,0
V_VDD         N00303 0 20Vdc
V_VGG         0 N00358 1.5Vdc
J_J1          N00315 N00351 0 J2N3819
.PRINT       AC
+ VM([N00344])
.PRINT       AC
+ VM([N00351])
.PRINT       AC
+ VM([N00315])
.PRINT       AC
+ VM([N00326])
.END

****          Junction FET MODEL PARAMETERS
**********************************************************************************************
                 J2N3819
                 NJF
          VTO    -4
         BETA    625.000000E-06
       LAMBDA      2.250000E-03
           IS     33.570000E-15
          ISR    322.400000E-15
        ALPHA    311.700000E-06
           VK    243.6
           RD      1
           RS      1
          CGD      1.600000E-12
          CGS      2.414000E-12
            M       .3622
        VTOTC     -2.500000E-03
      BETATCE      -.5
           KF      9.882000E-18

****          SMALL SIGNAL BIAS SOLUTION          TEMPERATURE  =    27.000 DEG C
**********************************************************************************************
 NODE       VOLTAGE         NODE       VOLTAGE         NODE       VOLTAGE
(N00303)    20.0000         (N00315)   12.0020         (N00326)    0.0000
(N00344)     0.0000         (N00351)   -1.5000         (N00358)   -1.5000

  VOLTAGE SOURCE CURRENTS
  NAME       CURRENT
  V_Vi      0.000E+00
  V_VDD      -3.999E-03
  V_VGG      -1.366E-12

****          OPERATING POINT INFORMATION        TEMPERATURE  =   27.000 DEG C
**********************************************************************************************
**** JFETS
NAME              J_J1
MODEL             J2N3819
ID                4.00E-03
VGS              -1.50E+00
VDS               1.20E+01
GM                3.20E-03
GDS               8.76E-06
CGS               1.73E-12
CGD               6.07E-13

****          AC ANALYSIS                         TEMPERATURE  =    27.000 DEG C
**********************************************************************************************
 FREQ        VM(N00344)
  1.000E+04   1.000E-02

 FREQ        VM(N00351)
  1.000E+04   9.997E-03

 FREQ        VM(N00315)
  1.000E+04   6.275E-02

 FREQ        VM(N00326)
  1.000E+04   6.275E-02
```

FIG. 8.62

Output file for the network of Fig. 8.61.

degrees. In the following list of **Junction FET MODEL PARAMETERS** note that **VTO** is -4 V and **BETA** is 625E-6 $\text{A}/\text{V}^2 = 0.625\ \text{mA}/\text{V}^2$, as entered earlier. The **SMALL SIGNAL BIAS SOLUTION** reveals that the voltage at both ends of R_G is -1.5 V, resulting in $V_{GS} = -1.5$ V. The voltage levels of this section can be related to the original network by simply noting the assigned node list in the **CIRCUIT DESCRIPTION**. The voltage from drain to source (ground) is 12 V, leaving a drop of 8 V across R_D. The **AC ANALYSIS** listing reveals that the voltage at the source (N01707) is 10 mV as set, but the voltage at the other end of the capacitor is 3 μV less due to the impedance of the capacitor at 10 kHz—certainly a drop to be ignored. The choice of 0.02 μF for this frequency was obviously a good one. The voltages before and after the capacitor on the output side are exactly the same (to three places), revealing that the larger the capacitor, the closer are the characteristics to those of a short circuit. The output of 6.275E-2 = 62.75 mV reflects a gain of 6.275.

The **OPERATING POINT INFORMATION** reveals that I_D is 4 mA and g_m is 3.2 mS. We calculate the value of g_m from

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$g_m = \frac{2(10\text{ mA})}{4\text{ V}}\left[1 - \frac{(-1.5\text{ V})}{(-4\text{ V})}\right]$$

$$= 3.125\text{ mS}$$

which confirms our analysis.

JFET Voltage-Divider Configuration The next network to be analyzed in the ac domain is the voltage-divider bias configuration of Fig. 8.63. Note that the parameters chosen are different from those employed in earlier examples, with V_i at 24 mV and a frequency of 5 kHz. In addition, the dc levels are displayed, and a plot of the output and input voltages are displayed on the same screen.

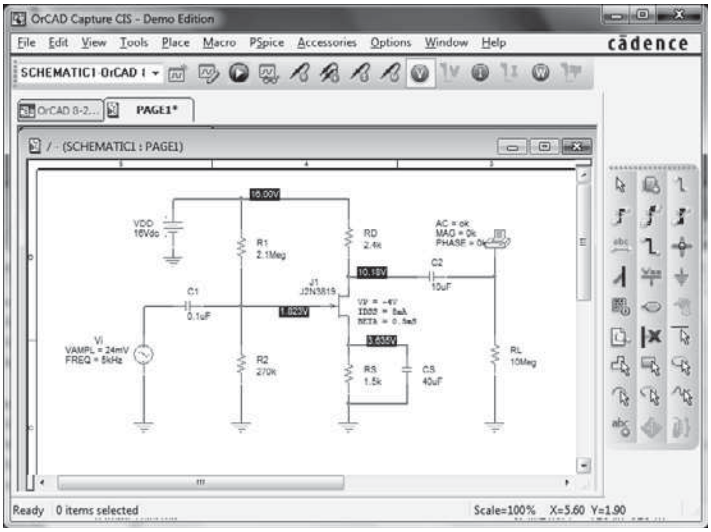

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD I
OrCAD 8-2...
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
16.00V
VDD
16Vdc
R1
2.1Meg
RD
2.4k
AC = ok
MAG = 0k
PHASE = 0k
10.18V
C2
10uF
C1
0.1uF
J1
J2N3819
1.823V
VP = -4V
IDSS = 8mA
BETA = 0.5m
3.635V
Vi
VAMPL = 24mV
FREQ = 5kHz
R2
270k
RS
1.5k
CS
40uF
RL
10Meg
Ready
0 items selected
Scale=100%
X=5.60 Y=1.90

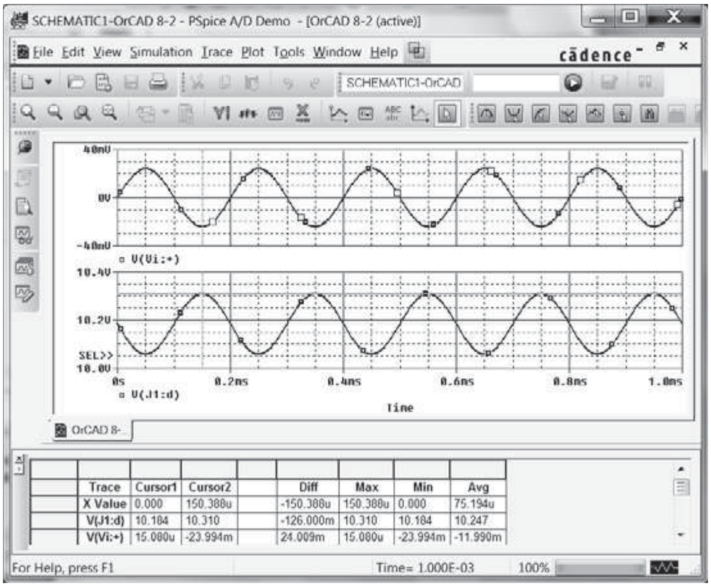
FIG. 8.63

JFET voltage-divider configuration with an ac source.

To run the analysis, select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. After entering **Name** of **OrCAD 8-2**, select **Create**, and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC/Sweep/Noise**, and then under **AC Sweep** choose **Linear**. The **Start Frequency** is **5 kHz**, the **End Frequency** is **5 kHz** and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key. A schematic will appear, which can be exited to result in the display of Fig. 8.63 with all the voltage levels displayed as controlled by the **V** option. The resulting dc levels reveal that V_{GS} is 1.823 V − 3.635 V = −1.812 V, comparing very well with the −1.8 V calculated in Example 7.4. V_D is 10.18 V, compared to the calculated level of 10.24 V, and V_{DS} is 10.18 V −3.635 V = 6.545 V, compared to 6.64 V.

For the ac solution, we can select **View-Output File** and find under **OPERATING POINT INFORMATION** that g_m is 2.22 mS, comparing very well with the hand-calculated value of 2.2 mS, and under **AC ANALYSIS** that the output ac voltage is 125.8 mV, resulting in a gain of 125.8 mV/24 mV = 5.24. The hand-calculated level is $g_mR_D = (2.2\text{ mS})(2.4\text{ k}\Omega) = 5.28$.

The ac waveform for the output voltage can be obtained by returning to the **Simulation Settings** dialog box and under **Analysis type** choosing **Time Domain (Transient)**. Then, since the period of a 5-kHz signal is 200 μs, select a **Run to** time of 1 ms, so that five cycles of the waveform will appear. Leave the **Start saving data after** option at 0 s, and under **Transient options** enter a **Maximum step size** of 2 μs, so that we have at least 100 plot points for each cycle of the waveform. An **OK**, and the **SCHEMATIC** screen will appear. Select **Trace-Add Trace-V(J1:d)** and the waveform at the bottom of Fig 8.64 appears. If you then choose


SCHEMATIC1-OrCAD 8-2 - PSpice A/D Demo - [OrCAD 8-2 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
40mV
0V
-40mV
V(Vi:+)
10.4V
10.2V
SEL>>
10.0V
0s
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
V(J1:d)
Time
OrCAD 8-
For Help, press F1
Time= 1.000E-03
100%

Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	0.000	150.388u		-150.388u	150.388u	0.000	75.194u
V(J1:d)	10.184	10.310		-126.000m	10.310	10.184	10.247
V(Vi:+)	15.080u	-23.994m		24.009m	15.080u	-23.994m	-11.990m

FIG. 8.64

The ac drain and gate voltage for the voltage-divider JFET configuration of Fig. 8.63.

Plot-Add Plot to Window-Trace-Add Trace-V(Vi:+), the waveform of the applied voltage appears at the top of Fig. 8.64. Now shift **SEL >>** to the bottom waveform by simply bringing the cursor down to the left of the other waveform and left clicking the mouse once. Now select **Trace-Cursor-Display**, and a horizontal line will appear at the dc level of the output voltage at 10.184 V (note the level of **V(J1:d)** in the **Probe Cursor** dialog box in the bottom right of the screen). A right click of the mouse, and a second set of intersecting lines will appear. Choose the **Cursor Peak** icon in the toolbar above the display, and the intersection will automatically go to the peak value of the waveform [(**V(Vi:+)** in the dialog box]. Note that **Cursor 2** indicates that the peak value occurs at about 150 μs and the instantaneous peak value is 10.31 V. The **Diff** is simply the difference between **Cursor 1** and **Cursor 2** intersections for time and amplitude.

Cascaded JFET Amplifier The extensive two-stage JFET amplifier of Fig. 8.65 can be created using the same procedures described in the previous examples using PSpice. For both JFETs, **Beta** was set at 0.625 mA/V^2 and **Vto** at -4 V as shown in Fig. 8.66. The applied frequency is 10 kHz to ensure that the capacitors take on a short-circuit approximation. The ac output at the output of each stage is requested.

After simulation, the output file of Fig. 8.67 results, revealing that the gain is 63.23 mV/10 mV = 6.3 after the first stage and 322.6 mV/10 mV = 32.3 after both stages. The gain

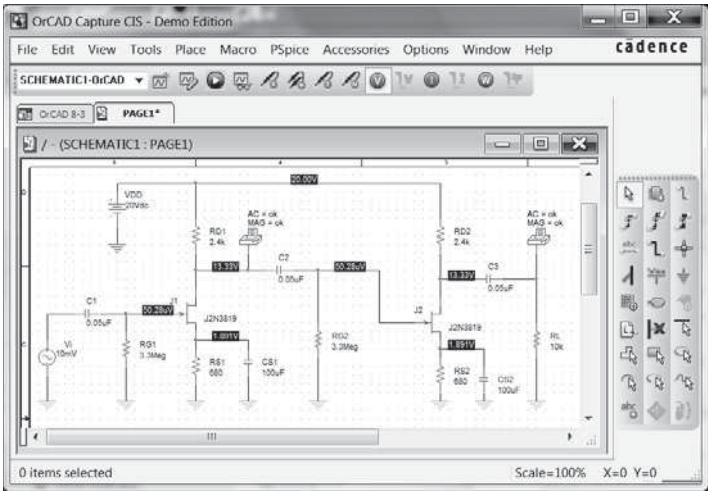
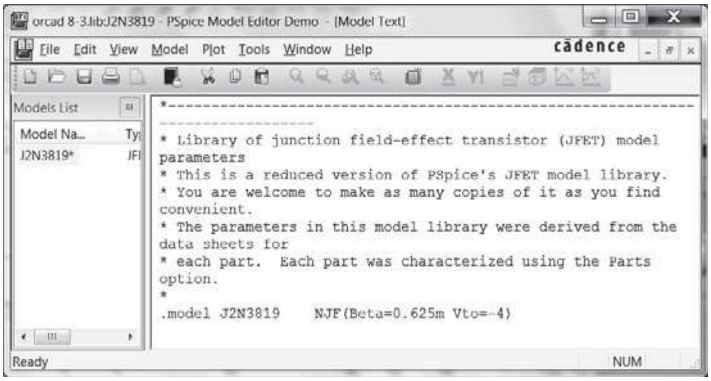

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cadence
SCHEMATIC1-OrCAD
OrCAD 8-3
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
20.00V
VDD
20Vdc
AC = ok
MAG = ok
RD1
2.4k
RD2
2.4k
13.33V
C2
0.05uF
50.28uV
C3
0.05uF
13.33V
C1
0.05uF
50.28uV
J1
J2N3819
J2
J2N3819
1.891V
1.891V
Vi
10mV
RG1
3.3Meg
RG2
3.3Meg
RS1
680
CS1
100uF
RS2
680
CS2
100uF
RL
10k
0 items selected
Scale=100%
X=0 Y=0

FIG. 8.65

Design Center network for analyzing cascaded JFET amplifiers.



```
*------------------------------------------------------------------------
-----------------
* Library of junction field-effect transistor (JFET) model
parameters
* This is a reduced version of PSpice's JFET model library.
* You are welcome to make as many copies of it as you find
convenient.
* The parameters in this model library were derived from the
data sheets for
* each part.  Each part was characterized using the Parts
option.
*
.model J2N3819    NJF(Beta=0.625m Vto=-4)
```

FIG. 8.66

Display of resulting JFET model definition.

```
****          CIRCUIT DESCRIPTION
**************************************************************************************
*Libraries:
* Profile Libraries :
* Local Libraries :
.LIB "../../../orcad 8-3-pspicefiles/orcad 8-3.lib"
* From [PSPICE NETLIST] section of C:\OrCAD\OrCAD_16.3_Demo\tools\PSpice\PSpice.ini file:
.lib "nomd.lib"
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"

**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-3
J_J1       N00328 N00336 N00332 J2N3819
J_J2       N00340 N00416 N00344 J2N3819
V_VDD       N00308 0 20Vdc
R_RD1       N00328 N00308  2.4k TC=0,0
R_RS1       0 N00332  680 TC=0,0
R_RG1       0 N00336  3.3Meg TC=0,0
R_RD2       N00340 N00308  2.4k TC=0,0
R_RS2       0 N00344  680 TC=0,0
R_RG2       0 N00416  3.3Meg TC=0,0
R_RL       0 N00361  10k TC=0,0
C_C1       N01393 N00336  0.05uF  TC=0,0
C_C2       N00328 N00416  0.05uF  TC=0,0
C_C3       N00340 N00361  0.05uF  TC=0,0
C_CS1       0 N00332  100uF  TC=0,0
C_CS2       0 N00344  100uF  TC=0,0

.PRINT       AC
+ VM([N00361])

.PRINT       AC
+ VM([N00328])
V_Vi       N01393 0 DC 0Vdc AC 10mV

**** RESUMING "OrCAD 8-3.cir" ****
.END

****          Junction FET MODEL PARAMETERS
**************************************************************************************

              J2N3819
              NJF
      VTO     -4
     BETA   625.000000E-06

****          SMALL SIGNAL BIAS SOLUTION          TEMPERATURE =    27.000  DEG C
**************************************************************************************
NODE      VOLTAGE     NODE      VOLTAGE     NODE      VOLTAGE    NODE      VOLTAGE
(N00308)  20.0000     (N00328)  13.3270     (N00332)  1.8908     N00336)   50.28E-06
(N00340)  13.3270     (N00344)   1.8908     (N00361)  0.0000     (N00416)  50.28E-06
(N01393)   0.0000

VOLTAGE SOURCE CURRENTS
NAME        CURRENT
V_VDD       -5.561E-03
V_Vi         0.000E+00

****          OPERATING POINT INFORMATION          TEMPERATURE =    27.000  DEG C
**************************************************************************************

**** JFETS
NAME        J_J1         J_J2
MODEL       J2N3819      J2N3819
ID          2.78E-03     2.78E-03
VGS        -1.89E+00    -1.89E+00
VDS         1.14E+01     1.14E+01
GM          2.64E-03     2.64E-03
GDS         0.00E+00     0.00E+00
CGS         0.00E+00     0.00E+00
CGD         0.00E+00     0.00E+00
****          AC ANALYSIS                          TEMPERATURE =    27.000  DEG C
**************************************************************************************
FREQ        VM(N00361)
1.000E+04   3.226E-01

****          AC ANALYSIS                          TEMPERATURE =    27.000  DEG C
**************************************************************************************
FREQ        VM(N00328)
1.000E+04   6.323E-02
```

FIG. 8.67

PSpice output for the network of Fig. 8.65.

for the second stage is 322.6 mV/63.23 mV = 5.1. The gains and output voltage are very close to the results obtained in Example 8.1.

In Fig. 8.67 the **V** option is selected to obtain the dc levels of the network. In particular, note how close the gate voltages are to 0 V, ensuring that the gate-to-source bias voltage is essentially the same as that across the source resistor. In fact, due to the isolation offered by the **C2** capacitor, the bias levels of each configuration are exactly the same.

Multisim

The ac gain for the JFET self-bias network of Fig. 8.68 will now be determined using Multisim. The entire procedure for setting up the network and obtaining the desired readings was described for BJT ac networks in Chapter 5. This particular network will appear again

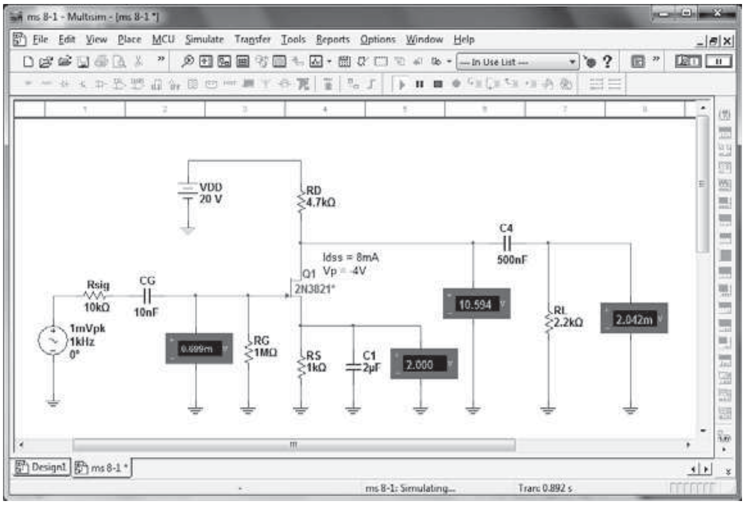

ms 8-1 - Multisim - [ms 8-1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
VDD
20 V
RD
4.7kΩ
C4
500nF
Idss = 8mA
Vp = -4V
Q1
2N3821*
Rsig
10kΩ
CG
10nF
1mVpk
1kHz
0°
0.699m
RG
1MΩ
RS
1kΩ
C1
2µF
2.000
10.594
RL
2.2kΩ
2.042m
Design1
ms 8-1 *
ms 8-1: Simulating...
Tran: 0.892 s

FIG. 8.68

Analysis of a JFET self-bias network using Multisim.

in Chapter 9 as Fig. 9.70 when we turn our attention to the frequency response of a loaded JFET amplifier. A detailed analysis is provided in Chapter 9, including determining the dc levels, the value of g_m, and the loaded gain. The drain current of Example 9.12 is 2 mA, resulting in a drain voltage of 10.6 V and a source voltage of 2 V, which compare very well with the 10.594 V and 2.0 V respectively, of Fig. 8.68. When a load such as R_L is added to the network, it will appear in parallel with R_D of the network, changing the gain equation to $-g_m R_D \| R_L$. For Example 9.12, g_m is 2 mS, resulting in a gain V_o/V_i of $(-2\text{ mS})(2.2\text{ k}\Omega \| 4.7\text{ k}\Omega) = -2.997$. The meters of Fig. 8.68 provide the effective values of the voltages at those points. Since we used a power source, the reading of the meter XMM1 is very close to that of the applied source. The difference is due solely to the ac drop of voltage across $\boldsymbol{R}_{\text{sig}}$ and **CG**. The magnitude of the ac gain (V_o/V_i) of the configuration is $2.042\text{ mV}/0.699\text{ mV} = 2.921$, which is very close to the hand-calculated solution.

PROBLEMS

Note: Asterisks indicate more difficult questions.

8.2 FET Small-Signal Model

1. Calculate g_{m0} for a JFET having device parameters $I_{DSS} = 12$ mA and $V_P = -4$ V.
2. Determine the pinch-off voltage of a JFET with $g_{m0} = 10$ mS and $I_{DSS} = 12$ mA.
3. For a JFET having device parameters $g_{m0} = 5$ mS and $V_P = -4$ V, what is the device current at $V_{GS} = 0$ V?
4. Calculate the value of g_m for a JFET ($I_{DSS} = 12$ mA, $V_P = -3$ V) at a bias point of $V_{GS} = -0.5$ V.
5. For a JFET having $g_m = 6$ mS at $V_{GS_Q} = -1$ V, what is the value of I_{DSS} if $V_P = -2.5$ V?
6. A JFET ($I_{DSS} = 10$ mA ,$V_P = -5$ V) is biased at $I_D = I_{DSS}/4$. What is the value of g_m at that bias point?
7. Determine the value of g_m for a JFET ($I_{DSS} = 8$ mA, $V_P = -5$ V) when biased at $V_{GS_Q} = V_P/4$.
8. A specification sheet provides the following data (at a listed drain-source current):

$$g_{fs} = 4.5\text{ mS}, \qquad g_{os} = 25\ \mu\text{S}$$

   At the listed drain–source current, determine:
   - **a.** g_m.
   - **b.** r_d.
9. For a JFET having specified values of $g_{fs} = 4.5$ mS and $g_{os} = 25\ \mu$S, determine the device output impedance Z_o(FET) and device ideal voltage gain A_v(FET).
10. If a JFET having a specified value of $r_d = 100\text{ k}\Omega$ has an ideal voltage gain of $A_v(\text{FET}) = -200$, what is the value of g_m?

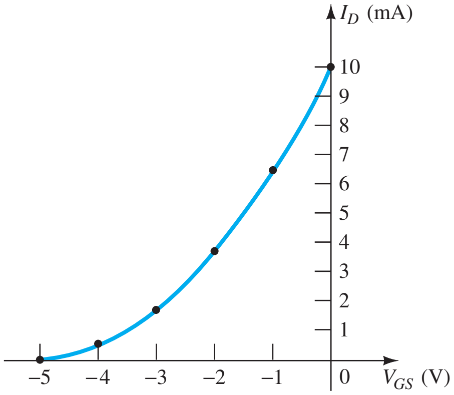


FIG. 8.69

JFET transfer characteristic for Problem 11.

11. Using the transfer characteristic of Fig. 8.69:

a. What is the value of g_{m0}?

b. Determine g_m at $V_{GS} = -0.5$ V graphically.

c. What is the value of g_m at $V_{GS_Q} = -0.5$ V using Eq. (8.6)? Compare with the solution to part (b).

d. Graphically determine g_m at $V_{GS} = -1$ V.

e. What is the value of g_m at $V_{GS_Q} = -1$ V using Eq. (8.6)? Compare with the solution to part (d).

12. Using the drain characteristic of Fig. 8.70:

a. What is the value of r_d for $V_{GS} = 0$ V?

b. What is the value of g_{m0} at $V_{DS} = 10$ V?

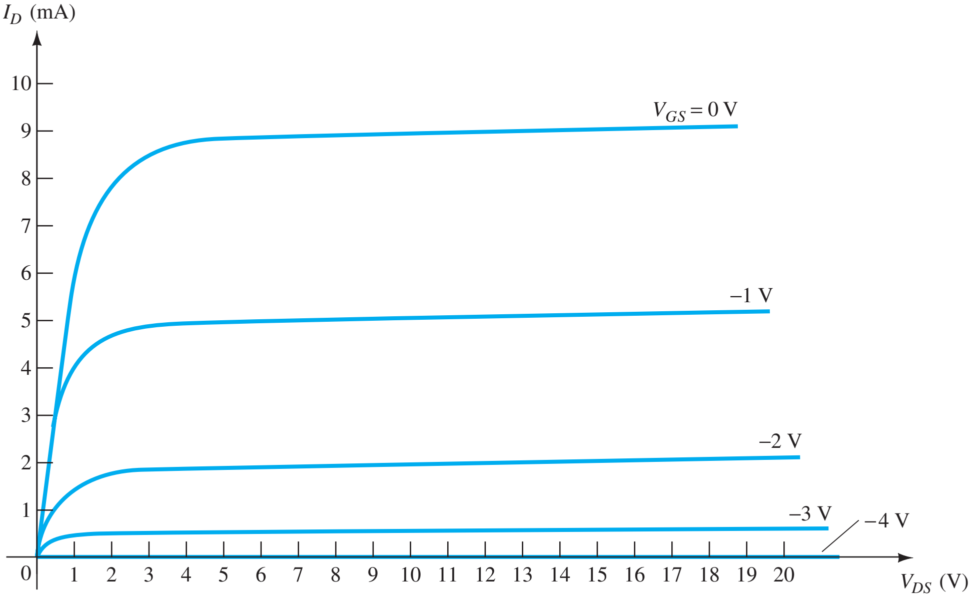


FIG. 8.70

JFET drain characteristic for Problem 12.

13. For a 2N4220 n-channel JFET [g_{fs}(minimum) = 750 μS, g_{os}(maximum) = 10 μS]:

a. What is the value of g_m?

b. What is the value of r_d?

14. a. Plot g_m versus V_{GS} for an n-channel JFET with $I_{DSS} = 12$ mA and $V_P = -6$ V.

b. Plot g_m versus I_D for the same n-channel JFET as part (a).

15. Sketch the ac equivalent model for a JFET if $g_{fs} = 5.6$ mS and $g_{os} = 15$ μS.

16. Sketch the ac equivalent model for a JFET if $I_{DSS} = 10$ mA, $V_P = -4$ V, $V_{GS_Q} = -2$ V, and $g_{os} = 25$ μS.

8.3 Fixed-Bias Configuration

17. Determine Z_i, Z_o, and A_v for the network of Fig. 8.71 if $I_{DSS} = 10\text{ mA}$, $V_P = -6\text{ V}$, and $r_d = 40\text{ k}\Omega$.

18. **a.** Determine Z_i, Z_o, and A_v for the network of Fig. 8.71 if I_{DSS} and V_P are one-half the values of Problems 17. This is $I_{DSS} = 5\text{ mA}$ and $V_P = -3\text{ V}$.
b. Compare the solutions to that of Problem 17.

19. **a.** Determine Z_i, Z_o, and A_v for the network of Fig. 8.72 if $I_{DSS} = 10\text{ mA}$, $V_P = -4\text{ V}$, and $r_d = 20\text{ k}\Omega$.
b. Repeat part (a) with $r_d = 40\text{ k}\Omega$. What was the impact on the results?

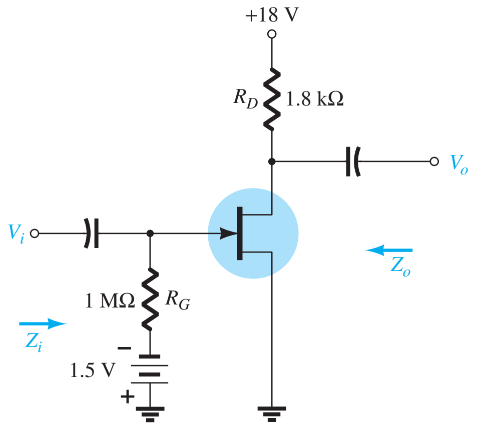

+18 V
R_D
1.8 kΩ
V_o
V_i
Z_o
1 MΩ
R_G
Z_i
1.5 V
–
+

FIG. 8.71
Fixed-bias amplifier for Problems 17 and 18.

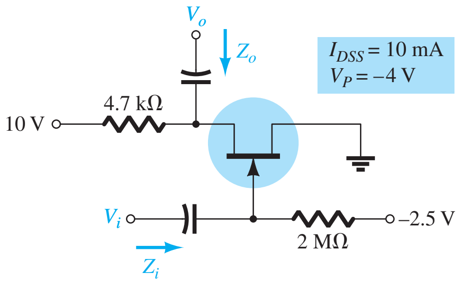

V_o
Z_o
I_{DSS} = 10 mA
V_P = –4 V
4.7 kΩ
10 V
V_i
–2.5 V
2 MΩ
Z_i

FIG. 8.72
Problem 19.

8.4 Self-Bias Configuration

20. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if $g_{fs} = 3000\ \mu\text{S}$ and $g_{os} = 50\ \mu\text{s}$.

21. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if the 20-μF capacitor is removed and the parameters of the network are the same as in Problem 20. Compare results with those of Problem 20.

22. Repeat Problem 20 if g_{os} is 10 μS. Compare the results to those of Problem 20.

23. **a.** Find the value of R_S to obtain a voltage gain of 2 for the network of Fig. 8.74 using $r_d = \infty\ \Omega$.
b. Repeat part (a) with $r_d = 30\text{ k}\Omega$. What was the impact of the change in r_d on the gain and the analysis?

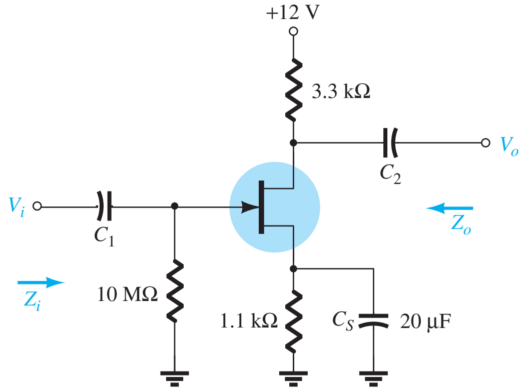

+12 V
3.3 kΩ
V_o
C_2
V_i
C_1
Z_o
Z_i
10 MΩ
1.1 kΩ
C_S
20 μF

FIG. 8.73
Problems 20, 21, 22, and 59.

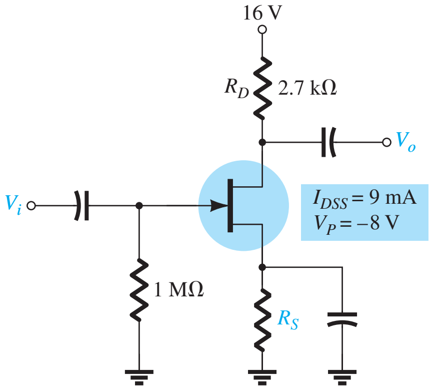

16 V
R_D
2.7 kΩ
V_o
V_i
I_{DSS} = 9 mA
V_P = –8 V
1 MΩ
R_S

FIG. 8.74
Problem 23.

24. Determine Z_i, Z_o, and A_v for the network of Fig. 8.75 if $I_{DSS} = 6\text{ mA}$, $V_P = -6\text{ V}$, and $g_{os} = 40\ \mu\text{S}$.

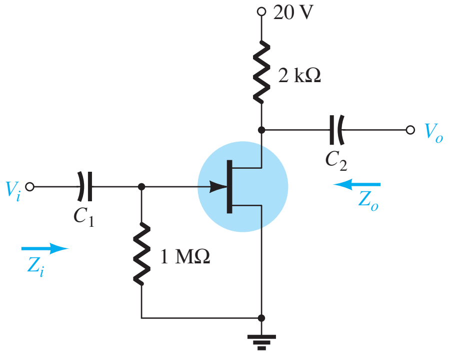

20 V
2 kΩ
C_2
V_o
Z_o
V_i
C_1
Z_i
1 MΩ

FIG. 8.75
Self-bias configuration for Problems 24 and 60.

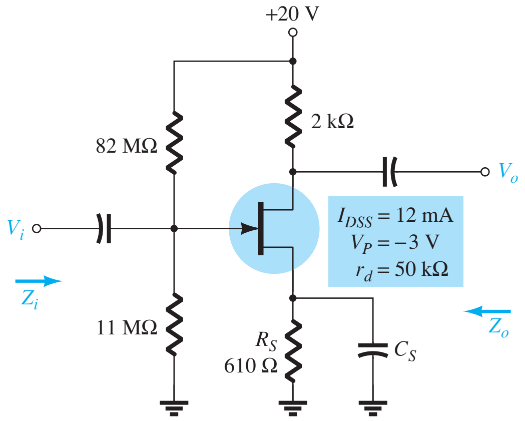

+20 V
2 kΩ
82 MΩ
V_o
V_i
$I_{DSS} = 12$ mA
$V_P = -3$ V
$r_d = 50$ kΩ
Z_i
Z_o
11 MΩ
R_S
610 Ω
C_S

FIG. 8.76
Problems 25 to 28 and 61.

8.5 Voltage-Divider Configuration

25. Determine Z_i, Z_o, and V_o for the network of Fig. 8.76 if $V_i = 20$ mV.

26. Repeat Problem 25 with the capacitor C_S removed and compare results.

27. Repeat Problem 25 if $r_d = 20\text{ k}\Omega$ and compare results.

28. Repeat Problem 26 if $r_d = 20\text{ k}\Omega$ and compare results.

8.6 JFET Common-Gate Configuration

29. Determine Z_i, Z_o, and V_o for the network of Fig. 8.77 if $V_i = 4$ mV.

30. Repeat Problem 29 if $r_d = 20\text{ k}\Omega$ and compare results.

31. Determine Z_i, Z_o, and A_v for the network of Fig. 8.78 if $r_d = 30\text{ k}\Omega$.

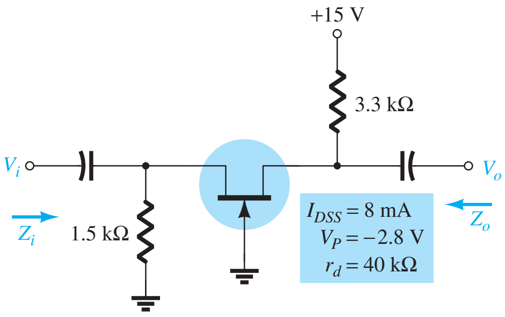

+15 V
3.3 kΩ
V_i
V_o
Z_i
1.5 kΩ
$I_{DSS} = 8$ mA
$V_P = -2.8$ V
$r_d = 40$ kΩ
Z_o

FIG. 8.77
Problems 29, 30, and 62.

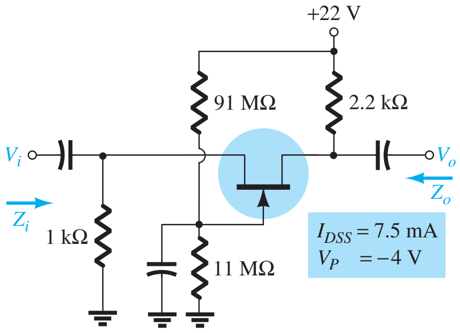

+22 V
91 MΩ
2.2 kΩ
V_i
V_o
Z_o
Z_i
1 kΩ
11 MΩ
$I_{DSS} = 7.5$ mA
$V_P = -4$ V

FIG. 8.78
Problem 31.

8.7 JFET Source-Follower Configuration

32. Determine Z_i, Z_o, and A_v for the network of Fig. 8.79.

33. Repeat Problem 32 if $r_d = 20\text{ k}\Omega$ and compare results.

34. Determine Z_i, Z_o, and A_v for the network of Fig. 8.80.

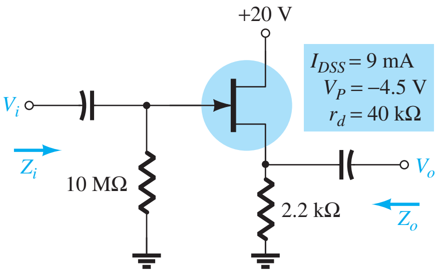

+20 V
$I_{DSS} = 9$ mA
$V_P = -4.5$ V
$r_d = 40$ kΩ
V_i
Z_i
10 MΩ
V_o
2.2 kΩ
Z_o

FIG. 8.79
Problems 32 and 33.

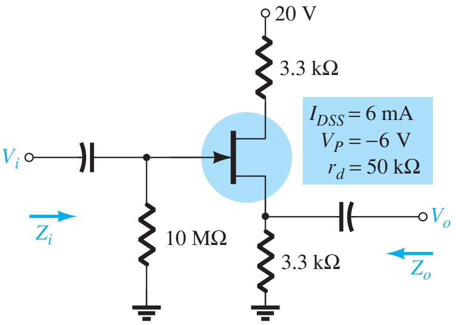

20 V
3.3 kΩ
$I_{DSS} = 6$ mA
$V_P = -6$ V
$r_d = 50$ kΩ
V_i
V_o
Z_i
10 MΩ
3.3 kΩ
Z_o

FIG. 8.80
Problem 34.

8.8 Depletion-Type MOSFETs

35. Determine V_o for the network of Fig. 8.81 if $g_{os} = 20\ \mu S$.

36. Determine Z_i, Z_o, and A_v for the network of Fig. 8.82 if $r_d = 60\ k\Omega$.

37. Repeat Problem 36 if $r_d = 25\ k\Omega$ and compare results.

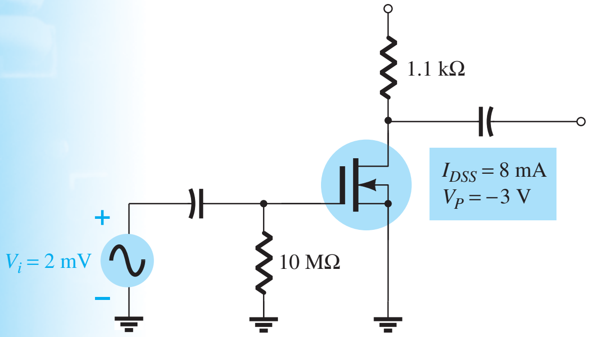

+16 V
1.1 kΩ
V_o
I_{DSS} = 8 mA
V_P = −3 V
+
V_i = 2 mV
−
10 MΩ

FIG. 8.81
Problem 35.

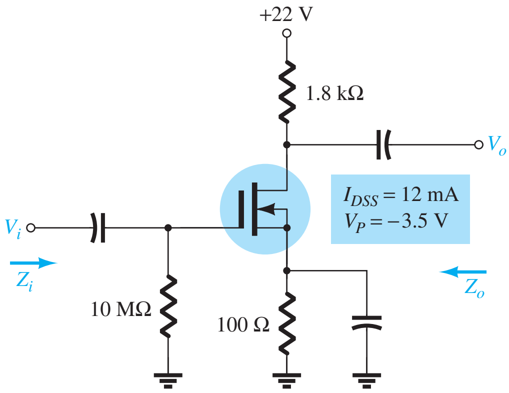

+22 V
1.8 kΩ
V_o
I_{DSS} = 12 mA
V_P = −3.5 V
V_i
Z_i
Z_o
10 MΩ
100 Ω

FIG. 8.82
Problems 36, 37, and 63.

38. Determine V_o for the network of Fig. 8.83 if $V_i = 1.8$ mV.

39. Determine Z_i, Z_o, and A_v for the network of Fig. 8.84.

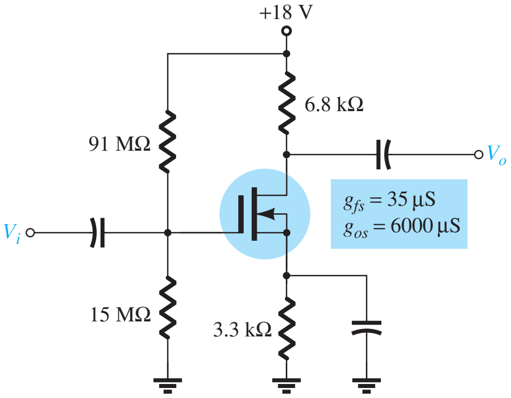

+18 V
6.8 kΩ
91 MΩ
V_o
g_{fs} = 35 μS
g_{os} = 6000 μS
V_i
15 MΩ
3.3 kΩ

FIG. 8.83
Problem 38.

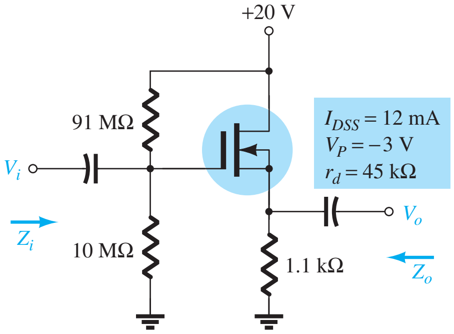

+20 V
91 MΩ
I_{DSS} = 12 mA
V_P = −3 V
r_d = 45 kΩ
V_i
V_o
Z_i
10 MΩ
1.1 kΩ
Z_o

FIG. 8.84
Problem 39.

8.10 E-MOSFET Drain-Feedback Configuration

40. Determine g_m for a MOSFET if $V_{GS(\text{Th})} = 3$ V and it is biased at $V_{GS_Q} = 8$ V. Assume $k = 0.3 \times 10^{-3}$.

41. Determine Z_i, Z_o, and A_v for the amplifier of Fig. 8.85 if $k = 0.3 \times 10^{-3}$.

42. Repeat Problem 41 if k drops to 0.2×10^{-3}. Compare results.

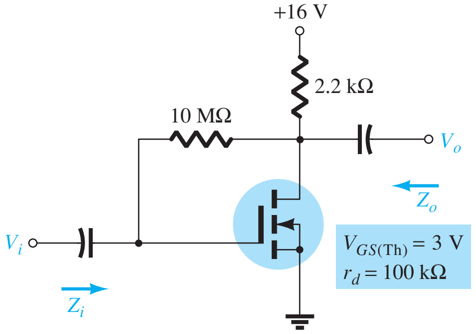
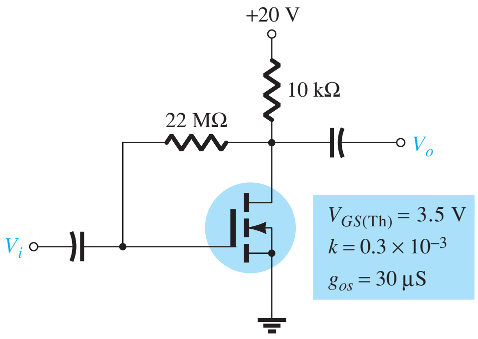

+16 V
2.2 kΩ
10 MΩ
V_o
Z_o
V_i
$V_{GS(\text{Th})}$ = 3 V
r_d = 100 kΩ
Z_i

FIG. 8.85
Problems 41, 42, and 64.

43. Determine V_o for the network of Fig. 8.86 if $V_i = 20$ mV.

44. Determine V_o for the network of Fig. 8.86 if $V_i = 4$ mV, $V_{GS(\text{Th})} = 4$ V, and $I_{D(\text{on})} = 4$ mA, with $V_{GS(\text{on})} = 7$ V and $g_{os} = 20\ \mu$S.

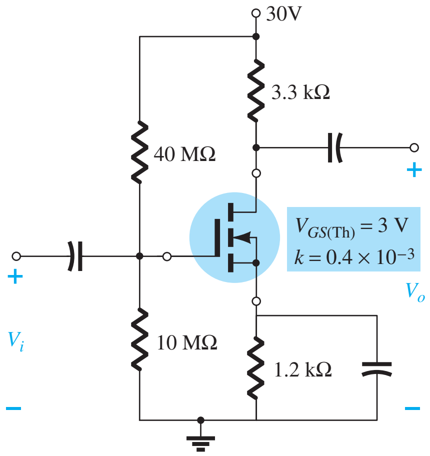


+20 V
10 kΩ
22 MΩ
V_o
V_i
$V_{GS(\text{Th})} = 3.5$ V
$k = 0.3 \times 10^{-3}$
$g_{os} = 30\ \mu$S

FIG. 8.86
Problems 43 and 44.

8.11 E-MOSFET Voltage-Divider Configuration

45. Determine the output voltage for the network of Fig. 8.87 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.



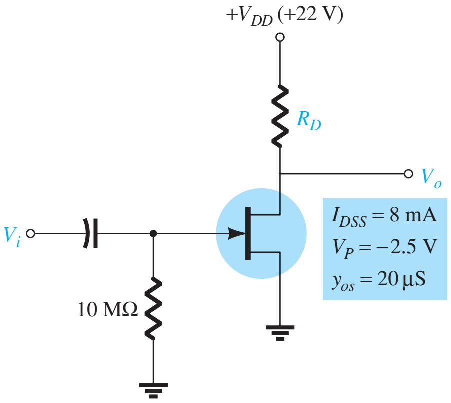
30V
3.3 kΩ
40 MΩ
+
$V_{GS(\text{Th})} = 3$ V
$k = 0.4 \times 10^{-3}$
+
V_o
V_i
10 MΩ
1.2 kΩ
–
–

FIG. 8.87
Problem 45.

8.12 Designing FET Amplifier Networks

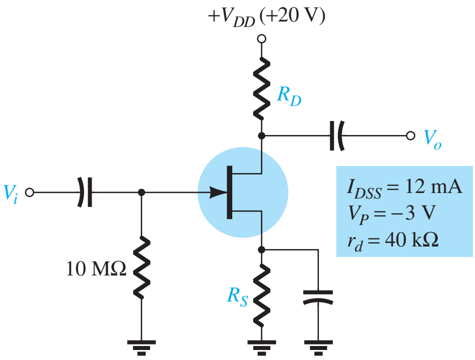
46. Design the fixed-bias network of Fig. 8.88 to have a gain of 8.

47. Design the self-bias network of Fig. 8.89 to have a gain of 10. The device should be biased at $V_{GS_Q} = \frac{1}{3}V_P$.



$+V_{DD}$ (+22 V)
R_D
V_o
V_i
$I_{DSS} = 8$ mA
$V_P = -2.5$ V
$y_{os} = 20\ \mu$S
10 MΩ

FIG. 8.88
Problem 46.



$+V_{DD}$ (+20 V)
R_D
V_o
V_i
$I_{DSS} = 12$ mA
$V_P = -3$ V
$r_d = 40$ kΩ
10 MΩ
R_S

FIG. 8.89
Problem 47.

8.14 Effect of R_L and R_{sig}

48. For the self-bias JFET network of Fig. 8.90:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_{sig} to 10 kΩ and calculate the new levels of A_{v_L} and A_{v_s}. How is the voltage gain affected by an increase in R_s?

e. For the change of part (d), determine Z_i and Z_o. What was the effect on both impedances?

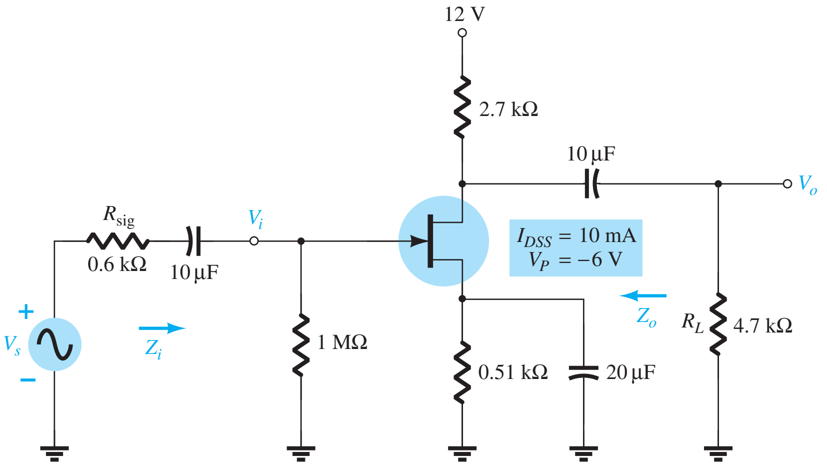


FIG. 8.90
Problem 48.

49. For the source-follower network of Fig. 8.91:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_L to 4.7 kΩ and calculate A_{v_L} and A_{v_s}. What was the effect of increasing levels of R_L on both voltage gains?

e. Change R_{sig} to 20 kΩ (with R_L at 2.2 kΩ) and calculate A_{v_L} and A_{v_s}. What was the effect of increasing levels of R_{sig} on both voltage gains?

f. Change R_L to 4.7 kΩ and R_{sig} to 20 kΩ and calculate Z_i and Z_o. What was the effect on both impedance parameters?

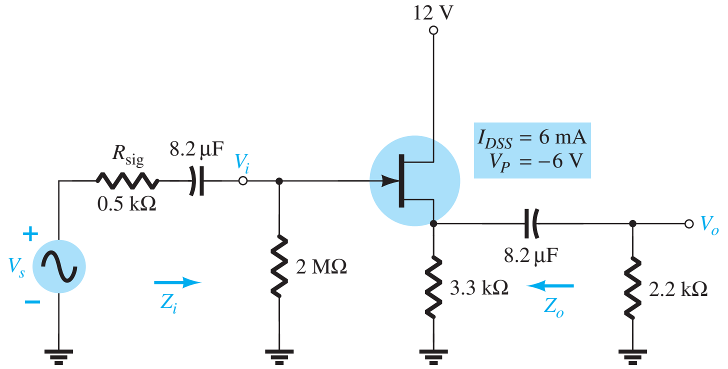


FIG. 8.91
Problem 49.

50. For the common-gate configuration of Fig. 8.92:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_L to 2.2 kΩ and calculate A_{v_L} and A_{v_s}. What was the effect of changing R_L on the voltage gains?

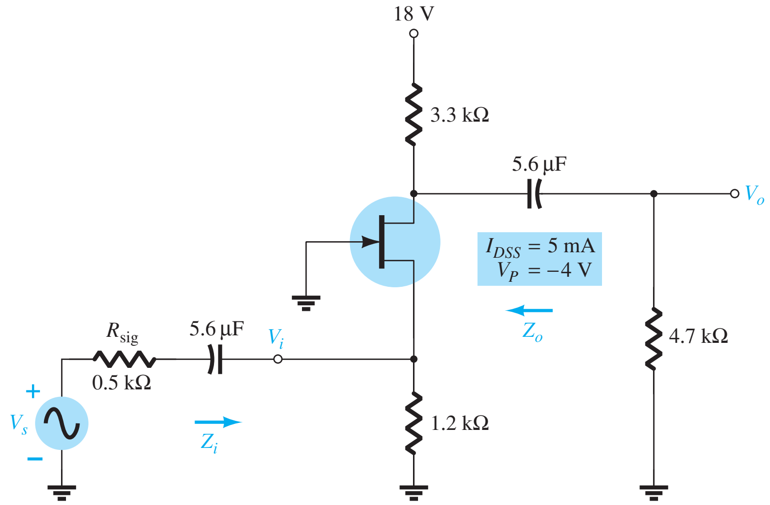

18 V
3.3 kΩ
5.6 μF
V_o
I_{DSS} = 5 mA
V_P = −4 V
Z_o
4.7 kΩ
R_{sig}
0.5 kΩ
5.6 μF
V_i
Z_i
+
V_s
−
1.2 kΩ

FIG. 8.92
Problem 50.

e. Change R_{sig} to 0.1 kΩ (with R_L at 4.7 kΩ) and calculate A_{v_L} and A_{v_s}. What was the effect of changing R_{sig} on the voltage gains?

f. Change R_L to 2.2 kΩ and R_{sig} to 0.1 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

g. What general conclusions can you draw from the above calculations?

8.15 Cascade Configuration

51. For the JFET cascade amplifier in Fig. 8.93, calculate the dc bias conditions for the two identical stages, using JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V.

52. For the JFET cascade amplifier of Fig. 8.93, using identical JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V, calculate the voltage gain of each stage, the overall gain of the amplifier, and the output voltage V_o.

53. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having specifications $I_{DSS} = 12$ mA and $V_P = -3$ V, calculate the resulting dc bias of each stage.

54. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having the specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $g_{os} = 25\ \mu$S, calculate the resulting voltage gain for each stage, the overall voltage gain, and the output voltage, V_o.

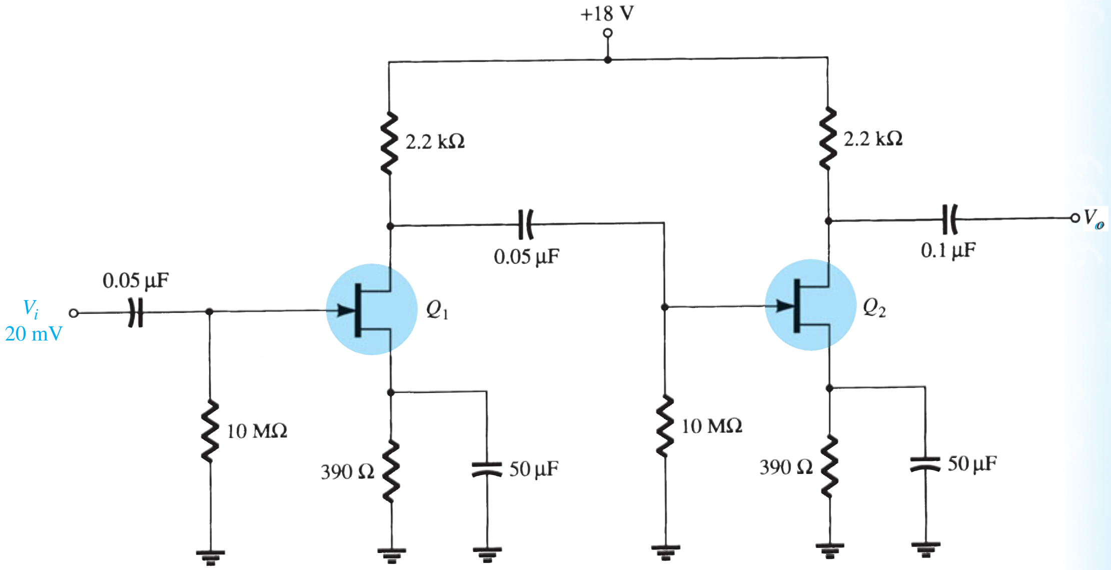

+18 V
2.2 kΩ
2.2 kΩ
0.05 μF
0.1 μF
V_o
0.05 μF
V_i
20 mV
Q_1
Q_2
10 MΩ
10 MΩ
390 Ω
50 μF
390 Ω
50 μF

FIG. 8.93
Problems 51 to 55, 65, and 66.

55. For the cascade amplifier of Fig. 8.93, using JFETs with specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $g_{os} = 25\ \mu$S, calculate the circuit input impedance (Z_i) and output impedance (Z_o).

56. For the cascade amplifier of Fig. 8.94, calculate the dc bias voltages currents of each stage.

57. For the amplifier circuit of Fig. 8.94, calculate the voltage gain of each stage and the overall amplifier voltage gain.

58. Calculate the input impedance (Z_i) and output impedance (Z_o) for the amplifier circuit of Fig. 8.94.

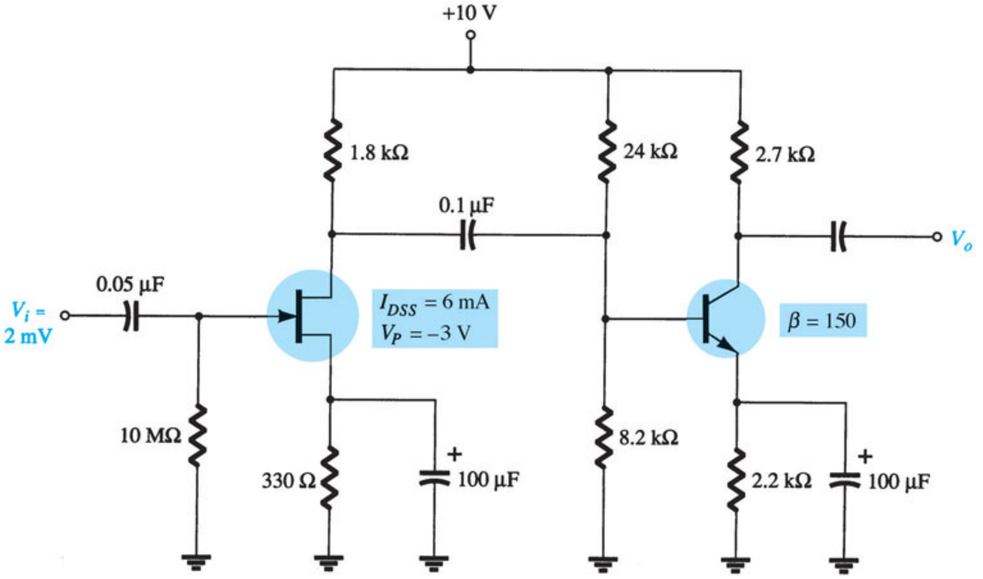


FIG. 8.94
Problems 56 to 58.

8.19 Computer Analysis

59. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.73.

60. Using Multisim, determine the voltage gain for the network of Fig. 8.75.

61. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.76.

62. Using Multisim, determine the voltage gain for the network of Fig. 8.77.

63. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.82.

64. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.85.

***65.** Use the Design Center to draw a schematic circuit of the cascade JFET amplifier as in Fig. 8.93. Set the JFET parameters for $I_{DSS} = 12$ mA and $V_P = 3$ V, and have the analysis determine the dc bias.

***66.** Use the Design Center to draw a schematic circuit for a cascade JFET amplifier as shown in Fig. 8.93. Set the analysis to calculate the ac output voltage V_o for $I_{DSS} = 12$ mA and $V_P = -3$ V.

9

BJT and JFET Frequency Response

CHAPTER OBJECTIVES

- Develop confidence in the use of logarithms, understand the concept of decibels, and be able to accurately read a logarithmic plot.
- Become acquainted with the frequency response of a BJT and FET amplifier.
- Be able to normalize a frequency plot, establish the dB plot, and find the cutoff frequencies and bandwidth.
- Understand how straight-line segments and cutoff frequencies can result in a Bode plot that will define the frequency response of an amplifier.
- Be able to find the Miller effect capacitance at the input and output of an amplifier due to a feedback capacitor.
- Become familiar with square-wave testing to determine the frequency response of an amplifier.

9.1 INTRODUCTION

The analysis thus far has been limited to a particular frequency. For the amplifier, it was a frequency that normally permitted ignoring the effects of the capacitive elements, reducing the analysis to one that included only resistive elements and sources of the independent and controlled variety. We will now investigate the frequency effects introduced by the larger capacitive elements of the network at low frequencies and the smaller capacitive elements of the active device at high frequencies. Because the analysis will extend through a wide frequency range, the logarithmic scale will be defined and used throughout the analysis. In addition, because industry typically uses a decibel scale on its frequency plots, the concept of the decibel is introduced in some detail. The similarities between the frequency response analyses of both BJTs and FETs permit the coverage of both in the same chapter.

9.2 LOGARITHMS

In this field, there is no escaping the need to become comfortable with the logarithmic function. The plotting of a variable between wide limits, comparing levels without having to deal with unwieldy numbers, and identifying levels of particular importance in the design, review, and analysis procedures are all positive features of using the logarithmic function.

As a first step in clarifying the relationship between the variables of a logarithmic function, consider the following mathematical equations:

$$\boxed{a = b^x, \qquad x = \log_b a} \tag{9.1}$$

The variables a, b, and x are the same in each equation. If a is determined by taking the base b to the x power, the same x will result if the log of a is taken to the base b. For instance, if $b = 10$ and $x = 2$,

$$a = b^x = (10)^2 = 100$$

but

$$x = \log_b a = \log_{10} 100 = 2$$

In other words, if you were asked to find the power of a number that would result in a particular level such as

$$10{,}000 = 10^x$$

you could determine the level of x using logarithms. That is,

$$x = \log_{10} 10{,}000 = 4$$

For the electrical/electronics industry and in fact for the vast majority of scientific research, the base in the logarithmic equation is chosen as either 10 or the number $e = 2.71828 \ldots$.

Logarithms taken to the base 10 are referred to as *common logarithms,* whereas logarithms taken to the base e are referred to as *natural logarithms.* In summary:

$$\boxed{\text{Common logarithm:} \quad x = \log_{10} a} \tag{9.2}$$

$$\boxed{\text{Natural logarithm:} \quad y = \log_e a} \tag{9.3}$$

The two are related by

$$\boxed{\log_e a = 2.3 \log_{10} a} \tag{9.4}$$

On scientific calculators, the common logarithm is typically denoted by the **log** key and the natural logarithm by the **ln** key.

EXAMPLE 9.1 Using the calculator, determine the logarithm of the following numbers to the base indicated:

a. $\log_{10} 10^6$.
b. $\log_e e^3$.
c. $\log_{10} 10^{-2}$.
d. $\log_e e^{-1}$.

Solution:

a. **6** b. **3** c. **−2** d. **−1**

The results in Example 9.1 clearly reveal that

the logarithm of a number taken to a power is simply the power of the number if the number matches the base of the logarithm.

In the next example, the base and the variable x are not related by an integer power of the base.

EXAMPLE 9.2 Using the calculator, determine the logarithm of the following numbers:

a. $\log_{10} 64$.
b. $\log_e 64$.
c. $\log_{10} 1600$.
d. $\log_{10} 8000$.

Solution:

a. **1.806** b. **4.159** c. **3.204** d. **3.903**

Note in parts (a) and (b) of Example 9.2 that the logarithms $\log_{10} a$ and $\log_e a$ are indeed related as defined by Eq. (9.4). In addition, note that the logarithm of a number does not increase in the same linear fashion as the number. That is, 8000 is 125 times larger than 64, but the logarithm of 8000 is only about 2.16 times larger than the magnitude of the logarithm of 64, revealing a very nonlinear relationship. In fact, Table 9.1 clearly shows how the logarithm of a number increases only as the exponent of the number. If the antilogarithm of a number is desired, the 10^x or e^x calculator function is employed.

TABLE 9.1

$\log_{10} 10^0 = 0$
$\log_{10} 10 = 1$
$\log_{10} 100 = 2$
$\log_{10} 1{,}000 = 3$
$\log_{10} 10{,}000 = 4$
$\log_{10} 100{,}000 = 5$
$\log_{10} 1{,}000{,}000 = 6$
$\log_{10} 10{,}000{,}000 = 7$
$\log_{10} 100{,}000{,}000 = 8$
etc.

EXAMPLE 9.3 Using a calculator, determine the antilogarithm of the following expressions:

a. $1.6 = \log_{10} a$.
b. $0.04 = \log_e a$.

Solution:

a. $a = 10^{1.6}$
Using the 10^x key: $a = \mathbf{39.81}$
b. $a = e^{0.04}$
Using the e^x key: $a = \mathbf{1.0408}$

Because the remaining analysis of this chapter employs the common logarithm, we review a few properties of logarithms using solely the common logarithm. In general, however, the same relationships hold true for logarithms to any base. First, note that

$$\boxed{\log_{10} 1 = 0} \tag{9.5}$$

as clearly revealed by Table 9.1, because $10^0 = 1$. Next,

$$\boxed{\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b} \tag{9.6}$$

which for the special case of $a = 1$ becomes

$$\boxed{\log_{10} \frac{1}{b} = -\log_{10} b} \tag{9.7}$$

which shows that for any b greater than 1, the logarithm of a number less than 1 is always negative. Finally,

$$\boxed{\log_{10} ab = \log_{10} a + \log_{10} b} \tag{9.8}$$

In each case, the equations employing natural logarithms have the same format.

EXAMPLE 9.4 Using a calculator, determine the logarithm of the following numbers:

a. $\log_{10} 0.5$.

b. $\log_{10} \dfrac{4000}{250}$.

c. $\log_{10} (0.6 \times 30)$.

Solution:

a. $\mathbf{-0.3}$

b. $\log_{10} 4000 - \log_{10} 250 = 3.602 - 2.398 = \mathbf{1.204}$

$$\text{Check: } \log_{10} \frac{4000}{250} = \log_{10} 16 = \mathbf{1.204}$$

c. $\log_{10} 0.6 + \log_{10} 30 = -0.2218 + 1.477 = \mathbf{1.255}$

$$\text{Check: } \log_{10} (0.6 \times 30) = \log_{10} 18 = \mathbf{1.255}$$

The use of log scales can significantly expand the range of variation of a particular variable on a graph. Most graph paper available is of the semilog or double-log (log-log) variety. The term *semi* (meaning one-half) indicates that only one of the two scales is a log scale, whereas double-log indicates that both scales are log scales. A semilog scale appears in Fig. 9.1. Note that the vertical scale is a linear scale with equal divisions. The spacing between the lines of the log plot is shown on the graph. The log of 2 to the base 10 is approximately 0.3. The distance from 1 ($\log_{10} 1 = 0$) to 2 is therefore 30% of the span. The log of 3 to the base 10 is 0.4771 or almost 48% of the span (very close to one-half

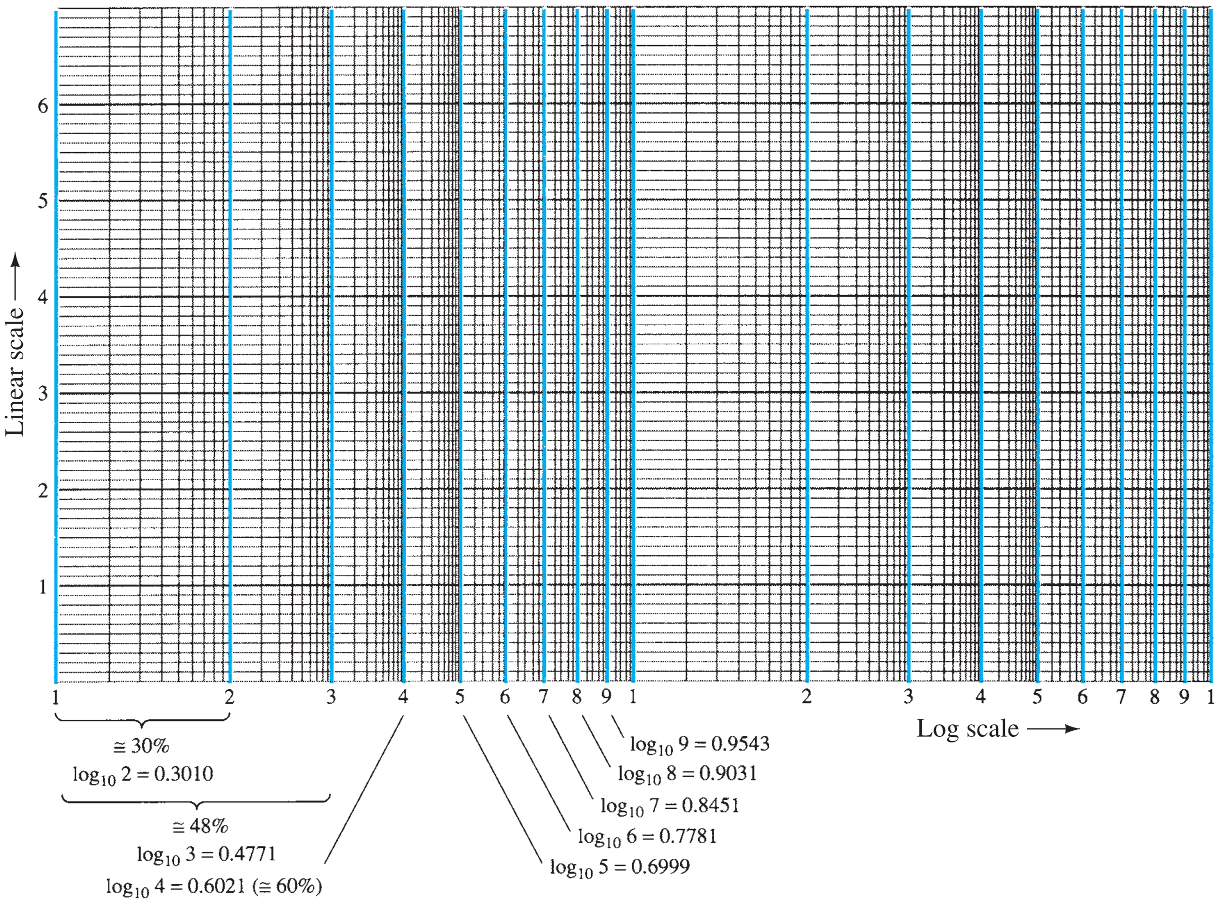


FIG. 9.1

Semilog graph paper.

the distance between power-of-10 increments on the log scale). Because $\log_{10} 5 \cong 0.7$, it is marked off at a point 70% of the distance. Note that between any two digits the same compression of the lines appears as you progress from the left to the right. It is important to note the resulting numerical value and the spacing, because plots will typically only have the tic marks indicated in Fig. 9.2 due to a lack of space. The longer bars for this figure have the numerical values of 0.3, 3, and 30 associated with them, whereas the next-shorter bars have values of 0.5, 5, and 50 and the shortest bars 0.7, 7, and 70.

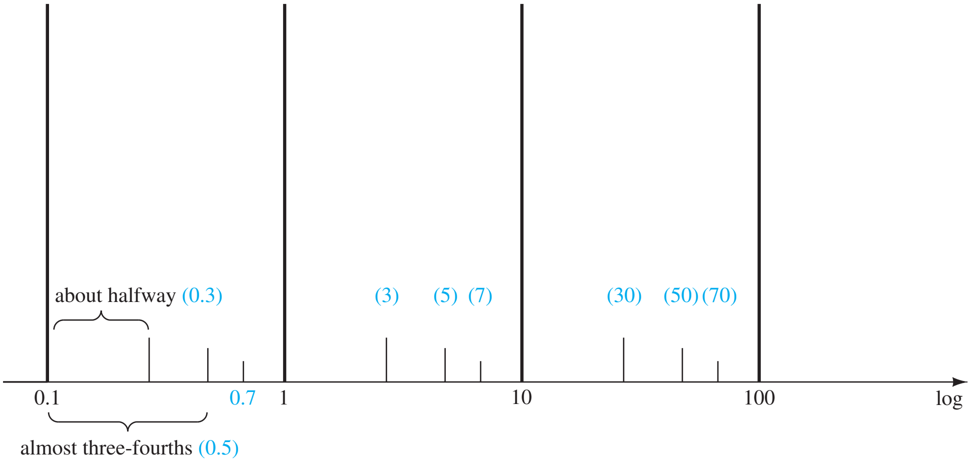


FIG. 9.2
Identifying the numerical values of the tic marks on a log scale.

On many log plots, the tick marks for most of the intermediate levels are left off because of space constraints. The following equation can be used to determine the logarithmic level at a particular point between known levels using a ruler or simply estimating the distances. The parameters are defined by Fig. 9.3.

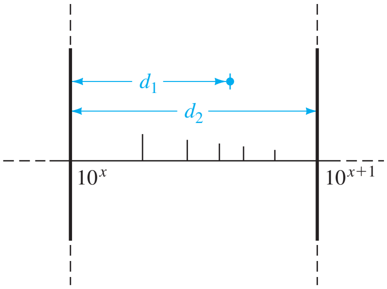


FIG. 9.3
Finding a value on a log plot.

$$\boxed{\text{Value} = 10^x \times 10^{d_1/d_2}} \qquad \textbf{(9.9)}$$

The derivation of Eq. (9.9) is simply an extension of the details regarding distance appearing in Fig. 9.1.

EXAMPLE 9.5 Determine the value of the point appearing on the logarithmic plot in Fig. 9.4 using the measurements made by a ruler (linear).

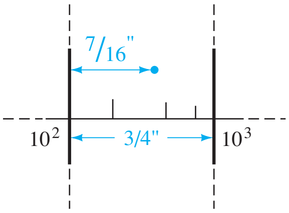


FIG. 9.4
Example 9.5.

Solution:

$$\frac{d_1}{d_2} = \frac{7/16''}{3/4''} = \frac{0.438''}{0.750''} = 0.584$$

Using a calculator:

$$10^{d_1/d_2} = 10^{0.584} = 3.837$$

Applying Eq. (9.9):

$$\begin{aligned}\text{Value} &= 10^x \times 10^{d_1/d_2} = 10^2 \times 3.837\\ &= \mathbf{383.7}\end{aligned}$$

Plotting a function on a log scale can change the general appearance of the waveform as compared to a plot on a linear scale. A straight-line plot on a linear scale can develop a curve on a log scale, and a nonlinear plot on a linear scale can take on the appearance of a straight line on a log plot. The important point is that the results extracted at each level should be correctly labeled by developing a familiarity with the spacing of Figs. 9.1 and 9.2. This is particularly true for some of the log-log plots that appear later in this book.

9.3 DECIBELS

Power Levels

The concept of the decibel (dB) and the associated calculations will become increasingly important in the remaining sections of this chapter. The term *decibel* has its origin in the fact that power and audio levels are related on a logarithmic basis. That is, an increase in power level from, say, 4 W to 16 W does not result in an audio level increase by a factor of $16/4 = 4$, but by a factor of 2, as derived from the power of 4 in the following manner: $(4)^2 = 16$. For a change of 4 W to 64 W, the audio level will increase by a factor of 3 because $(4)^3 = 64$. In logarithmic form, the relationship can be written as $\log_4 64 = 3$.

The term *bel* is derived from the surname of Alexander Graham Bell. For standardization, the bel (B) is defined by the following equation relating two power levels, P_1 and P_2:

$$\boxed{G = \log_{10}\frac{P_2}{P_1}} \quad \text{bel} \tag{9.10}$$

It was found, however, that the bel was too large a unit of measurement for practical purposes, so the decibel (dB) is defined such that 10 decibels = 1 bel. Therefore,

$$\boxed{G_{\text{dB}} = 10\log_{10}\frac{P_2}{P_1}} \quad \text{dB} \tag{9.11}$$

The terminal rating of electronic communication equipment (amplifiers, microphones, etc.) is commonly in decibels. Equation (9.11) indicates clearly, however, that the decibel rating is a measure of the difference in magnitude between *two* power levels. For a specified terminal (output) power (P_2) there must be a reference power level (P_1). The reference level is generally accepted to be 1 mW, although on occasion, the 6-mW standard of earlier years is applied. The resistance associated with the 1-mW power level is 600 Ω, chosen because it is the characteristic impedance of audio transmission lines. When the 1-mW level is employed as the reference level, the decibel symbol frequently appears as dBm. In equation form,

$$\boxed{G_{\text{dBm}} = 10\log_{10}\left.\frac{P_2}{1\text{ mW}}\right|_{600\,\Omega}} \quad \text{dBm} \tag{9.12}$$

There exists a second equation for decibels that is applied frequently. It can be best described through the system of Fig. 9.5. For V_i equal to some value V_1, $P_1 = V_1^2/R_i$, where R_i is the input resistance of the system of Fig. 9.5. If V_i should be increased (or decreased) to some other level, V_2 then $P_2 = V_2^2/R_i$. If we substitute into Eq. (9.11) to determine the resulting difference in decibels between the power levels, we obtain

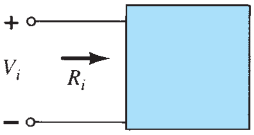


FIG. 9.5
Configuration employed in the discussion of Eq. (9.13).

$$G_{\text{dB}} = 10\log_{10}\frac{P_2}{P_1} = 10\log_{10}\frac{V_2^2/R_i}{V_1^2/R_i} = 10\log_{10}\left(\frac{V_2}{V_1}\right)^2$$

and

$$\boxed{G_{\text{dB}} = 20\log_{10}\frac{V_2}{V_1}} \quad \text{dB} \tag{9.13}$$

Frequently, the effect of different impedances ($R_1 \neq R_2$) is ignored and Eq. (9.13) applied simply to establish a basis of comparison between levels—voltage or current. For situations of this type, the decibel gain should more correctly be referred to as the voltage or current gain in decibels to differentiate it from the common usage of decibel as applied to power levels.

In particular note the multiplying factor of 20 rather than the 10 of earlier equations.

Cascaded Stages

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages. For example, the magnitude of the overall voltage gain of a cascaded system is given by

$$|A_{v_T}| = |A_{v_1}| \cdot |A_{v_2}| \cdot |A_{v_3}| \cdots |A_{v_n}| \tag{9.14}$$

Applying the proper logarithmic relationship results in

$$G_v = 20\log_{10}|A_{v_T}| = 20\log_{10}|A_{v_1}| + 20\log_{10}|A_{v_2}| \\ +20\log_{10}|A_{v_3}| + \cdots + 20\log_{10}|A_{v_n}| \qquad \text{(db)} \qquad \mathbf{(9.15)}$$

In words, the equation states that the decibel gain of a cascaded system is simply the sum of the decibel gains of each stage, that is,

$$\boxed{G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \cdots + G_{\text{dB}_n}} \quad \text{dB} \qquad \mathbf{(9.16)}$$

Voltage Gains versus dB Levels

Table 9.2 shows the association between dB levels and voltage gains. First note that a gain of 2 results in a dB level of +6 dB, whereas a drop to $\frac{1}{2}$ results in a −6-dB level. A change in V_o/V_i from 1 to 10, 10 to 100, or 100 to 1000 results in the same 20-dB change in level. When $V_o = V_i$, $V_o/V_i = 1$, and the dB level is 0. At a very high gain of 1000, the dB level is 60, whereas at the much higher gain of 10,000, the dB level is 80 dB, an increase of only 20 dB—a result of the logarithmic relationship. Table 9.2 clearly reveals that voltage gains of 50 dB or higher should immediately be recognized as being quite high.

TABLE 9.2

Comparing $A_v = \dfrac{V_o}{V_i}$ *to dB*

Voltage Gain, V_o/V_i	dB Level
0.5	−6
0.707	−3
1	0
2	6
10	20
40	32
100	40
1000	60
10,000	80
etc.	

EXAMPLE 9.6 Find the magnitude gain corresponding to a voltage gain of 100 dB.

Solution: By Eq. (9.13),

$$G_{\text{dB}} = 20\log_{10}\frac{V_2}{V_1} = 100\ \text{dB} \Rightarrow \log_{10}\frac{V_2}{V_1} = 5$$

so that

$$\frac{V_2}{V_1} = \mathbf{10^5 = 100{,}000}$$

EXAMPLE 9.7 The input power to a device is 10,000 W at a voltage of 1000 V. The output power is 500 W and the output impedance is 20 Ω.

a. Find the power gain in decibels.
b. Find the voltage gain in decibels.
c. Explain why parts (a) and (b) agree or disagree.

Solution:

a. $G_{\text{dB}} = 10\log_{10}\dfrac{P_o}{P_i} = 10\log_{10}\dfrac{500\ \text{W}}{10\ \text{kW}} = 10\log_{10}\dfrac{1}{20} = -10\log_{10}20$

$$= -10(1.301) = \mathbf{-13.01\ dB}$$

b. $G_v = 20\log_{10}\dfrac{V_o}{V_i} = 20\log_{10}\dfrac{\sqrt{PR}}{1000} = 20\log_{10}\dfrac{\sqrt{(500\ \text{W})(20\ \Omega)}}{1000\ \text{V}}$

$$= 20\log_{10}\frac{100}{1000} = 20\log_{10}\frac{1}{10} = -20\log_{10}10 = \mathbf{-20\ dB}$$

c. $R_i = \dfrac{V_i^2}{P_i} = \dfrac{(1\ \text{kV})^2}{10\ \text{kW}} = \dfrac{10^6}{10^4} = \mathbf{100\ \Omega \neq R_o = 20\ \Omega}$

EXAMPLE 9.8 An amplifier rated at 40-W output is connected to a 10-Ω speaker.

a. Calculate the input power required for full power output if the power gain is 25 dB.
b. Calculate the input voltage for rated output if the amplifier voltage gain is 40 dB.

Solution:

a. Eq. (9.11): $25 = 10\log_{10}\dfrac{40\ \text{W}}{P_i} \Rightarrow P_i = \dfrac{40\ \text{W}}{\text{antilog}\,(2.5)} = \dfrac{40\ \text{W}}{3.16 \times 10^2}$

$$= \frac{40\ \text{W}}{316} \cong \mathbf{126.5\ mW}$$

b. $G_v = 20\log_{10}\dfrac{V_o}{V_i} \Rightarrow 40 = 20\log_{10}\dfrac{V_o}{V_i}$

$$\frac{V_o}{V_i} = \text{antilog } 2 = 100$$

$$V_o = \sqrt{PR} = \sqrt{(40\text{ W})(10\text{ V})} = 20\text{ V}$$

$$V_i = \frac{V_o}{100} = \frac{20\text{ V}}{100} = 0.2\text{ V} = \mathbf{200\text{ mV}}$$

Human Auditory Response

One of the most frequent applications of the decibel scale is in the communication and entertainment industries. The human ear does not respond in a linear fashion to changes in source power level, that is, a doubling of the audio power level from 1/2 W to 1 W does not result in a doubling of the loudness level for the human ear. In addition, a change from 5 W to 10 W is received by the ear as the same change in sound intensity as experienced from 1/2 W to 1 W. In other words, the ratio between levels is the same in each case (1 W/0.5 W = 10 W/5 W = 2), resulting in the same decibel or logarithmic change defined by Eq. (9.11). The ear, therefore, responds in a logarithmic fashion to changes in audio power levels.

To establish a basis for comparison between audio levels, a reference level of 0.0002 **microbar** (μbar) was chosen, where 1 μbar is equal to the sound pressure of 1 dyne per square centimeter, or about 1 millionth of the normal atmospheric pressure at sea level. The 0.0002 μbar level is the threshold level of hearing. Using this reference level, the sound pressure level in decibels is defined by the following equation:

$$\boxed{\text{dB}_s = 20\log_{10}\frac{P}{0.0002\ \mu\text{bar}}} \qquad \textbf{(9.17)}$$

where P is the sound pressure in microbars.

The decibel levels in Table 9.3 are defined by Eq. (9.17). Meters designed to measure audio levels are calibrated to the levels defined by Eq. (9.17) and shown in Table 9.3.

In particular take note of the sound level for iPods and MP3 players, for which it is suggested, based on research, that they should not be used for more than 1 hour a day at 60% volume to prevent permanent hearing damage. Always remember that hearing damage is usually not reversible, so that any loss is for the long term.

A common question regarding audio levels is how much the power level of an acoustical source must be increased to double the sound level received by the human ear. The question is not as simple as it first seems due to considerations such as the frequency content of the sound, the acoustical conditions of the surrounding area, the physical characteristics of the surrounding medium, and—of course—the unique characteristics of the human ear. However, a general conclusion can be formulated that has practical value if we note the power levels of an acoustical source appearing to the left in Table 9.3. Each power level is associated with a particular decibel level, and a change of 10 dB in the scale corresponds to an increase or a decrease in power by a factor of 10. For instance, a change from 90 dB to 100 dB is associated with a change in wattage from 3 W to 30 W. Through experimentation, it has been found that on an average basis the loudness level doubles for every 10 dB change in audio level—a conclusion somewhat verified by the examples to the right in Table 9.3.

To double the sound level received by the human ear, the power rating of the acoustical source (in watts) must be increased by a factor of 10.

In other words, doubling the sound level available from a 1 W acoustical source requires moving up to a 10 W source.

Further:

At normal hearing levels, it would take a change of about 3 dB (twice the power level) for the change to be noticeable to the human ear.

At low levels of sound, a change of 2 dB may be noticeable, but it may take a 6 dB (four times the power level) change for much higher levels of sound.

TABLE 9.3

Typical sound levels and their decibel levels.

Output Power. Average value in watts.	dB_s		
	160	Jet engine	
	150		
	140	Community siren	
	130	Jackhammer	
Threshold of pain	120	Live music concert, iPods and MP3 players at full volume	
300	110	Health club, movie theater	
100		Chain saw	
30	100	Very loud music, motorcycle	
10			
3	90	Loud music, heavy truck, subway train	
1			
0.3	80	Orchestra, highway traffic, alarm clock	
0.1			
0.03	70		
0.01		Average conversation	
0.003	60	Quiet music	Dynamic range ≅ 120 dB_s
0.001			
0.0003	50	Average residence, computer system	
	40	Background music	
	30	Quiet office, computer hard drive	
	20	Whispering	
	10	Faint sounds, paper rustling	
0.0002 μbar of pressure	0	Threshold of hearing	

One final example of the use of dB as a unit of measurement is the LRAD (Long Range Acoustic Device) appearing in Fig. 9.6. It emits a tone between 2100 Hz and 3100 Hz at 145 dB that is effective at up to 500 m, or almost two football fields. The sound at its peak is thousands of times louder than a smoke alarm. It can be used to transmit critical information and instructions and is capable of strong deterrent tones against intruders.

FIG. 9.6

LRAD (Long Range Acoustic Device) 1000X. (Courtesy of LRAD Corporation.)

Instrumentation

A number of modern VOMs and DMMs have a dB scale designed to provide an indication of power ratios referenced to a standard level of 1 mW at 600 Ω. Since the reading is accurate only if the load has a characteristic impedance of 600 Ω, the 1 mW, 600 Ω reference level is normally printed somewhere on the face of the meter, as shown in Fig. 9.7. The dB scale is usually calibrated to the lowest ac scale of the meter. In other words, when making the dB measurement, choose the lowest ac voltage scale, but read the dB scale. If a higher voltage scale is chosen, a correction factor must be used, which is sometimes printed on the face of the meter but is always available in the meter manual. If the impedance is other than 600 Ω or not purely resistive, other correction factors must be used that are normally included in the meter manual. Using the basic power equation $P = V^2/R$ reveals that 1 mW across a 600 Ω load is the same as applying 0.775 V rms across a 600 Ω load; that is, $V = \sqrt{PR} = \sqrt{(1\text{ mW})(600\ \Omega)} = 0.775$ V. The result is that an analog display will have 0 dB [defining the reference point of 1 mW, $\text{dB} = 10 \log_{10} P_2/P_1 = 10 \log_{10} (1\text{mW}/1\text{ mW(ref)}) = 0$ dB] and 0.775 V rms on the same pointer projection, as shown in Fig. 9.7. A voltage of 2.5 V across a 600 Ω load results in a dB level of $\text{dB} = 20 \log_{10} V_2/V_1 = 20 \log_{10} 25\text{ V}/0.775 = 10.17$ dB, resulting in 2.5 V and 10.17 dB appearing along the same pointer projection. A voltage of less than 0.775 V, such as 0.5 V, results in a dB level of $\text{dB} = 20 \log_{10} V_2/V_1 = 20 \log_{10} 0.5\text{ V}/0.775\text{ V} = -3.8$ dB, also shown on the scale in Fig. 9.7. Although a reading of 10 dB reveals that the power level is 10 times the reference, don't assume that a reading of 5 dB means that the output level is 5 mW. The 10 : 1 ratio is a special one in logarithmic use. For the 5 dB level, the power level must be found using the antilogarithm (3.126), which reveals that the power level associated with 5 dB is about 3.1 times the reference or 3.1 mW. A conversion table is usually provided in the manual for such conversions.

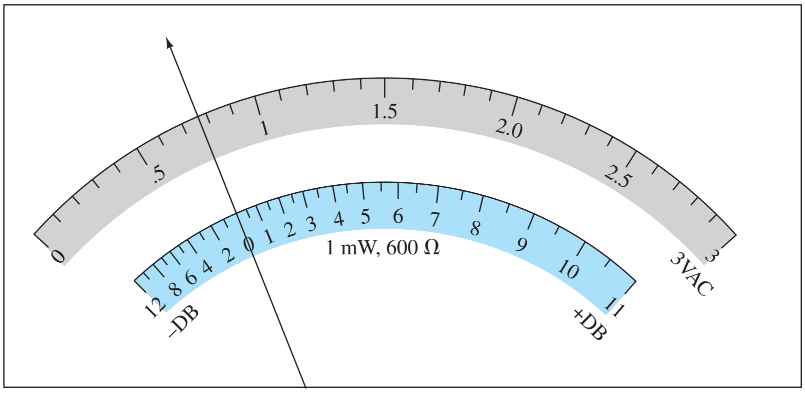


FIG. 9.7

Defining the relationship between a dB scale referenced to 1 mW, 600 Ω and a 3 V rms voltage scale.

9.4 GENERAL FREQUENCY CONSIDERATIONS

The frequency of the applied signal can have a pronounced effect on the response of a single-stage or multistage network. The analysis thus far has been for the midfrequency spectrum. At low frequencies, we shall find that the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements. The frequency-dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system. An increase in the number of stages of a cascaded system will also limit both the high- and low-frequency responses.

Low-Frequency Range

To demonstrate how the larger coupling and bypass capacitors of a network will affect the frequency response of a system, the reactance of a 1-μF (typical value for such applications) capacitor is tabulated in Table 9.4 for a wide range of frequencies.

TABLE 9.4

Variation in $X_C = \dfrac{1}{2\pi f_C}$ *with frequency for a 1-μF capacitor*

f	X_C	
10 Hz	15.91 kΩ	Range of possible effect
100 Hz	1.59 kΩ	
1 kHz	159 Ω	
10 kHz	15.9 Ω	
100 kHz	1.59 Ω	Range of lesser concern (≅ short-circuit equivalence)
1 MHz	0.159 Ω	
10 MHz	15.9 mΩ	
100 MHz	1.59 mΩ	

Two regions have been defined in Table 9.4. For the range of 10 Hz to 10 kHz the magnitude of the reactance is sufficiently large that it may have an impact on the response of the system. However, for much higher frequencies it appears as though the capacitor is behaving much like the short-circuit equivalent it is designed to match.

Clearly, therefore,

the larger capacitors of a system will have an important impact on the response of a system in the low-frequency range and can be ignored for the high-frequency region.

High-Frequency Range

For the smaller capacitors that come into play due to the parasitic capacitances of the device or network, the frequency range of concern will be the higher frequencies. Consider a 5-pF capacitor, typical of a parasitic capacitance of a transistor or the level of capacitance introduced simply by the wiring of the network, and the level of reactance that results for the same frequency range appearing in Table 9.4. The results appear in Table 9.5 and clearly reveal that at low frequencies they have a very large impedance matching the desired open-circuit equivalence. However, at higher frequencies they are approaching a short-circuit equivalence that can severely affect the response of a network.

TABLE 9.5

Variation in $X_C = \dfrac{1}{2\pi fC}$ *with frequency for a 5 pF capacitor*

f	X_C	
10 Hz	3,183 MΩ	Range of lesser concern (≅ open-circuit equivalent)
100 Hz	318.3 MΩ	
1 kHz	31.83 MΩ	
10 kHz	3.183 MΩ	
100 kHz	318.3 kΩ	Range of possible effect
1 MHz	31.83 kΩ	
10 MHz	3.183 kΩ	
100 MHz	318.3 Ω	

Clearly, therefore,

the smaller capacitors of a system will have an important impact on the response of a system in the high-frequency range and can be ignored for the low-frequency region.

Mid-Frequency Range

In the mid-frequency range the effect of the capacitive elements is largely ignored and the amplifier considered ideal and composed simply of resistive elements and controlled sources.

The result is that

the effect of the capacitive elements in an amplifier are ignored for the mid-frequency range when important quantities such as the gain and impedance levels are determined.

Typical Frequency Response

The magnitudes of the gain response curves of an *RC*-coupled, direct-coupled, and transformer-coupled amplifier system are provided in Fig. 9.8. Note that the horizontal scale is a logarithmic scale to permit a plot extending from the low- to the high-frequency regions. For each plot, a low-, a high-, and a mid-frequency region has been defined. In addition, the primary reasons for the drop in gain at low and high frequencies have also been indicated within the parentheses. For the *RC*-coupled amplifier, the drop at low frequencies is due to the increasing reactance of C_C, C_s, or C_E, whereas its upper frequency limit is determined by either the parasitic capacitive elements of the network or the frequency dependence of the gain of the active device. An explanation of the drop in gain for the transformer-coupled system requires a basic understanding of “transformer action” and the transformer equivalent circuit. For the moment, let us say that it is simply due to the “shorting effect” (across the input terminals of the transformer) of the magnetizing inductive reactance at low frequencies ($X_L = 2\pi fL$). The gain must obviously be zero at $f = 0$ because at this point there is no longer a changing flux established through the core to induce a secondary or output voltage. As indicated in Fig. 9.8, the high-frequency response is controlled primarily by the stray capacitance between the turns of the primary and secondary windings. For the direct-coupled amplifier, there are no coupling or bypass capacitors to cause a drop in gain at low frequencies. As the figure indicates, it is a flat response to the upper cutoff

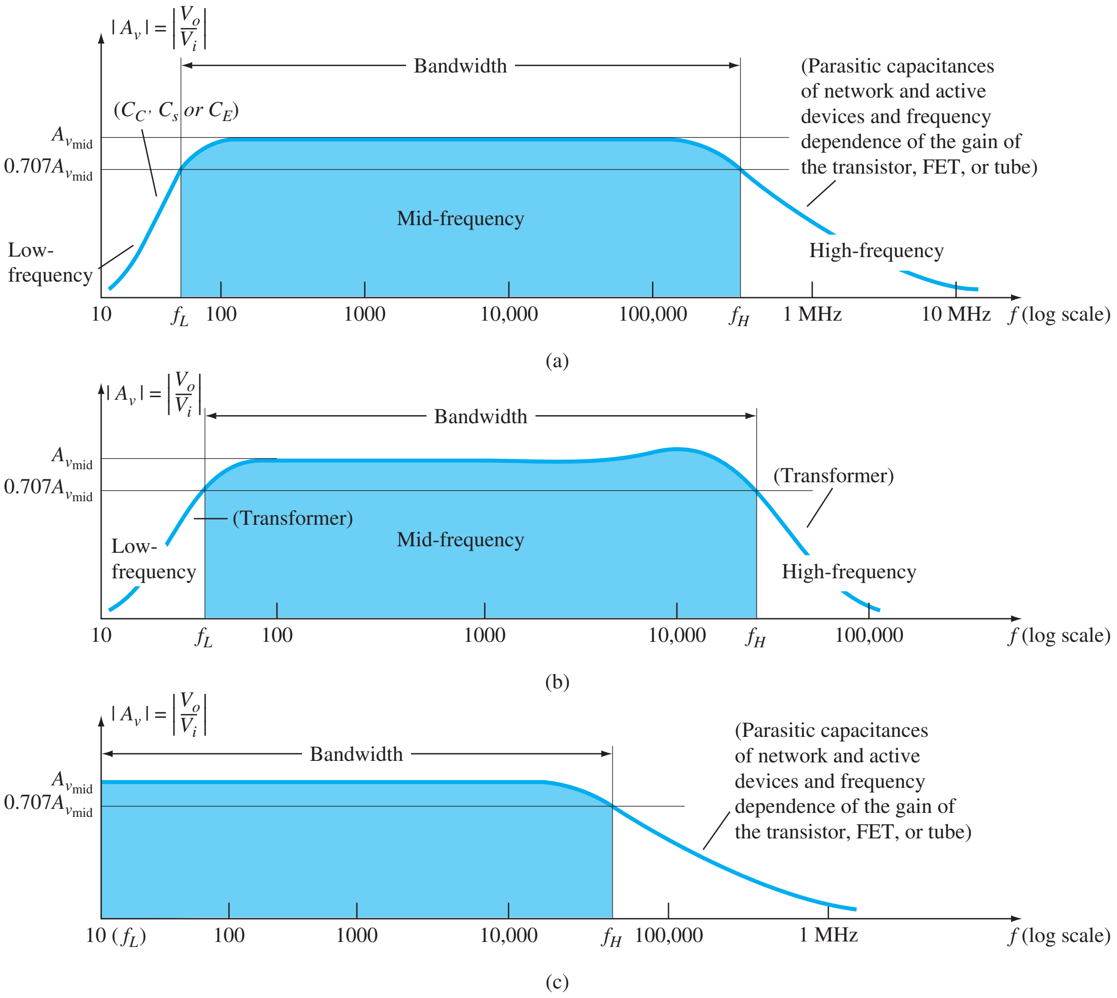


FIG. 9.8

Gain versus frequency: (a) RC-coupled amplifiers; (b) transformer-coupled amplifiers; (c) direct-coupled amplifiers.

frequency, which is determined by either the parasitic capacitances of the circuit or the frequency dependence of the gain of the active device.

For each system of Fig. 9.8, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the midband value. To fix the frequency boundaries of relatively high gain, $0.707A_{v_{\text{mid}}}$ was chosen to be the gain at the cutoff levels. The corresponding frequencies f_1 and f_2 are generally called the *corner, cutoff, band, break,* or *half-power frequencies.* The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies,

$$P_{o_{\text{mid}}} = \frac{|V_o^2|}{R_o} = \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and at the half-power frequencies,

$$P_{o_{HPF}} = \frac{|0.707\, A_{v_{\text{mid}}} V_i|^2}{R_o} = 0.5 \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and

$$\boxed{P_{o_{HPF}} = 0.5\, P_{o_{\text{mid}}}} \qquad \textbf{(9.18)}$$

The bandwidth (or passband) of each system is determined by f_H and f_L, that is,

$$\boxed{\text{bandwidth (BW)} = f_H - f_L} \qquad \textbf{(9.19)}$$

with f_H and f_L defined in each curve of Fig. 9.8.

9.5 NORMALIZATION PROCESS

For applications of a communication nature (audio, video) a decibel plot versus frequency is normally provided rather than the gain versus frequency plot of Fig. 9.8. In other words, when you pick up a specification sheet on a particular amplifier or system, the plot will typically be of dB versus frequency rather than gain versus frequency.

To obtain such a dB plot the curve is first *normalized*—a process whereby the vertical parameter is divided by a specific level or quantity sensitive to a combination or variables of the system. For this area of investigation, it is usually the midband or maximum gain for the frequency range of interest.

For example, in Fig. 9.9 the curve of Fig. 9.8a is normalized by dividing the output voltage gain at each frequency by the midband level. Note that the curve has the same shape, but the band frequencies are now defined by simply the 0.707 level and not linked to the actual midband level. It clearly reveals that

The band frequencies define a level where the gain or quantity of interest will be 70.7% or its maximum value.

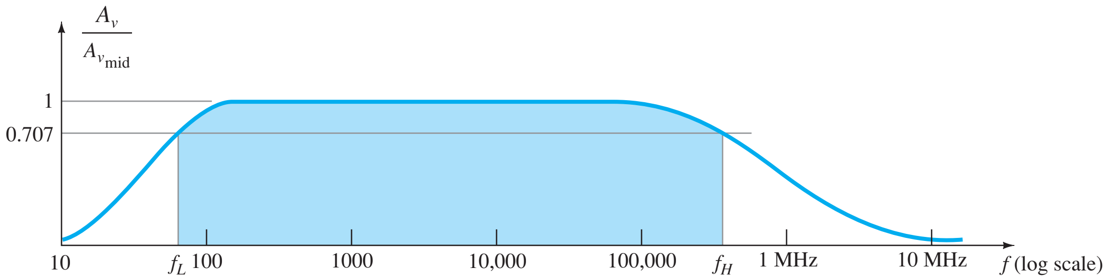


FIG. 9.9

Normalized gain versus frequency plot.

Consider also that the plot of Fig. 9.9 is not sensitive to the actual level of the midband gain. The midband gain could be 50, 100, or even 200, and the resulting plot of Fig. 9.9 would be the same. The plot of Fig. 9.9 is now defining frequencies where the relative gain is defined rather than concerning itself with the "actual gain."

The next example will demonstrate the normalization process for a typical amplifier response.

EXAMPLE 9.9 Given the frequency response of Fig. 9.10:

a. Find the cutoff frequencies f_L and f_H using the measurements provided.
b. Find the bandwidth of the response.
c. Sketch the normalized response.

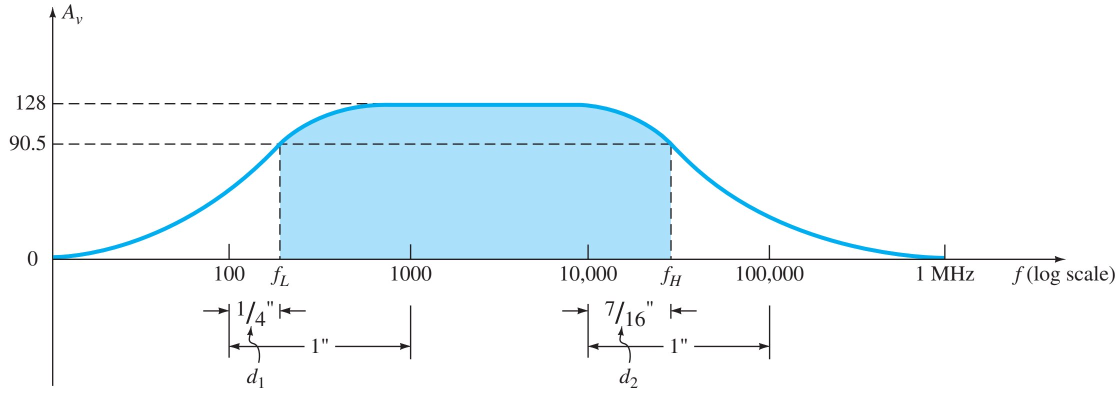


FIG. 9.10
Gain plot for Example 9.8.

Solution:

a. For f_L: $\dfrac{d_1}{d_2} = \dfrac{1/4''}{1''} = 0.25$

$$10^{d_1/d_2} = 10^{0.25} = 1.7783$$

$$\text{Value} = 10^x \times 10^{d_1/d_2} = 10^2 \times 1.7783 = \mathbf{177.83\ Hz}$$

For f_H: $\dfrac{d_1}{d_2} = \dfrac{7/16''}{1''} = 0.438$

$$10^{d_1/d_2} = 10^{0.438} = 2.7416$$

$$\text{Value} = 10^x \times 10^{d_1/d_2} = 10^4 \times 2.7416 = \mathbf{27{,}416\ Hz}$$

b. The bandwidth:

$$\text{BW} = f_H - f_L = 27{,}416\ \text{Hz} - 177.83\ \text{Hz} \cong \mathbf{27.24\ KHz}$$

c. The normalized response is determined by simply dividing each level of Fig. 9.10 by the midband level of 128, as shown in Fig. 9.11. The result is a maximum value of 1 and cutoff levels of 0.707.

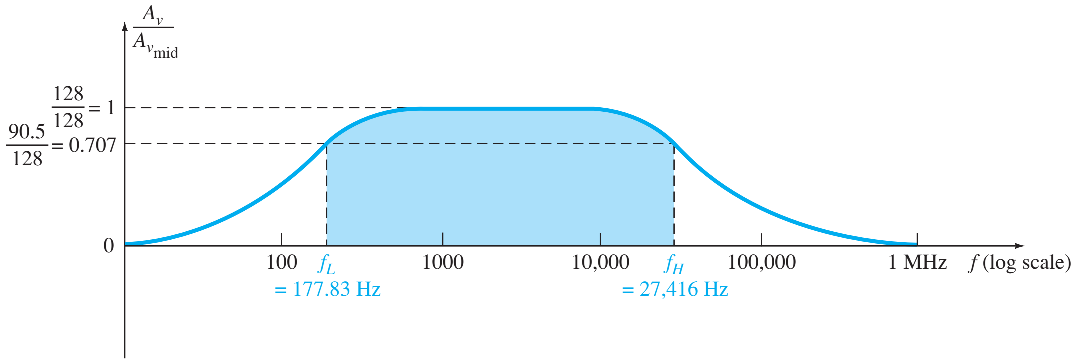


FIG. 9.11
Narmalized plot of Fig. 9.10.

A decibel plot of Fig. 9.11 can be obtained by applying Eq. (9.13) in the following manner:

$$\boxed{\left.\frac{A_v}{A_{v_{\text{mid}}}}\right|_{\text{dB}} = 20 \log_{10} \frac{A_v}{A_{v_{\text{mid}}}}} \qquad \textbf{(9.20)}$$

At midband frequencies, $20 \log_{10} 1 = 0$, and at the cutoff frequencies, $20 \log_{10} 1/\sqrt{2} = -3$ dB. Both values are clearly indicated in the resulting decibel plot of Fig. 9.12. The smaller the fraction ratio, the more negative is the decibel level.

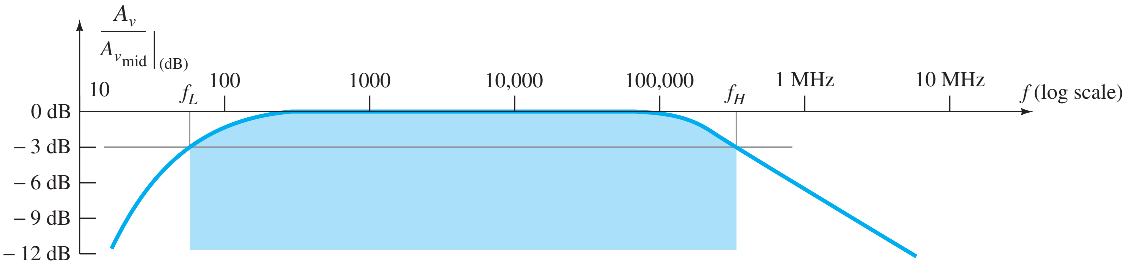


FIG. 9.12

Decibel plot of the normalized gain versus frequency plot of Fig. 9.9.

For the greater part of the discussion to follow, a decibel plot will be made only for the low- and high-frequency regions. Keep Fig. 9.12 in mind, therefore, to permit a visualization of the broad system response.

Most amplifiers introduce a 180° phase shift between input and output signals. This fact must now be expanded to indicate that this is the case only in the midband region. At low frequencies, there is a phase shift such that V_o lags V_i by an increased angle. At high frequencies, the phase shift drops below 180°. Figure 9.13 is a standard phase plot for an *RC*-coupled amplifier.

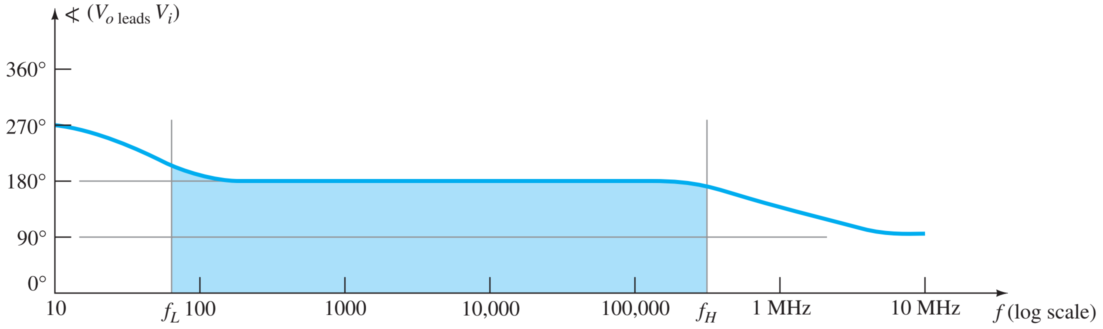


FIG. 9.13

Phase plot for an RC-coupled amplifier system.

9.6 LOW-FREQUENCY ANALYSIS—BODE PLOT

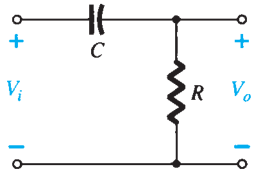


FIG. 9.14

RC combination that will define a low-cutoff frequency.

In the low-frequency region of the single-stage BJT or FET amplifier, it is the *RC* combinations formed by the network capacitors C_C, C_E, and C_s and the network resistive parameters that determine the cutoff frequencies. In fact, an *RC* network similar to Fig. 9.14 can be established for each capacitive element, and the frequency at which the output voltage drops to 0.707 of its maximum value can be determined. Once the cutoff frequencies due to each capacitor are determined, they can be compared to establish which will determine the low-cutoff frequency for the system.

Consider, for example, the voltage-divider BJT network of Fig. 9.15 that was analyzed in detail in Section 5.6. The analysis of that section resulted in an input impedance of

$$Z_i = R_i = R_1 \| R_2 \| \beta r_e$$

and an equivalent circuit at the input as shown in Fig. 9.16.

For the mid-frequency range the capacitor C_s is assumed to be an equivalent short-circuit state, and $V_b = V_i$. The result is a high midband gain for the amplifier that is not affected by the coupling or bypass capacitors. However, as we lower the applied frequency the reactance of the capacitor will increase and take an increasing share of the applied voltage V_i. Neglecting the effects of the coupling capacitor C_C and bypass capacitor C_E for the moment, if the voltage V_b should decrease, it will result in the same decrease in overall gain V_o/V_i.

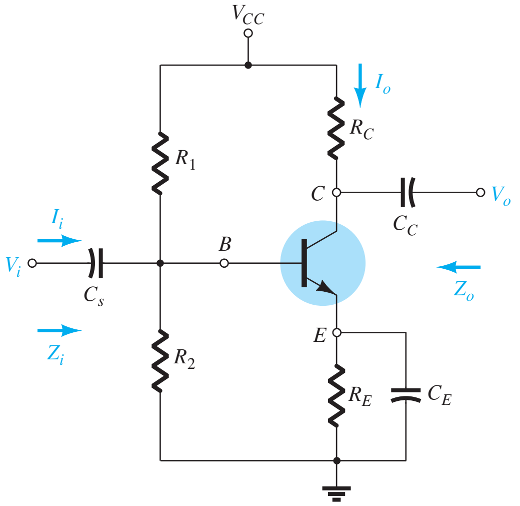


FIG. 9.15
Voltage-divider bias configuration.

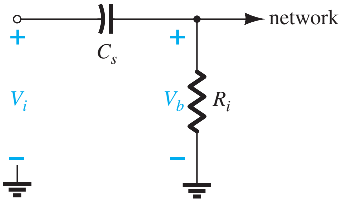


FIG. 9.16
Equivalent input circuit for the network of Fig. 9.15.

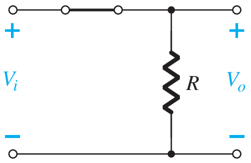


FIG. 9.17
RC circuit of Fig. 9.14 at very high frequencies.

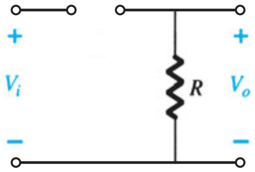


FIG. 9.18
RC circuit of Fig. 9.14 at f = 0 Hz.

Less of the applied voltage is reaching the base of the transistor reducing the output voltage V_o. In fact if the V_b should drop to 0.707 of the peak possible value of V_i the overall gain will drop the same amount. In total, therefore, if we find the frequency that will result in V_b being only 0.707 V_i, we will have the low-cutoff frequency for the full amplifier response.

Finding this frequency will now be examined by analyzing the generic *RC* network of Fig. 9.14 introduced above. Once the results are obtained it can be applied to any *RC* combination that may develop due to the other coupling capacitors or bypass capacitors. At high frequencies, the reactance of the capacitor of Fig. 9.14 is

$$X_C = \frac{1}{2\pi fC} \cong 0\ \Omega$$

and the short-circuit equivalent can be substituted for the capacitor as shown in Fig. 9.17. The result is that $V_o \cong V_i$ at high frequencies. At $f = 0$ Hz,

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(0)C} = \infty\ \Omega$$

and the open-circuit approximation can be applied as shown in Fig. 9.18, with the result that $V_o = 0$ V.

Between the two extremes, the ratio $A_v = V_o/V_i$ will vary as shown in Fig. 9.19. As the frequency increases, the capacitive reactance decreases, and more of the input voltage appears across the output terminals.

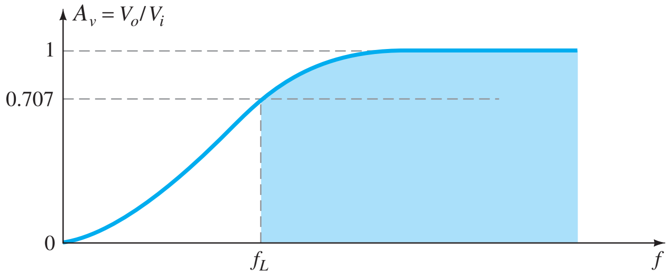


FIG. 9.19
Low-frequency response for the RC circuit of Fig. 9.14.

The output and input voltages are related by the voltage-divider rule in the following manner:

$$\mathbf{V_o = \frac{RV_i}{R + X_C}}$$

where the boldface roman characters represent magnitude and angle of each quantity.

The magnitude of V_o is determined as follows:

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}}$$

For the special case where $X_C = R$,

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}} = \frac{RV_i}{\sqrt{R^2 + R^2}} = \frac{RV_i}{\sqrt{2R^2}} = \frac{RV_i}{\sqrt{2}R} = \frac{1}{\sqrt{2}}V_i$$

and

$$\boxed{|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707|_{X_C=R}} \tag{9.21}$$

the level of which is indicated on Fig. 9.19. In other words, at the frequency for which $X_C = R$, the output will be 70.7% of the input for the network of Fig. 9.14.

The frequency at which this occurs is determined from

$$X_C = \frac{1}{2\pi f_L C} = R$$

and

$$\boxed{f_L = \frac{1}{2\pi RC}} \tag{9.22}$$

In terms of logs,

$$G_v = 20 \log_{10} A_v = 20 \log_{10} \frac{1}{\sqrt{2}} = -3 \text{ dB}$$

whereas at $A_v = V_o/V_i = 1$ or $V_o = V_i$ (the maximum value),

$$G_v = 20 \log_{10} 1 = 20(0) = 0 \text{ dB}$$

In Fig. 9.8, we recognize that there is a 3-dB drop in gain from the midband level when $f = f_L$. In a moment, we will find that an RC network will determine the low-frequency cutoff for a BJT transistor and f_L will be determined by Eq. (9.22).

If the gain equation is written as

$$A_v = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j(1/\omega CR)} = \frac{1}{1 - j(1/2\pi fCR)}$$

we obtain, using the frequency defined above,

$$\boxed{A_v = \frac{1}{1 - j(f_L/f)}} \tag{9.23}$$

In the magnitude and phase form,

$$A_v = \frac{V_o}{V_i} = \underbrace{\frac{1}{\sqrt{1 + (f_L/f)^2}}}_{\text{magnitude of } A_v} \underbrace{\angle \tan^{-1}(f_L/f)}_{\substack{\text{phase} \sphericalangle \text{ by which} \\ V_o \text{ leads } V_i}} \tag{9.24}$$

For the magnitude when $f = f_L$,

$$|A_v| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \Rightarrow -3 \text{ dB}$$

In the logarithmic form, the gain in dB is

$$\boxed{A_{v(\text{dB})} = 20 \log_{10} \frac{1}{\sqrt{1 + (f_L/f)^2}}} \tag{9.25}$$

Expanding Eq. (9.25):

$$
\begin{aligned}
A_{v(\mathrm{dB})} &= -20\log_{10}\left[1+\left(\frac{f_L}{f}\right)^2\right]^{1/2}\\
&= -\left(\tfrac{1}{2}\right)(20)\log_{10}\left[1+\left(\frac{f_L}{f}\right)^2\right]\\
&= -10\log_{10}\left[1+\left(\frac{f_L}{f}\right)^2\right]
\end{aligned}
$$

For frequencies where $f \ll f_L$ or $(f_L/f)^2 \gg 1$, the equation above can be approximated by

$$A_{v(\mathrm{dB})} = -10\log_{10}\left(\frac{f_L}{f}\right)^2$$

and finally,

$$\boxed{A_{v(\mathrm{dB})} = -20\log_{10}\frac{f_L}{f}}_{f \ll f_L} \qquad \textbf{(9.26)}$$

Ignoring the condition $f \ll f_L$ for a moment, we find that a plot of Eq. (9.26) on a frequency log scale yields a result very useful for future decibel plots.

$$\text{At } f = f_L\!: \quad \frac{f_L}{f} = 1 \text{ and } -20\log_{10}1 = 0\text{ dB}$$

$$\text{At } f = \tfrac{1}{2}f_L\!: \quad \frac{f_L}{f} = 2 \text{ and } -20\log_{10}2 \cong -6\text{ dB}$$

$$\text{At } f = \tfrac{1}{4}f_L\!: \quad \frac{f_L}{f} = 4 \text{ and } -20\log_{10}4 \cong -12\text{ dB}$$

$$\text{At } f = \tfrac{1}{10}f_L\!: \quad \frac{f_L}{f} = 10 \text{ and } -20\log_{10}10 = -20\text{ dB}$$

A plot of these points is indicated in Fig. 9.20 from $0.1f_L$ to f_L with a dark blue straight line. In the same figure, a straight line is also drawn for the condition of 0 dB for $f \gg f_L$. As stated earlier, the straight-line segments (asymptotes) are only accurate for 0 dB when $f \gg f_L$ and the sloped line when $f_L \gg f$. We know, however, that when $f = f_L$, there is a 3-dB drop from the midband level. Employing this information in association with the straight-line segments permits a fairly accurate plot of the frequency response as indicated in the same figure.

The piecewise linear plot of the asymptotes and associated breakpoints is called a Bode plot of the magnitude versus frequency.

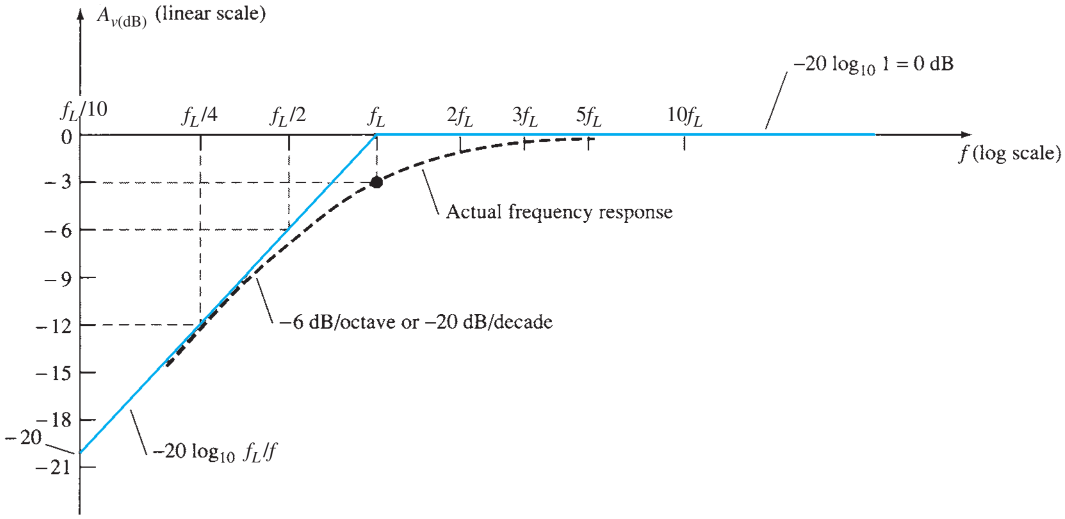


FIG. 9.20

Bode plot for the low-frequency region.

The approach was developed by Professor Hendrik Bode in the 1940s (Fig. 9.21).

The calculations above and the curve itself demonstrate clearly that:

A change in frequency by a factor of two, equivalent to one octave, results in a 6-dB change in the ratio, as shown by the change in gain from $f_L/2$ to f_L.

As noted by the change in gain from $f_L/2$ to f_L:

For a 10:1 change in frequency, equivalent to one decade, there is a 20-dB change in the ratio, as demonstrated between the frequencies of $f_L/10$ and f_L.

Therefore, a decibel plot can easily be obtained for a function having the format of Eq. (9.26). First, simply find f_L from the circuit parameters and then sketch two asymptotes—one along the 0-dB line and the other drawn through f_L sloped at 6 dB/octave or 20 dB/decade. Then, find the 3-dB point corresponding to f_L and sketch the curve.

The gain at any frequency can be determined from the frequency plot in the following manner:

$$A_{v(\text{dB})} = 20\log_{10}\frac{V_o}{V_i}$$

but

$$\frac{A_{v(\text{dB})}}{20} = \log_{10}\frac{V_o}{V_i}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = 10^{A_{v(\text{dB})}/20}} \qquad \textbf{(9.27)}$$

For example, if $A_{v(\text{dB})} = -3$ dB,

$$A_v = \frac{V_o}{V_i} = 10^{(-3/20)} = 10^{(-0.15)} \cong 0.707 \qquad \text{as expected}$$

The quantity $10^{-0.15}$ is determined using the 10^x function found on most scientific calculators.

The phase angle of θ is determined from

$$\boxed{\theta = \tan^{-1}\frac{f_L}{f}} \qquad \textbf{(9.28)}$$

from Eq. (9.24).

For frequencies $f \ll f_L$,

$$\theta = \tan^{-1}\frac{f_L}{f} \rightarrow 90^\circ$$

For instance, if $f_L = 100f$,

$$\theta = \tan^{-1}\frac{f_L}{f} = \tan^{-1}(100) = 89.4^\circ$$

For $f = f_L$,

$$\theta = \tan^{-1}\frac{f_L}{f} = \tan^{-1}1 = 45^\circ$$

For $f \gg f_L$,

$$\theta = \tan^{-1}\frac{f_L}{f} \rightarrow 0^\circ$$

For instance, if $f = 100f_L$,

$$\theta = \tan^{-1}\frac{f_L}{f} = \tan^{-1}0.01 = 0.573^\circ$$

A plot of $\theta = \tan^{-1}(f_L/f)$ is provided in Fig. 9.22. If we add the additional 180° phase shift introduced by an amplifier, the phase plot of Fig. 9.13 is obtained. The magnitude and phase response for an *RC* combination have now been established. In Section 9.7, each capacitor of importance in the low-frequency region will be redrawn in an *RC* format and the cutoff frequency for each determined to establish the low-frequency response for the BJT amplifier.

American (Madison, WI; Summit, NJ; Cambridge, MA)
(1905–1981)
V.P. at Bell Laboratories
Professor of Systems Engineering, Harvard University

In his early years at Bell Laboratories, Hendrik Bode was involved with *electric filter* and *equalizer design*. He then transferred to the Mathematics Research Group, where he specialized in research pertaining to electrical networks theory and its application to long distance communication facilities. In 1948 he was awarded the Presidential Certificate of Merit for his work in electronic fire control devices. In addition to the publication of the book *Network Analysis and Feedback Amplifier Design* in 1945, which is considered a classic in its field, he has been granted 25 patents in electrical engineering and systems design. Upon retirement, Bode was elected Gordon McKay Professor of Systems Engineering at Harvard University. He was a fellow of the IEEE and American Academy of Arts and Sciences.

FIG. 9.21
Hendrik Wade Bode.
(Courtesy of AT&T Archives and History Center.)

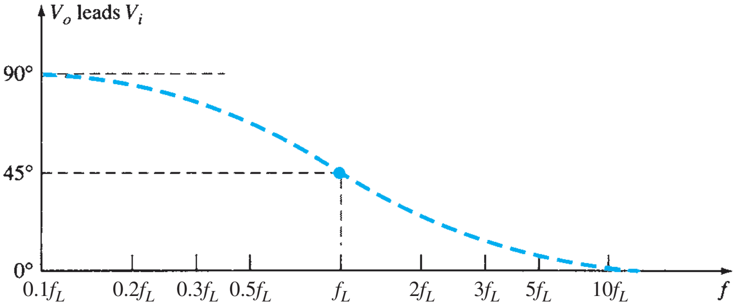


FIG. 9.22
Phase response for the RC circuit of Fig. 9.14.

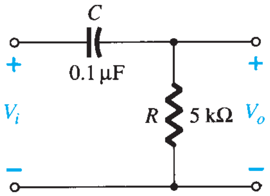


FIG. 9.23
Example 9.10.

EXAMPLE 9.10 For the network of Fig. 9.23:

a. Determine the break frequency.
b. Sketch the asymptotes and locate the −3-dB point.
c. Sketch the frequency response curve.
d. Find the gain at $A_{v(\text{dB})} = -6$ dB.

Solution:

a. $$f_L = \frac{1}{2\pi RC} = \frac{1}{(6.28)(5 \times 10^3\ \Omega)(0.1 \times 10^{-6}\text{ F})}$$

$$\cong \mathbf{318.5\ Hz}$$

b. and c. See Fig. 9.24.

d. Eq. (9.27): $$A_v = \frac{V_o}{V_i} = 10^{A_{v(\text{dB})}/20}$$

$$= 10^{(-6/20)} = 10^{-0.3} = 0.501$$

and $V_o = 0.501\ V_i$ or approximately 50% of V_i.

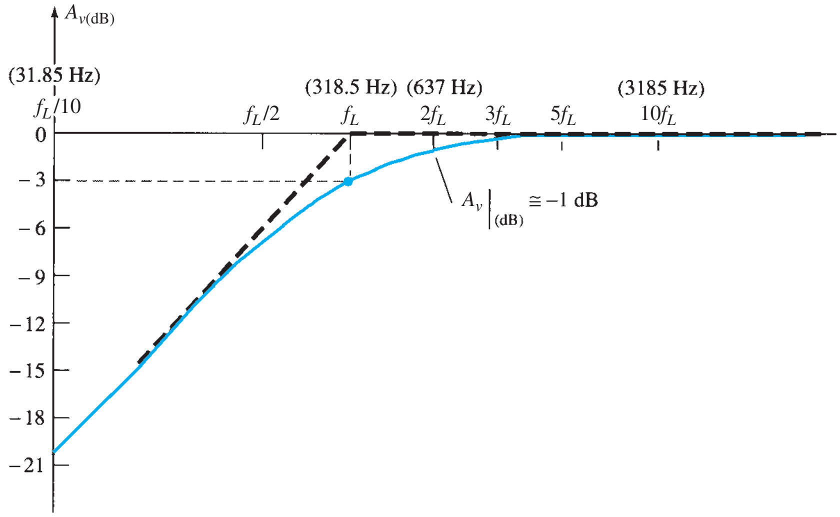


FIG. 9.24
Frequency response for the RC circuit of Fig. 9.23.

9.7 LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

The analysis of this section will employ the loaded (R_L) voltage-divider BJT bias configuration introduced earlier in Section 9.6. For the network of Fig. 9.25, the capacitors C_s, C_C, and C_E will determine the low-frequency response. We will now examine the impact of each independently in the order listed.

C_s Because C_s is normally connected between the applied source and the active device, the general form of the RC configuration is established by the network of Fig. 9.26, matching that of Fig. 9.16 with $R_i = R_1 \| R_2 \| \beta r_e$.

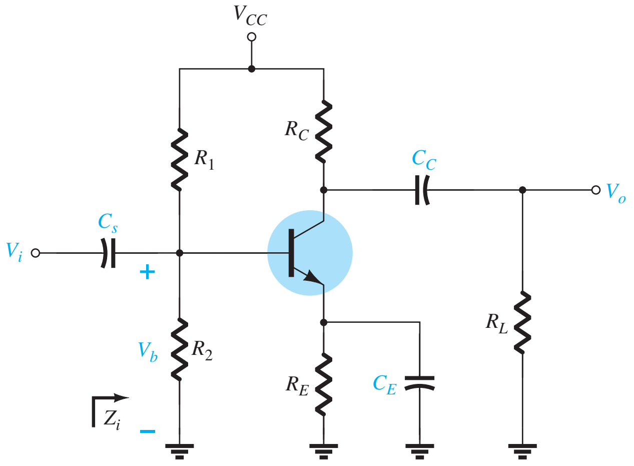


FIG. 9.25
Loaded BJT amplifier with capacitors that affect the low-frequency response.

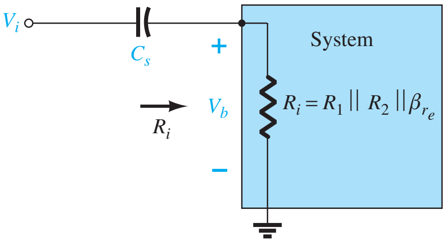


FIG. 9.26
Determining the effect of C_s on the low-frequency response.

Applying the voltage-divider rule:

$$\boxed{\mathbf{V}_b = \frac{R_i \mathbf{V}_i}{R_i - jX_{C_s}}} \tag{9.29}$$

The cutoff frequency defined by C_s can be determined by manipulating the above equation into a standard form or simply using the results of Section 9.6. As a verification of the results of Section 9.6 the manipulation process is defined in detail below. For future RC networks, the results of Section 9.6 will simply be applied.

Rewriting Eq. (9.29):

$$\frac{\mathbf{V}_b}{\mathbf{V}_i} = \frac{R_i}{R_i - jX_{C_s}} = \frac{1}{1 - j\dfrac{X_{C_s}}{R_i}}$$

The factor

$$\frac{X_{C_s}}{R_i} = \left(\frac{1}{2\pi f C_s}\right)\left(\frac{1}{R_i}\right) = \frac{1}{2\pi f R_i C_s}$$

Defining

$$\boxed{f_{L_s} = \frac{1}{2\pi R_i C_s}} \tag{9.30}$$

we have

$$\boxed{\mathbf{A}_v = \frac{\mathbf{V}_b}{\mathbf{V}_i} = \frac{1}{1 - j(f_{L_s}/f)}} \tag{9.31}$$

At f_{L_s} the voltage V_b will be 70.7% of the mid band value assuming C_s is the only capacitive element controlling the low-frequency response.

For the network of Fig. 9.25, when we analyze the effects of C_s we must make the assumption that C_E and C_C are performing their designed function or the analysis becomes too unwieldy, that is, that the magnitudes of the reactances of C_E and C_C permit employing a short-circuit equivalent in comparison to the magnitude of the other series impedances.

C_C Because the coupling capacitor is normally connected between the output of the active device and the applied load, the *RC* configuration that determines the low-cutoff frequency due to C_C appears in Fig. 9.27. The total series resistance is now $R_o + R_L$, and the cutoff frequency due to C_C is determined by

$$\boxed{f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}} \tag{9.32}$$

Ignoring the effects of C_s and C_E, we find that the output voltage V_o will be 70.7% of its midband value at f_{L_C}. For the network of Fig. 9.25, the ac equivalent network for the output section with $V_i = 0$ V appears in Fig. 9.28. The resulting value for R_o in Eq. (9.32) is then simply

$$\boxed{R_o = R_C \| r_o} \tag{9.33}$$

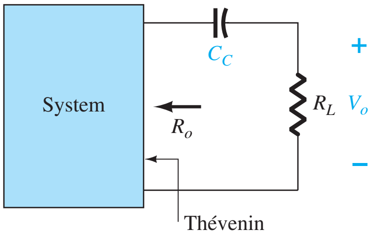


FIG. 9.27
Determining the effect of C_C on the low-frequency response.

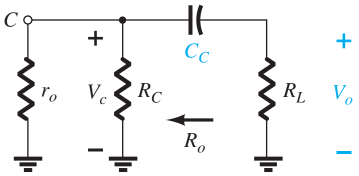


FIG. 9.28
Localized ac equivalent for C_C with $V_i = 0$ V.

C_E To determine f_{L_E}, the network "seen" by C_E must be determined as shown in Fig. 9.29. Once the level of R_e is established, the cutoff frequency due to C_E can be determined using the following equation:

$$\boxed{f_{L_E} = \frac{1}{2\pi R_e C_E}} \tag{9.34}$$

For the network of Fig. 9.25, the ac equivalent as "seen" by C_E appears in Fig. 9.30 as derived from Fig. 5.38. The value of R_e is therefore determined by

$$\boxed{R_e = R_E \| \left(\frac{R_1 \| R_2}{\beta} + r_e\right)} \tag{9.35}$$

The effect of C_E on the gain is best described in a quantitative manner by recalling that the gain for the configuration of Fig. 9.31 is given by

$$A_v = \frac{-R_C}{r_e + R_E}$$

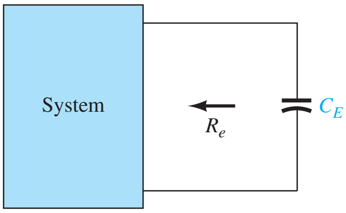


FIG. 9.29
Determining the effect of C_E on the low-frequency response.

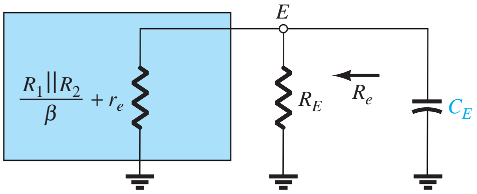


FIG. 9.30
Localized ac equivalent of C_E.

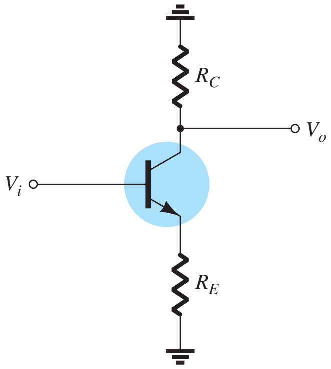


FIG. 9.31
Network employed to describe the effect of C_E on the amplifier gain.

The maximum gain is obviously available where R_E is 0 Ω. At low frequencies, with the bypass capacitor C_E in its "open-circuit" equivalent state, all of R_E appears in the gain equation above, resulting in the minimum gain. As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until the resistor R_E is effectively "shorted out" by C_E. The result is a maximum or midband gain determined by $A_v = -R_C/r_e$. At f_{L_E} the gain will be 3 dB below the midband value determined with R_E "shorted out."

Before continuing, keep in mind that C_s, C_C, and C_E will affect only the low-frequency response. At the midband frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain $A_v = V_o/V_i$ in a similar frequency range, the highest low-frequency cutoff determined by C_s, C_C, or C_E will have the greatest impact because it will be the last encountered before the midband level. If the frequencies are relatively far apart, the highest cutoff frequency will essentially determine the lower cutoff frequency for the entire system. If there are two or more "high" cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low-cutoff frequency. However, if the cutoff frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy—a fact that will be demonstrated by the printouts to appear in the following example.

EXAMPLE 9.11 Determine the cutoff frequencies for the network of Fig. 9.25 using the following parameters:

$C_s = 10\ \mu\text{F}, \qquad C_E = 20\ \mu\text{F}, \qquad C_C = 1\ \mu\text{F}$

$R_1 = 40\ \text{k}\Omega, \qquad R_2 = 10\ \text{k}\Omega, \qquad R_E = 2\ \text{k}\Omega, \qquad R_C = 4\ \text{k}\Omega,$

$R_L = 2.2\ \text{k}\Omega$

$\beta = 100, \qquad r_o = \infty\,\Omega, \qquad V_{CC} = 20\ \text{V}$

Solution: To determine r_e for dc conditions, we first apply the test equation:

$$\beta R_E = (100)(2\ \text{k}\Omega) = 200\ \text{k}\Omega \gg 10R_2 = 100\ \text{k}\Omega$$

Since satisfied the dc base voltage is determined by

$$V_B \cong \frac{R_2V_{CC}}{R_2 + R_1} = \frac{10\ \text{k}\Omega(20\ \text{V})}{10\ \text{k}\Omega + 40\ \text{k}\Omega} = \frac{200\ \text{V}}{50} = 4\ \text{V}$$

with
$$I_E = \frac{V_E}{R_E} = \frac{4\ \text{V} - 0.7\ \text{V}}{2\ \text{k}\Omega} = \frac{3.3\ \text{V}}{2\ \text{k}\Omega} = 1.65\ \text{mA}$$

so that
$$r_e = \frac{26\ \text{mV}}{1.65\ \text{mA}} \cong \mathbf{15.76\ \Omega}$$

and
$$\beta r_e = 100(15.76\ \Omega) = 1576\ \Omega = \mathbf{1.576\ k\Omega}$$

Midband Gain
$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} = -\frac{(4\ \text{k}\Omega)\|(2.2\ \text{k}\Omega)}{15.76\ \Omega} \cong -90$$

C_s
$$R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$$

$$f_{L_S} = \frac{1}{2\pi R_i C_s} = \frac{1}{(6.28)(1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$f_{L_S} \cong \mathbf{12.06\ Hz}$$

C_C
$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \quad \text{with} \quad R_o = R_C \| r_o \cong R_C$$

$$= \frac{1}{(6.28)(4\ \text{k}\Omega + 2.2\ \text{k}\Omega)(1\ \mu\text{F})}$$

$$\cong \mathbf{25.68\ Hz}$$

C_E

$$\begin{aligned}R_e &= R_E \| \left(\frac{R_1 \| R_2}{\beta} + r_e\right)\\ &= 2\text{ k}\Omega \| \left(\frac{40\text{ k}\Omega \| 10\text{ k}\Omega}{100} + 15.76\ \Omega\right)\\ &= 2\text{ k}\Omega \| \left(\frac{8\text{ k}\Omega}{100} + 15.76\ \Omega\right)\\ &= 2\text{ k}\Omega \| (80\ \Omega + 15.76\ \Omega)\\ &= 2\text{ k}\Omega \| 95.76\ \Omega\\ &= 91.38\ \Omega\end{aligned}$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(91.38\ \Omega)(20\ \mu\text{F})} = \frac{10^6}{11{,}477.73} \cong \mathbf{87.13\ Hz}$$

Since $f_{L_E} \gg f_{L_C}$ or f_{L_S} the bypass capacitor C_E is determining the lower cutoff frequency of the amplifier.

9.8 IMPACT OF R_S ON THE BJT LOW-FREQUENCY RESPONSE

In this section we will investigate the impact of the source resistance on the various cutoff frequencies. In Fig. 9.32 a signal source and associated resistance have been added to the configuration of Fig. 9.25. The gain will now be between the output voltage V_o and the signal source V_s.

C_s The equivalent circuit at the input is now as shown in Fig. 9.33, with R_i continuing to be equal to $R_1 \| R_2 \| \beta r_e$.

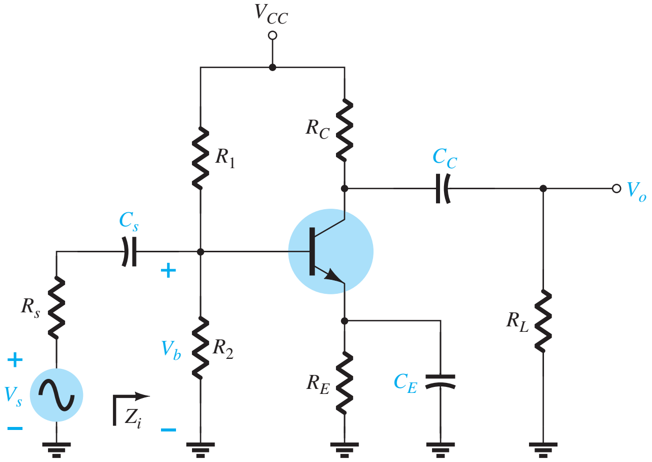


FIG. 9.32
Determining the effect of R_s on the low-frequency response of a BJT amplifier.

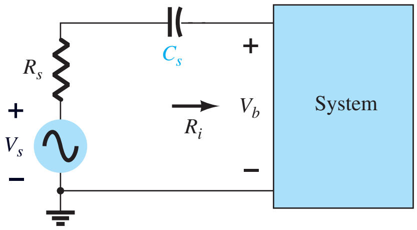


FIG. 9.33
Determining the effect of C_s on the low-frequency response.

Using the results of the last section it would appear we could simply find the total sum of the series resistors and plug it into Eq. (9.22). Doing so would result in the following equation for the cutoff frequency:

$$\boxed{f_{L_s} = \frac{1}{2\pi(R_i + R_s)C_s}} \qquad \mathbf{(9.36)}$$

However, it would be best to validate our assumption by first applying the voltage-divider rule in the following manner:

$$\boxed{\mathbf{V}_b = \frac{R_i\mathbf{V}_s}{R_s + R_i - jX_{C_s}}} \qquad \textbf{(9.37)}$$

The cutoff frequency defined by C_s can be determined by manipulating the above equation into a standard form, as demonstrated below.

Rewriting Eq. (9.37):

$$\frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{R_i}{R_s + R_i - jX_{C_s}} = \frac{1}{1 + \dfrac{R_s}{R_i} - j\dfrac{X_{C_s}}{R_i}}$$

$$= \frac{1}{\left(1 + \dfrac{R_s}{R_i}\right)\left[1 - j\dfrac{X_{C_s}}{R_i}\left(\dfrac{1}{1 + \dfrac{R_s}{R_i}}\right)\right]} = \frac{1}{\left(1 + \dfrac{R_s}{R_i}\right)\left(1 - j\dfrac{X_{C_s}}{R_i + R_s}\right)}$$

The factor

$$\frac{X_{C_s}}{R_i + R_s} = \left(\frac{1}{2\pi f C_s}\right)\left(\frac{1}{R_i + R_s}\right) = \frac{1}{2\pi f(R_i + R_s)C_s}$$

Defining

$$f_{L_s} = \frac{1}{2\pi(R_i + R_s)C_s}$$

we have

$$\frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{1}{\left(\dfrac{1}{1 + \frac{R_s}{R_i}}\right)\left(1 - \dfrac{1}{1 - jf_{L_{s/f}}}\right)}$$

and finally

$$\mathbf{A}_v = \frac{\mathbf{V}_b}{\mathbf{V}_s} = \left[\frac{R_i}{R_i + R_s}\right]\left[\frac{1}{1 - j(f_{L_s}/f)}\right]$$

For the midband frequencies, the input network will appear as shown in Fig. 9.34.

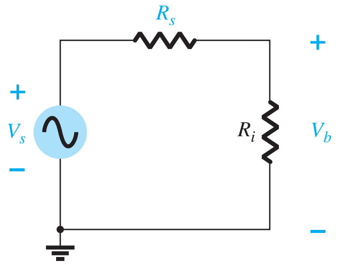


FIG. 9.34
Determining the effect of R_s on the gain A_{v_s}.

so that

$$\boxed{A_{v_{\text{mid}}} = \frac{\mathbf{V}_b}{\mathbf{V}_s} = \frac{R_i}{R_i + R_s}} \qquad \textbf{(9.38)}$$

and

$$\frac{A_v}{A_{v_{\text{mid}}}} = \frac{1}{1 - j(f_{L_s}/f)}$$

Noting the similarities with Eq. (9.23) the cutoff frequency is defined by f_{L_s} above and

$$\boxed{f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s}} \qquad \textbf{(9.39)}$$

as assumed in the derivation of Eq. (9.36).

At f_{L_s}, the voltage V_o will be 70.7% of the midband value determined by Eq. (9.38), assuming the C_s is the only capacitive element controlling the low-frequency response.

C_C Reviewing the analysis of Section 9.7 for the coupling capacitor C_C, we find that the derivation of the equation for the cutoff frequency remains the same. That is,

$$\boxed{f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}} \qquad \textbf{(9.40)}$$

C_E Again, following the analysis of Section 9.7 for the same capacitor, we find that R_s will affect the resistance level substituted into the cutoff equation so that

$$\boxed{f_{L_E} = \frac{1}{2\pi R_e C_E}} \qquad \textbf{(9.41)}$$

with
$$R_e = R_E \| \left(\frac{R'_s}{\beta} + r_e\right) \text{ and } R'_s = R_s \| R_1 \| R_2$$

In total, therefore, the introduction of the resistance R_s reduced the cutoff frequency defined by C_s and raised the cutoff frequency defined by C_E. The cutoff frequency defined by C_C remained the same. It is also important to note that the gain can be severely affected by the loss in signal voltage across the source resistance. This last factor will be demonstrated in the next example.

EXAMPLE 9.12

a. Repeat the analysis of Example 9.11 but with a source resistance R_s of 1 kΩ. The gain of interest will now be V_o/V_s rather than V_o/V_i. Compare results.
b. Sketch the frequency response using a Bode plot.
c. Verify the results using PSpice.

Solution: a. The dc conditions remain the same:

$$r_e = 15.76\ \Omega \text{ and } \beta r_e = 1.576\ \text{k}\Omega$$

Midband Gain $$A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} \cong -90 \text{ as before}$$

The input impedance is given by

$$\begin{aligned} Z_i = R_i &= R_1 \| R_2 \| \beta r_e \\ &= 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \\ &\cong 1.32\ \text{k}\Omega \end{aligned}$$

and from Fig. 9.35,

$$V_b = \frac{R_i V_s}{R_i + R_s}$$

or
$$\frac{V_b}{V_s} = \frac{R_i}{R_i + R_s} = \frac{1.32\ \text{k}\Omega}{1.32\ \text{k}\Omega + 1\ \text{k}\Omega} = 0.569$$

so that
$$\begin{aligned} A_{v_s} = \frac{V_o}{V_s} &= \frac{V_o}{V_i} \cdot \frac{V_b}{V_s} = (-90)(0.569) \\ &= \mathbf{-51.21} \end{aligned}$$

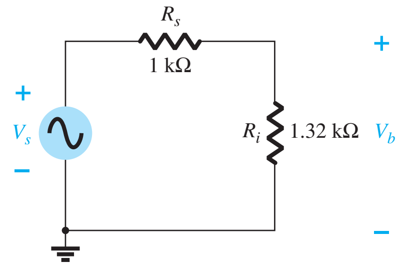


FIG. 9.35
Determining the effect of R_s on the gain A_{v_s}.

C_s
$$R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$$
$$f_{L_S} = \frac{1}{2\pi(R_s + R_i)C_s} = \frac{1}{(6.28)(1\ \text{k}\Omega + 1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$
$$f_{L_S} \cong 6.86\ \text{Hz vs. } 12.06\ \text{Hz without } R_s$$

C_C
$$\begin{aligned} f_{L_C} &= \frac{1}{2\pi(R_C + R_L)C_C} \\ &= \frac{1}{(6.28)(4\ \text{k}\Omega + 2.2\ \text{k}\Omega)(1\ \mu\text{F})} \\ &\cong \mathbf{25.68\ Hz} \text{ as before} \end{aligned}$$

C_E
$$R'_s = R_s \| R_1 \| R_2 = 1\ \text{k}\Omega \| 40\ \text{k}\Omega \| 10\ \text{k}\Omega \cong 0.889\ \text{k}\Omega$$
$$\begin{aligned} R_e = R_E \left\| \left(\frac{R'_s}{\beta} + r_e\right)\right. &= 2\ \text{k}\Omega \left\| \left(\frac{0.889\ \text{k}\Omega}{100} + 15.76\ \Omega\right)\right. \\ &= 2\ \text{k}\Omega \| (8.89\ \Omega + 15.76\ \Omega) = 2\ \text{k}\Omega \| 24.65\ \Omega \cong 24.35\ \Omega \end{aligned}$$
$$\begin{aligned} f_{L_E} &= \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(24.35\ \Omega)(20\ \mu\text{F})} = \frac{10^6}{3058.36} \\ &\cong \mathbf{327\ Hz} \text{ vs. } 87.13\ \text{Hz without } R_s. \end{aligned}$$

The net result is a severe reduction in overall gain (almost 43%) but a corresponding reduction in the lower cutoff frequency. Recall that the highest of the low cutoff frequencies will determine the overall low cutoff frequency for the amplifier. The results point out that the internal series resistance can have a very strong impact on the midband gain, but on the other side of the coin it can improve the overall bandwidth. In this case it is clear that the loss in gain far outweighs any gain in bandwidth.

b. It was mentioned earlier that dB plots are usually normalized by dividing the voltage gain A_v by the magnitude of the midband gain. For Fig. 9.32, the magnitude of the midband gain is 51.21, and naturally the ratio $|A_v/A_{v_{\text{mid}}}|$ will be 1 in the midband region. The result is a 0-dB asymptote in the midband region as shown in Fig. 9.36. Defining f_{L_E} as our lower cutoff frequency f_L, we can draw an asymptote at -6 dB/octave as shown in Fig. 9.36 to form the Bode plot and our envelope for the actual response. At f_1, the actual curve is -3 dB down from the midband level as defined by the $0.707A_{v_{\text{mid}}}$ level, permitting a sketch of the actual frequency response curve as shown in Fig. 9.36. A -6-dB/octave asymptote was drawn at each frequency defined in the analysis above to demonstrate clearly that it is f_{L_E} for this network that will determine the -3-dB point. It is not until about -24 dB that f_{L_C} begins to affect the shape of the envelope. The magnitude plot shows that the slope of the resultant asymptote is the sum of the asymptotes having the same sloping direction in the same frequency interval. Note in Fig. 9.36 that the slope has dropped to -12 dB/octave for frequencies less than f_{L_C} and could drop to -18 dB/octave if the three defined cutoff frequencies of Fig. 9.36 were closer together. Using Eq. (9.9), the cutoff frequency for the low-frequency region is about 325 Hz.

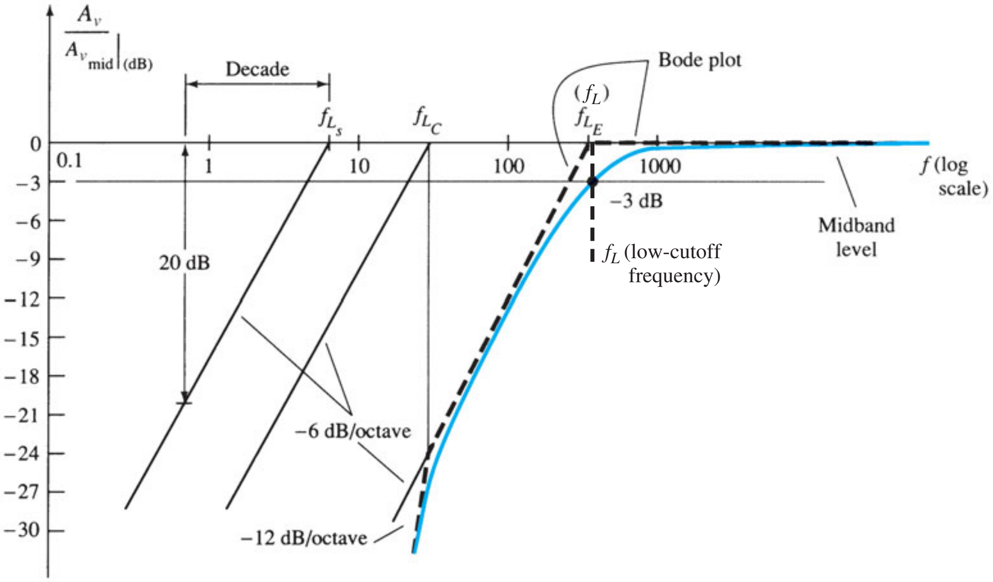


FIG. 9.36

Low-frequency plot for the network of Example 9.12.

c. The PSpice solution can be found in Section 9.15.

Keep in mind as we proceed to the next section that the analysis of this section is not limited to the networks of Figs. 9.25 and 9.32. For any transistor configuration it is simply necessary to isolate each *RC* combination formed by a capacitive element and determine the break frequencies. The resulting frequencies will then determine whether there is a strong interaction between capacitive elements in determining the overall response and which element will have the greatest effect on establishing the lower cutoff frequency. In fact, the analysis of the next section will parallel this section as we determine the low-cutoff frequencies for the FET amplifier.

9.9 LOW-FREQUENCY RESPONSE—FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier of Section 9.7. There are again three capacitors of primary concern as appearing in the network of Fig. 9.37: C_G, C_C, and C_S. Although Fig. 9.37

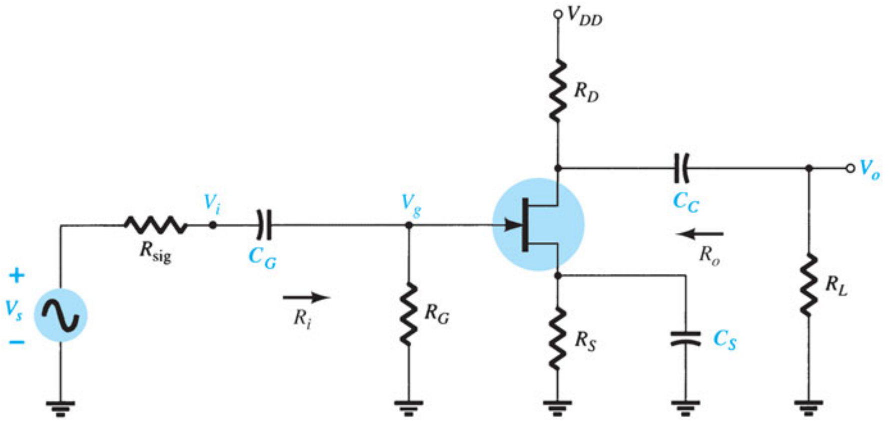


FIG. 9.37
Capacitive elements that affect the low-frequency response of a JFET amplifier.

will be used to establish the fundamental equations, the procedure and conclusions can be applied to any FET configuration. Most of the equations for impedance levels can be found in Table 8.2.

C_G For the coupling capacitor between the source and the active device, the ac equivalent network is as shown in Fig. 9.38. The cutoff frequency determined by C_G is

$$\boxed{f_{L_G} = \frac{1}{2\pi(R_{sig} + R_i)C_G}} \tag{9.42}$$

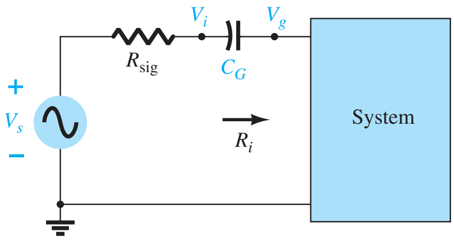


FIG. 9.38
Determining the effect of C_G on the low-frequency response.

which is an exact match of Eq. (9.39). For the network of Fig. 9.37,

$$\boxed{R_i = R_G} \tag{9.43}$$

Typically, $R_G \gg R_{sig}$, and the lower cutoff frequency is determined primarily by R_G and C_G. The fact that R_G is so large permits a relatively low level of C_G while maintaining a low cutoff frequency level for f_{L_G}.

C_C For the coupling capacitor between the active device and the load the network of Fig. 9.39 results, which is also an exact match of Fig. 9.27. The resulting cutoff frequency is

$$\boxed{f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}} \tag{9.44}$$

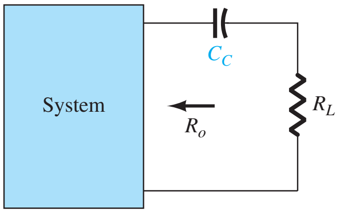


FIG. 9.39
Determining the effect of C_C on the low-frequency response.

For the network of Fig. 9.37,

$$\boxed{R_o = R_D \| r_d} \tag{9.45}$$

C_S For the source capacitor C_S, the resistance level of importance is defined by Fig. 9.40. The cutoff frequency is defined by

$$\boxed{f_{L_S} = \frac{1}{2\pi R_{eq}C_S}} \tag{9.46}$$

For Fig. 9.37, the resulting value of R_{eq} is

$$\boxed{R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)}} \tag{9.47}$$

which for $r_d \cong \infty\,\Omega$ becomes

$$\boxed{R_{eq} = R_S \| \frac{1}{g_m}}_{r_d \cong \infty\Omega} \tag{9.48}$$

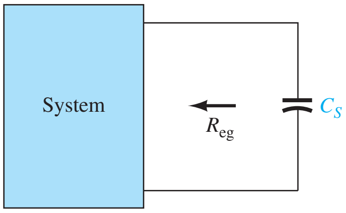


FIG. 9.40
Determining the effect of C_S on the low-frequency response.

EXAMPLE 9.13

a. Determine the lower cutoff frequency for the network of Fig. 9.37 using the following parameters:

$$C_G = 0.01\,\mu\text{F}, \quad C_C = 0.5\,\mu\text{F}, \quad C_S = 2\,\mu\text{F}$$
$$R_{sig} = 10\,\text{k}\Omega, \quad R_G = 1\,\text{M}\Omega, \quad R_D = 4.7\,\text{k}\Omega, \quad R_S = 1\,\text{k}\Omega, \quad R_L = 2.2\,\text{k}\Omega$$
$$I_{DSS} = 8\,\text{mA}, \quad V_P = -4\,\text{V}, \quad r_d = \infty\,\Omega, \quad V_{DD} = 20\,\text{V}$$

b. Sketch the frequency response using a Bode plot.
c. Verify the results of part (b) using PSpice.
d. Perform a complete analysis of the network of Fig. 9.37 using Multisim.

Solution:

a. DC analysis: Plotting the transfer curve of $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ and superimposing the curve defined by $V_{GS} = -I_D R_S$ results in an intersection at $V_{GS_Q} = -2$ V and $I_{D_Q} = 2$ mA. In addition,

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\,\text{mA})}{4\,\text{V}} = 4\,\text{mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\,\text{mS}\left(1 - \frac{-2\,\text{V}}{-4\,\text{V}}\right) = 2\,\text{mS}$$

C_G Eq. (9.36): $f_{L_G} = \dfrac{1}{2\pi(R_{sig} + R_i)C_G} = \dfrac{1}{2\pi(10\,\text{k}\Omega + 1\,\text{M}\Omega)(0.01\,\mu\text{F})} \cong \mathbf{15.8\,Hz}$

C_C Eq. (9.38): $f_{L_C} = \dfrac{1}{2\pi(R_o + R_L)C_C} = \dfrac{1}{2\pi(4.7\,\text{k}\Omega + 2.2\,\text{k}\Omega)(0.5\,\mu\text{F})} \cong \mathbf{46.13\,Hz}$

C_S $R_{eq} = R_S \| \dfrac{1}{g_m} = 1\,\text{k}\Omega \| \dfrac{1}{2\,\text{mS}} = 1\,\text{k}\Omega \| 0.5\,\text{k}\Omega = 333.33\,\Omega$

Eq. (9.40): $f_{L_S} = \dfrac{1}{2\pi R_{eq}C_S} = \dfrac{1}{2\pi(333.33\,\Omega)(2\,\mu\text{F})} = \mathbf{238.73\,Hz}$

Because f_{L_s} is the largest of the three cutoff frequencies, it defines the low-cutoff frequency for the network of Fig. 9.37.

b. The midband gain of the system is determined by

$$A_{v_{mid}} = \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2\,\text{mS})(4.7\,\text{k}\Omega \| 2.2\,\text{k}\Omega)$$
$$= -(2\,\text{mS})(1.499\,\text{k}\Omega)$$
$$\cong \mathbf{-3}$$

Using the midband gain to normalize the response for the network of Fig. 9.37 results in the frequency plot of Fig. 9.41.

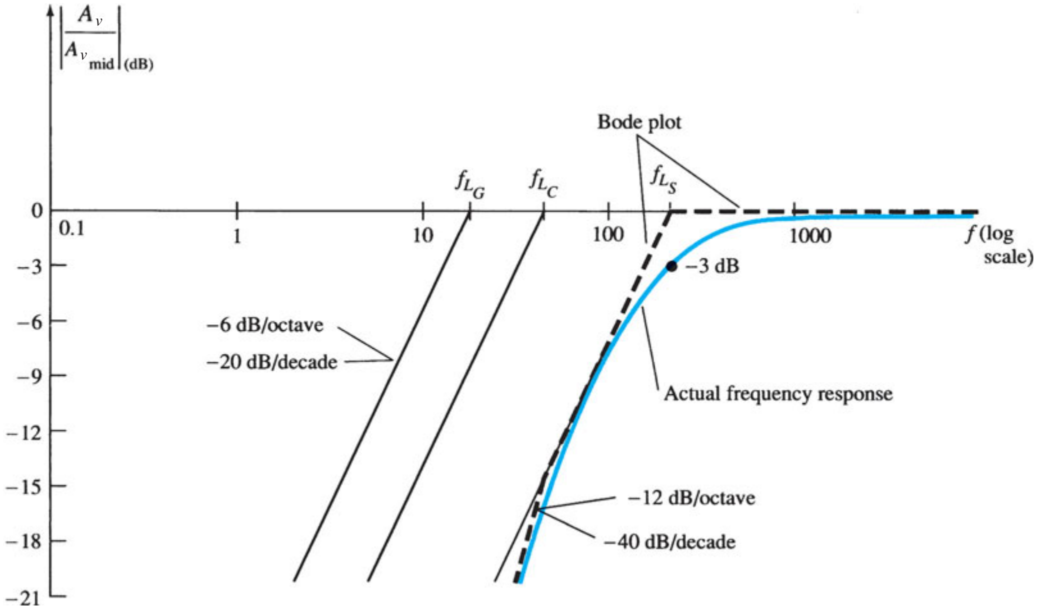


FIG. 9.41
Low-frequency response for the JFET configuration of Example 9.13.

c. and d. The computer solutions can be found in Section 9.15.

9.10 MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the interelectrode (between-terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response are all replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of 180° between input and output, resulting in a negative value for A_v), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier. In Fig. 9.42, this “feedback” capacitance is defined by C_f.

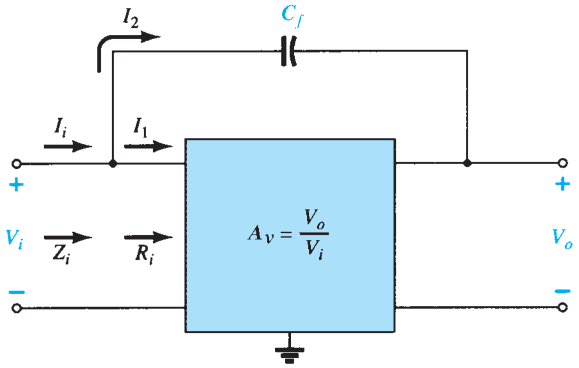


FIG. 9.42
Network employed in the derivation of an equation for the Miller input capacitance.

Applying Kirchhoff's current law gives

$$I_i = I_1 + I_2$$

Using Ohm's law yields

$$I_i = \frac{V_i}{Z_i}, \quad I_1 = \frac{V_i}{R_i}$$

and

$$I_2 = \frac{V_i - V_o}{X_{C_f}} = \frac{V_i - A_v V_i}{X_{C_f}} = \frac{(1 - A_v)V_i}{X_{C_f}}$$

Substituting, we obtain

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_v)V_i}{X_{C_f}}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_f}/(1 - A_v)}$$

but

$$\frac{X_{C_f}}{1 - A_v} = \frac{1}{\underbrace{\omega(1 - A_v)C_f}_{C_M}} = X_{C_M}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$

establishing the equivalent network of Fig. 9.43. The result is an equivalent input impedance to the amplifier of Fig. 9.44 that includes the same R_i that we dealt with in previous chapters, with the addition of a feedback capacitor magnified by the gain of the amplifier. Any interelectrode capacitance at the input terminals to the amplifier will simply be added in parallel with the elements of Fig. 9.43.

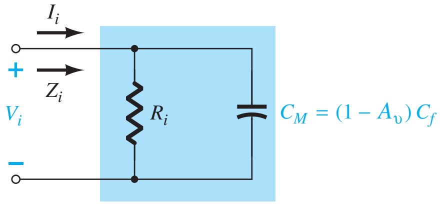


FIG. 9.43

Demonstrating the effect of the Miller effect capacitance.

In general, therefore, the Miller effect input capacitance is defined by

$$\boxed{C_{M_i} = (1 - A_v)C_f} \qquad \textbf{(9.49)}$$

This shows us that:

For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode (parasitic) capacitance between the input and output terminals of the active device.

The dilemma of an equation such as Eq. (9.49) is that at high frequencies the gain A_v will be a function of the level of C_{M_i}. However, because the maximum gain is the midband value, using the midband value will result in the highest level of C_{M_i} and the worst-case scenario. In general, therefore, the midband value is typically employed for A_v in Eq. (9.49).

The reason for the constraint that the amplifier be of the inverting variety is now more apparent when one examines Eq. (9.49). A positive value for A_v would result in a negative capacitance (for $A_v > 1$).

The Miller effect will also increase the level of output capacitance, which must also be considered when the high-frequency cutoff is determined. In Fig. 9.44, the parameters of

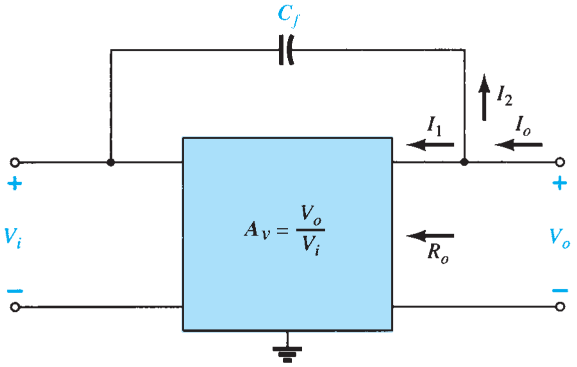


FIG. 9.44
Network employed in the derivation of an equation for the Miller output capacitance.

importance to determine the output Miller effect are in place. Applying Kirchhoff's current law results in

$$I_o = I_1 + I_2$$

with $$I_1 = \frac{V_o}{R_o} \quad \text{and} \quad I_2 = \frac{V_o - V_i}{X_{C_f}}$$

The resistance R_o is usually sufficiently large to permit ignoring the first term of the equation compared to the second term and assuming that

$$I_o \cong \frac{V_o - V_i}{X_{C_f}}$$

Substituting $V_i = V_o/A_v$ from $A_v = V_o/V_i$ results in

$$I_o = \frac{V_o - V_o/A_v}{X_{C_f}} = \frac{V_o(1 - 1/A_v)}{X_{C_f}}$$

and $$\frac{I_o}{V_o} = \frac{1 - 1/A_v}{X_{C_f}}$$

or $$\frac{V_o}{I_o} = \frac{X_{C_f}}{1 - 1/A_v} = \frac{1}{\omega C_f(1 - 1/A_v)} = \frac{1}{\omega C_{M_o}}$$

resulting in the following equation for the Miller output capacitance:

$$\boxed{C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_f} \tag{9.50}$$

For the usual situation where $A_v \gg 1$, Eq. (9.50) reduces to

$$\boxed{C_{M_o} \cong C_f}\Big|_{|A_v| \gg 1} \tag{9.51}$$

Examples of the use of Eq. (9.50) appear in the next two sections as we investigate the high-frequency responses of BJT and FET amplifiers.

For noninverting amplifiers such as the common-base and emitter-follower configurations, the Miller effect capacitance is not a contributing concern for high-frequency applications.

9.11 HIGH-FREQUENCY RESPONSE—BJT AMPLIFIER

At the high-frequency end, there are two factors that define the −3-dB cutoff point: the network capacitance (parasitic and introduced) and the frequency dependence of $h_{fe}(\beta)$.

Network Parameters

In the high-frequency region, the *RC* network of concern has the configuration appearing in Fig. 9.45. At increasing frequencies, the reactance X_C will decrease in magnitude, resulting in a shorting effect across the output and a decrease in gain. The derivation leading to the corner frequency for this R_C configuration follows along similar lines to that encountered for the low-frequency region. The most significant difference is in the following general form of A_v:

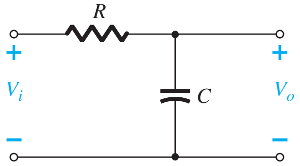


FIG. 9.45
RC combination that will define a high-cutoff frequency.

$$\boxed{A_v = \frac{1}{1 + j(f/f_H)}} \tag{9.52}$$

This results in a magnitude plot such as shown in Fig. 9.46 that drops off at 6 dB/octave with increasing frequency. Note that f_H is in the denominator of the frequency ratio rather than the numerator as occurred for f_L in Eq. (9.23).

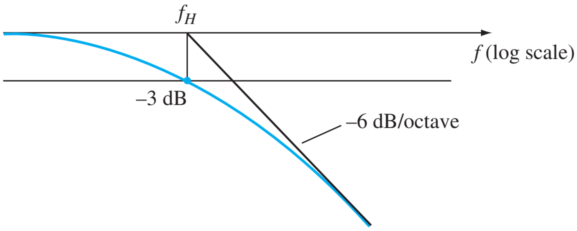


FIG. 9.46
Asymptotic plot as defined by Eq. (9.52).

In Fig. 9.47, the various parasitic capacitances (C_{be}, C_{bc}, C_{ce}) of the transistor are included with the wiring capacitances (C_{W_i}, C_{W_o}) introduced during construction. The high-frequency equivalent model for the network of Fig. 9.47 appears in Fig. 9.48. Note the absence of the capacitors C_s, C_C, and C_E, which are all assumed to be in the short-circuit state at these frequencies. The capacitance C_i includes the input wiring capacitance C_{W_i}, the transition capacitance C_{be}, and the Miller capacitance C_{M_i}. The capacitance C_o includes the output wiring capacitance C_{W_o}, the parasitic capacitance C_{ce}, and the output Miller capacitance C_{M_o}. In general, the capacitance C_{be} is the largest of the parasitic capacitances, with C_{ce} the smallest. In fact, most specification sheets simply provide the levels of C_{be} and C_{bc} and do not include C_{ce} unless it will affect the response of a particular type of transistor in a specific area of application.

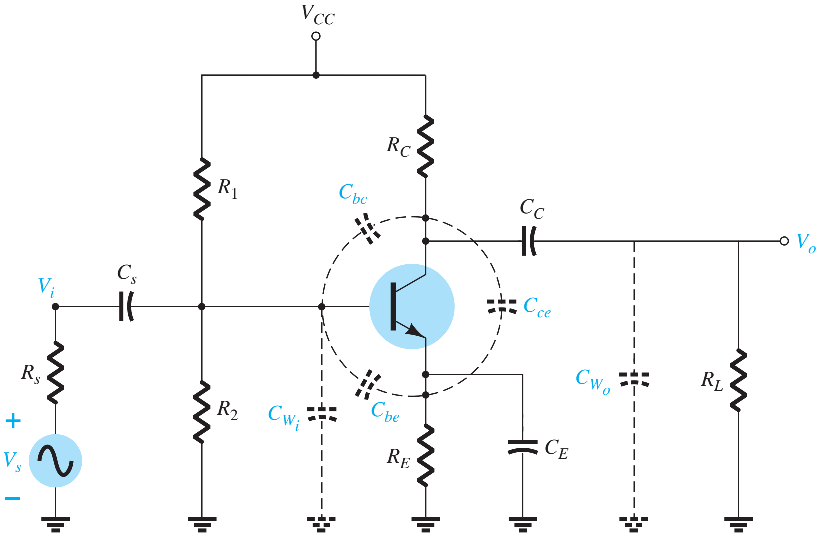
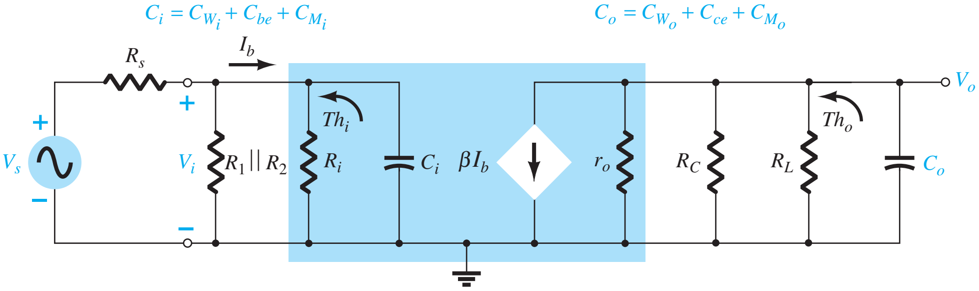


FIG. 9.47
Network of Fig. 9.25 with the capacitors that affect the high-frequency response.



$C_i = C_{W_i} + C_{be} + C_{M_i}$
$C_o = C_{W_o} + C_{ce} + C_{M_o}$
R_s
I_b
V_s
V_i
$R_1 \| R_2$
R_i
Th_i
C_i
βI_b
r_o
R_C
R_L
Th_o
C_o
V_o

FIG. 9.48

High-frequency ac equivalent model for the network of Fig. 9.47.

Determining the Thévenin equivalent circuit for the input and output networks of Fig. 9.48 results in the configurations of Fig. 9.49. For the input network, the −3-dB frequency is defined by

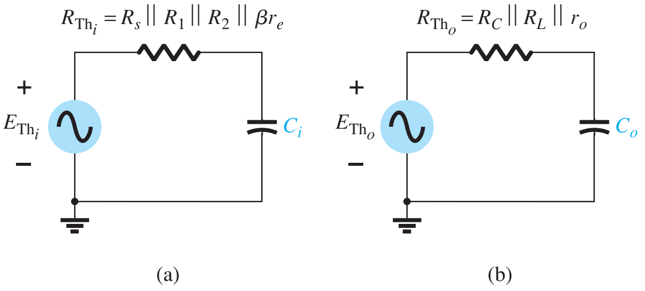
$$\boxed{f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i}} \tag{9.53}$$

with

$$\boxed{R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| \beta r_e} \tag{9.54}$$

and

$$\boxed{C_i = C_{W_i} + C_{be} + C_{M_i} = C_{W_i} + C_{be} + (1 - A_v)C_{bc}} \tag{9.55}$$



$R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| \beta r_e$
E_{Th_i}
C_i
$R_{\text{Th}_o} = R_C \| R_L \| r_o$
E_{Th_o}
C_o
(a)
(b)

FIG. 9.49

Thévenin circuits for the input and output networks of the network of Fig. 9.48.

At very high frequencies, the effect of C_i is to reduce the total impedance of the parallel combination of R_1, R_2, βr_e, and C_i in Fig. 9.48. The result is a reduced level of voltage across C_i, a reduction in I_b, and a gain for the system.

For the output network,

$$\boxed{f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o}} \tag{9.56}$$

with

$$\boxed{R_{\text{Th}_o} = R_C \| R_L \| r_o} \tag{9.57}$$

and

$$\boxed{C_o = C_{W_o} + C_{ce} + C_{M_o}} \tag{9.58}$$

or

$$C_o = C_{W_o} + C_{ce} + (1 - 1/A_v)C_{bc}$$

For A_v large (typical):

$$1 \gg 1/A_v$$

and

$$\boxed{C_o \cong C_{W_o} + C_{ce} + C_{bc}} \tag{9.59}$$

At very high frequencies, the capacitive reactance of C_o will decrease and consequently reduce the total impedance of the output parallel branches of Fig. 9.48. The net result is that V_o will also decline toward zero as the reactance X_C becomes smaller. The frequencies

f_{H_i} and f_{H_o} will each define a -6-dB/octave asymptote such as depicted in Fig. 9.46. If the parasitic capacitors were the only elements to determine the high-cutoff frequency, the lowest frequency would be the determining factor. However, the decrease in h_{fe} (or β) with frequency must also be considered as to whether its break frequency is lower than f_{H_i} or f_{H_o}.

h_{fe} (or β) Variation

The variation of h_{fe} (or β) with frequency will approach, with some degree of accuracy, the following relationship:

$$\boxed{h_{fe} = \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)}} \qquad \textbf{(9.60)}$$

The use of h_{fe} rather than β in some of this descriptive material is due primarily to the fact that manufacturers typically use the hybrid parameters when covering this issue in their specification sheets and so on.

The only undefined quantity, f_β, is determined by a set of parameters employed in the *hybrid* π or *Giacoletto* model of Fig. 9.50 introduced in Section 5.22. The resistance r_b includes the base contact, base bulk, and base spreading resistance. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistors, and the last is the actual resistance within the active base region. The resistances r_π, r_o, and r_u are the resistances between the indicated terminals when the device is in the active region. The same is true for the capacitances C_{bc} and C_{be}, although the former is a transition capacitance, whereas the latter is a diffusion capacitance. A more detailed explanation of the frequency dependence of each can be found in a number of readily available texts.

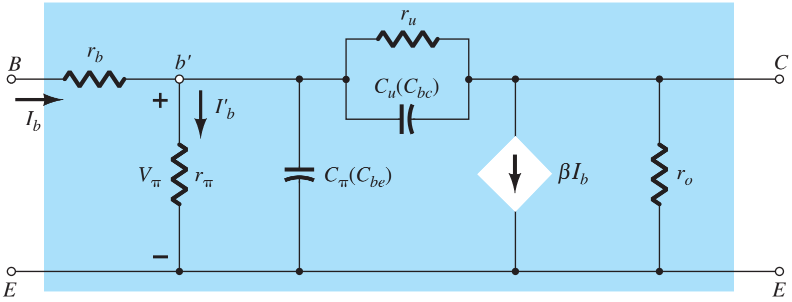


FIG. 9.50

Giacoletto (or hybrid π*) high-frequency transistor small-signal ac equivalent circuit.*

If we remove the base resistance r_b, the base-to-collector resistance r_u, and all the parasitic capacitances, the result is an ac equivalent circuit that matches the small-signal equivalent for the common-emitter configuration used in Chapter 5. The base-to-emitter resistance r_π is βr_e and the output resistance r_o is simply a value provided through the hybrid parameter h_{oe}. The controlled source is also βI_b as used in Chapter 5. However, if we include the resistance r_u (usually quite large) between base and collector, there is a feedback loop between output and input circuits to match the contribution of h_{r_e} for the hybrid equivalent circuit. Recall from Chapter 5 that the feedback term is normally inconsequential for most applications, but if a particular application puts it at the forefront, then the model of Fig. 9.50 will bring it into play. The resistance r_u is a result of the fact that the base current is somewhat sensitive to the collector-to-base voltage. Because the base-to-emitter voltage is linearly related to the base current through Ohm's law and the output voltage is equal to the difference between the base-to-emitter voltage and collector-to-base voltage, we can conclude that the base current is sensitive to the changes in output voltage as revealed by the hybrid parameter h_{r_e}.

In terms of these parameters,

$$\boxed{f_\beta(\text{often appearing as } f_{h_{fe}}) = \frac{1}{2\pi r_\pi(C_\pi + C_u)}} \tag{9.61}$$

or, because $r_\pi = \beta r_e = h_{fe_{\text{mid}}} r_e$,

$$\boxed{f_\beta = \frac{1}{h_{fe_{\text{mid}}}} \frac{1}{2\pi r_e(C_\pi + C_u)}} \tag{9.62}$$

or

Equation (9.62) clearly reveals that because r_e is a function of the network design:

f_β is a function of the bias configuration.

The basic format of Eq. (9.60) is exactly the same as Eq. (9.52) if we extract the multiplying factor $h_{fe_{\text{mid}}}$, revealing that h_{fe} will drop off from its midband value with a 6-dB/octave slope as shown in Fig. 9.51. The same figure has a plot of h_{fb} (or α) versus frequency. Note the small change in h_{fb} for the chosen frequency range, revealing that the common-base configuration displays improved high-frequency characteristics over the common-emitter configuration. Recall also the absence of the Miller effect capacitance due to the noninverting characteristics of the common-base configuration. For this very reason, common-base high-frequency parameters rather than common-emitter parameters are often specified for a transistor—especially those designed specifically to operate in the high-frequency regions.

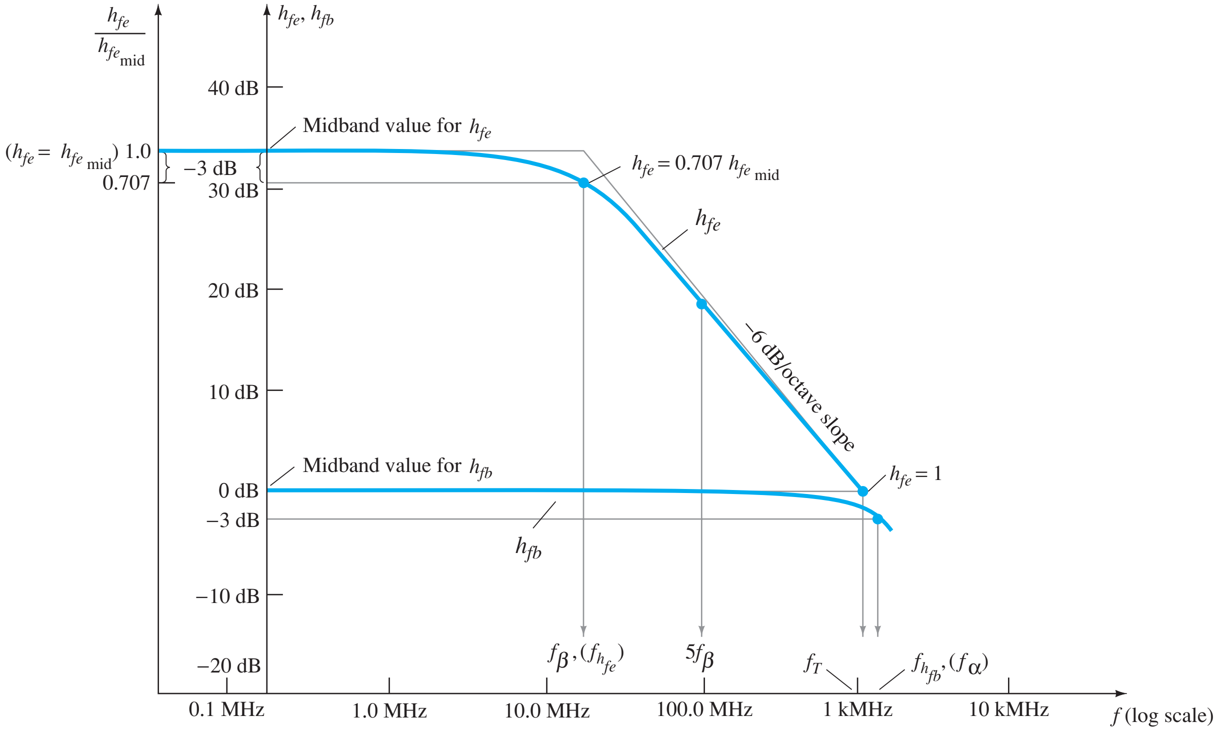


FIG. 9.51

h_{fe} and h_{fb} versus frequency in the high-frequency region.

The following equation permits a direct conversion for determining f_β if f_α and α are specified:

$$\boxed{f_\beta = f_\alpha(1 - \alpha)} \tag{9.63}$$

Gain-Bandwidth Product

There is a **Figure of Merit** applied to amplifiers called the **Gain-Bandwidth Product (GBP)** that is commonly used to initiate the design process of an amplifier. It provides important information about the relationship between the gain of the amplifier and the expected operating frequency range.

In Fig. 9.52 the frequency response of an amplifier with a gain of 100, a low cutoff frequency of 250 Hz, and an upper cutoff frequency of 1 MHz has been plotted on a linear scale rather than the typical log scale. Note that because a linear scale was chosen for the horizontal axis it is impossible to show the low cutoff frequency, and the curve appears as essentially a straight vertical line at $f = 0$ Hz. Because $f = 0$ Hz represents a dc situation,

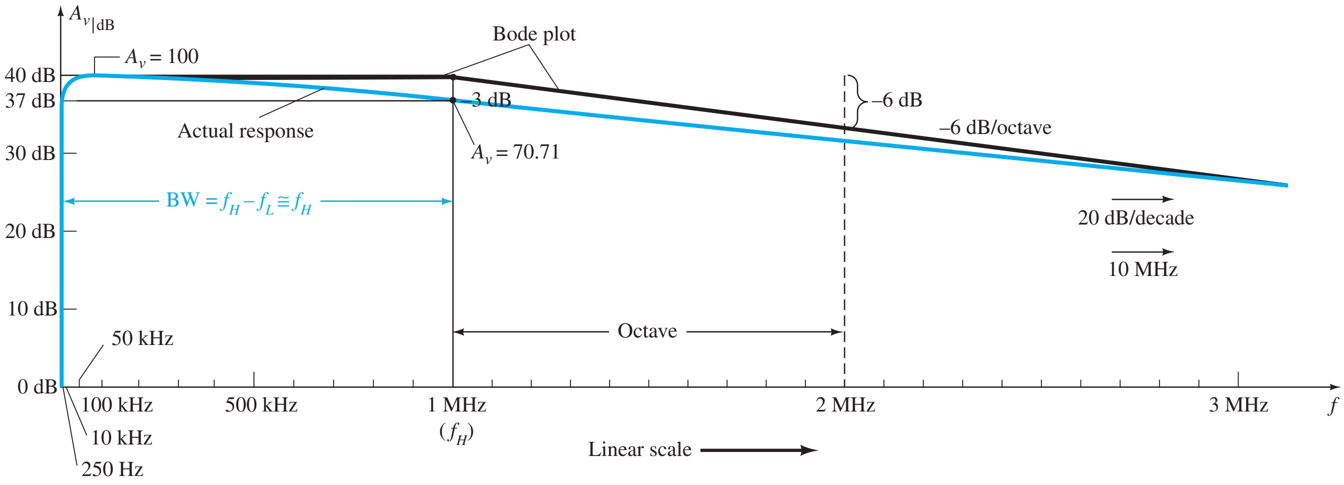


FIG. 9.52
Plotting the dB gain of an amplifier in a linear-frequency plot.

the gain at the low end of an amplifier is often called the DC gain.

Note also that the use of a linear horizontal axis results in a very slow decline in gain with frequency past the breakpoint. It would take many pages to show the full frequency plot at the high end.

It is also clear from Fig. 9.52 that the bandwidth is essentially defined by the upper cutoff frequency because the low cutoff frequency is so small in comparison.

If Fig. 9.52 were plotted using a log scale for the horizontal axis, the plot of Fig. 9.53 would result.

The low end is expanded and the frequency response at the upper end is complete with a boundary defined by the 20-dB drop per decade slope. The upper breakpoint frequency is labeled f_H with the lower breakpoint frequency labeled f_L.

At $A_v = A_{v_{\text{mid}}} = 100$ the bandwidth as shown in Fig. 9.53 is approximately 1 MHz.

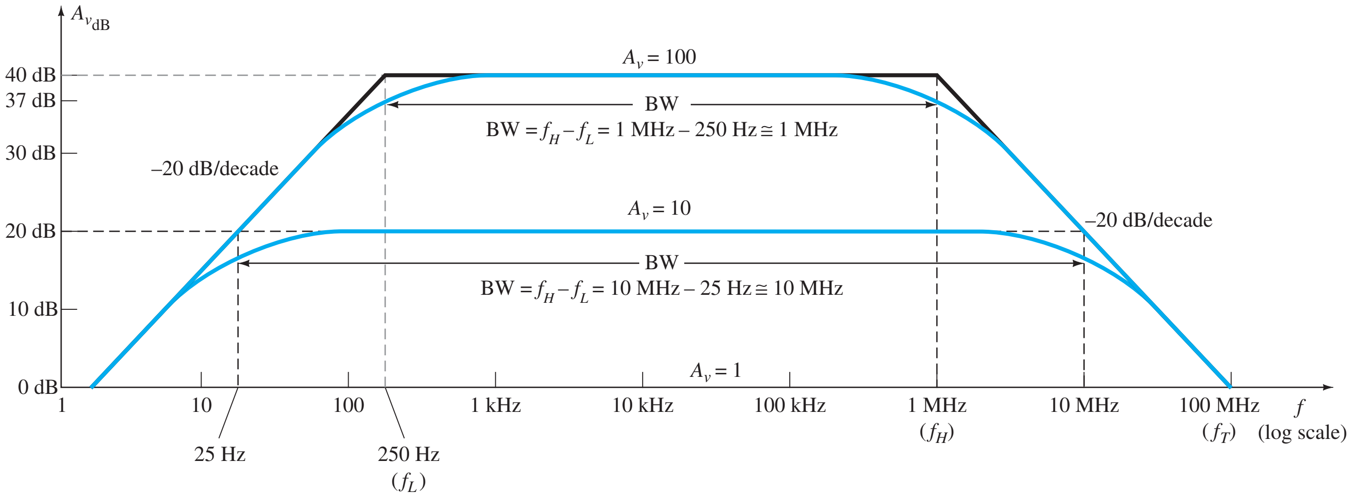


FIG. 9.53
Finding the bandwidth at two different gain levels.

The gain-bandwidth product is

$$\boxed{\text{GBP} = A_{v_{\text{mid}}}\text{BW}} \tag{9.64}$$

which for this example is

$$\text{GBP} = (100)(1\text{ MHz}) = 100\text{ MHz}$$

At $A_v = 10$, $20\log_{10}10 = 20$ and the bandwidth as shown in Fig. 9.53 is approximately 10 MHz.

The resulting gain-bandwidth product is now

$$\text{GBP} = (10)(10\text{ MHz}) = 100\text{ MHz}$$

In fact, at any level of gain the product of the two remains a constant.

At $A_v = 1$ or $A_v|_{dB} = 0$ bandwidth is defined as f_T in Fig. 9.53.

In general,

the frequency f_T is called the unity-gain frequency and is always equal to the product of the midband gain of an amplifier and the bandwidth at any level of gain.

That is,

$$\boxed{f_T = A_{v_{\text{mid}}} f_H} \quad (\text{Hz}) \tag{9.65a}$$

The result is that the expected bandwidth of an amplifier for any level of gain can be found quite directly. Consider an amplifier with a given f_T of 120 MHz. At a gain of 80 the expected f_H or bandwidth is $f_T/A_{v_{\text{mid}}} = 120\text{ MHz}/80 = 1.5\text{ MHz}$. At a gain of 60 the bandwidth is 120 MHz/60 = 2 MHz and so on—a very useful tool.

For transistors themselves, where a voltage gain has not been defined by a configuration, specification sheets will provide a value of f_T that relates to the transistor only. That is,

$$\boxed{f_T = h_{fe_{\text{mid}}} f_\beta} \quad (\text{Hz}) \tag{9.65b}$$

The dB plot would appear as shown in Fig. 9.49.

The general equation for the h_{f_e} variation with frequency is defined by Eq. 9.60. For the amplifier it is defined by

$$\boxed{A_v = \frac{A_{v_{\text{mid}}}}{1 + j(f/f_H)}} \tag{9.66}$$

Note that in each case the frequency f_H defines the corner frequency.

Substituting Eq. (9.62) for f_β in Eq. (9.65) gives

$$f_T = h_{fe_{\text{mid}}} \frac{1}{2\pi h_{fe_{\text{mid}}} r_e(C_\pi + C_u)}$$

and

$$\boxed{f_T \cong \frac{1}{2\pi r_e(C_\pi + C_u)}} \tag{9.67}$$

EXAMPLE 9.14 Use the network of Fig. 9.47 with the same parameters as in Example 9.12, that is,

$$R_s = 1\text{ k}\Omega, R_1 = 40\text{ k}\Omega, R_2 = 10\text{ k}\Omega, R_E = 2\text{ k}\Omega, R_C = 4\text{ k}\Omega, R_L = 2.2\text{ k}\Omega$$
$$C_s = 10\ \mu\text{F}, C_C = 1\ \mu\text{F}, C_E = 20\ \mu\text{F}$$
$$h_{fe} = 100, r_o = \infty\ \Omega, V_{CC} = 20\text{ V}$$

with the addition of

$$C_\pi(C_{be}) = 36\text{ pF}, C_u(C_{bc}) = 4\text{ pF}, C_{ce} = 1\text{ pF}, C_{W_i} = 6\text{ pF}, C_{W_o} = 8\text{ pF}$$

a. Determine f_{H_i} and f_{H_o}.
b. Find f_β and f_T.

c. Sketch the frequency response for the low- and high-frequency regions using the results of Example 9.12 and the results of parts (a) and (b).

d. Obtain the PSpice response for the full frequency spectrum and compare with the results of part (c).

Solution:

a. From Example 9.12:

$$\beta r_e = 1.576\text{ k}\Omega, \qquad A_{v_{\text{mid}}}(\text{amplifier—not including effects of } R_s) = -90$$

and
$$R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| \beta r_e = 1\text{ k}\Omega \| 40\text{ k}\Omega \| 10\text{ k}\Omega \| 1.576\text{ k}\Omega$$
$$\cong 0.57\text{ k}\Omega$$

with
$$C_i = C_{W_i} + C_{be} + (1 - A_v)C_{bc}$$
$$= 6\text{ pF} + 36\text{ pF} + [1 - (-90)]4\text{ pF}$$
$$= 406\text{ pF}$$

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i} = \frac{1}{2\pi(0.57\text{ k}\Omega)(406\text{ pF})}$$
$$= \mathbf{687.73\text{ kHz}}$$

$$R_{\text{Th}_o} = R_C \| R_L = 4\text{ k}\Omega \| 2.2\text{ k}\Omega = 1.419\text{ k}\Omega$$

$$C_o = C_{W_o} + C_{ce} + C_{M_o} = 8\text{ pF} + 1\text{ pF} + \left(1 - \frac{1}{-90}\right)4\text{ pF}$$
$$= 13.04\text{ pF}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o} = \frac{1}{2\pi(1.419\text{ k}\Omega)(13.04\text{ pF})}$$
$$= \mathbf{8.6\text{ MHz}}$$

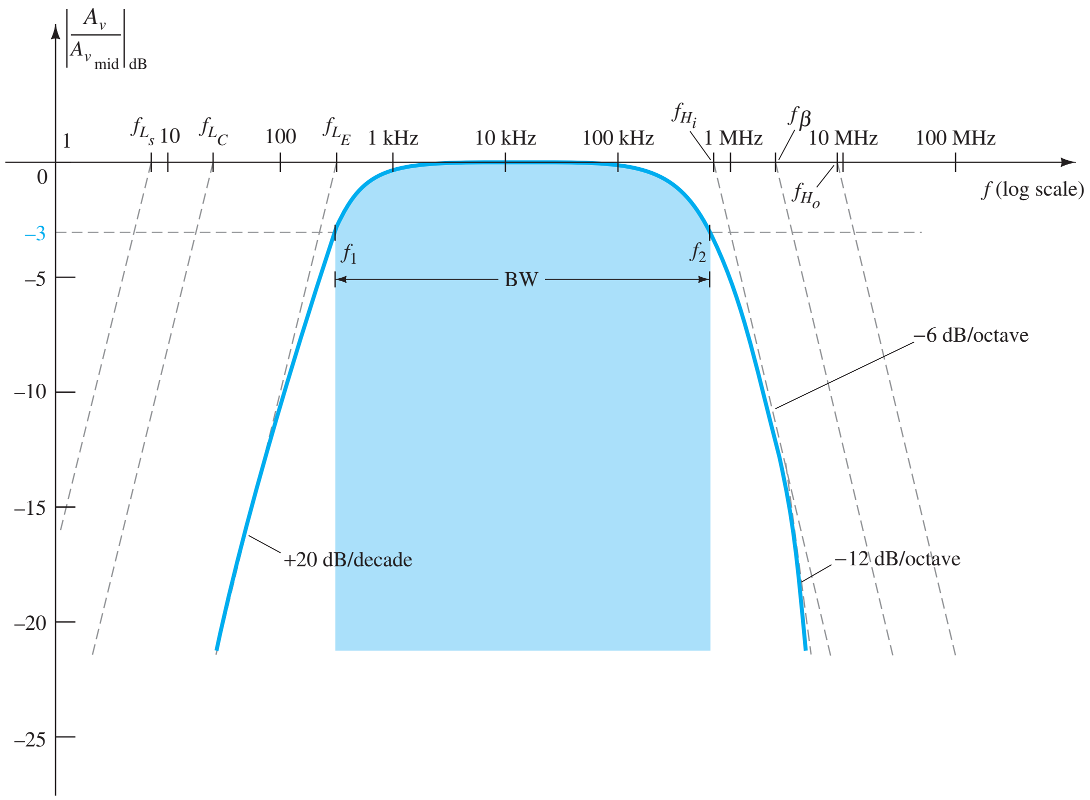


FIG. 9.54

Full frequency response for the network of Fig. 9.47.

b. Applying Eq. (9.63) gives

$$f_\beta = \frac{1}{2\pi h_{fe_{\text{mid}}} r_e (C_{be} + C_{bc})}$$

$$= \frac{1}{2\pi(100)(15.76\ \Omega)(36\text{ pF} + 4\text{ pF})} = \frac{1}{2\pi(100)(15.76\ \Omega)(40\text{ pF})}$$

$$= \mathbf{2.52\ MHz}$$

$$f_T = h_{fe_{\text{mid}}} f_\beta = (100)(2.52\text{ MHz})$$

$$= \mathbf{252\ MHz}$$

c. See Fig. 9.54. The corner frequency f_{H_i} will determine the high cutoff frequency and the bandwidth of the amplifier. The upper cutoff frequency is very close to 600 kHz.

d. The PSpice analysis will appear in Section 9.15.

9.12 HIGH-FREQUENCY RESPONSE—FET AMPLIFIER

The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier. As shown in Fig. 9.55, there are interelectrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier. The capacitors C_{gs} and C_{gd} typically vary from 1 pF to 10 pF, whereas the capacitance C_{ds} is usually quite a bit smaller, ranging from 0.1 pF to 1 pF.

Because the network of Fig. 9.55 is an inverting amplifier, a Miller effect capacitance will appear in the high-frequency ac equivalent network appearing in Fig. 9.56. At high frequencies, C_i will approach a short-circuit equivalent and V_{gs} will drop in value and reduce the overall gain. At frequencies where C_o approaches its short-circuit equivalent, the parallel output voltage V_o will drop in magnitude.

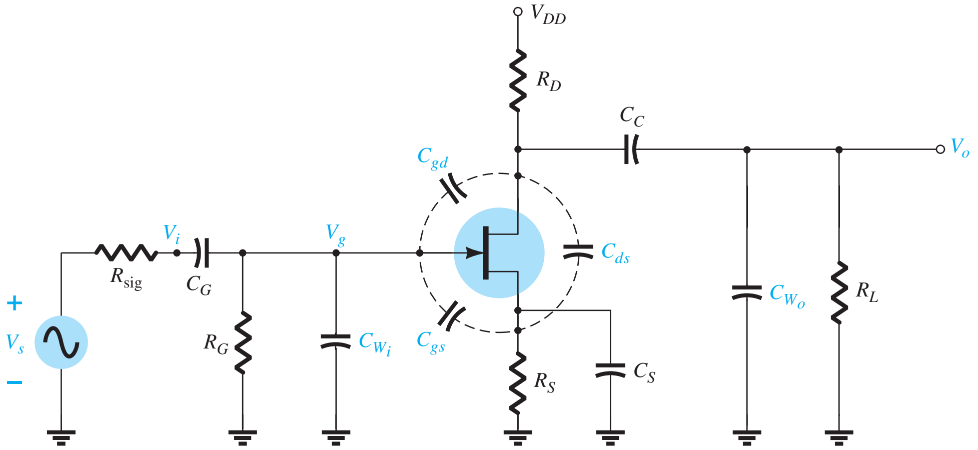


FIG. 9.55

Capacitive elements that affect the high-frequency response of a JFET amplifier.

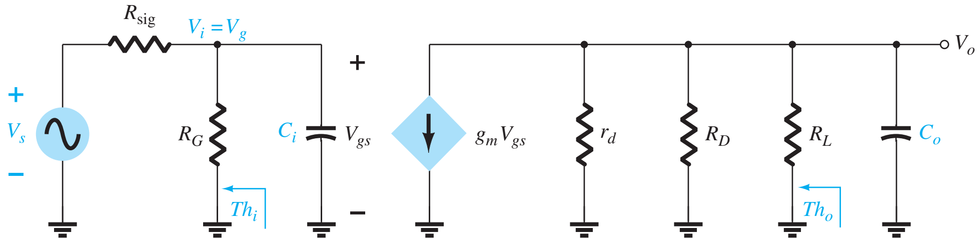


FIG. 9.56

High-frequency ac equivalent circuit for Fig. 9.55.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thévenin equivalent circuits for each section as shown in Fig. 9.57. For the input circuit,

$$\boxed{f_{H_i} = \frac{1}{2\pi R_{\mathrm{Th}_i} C_i}} \tag{9.68}$$

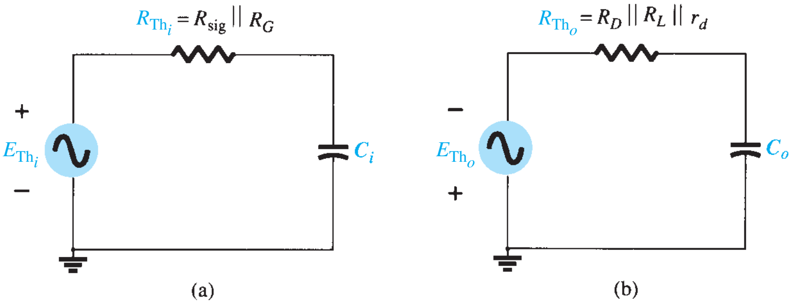

$R_{\mathrm{Th}_i} = R_{\mathrm{sig}} \| R_G$
+
E_{Th_i}
−
C_i
(a)
$R_{\mathrm{Th}_o} = R_D \| R_L \| r_d$
−
E_{Th_o}
+
C_o
(b)

FIG. 9.57

The Thévenin equivalent circuits for: (a) the input circuit and (b) the output circuit.

and

$$\boxed{R_{\mathrm{Th}_i} = R_{\mathrm{sig}} \| R_G} \tag{9.69}$$

with

$$\boxed{C_i = C_{W_i} + C_{gs} + C_{M_i}} \tag{9.70}$$

and

$$\boxed{C_{M_i} = (1 - A_v)C_{gd}} \tag{9.71}$$

for the output circuit,

$$\boxed{f_{H_o} = \frac{1}{2\pi R_{\mathrm{Th}_o} C_o}} \tag{9.72}$$

with

$$\boxed{R_{\mathrm{Th}_o} = R_D \| R_L \| r_d} \tag{9.73}$$

and

$$\boxed{C_o = C_{W_o} + C_{ds} + C_{M_o}} \tag{9.74}$$

and

$$\boxed{C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_{gd}} \tag{9.75}$$

EXAMPLE 9.15

a. Determine the high-cutoff frequencies for the network of Fig. 9.55 using the same parameters as Example 9.13:

$$C_G = 0.01\ \mu\text{F}, \quad C_C = 0.5\ \mu\text{F}, \quad C_S = 2\ \mu\text{F}$$
$$R_{\mathrm{sig}} = 10\ \text{k}\Omega, \quad R_G = 1\ \text{M}\Omega, \quad R_D = 4.7\ \text{k}\Omega, \quad R_S = 1\ \text{k}\Omega, \quad R_L = 2.2\ \text{k}\Omega$$
$$I_{DSS} = 8\ \text{mA}, \quad V_P = -4\ \text{V}, \quad r_d = \infty\ \Omega, \quad V_{DD} = 20\ \text{V}$$

with the addition of

$$C_{gd} = 2\ \text{pF}, \quad C_{gs} = 4\ \text{pF}, \quad C_{ds} = 0.5\ \text{pF}, \quad C_{W_i} = 5\ \text{pF}, \quad C_{W_o} = 6\ \text{pF}$$

b. Obtain a PSpice response for the full frequency range and note whether it supports the conclusions of Example 9.13 and the calculations above.

Solution:

a. $R_{\text{Th}_i} = R_{\text{sig}} \| R_G = 10\text{ k}\Omega \| 1\text{ M}\Omega = 9.9\text{ k}\Omega$

From Example 9.13, $A_v = -3$. We have

$$\begin{aligned} C_i &= C_{W_i} + C_{gs} + (1 - A_v)C_{gd} \\ &= 5\text{ pF} + 4\text{ pF} + (1 + 3)2\text{ pF} \\ &= 9\text{ pF} + 8\text{ pF} \\ &= 17\text{ pF} \\ f_{H_1} &= \frac{1}{2\pi R_{\text{Th}_i} C_i} \\ &= \frac{1}{2\pi(9.9\text{ k}\Omega)(17\text{ pF})} = \mathbf{945.67\text{ kHz}} \\ R_{\text{Th}_o} &= R_D \| R_L \\ &= 4.7\text{ k}\Omega \| 2.2\text{ k}\Omega \\ &\cong 1.5\text{ k}\Omega \\ C_o &= C_{W_o} + C_{ds} + C_{M_o} = 6\text{ pF} + 0.5\text{ pF} + \left(1 - \frac{1}{-3}\right)2\text{ pF} = 9.17\text{ pF} \\ f_{H_o} &= \frac{1}{2\pi(1.5\text{ k}\Omega)(9.17\text{ pF})} = \mathbf{11.57\text{ MHz}} \end{aligned}$$

The results above clearly indicate that the input capacitance with its Miller effect capacitance will determine the upper cutoff frequency. This is typically the case due to the smaller value of C_{ds} and the resistance levels encountered in the output circuit.

b. The PSpice analysis will appear in Section 9.15.

Even though the analysis of the last few sections has been limited to two configurations, the general procedure for determining the cutoff frequencies should support the analysis of any other transistor configuration. Keep in mind that the Miller capacitance is limited to inverting amplifiers and that f_α is significantly greater than f_β if the common-base configuration is encountered. There is a great deal more literature on the analysis of single-stage amplifiers that goes beyond the coverage of this chapter. However, the content of this chapter should provide a firm foundation for any analysis of frequency effects.

9.13 MULTISTAGE FREQUENCY EFFECTS

For a second transistor stage connected directly to the output of a first stage, there will be a significant change in the overall frequency response. In the high-frequency region, the output capacitance C_o must now include the wiring capacitance (C_{W_1}), parasitic capacitance (C_{be}), and Miller capacitance (C_{M_i}) of the following stage. Furthermore, there will be additional low-frequency cutoff levels due to the second stage, which will further reduce the overall gain of the system in this region. For each additional stage, the upper cutoff frequency will be determined primarily by the stage having the lowest cutoff frequency. The low-frequency cutoff is primarily determined by that stage having the highest low-frequency cutoff frequency. Obviously, therefore, one poorly designed stage can offset an otherwise well-designed cascaded system.

The effect of increasing the number of *identical* stages can be clearly demonstrated by considering the situations indicated in Fig. 9.58. In each case, the upper and lower cutoff frequencies of each of the cascaded stages are identical. For a single stage, the cutoff frequencies are f_L and f_H as indicated. For two identical stages in cascade, the drop-off rate in the high- and low-frequency regions has increased to -12 dB/octave or -40 dB/decade. At f_L and f_H, therefore, the decibel drop is now -6 dB rather than the defined band frequency gain level of -3 dB. The -3-dB point has shifted to f'_L and f'_H as indicated, with a resulting drop in the bandwidth. A -18-dB/octave or -60-dB/decade slope will result for a three-stage system of identical stages with the indicated reduction in bandwidth (f''_L and f''_H).

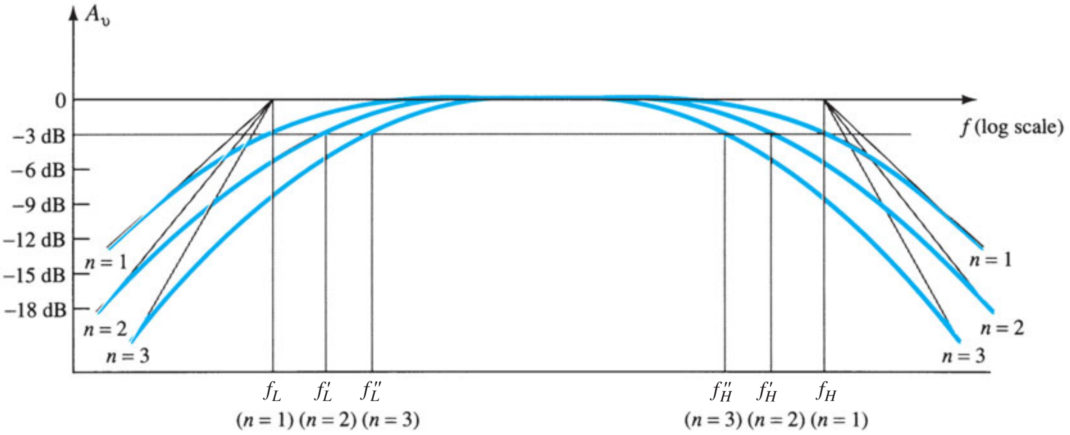


FIG. 9.58

Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

Assuming identical stages, we can determine an equation for each band frequency as a function of the number of stages (n) in the following manner: For the low-frequency region,

$$A_{v_{\text{low, (overall)}}} = A_{v_{1_{\text{low}}}} A_{v_{2_{\text{low}}}} A_{v_{3_{\text{low}}}} \cdots A_{v_{n_{\text{low}}}}$$

but because all stages are identical, $A_{v_{1_{\text{low}}}} = A_{v_{2_{\text{low}}}} =$ etc., and

$$A_{v_{\text{low, (overall)}}} = (A_{v_{1_{\text{low}}}})^n$$

or

$$\frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}}(\text{overall}) = \left(\frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}}\right)^n = \frac{1}{(1 - jf_L/f)^n}$$

Setting the magnitude of this result equal to $1/\sqrt{2}$(−3 dB level) results in

$$\frac{1}{\sqrt{[1 + (f_L/f'_L)^2]^n}} = \frac{1}{\sqrt{2}}$$

or

$$\left\{\left[1 + \left(\frac{f_L}{f'_L}\right)^{2-}\right]^{1/2}\right\}^n = \left\{\left[1 + \left(\frac{f_L}{f'_L}\right)^2\right]^n\right\}^{1/2} = (2)^{1/2}$$

so that

$$\left[1 + \left(\frac{f_L}{f'_L}\right)^2\right]^n = 2$$

and

$$1 + \left(\frac{f_L}{f'_L}\right)^2 = 2^{1/n}$$

with the result that

$$\boxed{f'_L = \frac{f_L}{\sqrt{2^{1/n} - 1}}} \qquad \textbf{(9.76)}$$

In a similar manner, it can be shown that for the high-frequency region,

$$\boxed{f'_H = (\sqrt{2^{1/n} - 1})f_H} \qquad \textbf{(9.77)}$$

Note the presence of the same factor $\sqrt{2^{1/n} - 1}$ in each equation. The magnitude of this factor for various values of n is listed below.

n	$\sqrt{2^{1/n} - 1}$
2	0.64
3	0.51
4	0.43
5	0.39

For $n = 2$, consider that the upper cutoff frequency $f'_H = 0.64f_H$, or 64% of the value obtained for a single stage, whereas $f'_L = (1/0.64)f_L = 1.56f_L$. For $n = 3, f'_H = 0.51f_H$, or approximately one-half the value of a single stage, and $f'_L = (1/0.51)f_L = 1.96f_L$, or approximately *twice* the single-stage value.

For the *RC*-coupled transistor amplifier, if $f_H = f_\beta$, or if they are close enough in magnitude for both to affect the upper 3-dB frequency, the number of stages must be increased by a factor of 2 when determining f'_H due to the increased number of factors $1/(1 + jf/f_x)$.

A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed and independent of the number of stages. For instance, if a single-stage amplifier produces a gain of 100 with a bandwidth of 10,000 Hz, the resulting gain–bandwidth product is $10^2 \times 10^4 = 10^6$. For a two-stage system the same gain can be obtained by having two stages with a gain of 10 ($10 \times 10 = 100$). The bandwidth of each stage would then increase by a factor of 10 to 100,000 due to the lower gain requirement and fixed gain–bandwidth product of 10^6. Of course, the design must be such as to permit the increased bandwidth and establish the lower gain level.

9.14 SQUARE-WAVE TESTING

A sense for the frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier and noting the output response. The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified. Using *square-wave testing* is significantly less time consuming than applying a series of sinusoidal signals at different frequencies and magnitudes to test the frequency response of the amplifier.

The reason for choosing a square-wave signal for the testing process is best described by examining the *Fourier series* expansion of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies. The summation of all the terms of the series will result in the original waveform. In other words, even though a waveform may not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies and magnitudes.

The Fourier series expansion for the square wave of Fig. 9.59 is

$$v = \frac{4}{\pi} V_m \left(\underbrace{\sin 2\pi f_s t}_{\text{fundamental}} + \underbrace{\frac{1}{3}\sin 2\pi(3f_s)t}_{\text{third harmonic}} + \underbrace{\frac{1}{5}\sin 2\pi(5f_s)t}_{\text{fifth harmonic}} + \underbrace{\frac{1}{7}\sin 2\pi(7f_s)t}_{\text{seventh harmonic}} + \underbrace{\frac{1}{9}\sin 2\pi(9f_s)t}_{\text{ninth harmonic}} + \cdots + \underbrace{\frac{1}{n}\sin 2\pi(nf_s)t}_{n\text{th harmonic}} \right) \quad \textbf{(9.78)}$$

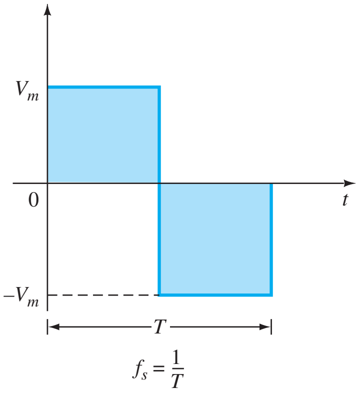


FIG. 9.59
Square wave.

The first term of the series is called the *fundamental* term and in this case has the same frequency, f_s, as the square wave. The next term has a frequency equal to three times the fundamental and is referred to as the *third harmonic*. Its magnitude is one-third the magnitude of the fundamental term. The frequencies of the succeeding terms are odd multiples of the fundamental term, and the magnitude decreases with each higher harmonic. Figure 9.58 demonstrates how the summation of terms of a Fourier series can result in a nonsinusoidal waveform. The generation of the square wave of Fig. 9.59 would require an infinite number of terms. However, the summation of just the fundamental term and the third harmonic in Fig. 9.60a clearly results in a waveform that is beginning to take on the appearance of a square wave. Including the fifth and seventh harmonics as in Fig. 9.60b takes us a step closer to the waveform of Fig. 9.59.

Because the ninth harmonic has a magnitude greater than 10% of the fundamental term [$\frac{1}{9}(100\%) = 11.1\%$], the terms from the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function. It is therefore reasonable to assume that if the application of a square wave of a particular frequency results in a nice clean square wave at the output, then the terms from the fundamental through the ninth harmonic are being amplified without visual distortion by the amplifier. For instance, if an audio amplifier with a bandwidth of 20 kHz (audio range is from 20 Hz to 20 kHz) is to be tested, the frequency of the applied signal should be at least 20 kHz/9 = 2.22 kHz.

If the response of an amplifier to an applied square wave is an undistorted replica of the input, the frequency response (or BW) of the amplifier is obviously sufficient for the applied frequency. If the response is as shown in Fig. 9.61a and b, the low frequencies are not being amplified properly and the low cutoff frequency has to be investigated. If the waveform has the appearance of Fig. 9.61c and d, the high-frequency components are not receiving sufficient amplification and the high-cutoff frequency (or BW) has to be reviewed.

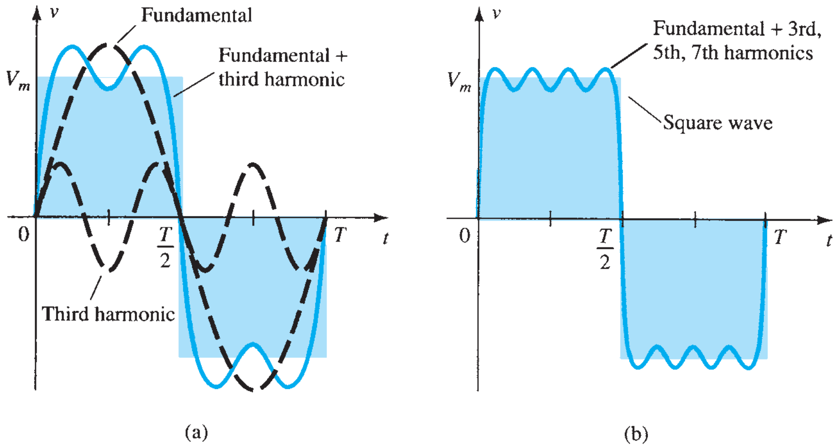


FIG. 9.60
Harmonic content of a square wave.

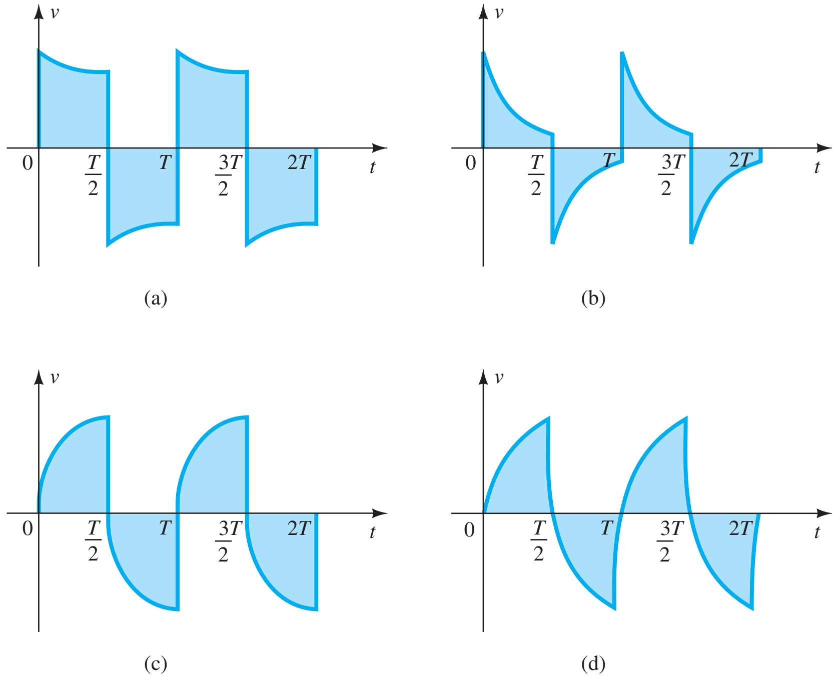


FIG. 9.61
(a) Poor low-frequency response; (b) very poor low-frequency response; (c) poor high-frequency response; (d) very poor high-frequency response.

The actual high-cutoff frequency (or BW) can be determined from the output waveform by carefully measuring the rise time defined between 10% and 90% of the peak value, as shown in Fig. 9.62. Substituting into the following equation will provide the upper cutoff frequency, and because $\mathrm{BW} = f_{H_i} - f_{L_o} \cong f_{H_i}$, the equation also provides an indication of the BW of the amplifier:

$$\boxed{\mathrm{BW} \cong f_{H_i} = \frac{0.35}{t_r}} \tag{9.79}$$

The low-cutoff frequency can be determined from the output response by carefully measuring the tilt of Fig. 9.62 and substituting into one of the following equations:

$$\boxed{\%\ \text{tilt} = P\% = \frac{V - V'}{V} \times 100\%} \tag{9.80}$$

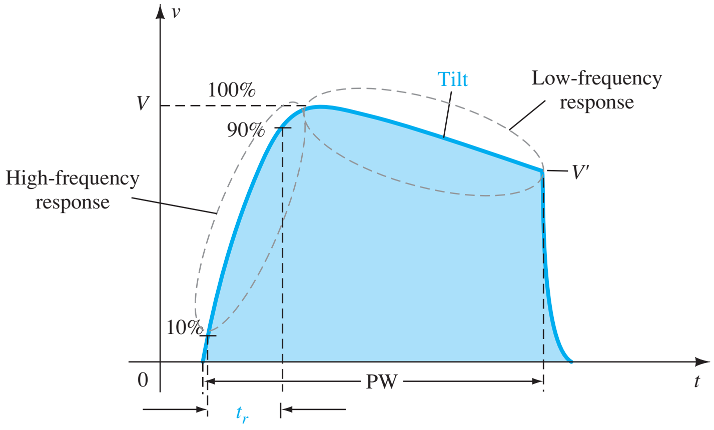


FIG. 9.62

Defining the rise time and tilt of a square wave response.

$$\boxed{\text{tilt} = P = \frac{V - V'}{V}} \qquad \text{(decimal form)} \tag{9.81}$$

The low-cutoff frequency is then determined from

$$\boxed{f_{L_o} = \frac{P}{\pi} f_s} \tag{9.82}$$

EXAMPLE 9.16 The application of a 1-mV, 5-kHz square wave to an amplifier resulted in the output waveform of Fig. 9.63.

a. Write the Fourier series expansion for the square wave through the ninth harmonic.
b. Determine the bandwidth of the amplifier.
c. Calculate the low-cutoff frequency.

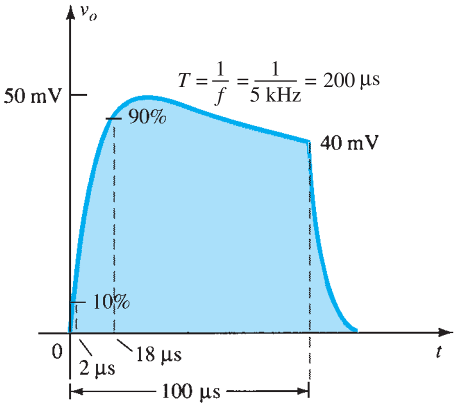


FIG. 9.63

Example 9.16.

Solution:

a. $v_i = \dfrac{4\text{ mV}}{\pi}\left(\sin 2\pi\,(5 \times 10^3)t + \dfrac{1}{3}\sin 2\pi(15 \times 10^3)t + \dfrac{1}{5}\sin 2\pi(25 \times 10^3)t + \dfrac{1}{7}\sin 2\pi(35 \times 10^3)t + \dfrac{1}{9}\sin 2\pi(45 \times 10^3)t\right)$

b. $t_r = 18\ \mu\text{s} - 2\ \mu\text{s} = 16\ \mu\text{s}$

$$\text{BW} \cong \frac{0.35}{t_r} = \frac{0.35}{16\ \mu\text{s}} = \mathbf{21{,}875\ Hz} \cong 4.4 f_s$$

c. $P = \dfrac{V - V'}{V} = \dfrac{50\text{ mV} - 40\text{ mV}}{50\text{ mV}} = 0.2$

$$f_{L_o} = \frac{P}{\pi} f_s = \left(\frac{0.2}{\pi}\right)(5\text{ kHz}) = \mathbf{318.31\text{ Hz}}$$

9.15 SUMMARY

Important Conclusions and Concepts

1. The logarithm of a number gives the **power to which the base must be brought to obtain the same number.** If the base is 10, it is referred to as the **common logarithm;** if the base is $e = 2.71828\ldots$, it is called the **natural logarithm.**
2. Because the decibel rating of any piece of equipment is a **comparison between levels,** a reference level must be selected for each area of application. For audio systems the reference level is generally accepted as **1 mW.** When using voltage levels to determine the gain in dB between two points, any difference in resistance level is generally ignored.
3. The dB gain of cascaded systems is simply the **sum** of the dB gains of each stage.
4. It is the **capacitive elements** of a network that determine the **bandwidth** of a system. The **larger** capacitive elements of the basic design determine the **low**-cutoff frequency, whereas the **smaller** parasitic capacitors determine the **high**-cutoff frequencies.
5. The frequencies at which the gain drops to 70.7% of the midband value are called the **cutoff, corner, band, break,** or **half-power** frequencies.
6. The **narrower** the bandwidth, the **smaller** is the range of frequencies that will permit a transfer of power to the load that is at least 50% of the midband level.
7. A change in frequency by a factor of **two,** equivalent to **one octave,** results in a **6-dB change in gain.** For a **10:1** change in frequency, equivalent to **one decade,** there is a **20-dB change in gain.**
8. For any **inverting** amplifier, the input capacitance will be increased by a **Miller effect** capacitance determined by the **gain** of the amplifier and the **interelectrode** (parasitic) capacitance between the input and output terminals of the active device.
9. A **3-dB drop in beta** (h_{fe}) will occur at a frequency defined by f_β that is sensitive to the **dc operating conditions** of the transistor. This variation in beta can define the upper cutoff frequency of the design.
10. The **high- and low-cutoff frequencies** of an amplifier can be determined by the response of the system to a **square-wave input.** The general appearance will immediately reveal whether the low- or high-frequency response of the system is too limited for the applied frequency, whereas a more detailed examination of the response will reveal the actual bandwidth of the amplifier.

Equations

Logarithms:

$$a = b^x, \qquad x = \log_b a, \qquad \log_{10}\frac{a}{b} = \log_{10} a - \log_{10} b$$

$$\log_{10} ab = \log_{10} a + \log_{10} b, \qquad G_{\text{dB}} = 10 \log_{10}\frac{P_2}{P_1} = 20 \log_{10}\frac{V_2}{V_1}$$

$$G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \cdots + G_{\text{dB}_n}$$

Low-frequency response:

$$A_v = \frac{1}{1 - j(f_L/f)}, \qquad f_L = \frac{1}{2\pi RC}$$

BJT low-frequency response:

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s}, \qquad R_i = R_1 \| R_2 \| \beta r_e$$

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}, \qquad R_o = R_C \| r_o$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E}, \qquad R_e = R_E \| \left(\frac{R_s'}{\beta} + r_e\right), \qquad R_s' = R_s \| R_1 \| R_2$$

FET low-frequency response:

$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G}, \qquad R_i = R_G$$

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}, \qquad R_o = R_D \| r_d$$

$$f_{L_S} = \frac{1}{2\pi R_{eq} C_S}, \qquad R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)} \cong R_S \bigg\| \frac{1}{g_m}\bigg|_{r_d \cong \infty\Omega}$$

Miller effect capacitance:

$$C_{M_i} = (1 - A_v)C_f, \qquad C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_f$$

BJT high-frequency response:

$$A_v = \frac{1}{1 + j(f/f_H)}, \qquad f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i}, \qquad R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| R_i,$$

$$C_i = C_{W_i} + C_{be} + C_{M_i}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o}, \qquad R_{\text{Th}_o} = R_C \| R_L \| r_o, \qquad C_o = C_{W_o} + C_{ce} + C_{M_o},$$

$$h_{fe} = \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)}$$

$$f_\beta \cong \frac{1}{2\pi \beta_{\text{mid}} r_e (C_{be} + C_{bc})}$$

$$f_T \cong h_{fe_{\text{mid}}} f_\beta$$

FET high-frequency response:

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i}, \qquad R_{\text{Th}_i} = R_{\text{sig}} \| R_G, \qquad C_i = C_{W_i} + C_{gs} + C_{M_i},$$

$$C_{M_i} = (1 - A_v)C_{gd}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o}, \qquad R_{\text{Th}_o} = R_D \| R_L \| r_d, \qquad C_o = C_{W_o} + C_{ds} + C_{M_o},$$

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_{gd}$$

Multistage effects:

$$f_L' = \frac{f_L}{\sqrt{2^{1/n} - 1}}, \qquad f_H' = (\sqrt{2^{1/n} - 1})f_H$$

Square-wave testing:

$$\text{BW} \cong f_{H_i} = \frac{0.35}{t_r}, \qquad f_{L_o} = \frac{P}{\pi} f_s, \qquad P = \frac{V - V'}{V}$$

9.16 COMPUTER ANALYSIS

The computer analysis of this section will verify the results of a number of examples appearing in this chapter.

Low-Frequency BJT Response

The network of Example 9.12 with its various capacitors appears in Fig. 9.64. The sequence **Edit-PSpice Model** was used to set I_s to 2E-15A and beta to 100. The remaining parameters of the **PSpice Model** for the transistor were removed to idealize the response to the greatest degree possible. In the **Simulation Settings** dialog box **AC Sweep/Noise** was selected under the **Analysis type** heading, and **Linear** was chosen under the **AC Sweep Type.** The **Start Frequency** was set at 10 kHz, the **End Frequency** at 10 kHz, and the

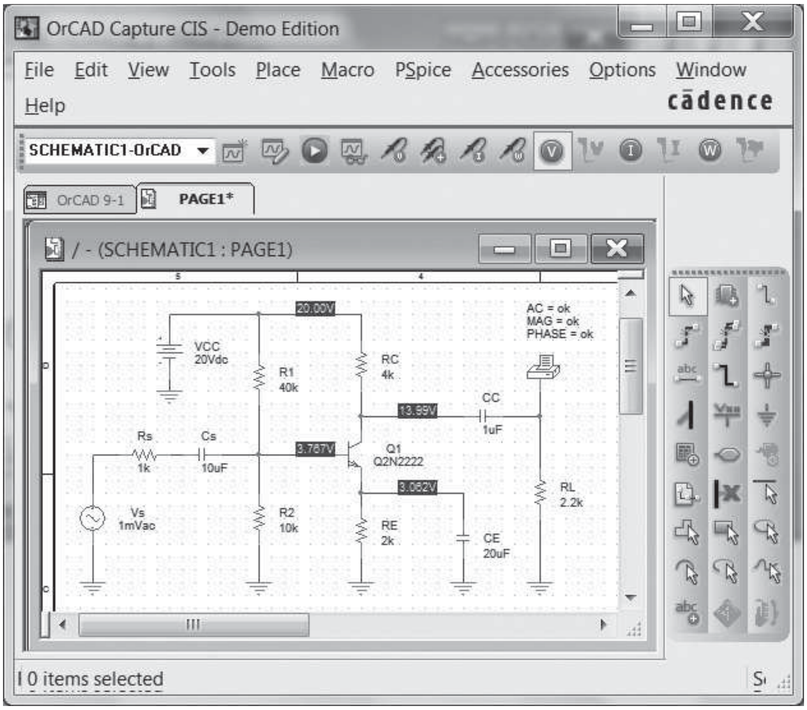


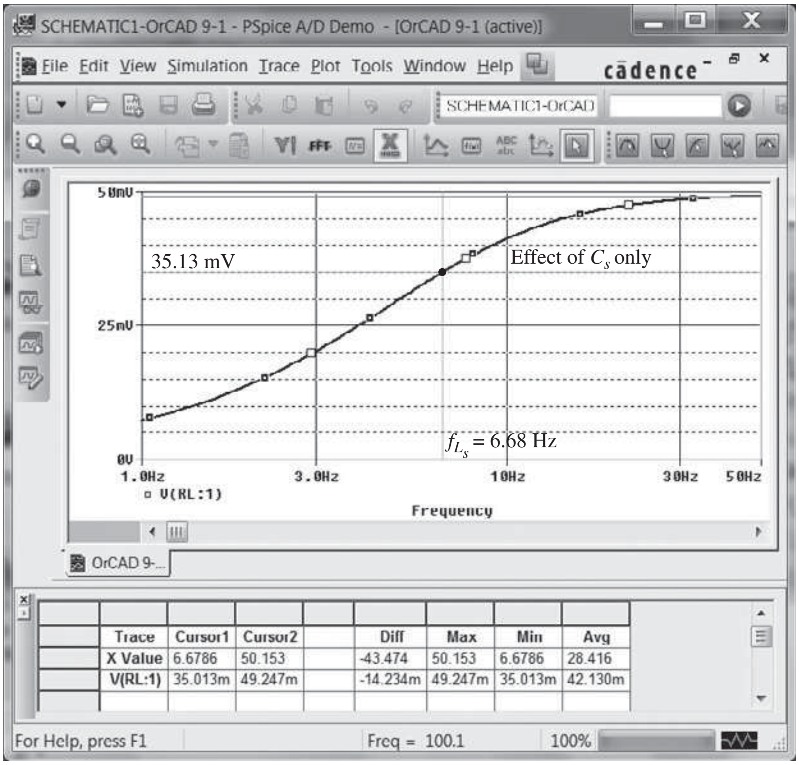
FIG. 9.64

Network of Fig. 9.32 with assigned values.

number of **Points** at 1. A **Simulation** resulted in the dc bias voltage levels of Fig. 9.64. Note that V_B is 3.767 V, compared to the calculated level of 4 V, and that V_E is 3.062 V, compared to the calculated level of 3.3 V. These values are very close when you consider that the approximate model was used to represent the transistor. The output file reveals that the ac voltage across the load at a frequency of 10 kHz is 49.69 mV, resulting in a gain of 49.69, which is very close to the calculated level of 51.21.

A plot of the gain versus frequency will now be obtained with only C_s as a determining factor. The other capacitors, C_C and C_E, will be set to very high values, so they are essentially short circuits at any of the frequencies of interest. Setting C_C and C_E to 1 F will remove any effect they might have on the response in the low-frequency region. Here, however, one must be careful because the program does not recognize 1 F as one farad. It must be entered as 1E6uF. Because the plot desired is gain versus frequency, we must set the **Simulation** to run through a range of frequencies, not as in the first **Simulation** where the frequency was fixed at 10 kHz. This is accomplished by first selecting the **New Simulation key**, giving the run a new **Name,** and proceeding to the **Simulation Settings** dialog box. Under **Analysis type, AC Sweep/Noise** is selected, and under **AC Sweep Type, Linear** is chosen, followed by a **Start Frequency** of 1 Hz, an **End Frequency** of 100 Hz, and **Points** set at 1000. The **Start Frequency** is set at 1 Hz because 0 Hz is an invalid entry. If one is really concerned about what happens between 0 Hz and 1 Hz, one could choose the start frequency as 0.001 Hz and work from there. However, 1 Hz is only 1/100 of the full scale and will be fine for this analysis. The **End Frequency** was selected as 100 Hz because we limit our interest to the low-frequency range. With 1000 points there will be sufficient data points to provide a smooth plot throughout the frequency range. Once **Simulation** is enacted followed by **Trace-Add Trace-V(RL:1)**, a plot appears extending to 120 Hz. Note also that the computer selected a log scale even though we called for a **Linear** plot. If we choose **Plot-Axis Settings-X-Axis-Linear,** we get a linear plot to 120 Hz, but the curve of interest is in the low end—the log axis obviously provided a better plot for our region of interest. Returning to **Plot-Axis Settings-X-Axis-Log** returns the original plot. Our interest lies in the region of 1 Hz to 50 Hz, so the remaining frequencies to 1 kHz should be removed with **Plot-Axis Settings-User Defined-1 Hz to 100 Hz-OK.** The vertical axis also goes to 60 mV, and we want to limit the range to 50 mV for this frequency range. This is accomplished through **Plot-Axis Settings-Y-Axis User Defined-0V to 50 mV-OK,** after which the plot of Fig. 9.65 will be obtained.

Note how closely the curve approaches 50 mV in this range. The cutoff level is determined by 0.707(49.69 mV) = 35.13 mV, which can be found using the **Cursor** option.


SCHEMATIC1-OrCAD 9-1 - PSpice A/D Demo - [OrCAD 9-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
50mV
25mV
0V
35.13 mV
Effect of C_s only
f_{L_s} = 6.68 Hz
1.0Hz
3.0Hz
10Hz
30Hz
50Hz
V(RL:1)
Frequency
OrCAD 9-...

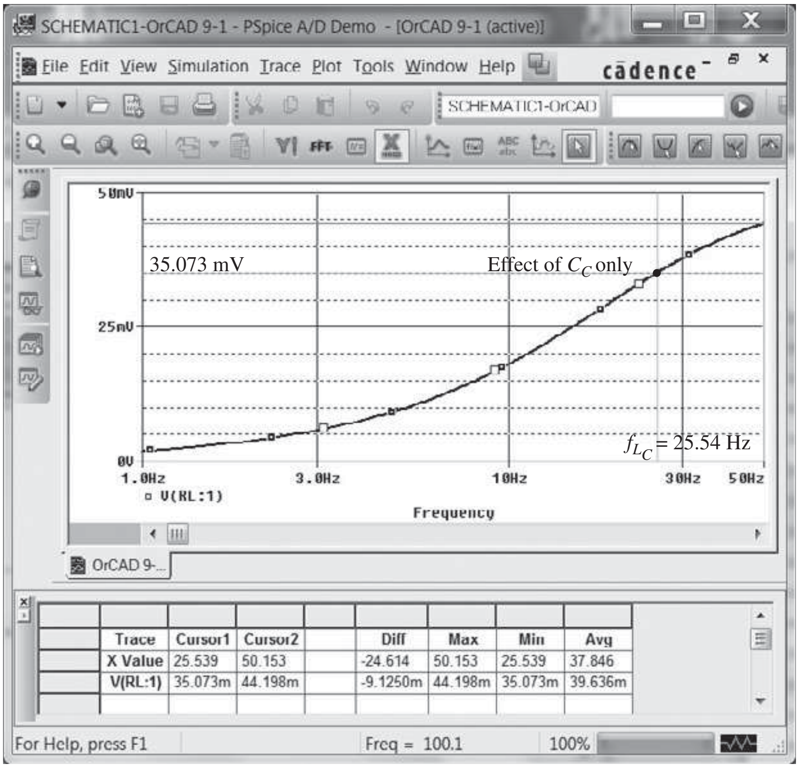
Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	6.6786	50.153		-43.474	50.153	6.6786	28.416
V(RL:1)	35.013m	49.247m		-14.234m	49.247m	35.013m	42.130m

For Help, press F1 Freq = 100.1 100%

FIG. 9.65

Low-frequency response due to C_s.

Going to **Trace-Cursor** results in intersecting lines whose horizontal and vertical values at the intersection appear in the **Probe Cursor** box in the bottom right of the plot. Moving **Cursor 1** along the curve until we are as close to the 35.13-mV level as possible results in the intersection shown in Fig. 9.65 at 35.13 mV. Note that the corresponding frequency is 6.6786 Hz, which corresponds very closely to the predicted value of 6.69 Hz. **Cursor 2**


SCHEMATIC1-OrCAD 9-1 - PSpice A/D Demo - [OrCAD 9-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
50mV
25mV
0V
35.073 mV
Effect of C_C only
f_{L_C} = 25.54 Hz
1.0Hz
3.0Hz
10Hz
30Hz
50Hz
V(RL:1)
Frequency
OrCAD 9-...

Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	25.539	50.153		-24.614	50.153	25.539	37.846
V(RL:1)	35.073m	44.198m		-9.1250m	44.198m	35.073m	39.636m

For Help, press F1 Freq = 100.1 100%

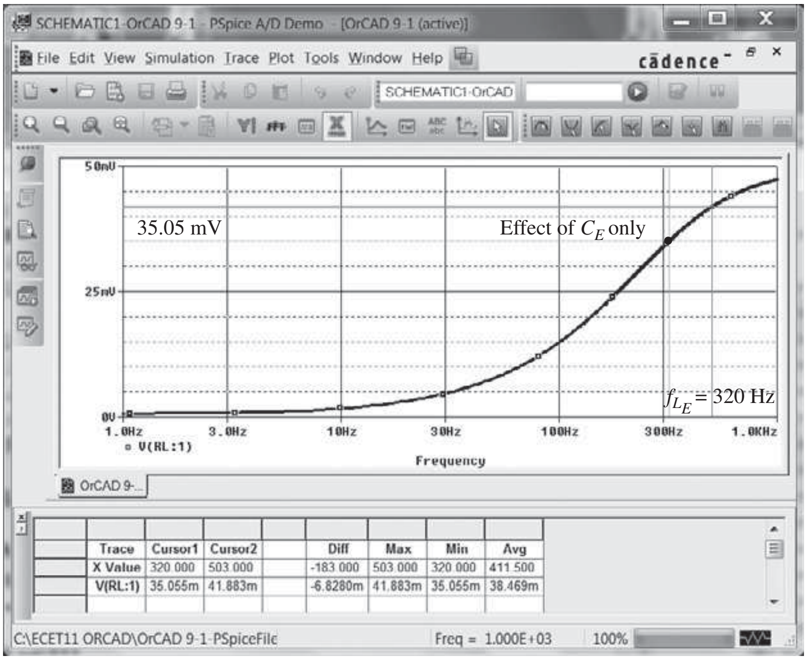
FIG. 9.66

Low-frequency response to C_C.

was placed close to 50 Hz to obtain a level of 49.247 mV. The labels were added using the **Tools-Label-Text** option.

To investigate the effects of C_C on the lower cutoff frequency, both C_S and C_E must be set to 1 F as described above. Following the procedure outlined above results in the plot of Fig. 9.66, with a cutoff frequency of 25.539 Hz, providing a close match with the calculated level of 25.68 Hz.

The effect of C_E can be examined using PSpice Windows by setting both C_s and C_C to 1 F. In addition, because the frequency range is greater, the start frequency has to be changed to 10 Hz and the final frequency to 1 kHz. The result is the plot of Fig. 9.67, with a cutoff frequency of 320 Hz, providing a close match with the calculated value of 327 Hz.



Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	320.000	503.000		-183.000	503.000	320.000	411.500
V(RL:1)	35.055m	41.883m		-6.8280m	41.883m	35.055m	38.469m

FIG. 9.67

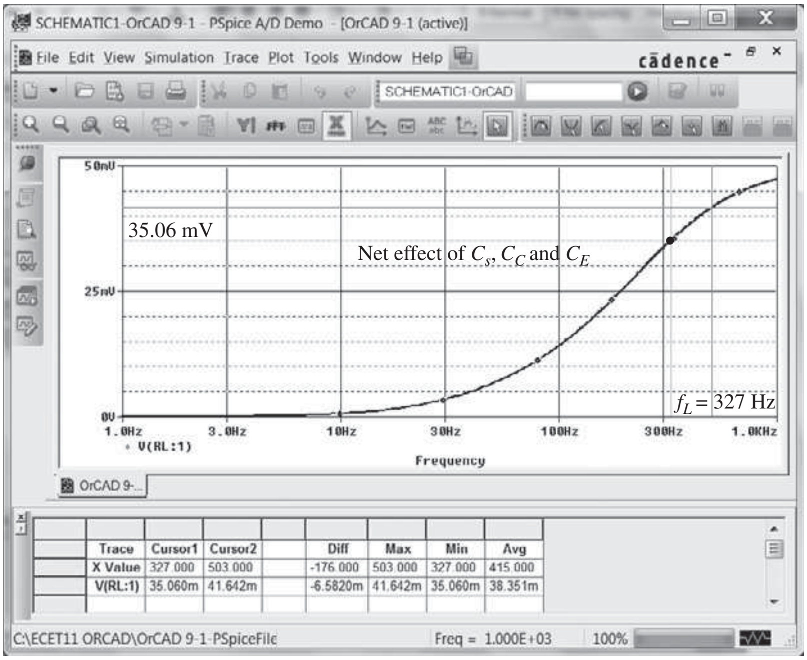
Low-frequency response due to C_E.

The fact that f_{L_E} is significantly higher than f_{L_S} or f_{L_C} suggests that it will be the predominant factor in determining the low-frequency response for the complete system. To test the accuracy of our hypothesis, the network is simulated with all the initial values of capacitance level to obtain the results of Fig. 9.68. Note the strong similarity with the waveform of Fig. 9.67, with the only visible difference being the higher gain at lower frequencies on Fig. 9.67. Without question, the plot supports the fact that the highest of the low cutoff frequencies will have the most impact on the low cutoff frequency for the system. The result is that $f_L \cong 327$ Hz.

A dB plot of the low-frequency response can be obtained by creating a **Simulation** for the frequency range and then, when the **Add Traces** dialog box appears, creating the desired **Trace Expression** using the provided listings. For a plot of $20 \log_{10}|A_v/A_{v_{\text{mid}}}|$ the ratio $A_v/A_{v_{\text{mid}}}$ can also be written as $(V_o/V_i)/(V_{o_{\text{mid}}}/V_i) = V_o/V_{o_{\text{mid}}}$, resulting in the following expression for the dB gain:

$$20 \log_{10} |A_v/A_{v_{\text{mid}}}| = 20 \log_{10}|V_o/V_{o_{\text{mid}}}| = \text{dB}(V_o/V_{o_{\text{mid}}}) = \text{dB}(V_{R_L}/49.7 \text{ mV})$$

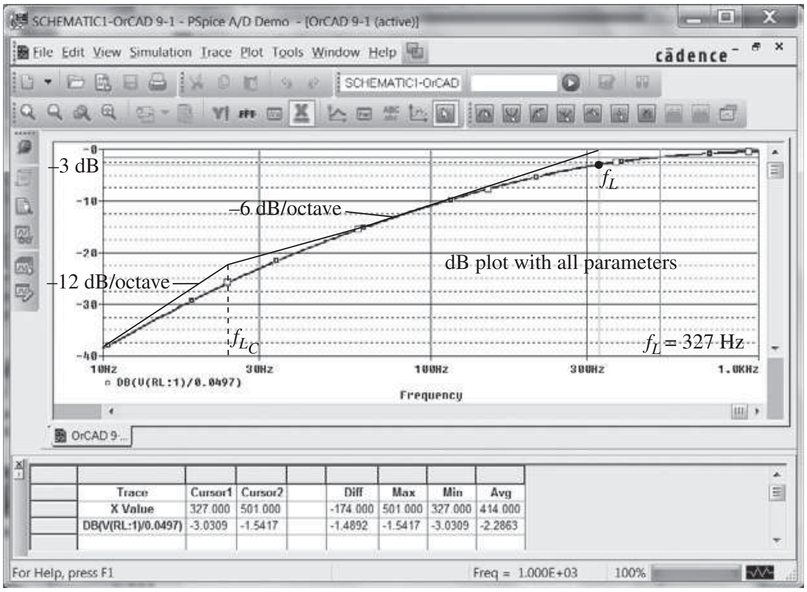
The **Trace Expression** can be created by first selecting **DB** from the **Function** list and then selecting **V(RL:1)** from the **Simulation Output Variable** list. Note that the second selection will appear within the parentheses of the first. Then be sure to enter the division sign and the number 0.0497 V = 49.7 mV within the parentheses. Of course, the entire expression can be written directly if you prefer not to use the listings. Once the expression is properly written, select **OK** and the plot of Fig. 9.69 will result. The plot clearly reveals the change in slope of the asymptote at f_{L_C} and how the actual curve follows the envelope created by the Bode plot. In addition, note the 3-dB drop at f_L.


SCHEMATIC1-OrCAD 9-1 - PSpice A/D Demo - [OrCAD 9-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
50mV
25mV
0V
35.06 mV
Net effect of C_s, C_C and C_E
f_L = 327 Hz
1.0Hz
3.0Hz
10Hz
30Hz
100Hz
300Hz
1.0KHz
V(RL:1)
Frequency
OrCAD 9-...
C:\ECET11 ORCAD\OrCAD 9-1-PSpiceFile
Freq = 1.000E+03
100%

Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	327.000	503.000		-176.000	503.000	327.000	415.000
V(RL:1)	35.060m	41.642m		-6.5820m	41.642m	35.060m	38.351m

FIG. 9.68

Low-frequency response due to C_S, C_E, and C_C.


SCHEMATIC1-OrCAD 9-1 - PSpice A/D Demo - [OrCAD 9-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
-0
-10
-20
-30
-40
−3 dB
−6 dB/octave
−12 dB/octave
dB plot with all parameters
f_L
f_{L_C}
f_L = 327 Hz
10Hz
30Hz
100Hz
300Hz
1.0KHz
DB(V(RL:1)/0.0497)
Frequency
OrCAD 9-...
For Help, press F1
Freq = 1.000E+03
100%

Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
X Value	327.000	501.000		-174.000	501.000	327.000	414.000
DB(V(RL:1)/0.0497)	-3.0309	-1.5417		-1.4892	-1.5417	-3.0309	-2.2863

FIG. 9.69

dB plot of the low-frequency response of the BJT amplifier of Fig. 9.32.

Low-Frequency JFET Response

PSpice Applying PSpice to the network of Fig. 9.37 results in the display of Fig. 9.70. The JFET parameters were set at **Beta** = 0.5 mA/V^2 and **Vto** at -4 V with all other parameters in the model listing deleted. The frequency of interest is 10 kHz. The resulting dc levels confirm that V_{GS} is -2 V with V_D at 10.60 V, which should be in the middle of the linear active region because $V_{GS} = \frac{1}{2} V_D$ and $V_{DS} = \frac{1}{2} V_{DD}$. The ac response reveals that the output voltage is 2.993 mV for a gain of 2.993, which is essentially equal to the calculated gain of 3.

If we establish a **New Simulation** and set the **Analysis type** to **AC Sweep/Noise,** we can generate a plot for the low-frequency region. The **Start Frequency** is set at 10 Hz, the

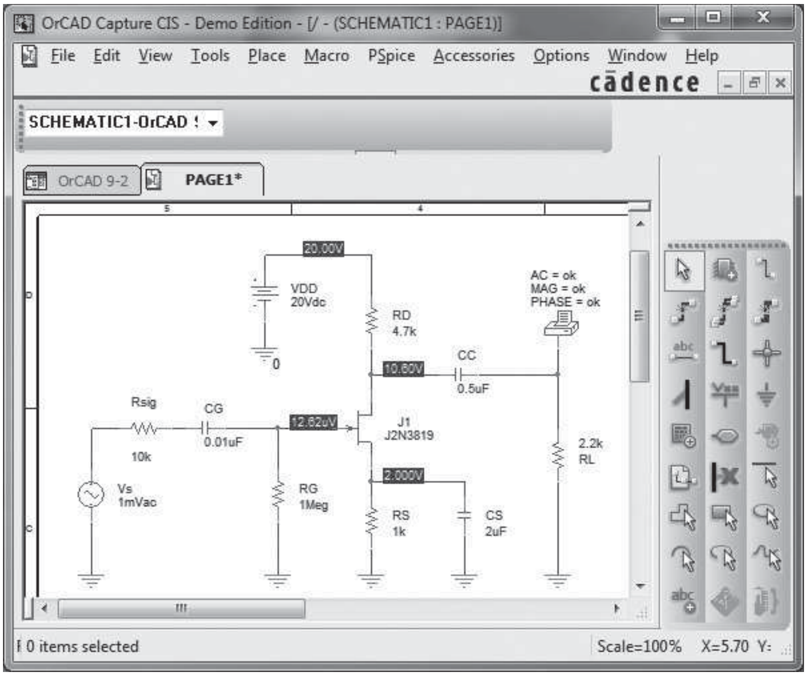
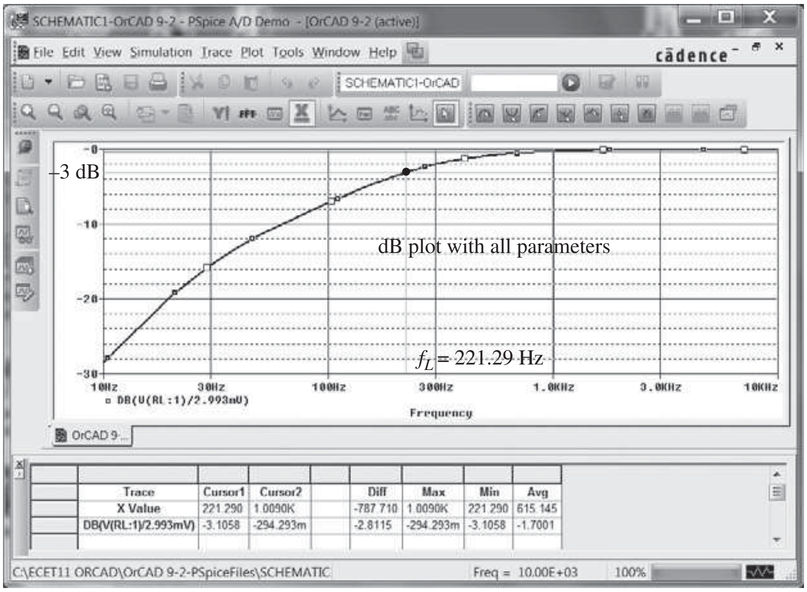

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 9-2
PAGE1*
20.00V
VDD
20Vdc
0
RD
4.7k
10.60V
CC
0.5uF
AC = ok
MAG = ok
PHASE = ok
Rsig
CG
10k
0.01uF
12.62uV
J1
J2N3819
2.2k
RL
Vs
1mVac
RG
1Meg
2.000V
RS
1k
CS
2uF
0 items selected
Scale=100%
X=5.70 Y:

FIG. 9.70
Schematic network for Example 9.13.

End Frequency at 10 kHz, and the number of **Points** at 1000. The sequence **Simulation-Trace-Add Trace** then permits establishing the **Trace Expression DB(V(RL:1)/2.993 mV),** which, following an **OK,** results in the plot of Fig. 9.71. The low cutoff frequency of 221.29 Hz was primarily determined by the capacitance **CS.**


SCHEMATIC1-OrCAD 9-2 - PSpice A/D Demo - [OrCAD 9-2 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
-0
–3 dB
-10
dB plot with all parameters
-20
f_L = 221.29 Hz
-30
10Hz
30Hz
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
□ DB(V(RL:1)/2.993mV)
Frequency
OrCAD 9-...
C:\ECET11 ORCAD\OrCAD 9-2-PSpiceFiles\SCHEMATIC
Freq = 10.00E+03
100%

Trace	Cursor1	Cursor2	Diff	Max	Min	Avg
X Value	221.290	1.0090K	-787.710	1.0090K	221.290	615.145
DB(V(RL:1)/2.993mV)	-3.1058	-294.293m	-2.8115	-294.293m	-3.1058	-1.7001

FIG. 9.71
dB response for the low-frequency region in the network of Example 9.13.

Multisim Multisim can also provide a frequency plot of the gain and phase response of a BJT or a JFET network by first constructing the network or calling it up from storage. Because the network of Fig. 9.70 is the same as that analyzed using Multisim in Chapter 8, Fig. 8.63 is retrieved and displayed as Fig. 9.72 with its dc levels at the drain and source terminals. Next the sequence **Simulate-Analyses-AC Analysis** is applied to obtain the **AC Analysis** dialog box. Under **Frequency Parameters,** the **Start frequency** is selected as **10 Hz** and the **Stop frequency** as **10 kHz** to match the plot of Fig. 9.71. The **Sweep type** is left at the default selection of **decade,** and the **Number of points** per decade is also left at **100.** Finally, the vertical scale is set in the linear mode because it is the magnitude of the output voltage versus frequency rather than the dB gain as in Fig. 9.71.

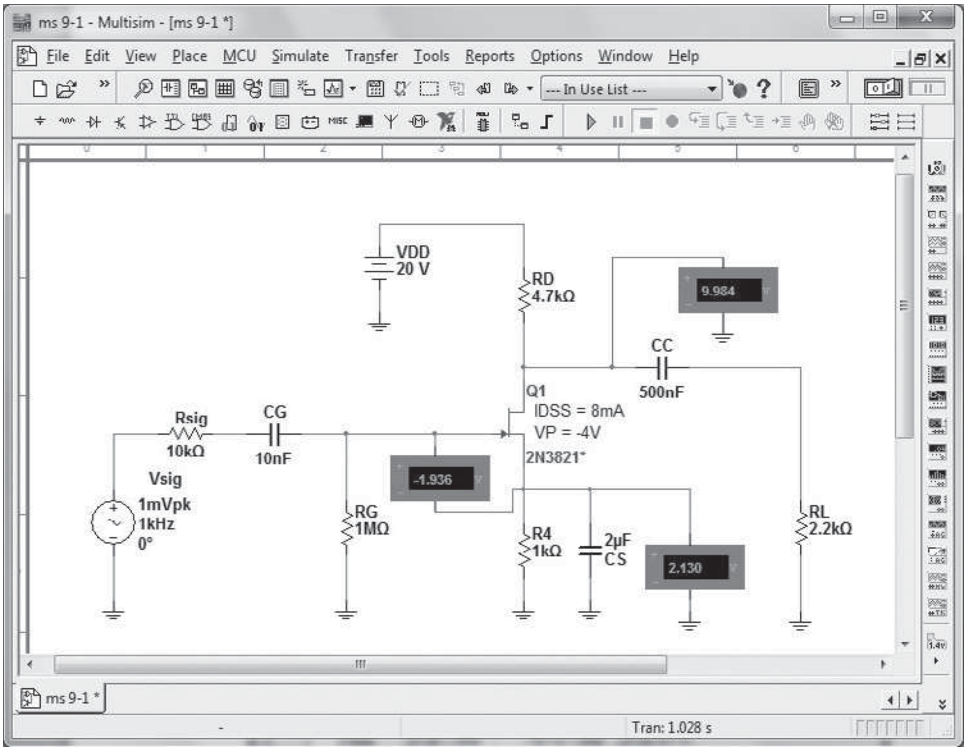


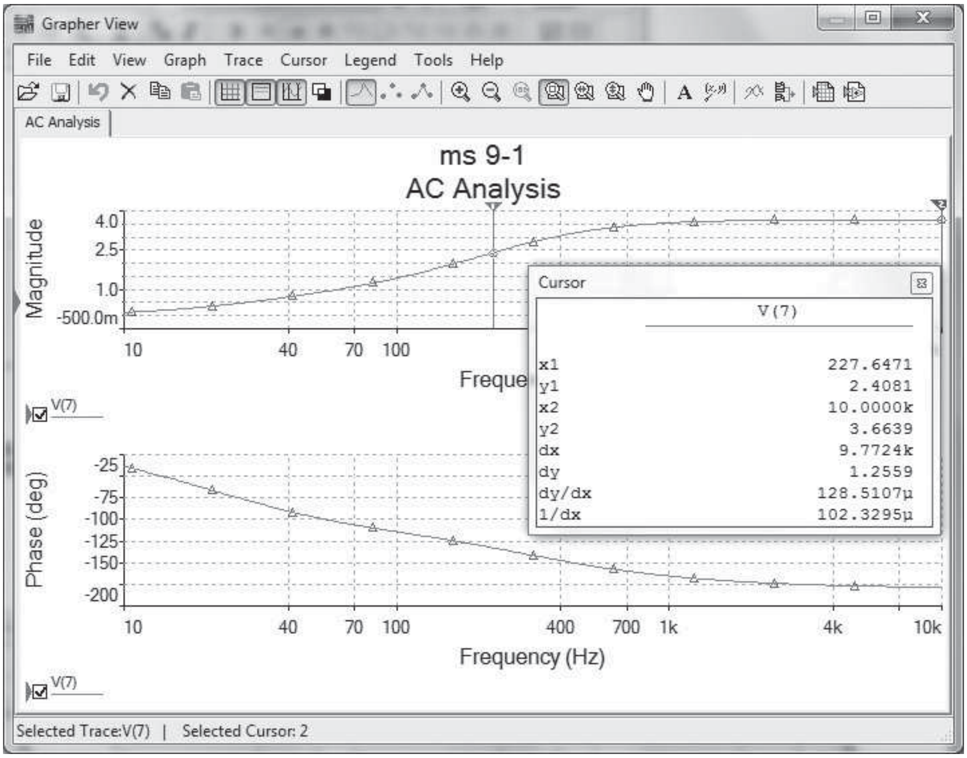
FIG. 9.72

Examining the network of Fig. 9.37 (Example 9.13) using Multisim.

Next, **Output variables** are selected in the dialog box. Under the heading **Variables in circuit,** select **Voltage** to reduce the number of options. Because we want a plot of the output voltage versus frequency, we select **$24** under **Variables in circuit,** followed by **Add** to place it in the **Selected variables for analysis.** We then choose **Simulate,** and the plot of Fig. 9.73 results.

At first, the plot may appear without a grid structure to help define the levels at each frequency. This is corrected by the sequence **View-Show/Hide Grid** as shown in Fig. 9.73. Always be aware that the red arrow along the left vertical column defines the plot under review. To add the grid to the phase plot, simply click on the lower graph at any point, and the red arrow will drop down. Then follow with the same sequence as above to establish the grid structure. If you want the graph to fill the entire screen, simply select the full-screen option at the top right corner of the **Analysis Graphs.**

Finally, cursors can be added to define the level of the plotted function at any frequency. Simply select **View-Show/Hide Cursors,** and the cursors will appear on the selected graph (which is the magnitude plot in Fig. 9.73). Then click on cursor 1, and the **AC Analysis** dialog box on the screen will reveal the level of the voltage and the frequency. By clicking on cursor 1 and moving it to the right, we can find an **x1** value of 227.65 to match the −3-dB point of Fig. 9.71. At this frequency the output voltage **(y1)** is 2.41 V, which is very close to the 0.707 level of the 2.93 gain (actually 2.07 V) obtained in Chapter 8. Cursor 2 was moved to an **x2** value of 10 kHz to obtain a voltage of 3.67 V. Before leaving Fig. 9.73, note that the higher the frequency, the closer is the phase shift to 180° as the relatively large, low-frequency capacitors lose their effect.


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
AC Analysis
ms 9-1
AC Analysis
Magnitude
4.0
2.5
1.0
-500.0m
10
40
70
100
Freque
V(7)
Phase (deg)
-25
-75
-100
-125
-150
-200
10
40
70
100
400
700
1k
4k
10k
Frequency (Hz)
V(7)
Cursor

```
        V(7)
x1      227.6471
y1      2.4081
x2      10.0000k
y2      3.6639
dx      9.7724k
dy      1.2559
dy/dx   128.5107μ
1/dx    102.3295μ
```

Selected Trace:V(7) | Selected Cursor: 2

FIG. 9.73
Multisim plot for Example 9.13.

Full-Frequency BJT Response

PSpice To obtain a PSpice analysis for the full frequency range for the network of Fig. 9.32, the parasitic capacitances have been added to the network as shown in Fig. 9.74.

An **Analysis** will result in the plot of Fig. 9.75 using the **Trace Expression** appearing at the bottom of the plot. The vertical scale was changed from −60 to 0 dB to −30 to 0 dB to highlight the area of interest using the **Y-Axis Settings.** The low-cutoff frequency

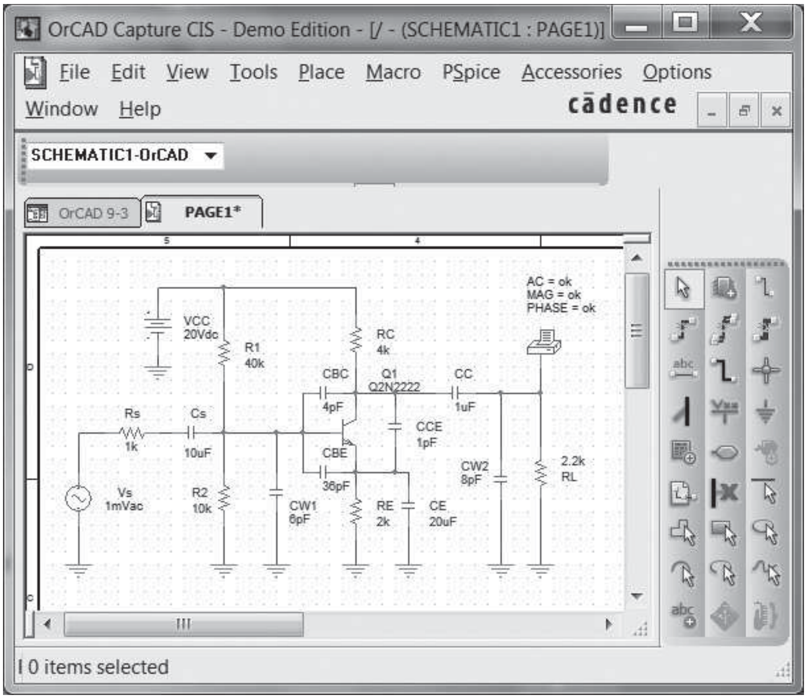
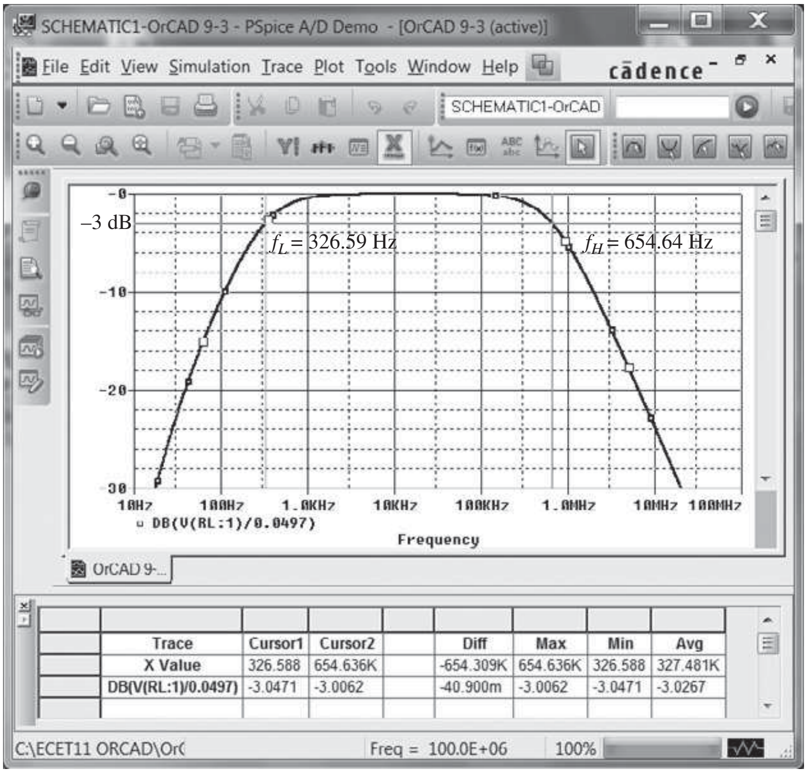

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options
Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 9-3
PAGE1*
AC = ok
MAG = ok
PHASE = ok
VCC
20Vdc
R1
40k
RC
4k
CBC
4pF
Q1
Q2N2222
CC
1uF
Rs
1k
Cs
10uF
CCE
1pF
CBE
36pF
CW2
8pF
2.2k
RL
Vs
1mVac
R2
10k
CW1
6pF
RE
2k
CE
20uF
0 items selected

FIG. 9.74
Network of Fig. 9.32 with parasitic capacitances in place.


SCHEMATIC1-OrCAD 9-3 - PSpice A/D Demo - [OrCAD 9-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
–3 dB
f_L = 326.59 Hz
f_H = 654.64 Hz
-0
-10
-20
-30
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
DB(V(RL:1)/0.0497)
Frequency
OrCAD 9-...
C:\ECET11 ORCAD\Or(
Freq = 100.0E+06
100%

Trace	Cursor1	Cursor2	Diff	Max	Min	Avg
X Value	326.588	654.636K	-654.309K	654.636K	326.588	327.481K
DB(V(RL:1)/0.0497)	-3.0471	-3.0062	-40.900m	-3.0062	-3.0471	-3.0267

FIG. 9.75

Full frequency response for the network of Fig. 9.74.

of 326.59 Hz is as determined primarily by f_{L_E}, and the high-cutoff frequency is near 654.64 kHz. Even though f_{H_o} is more than a decade higher than f_{H_i}, it will have an effect on the high-cutoff frequency. In total, however, the PSpice analysis is a welcome verification of the handwritten approach.

Full-Frequency JFET Response

PSpice The schematic for the network of Fig. 9.55 appears as shown in Fig. 9.76 with the parasitic capacitances in place.

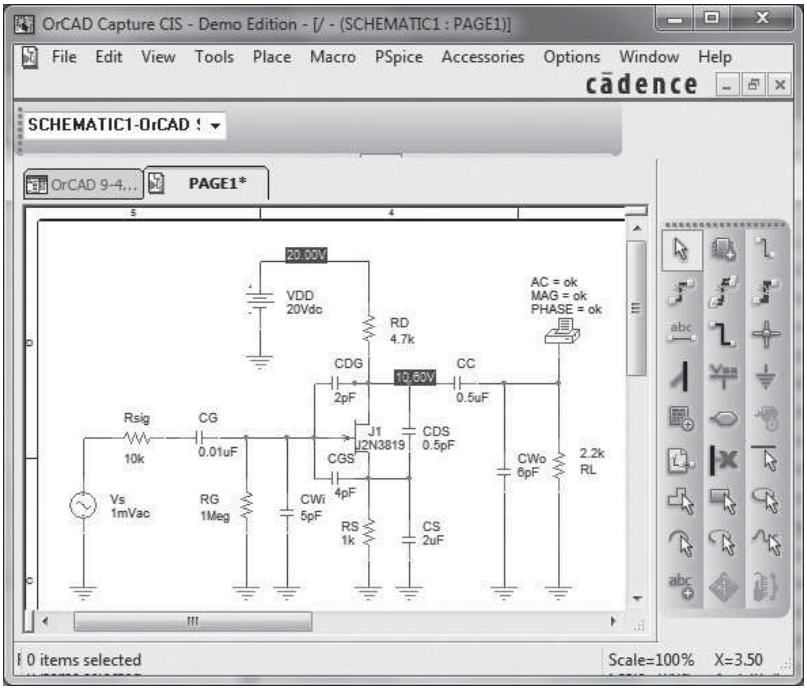
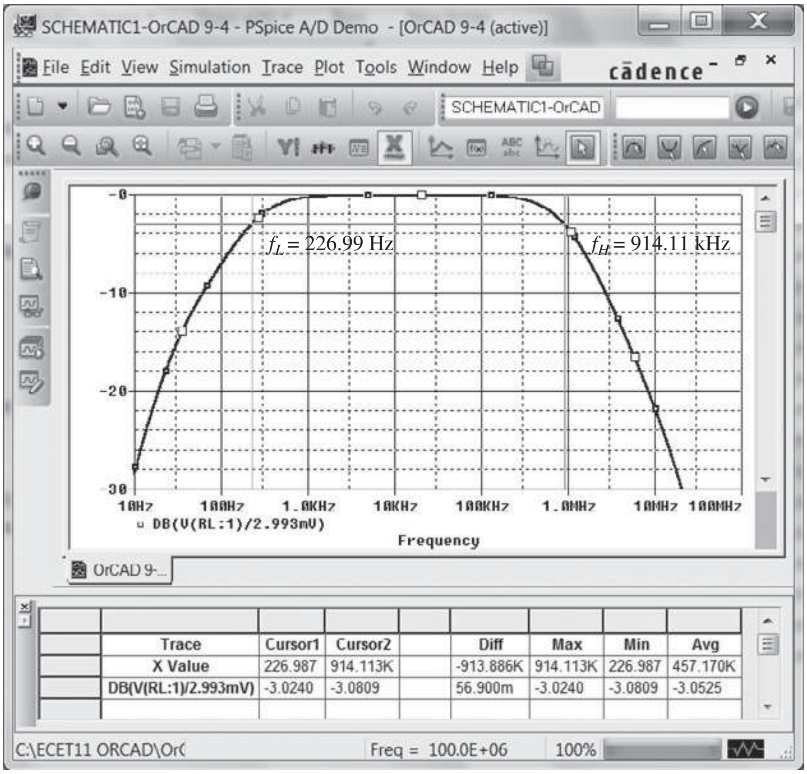

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 9-4...
PAGE1*
20.00V
VDD
20Vdc
RD
4.7k
AC = ok
MAG = ok
PHASE = ok
CDG
2pF
10.60V
CC
0.5uF
Rsig
10k
CG
0.01uF
J1
J2N3819
CDS
0.5pF
CGS
4pF
CWo
6pF
2.2k
RL
Vs
1mVac
RG
1Meg
CWi
5pF
RS
1k
CS
2uF
0 items selected
Scale=100%
X=3.50

FIG. 9.76

Network of Fig. 9.55 with assigned values.


SCHEMATIC1-OrCAD 9-4 - PSpice A/D Demo - [OrCAD 9-4 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD
f_L = 226.99 Hz
f_H = 914.11 kHz
-0
-10
-20
-30
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
DB(V(RL:1)/2.993mV)
Frequency
OrCAD 9-...
C:\ECET11 ORCAD\Or(
Freq = 100.0E+06
100%

	Trace	Cursor1	Cursor2		Diff	Max	Min	Avg
	X Value	226.987	914.113K		-913.886K	914.113K	226.987	457.170K
	DB(V(RL:1)/2.993mV)	-3.0240	-3.0809		56.900m	-3.0240	-3.0809	-3.0525

FIG. 9.77

Frequency response for the network of Example 9.15.

For the full frequency response the **Start Frequency** is set at 10 Hz and the **End Frequency** at 10 MHz, and 1000 **Points** is selected. The **Trace Expression** is set as **DB(V(RL:1)/2.993 mV)** to obtain the plot of Fig. 9.77. Consider how much time it would take to sketch the curve of Fig. 9.77 using a handheld calculator. We often forget how computer methods can save us an enormous amount of time.

Using the cursor, we find the lower and upper cutoff frequencies to be 226.99 Hz and 914.11 kHz, respectively, providing a nice match with the calculated values.

PROBLEMS

**Note*: Asterisks indicate more difficult problems.

9.2 Logarithms

1. **a.** Determine the common logarithm of the following numbers: 10^3, 50, and 0.707.
b. Determine the natural logarithm of the numbers appearing in part (a).
c. Compare the solutions of parts (a) and (b).

2. **a.** Determine the common logarithm of the number 0.24×10^6.
b. Determine the natural logarithm of the number of part (a) using Eq. (9.4).
c. Determine the natural logarithm of the number of part (a) using natural logarithms and compare with the solution of part (b).

3. Determine:
a. $20 \log_{10}(\frac{84}{6})$ using Eq. (9.6) and compare with $20 \log_{10} 14$.
b. $10 \log_{10}(\frac{1}{250})$ using Eq. (9.7) and compare with $10 \log_{10} 4 \times 10^{-3}$.
c. $\log_{10}(40)(0.2)$ using Eq. (9.8) and compare with $\log_{10} 8$.

4. Calculate the power gain in decibels for each of the following cases.
a. $P_o = 100$ W, $P_i = 5$ W.
b. $P_o = 100$ mW, $P_i = 5$ mW.
c. $P_o = 100$ mW, $P_i = 20\ \mu$W.

5. Determine G_{dBm} for an output power level of 25 W.

6. Two voltage measurements made across the same resistance are $V_1 = 110$ V and $V_2 = 220$ V. Calculate the power gain in decibels of the second reading over the first reading.

7. Input and output voltage measurements of $V_i = 10\text{ mV}$ and $V_o = 25\text{ V}$ are made. What is the voltage gain in decibels?

***8.** **a.** The total decibel gain of a three-stage system is 120 dB. Determine the decibel gain of each stage if the second stage has twice the decibel gain of the first and the third has 2.7 times the decibel gain of the first.
b. Determine the voltage gain of each stage.

***9.** If the applied ac power to a system is $5\ \mu\text{W}$ at 100 mV and the output power is 48 W, determine:
a. The power gain in decibels.
b. The voltage gain in decibels if the output impedance is $40\text{ k}\Omega$.
c. The input impedance.
d. The output voltage.

9.4 General Frequency Considerations

10. Given the characteristics of Fig. 9.78, sketch:
a. The normalized gain.
b. The normalized dB gain (and determine the bandwidth and cutoff frequencies).

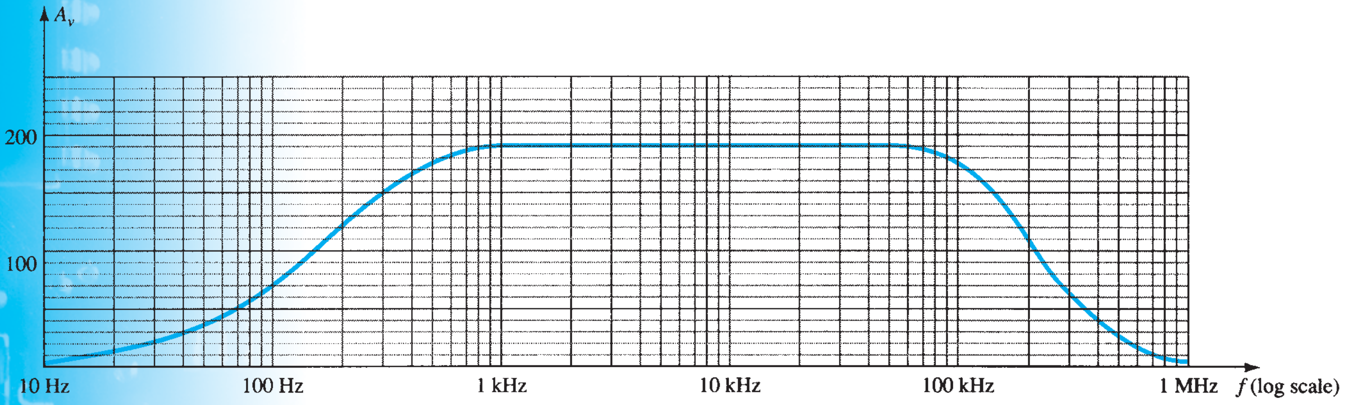


FIG. 9.78
Problem 10.

9.6 Low-Frequency Analysis–Bode Plot

11. For the network of Fig. 9.79:
a. Determine the mathematical expression for the magnitude of the ratio V_o/V_i.
b. Using the results of part (a), determine V_o/V_i at 100 Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz. Use a log scale.
c. Determine the break frequency.
d. Sketch the asymptotes and locate the −3-dB point.
e. Sketch the frequency response for V_o/V_i and compare to the results of part (b).

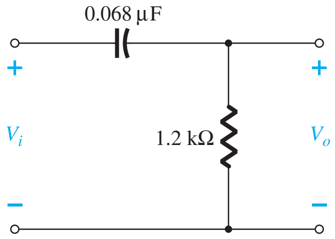


FIG. 9.79
Problems 11, 12, and 37.

12. For the network of Fig. 9.79:
a. Determine the mathematical expression for the angle by which V_o leads V_i.
b. Determine the phase angle at $f = 100$ Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz.
c. Determine the break frequency.
d. Sketch the frequency response of θ for the frequency spectrum of part (b) and compare results.

13. **a.** What frequency is one octave above 5 kHz?
b. What frequency is one decade below 10 kHz?
c. What frequency is two octaves below 20 kHz?
d. What frequency is two decades above 1 kHz?

9.7 Low-Frequency Response—BJT Amplifier with R_L

14. Repeat the analysis of Example 9.11 with $r_o = 40\ \text{k}\Omega$. What is the effect on $A_{v_{\text{mid}}}$, f_{L_S}, f_{L_C}, f_{L_E}, and the resulting cutoff frequency?

15. For the network of Fig. 9.80:
a. Determine r_e.
b. Find $A_{v_{\text{mid}}} = V_o/V_i$.
c. Calculate Z_i.
d. Determine f_{L_S}, f_{L_C}, and f_{L_E}.
e. Determine the low cutoff frequency.
f. Sketch the asymptotes of the Bode plot defined by the cutoff frequencies of part (d).
g. Sketch the low-frequency response for the amplifier using the results of part (e).

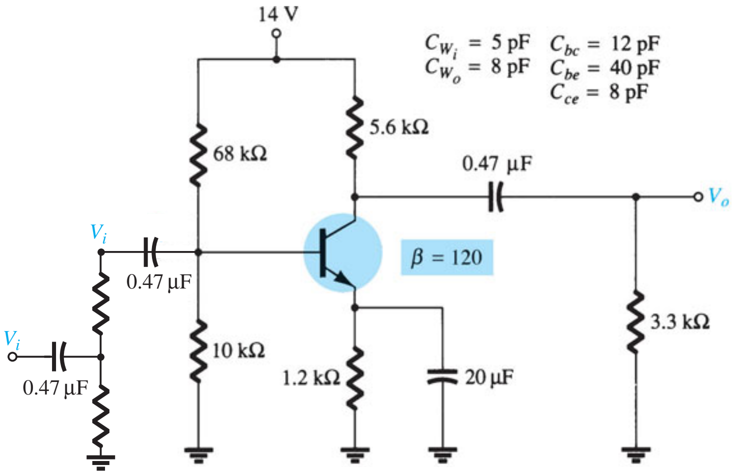

14 V
C_{W_i} = 5 pF
C_{W_o} = 8 pF
C_{bc} = 12 pF
C_{be} = 40 pF
C_{ce} = 8 pF
5.6 kΩ
68 kΩ
0.47 μF
V_o
V_i
0.47 μF
β = 120
V_i
3.3 kΩ
10 kΩ
0.47 μF
1.2 kΩ
20 μF

FIG. 9.80
Problems 15, 19, 27, and 38.

***16.** Repeat Problem 15 for the emitter-stabilized network of Fig. 9.81.

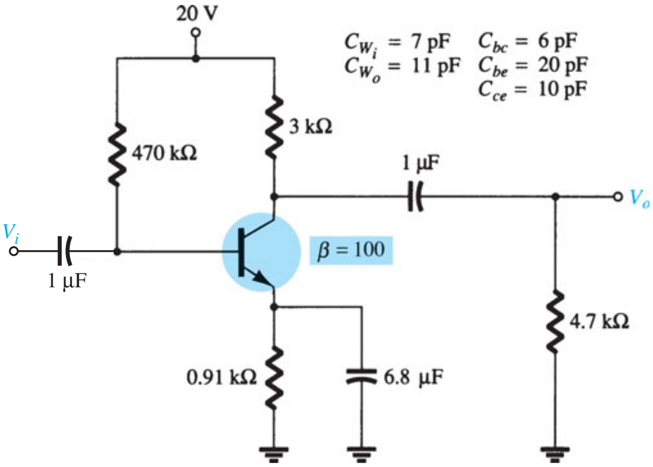

20 V
C_{W_i} = 7 pF
C_{W_o} = 11 pF
C_{bc} = 6 pF
C_{be} = 20 pF
C_{ce} = 10 pF
3 kΩ
470 kΩ
1 μF
V_o
V_i
β = 100
1 μF
4.7 kΩ
0.91 kΩ
6.8 μF

FIG. 9.81
Problems 16, 20, and 28.

***17.** Repeat Problem 15 for the emitter-follower network of Fig. 9.82.

***18.** Repeat Problem 15 for the common-base configuration of Fig. 9.83. Keep in mind that the common-base configuration is a noninverting network when you consider the Miller effect.

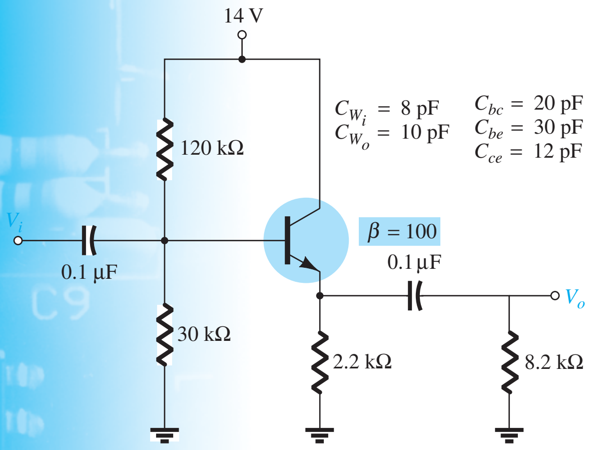

14 V
120 kΩ
C_{W_i} = 8 pF
C_{W_o} = 10 pF
C_{bc} = 20 pF
C_{be} = 30 pF
C_{ce} = 12 pF
V_i
0.1 μF
β = 100
0.1 μF
V_o
30 kΩ
2.2 kΩ
8.2 kΩ

FIG. 9.82
Problems 17, 21, and 29.

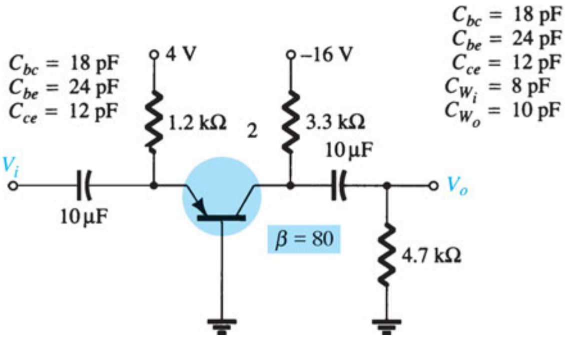

C_{bc} = 18 pF
C_{be} = 24 pF
C_{ce} = 12 pF
4 V
−16 V
1.2 kΩ
2
3.3 kΩ
10 μF
V_i
10 μF
β = 80
V_o
4.7 kΩ
C_{bc} = 18 pF
C_{be} = 24 pF
C_{ce} = 12 pF
C_{W_i} = 8 pF
C_{W_o} = 10 pF

FIG. 9.83
Problems 18, 22, and 39.

9.8 Impact of R_s on the BJT Low-Frequency Response

19. Repeat the analysis of problem 15 for the network of Fig. 9.80 with the addition of a source resistance and signal source as shown in Fig. 9.84. Plot the gain $A_{v_s} = \frac{V_o}{V_s}$ and comment on the change in low-frequency cutoff as compared to problem 15.

20. Repeat the analysis of problem 15 for the network of Fig. 9.81 with the addition of a source resistance and signal source as shown in Fig. 9.85. Plot the gain $A_{v_s} = \frac{V_o}{V_s}$ and comment on the change in low-frequency cutoff as compared to problem 16.

21. Repeat the analysis of problem 15 for the network of Fig. 9.82 with the addition of a source resistance and signal source as shown in Fig. 9.86. Plot the gain $A_{v_s} = \frac{V_o}{V_s}$ and comment on the change in low-frequency cutoff as compared to problem 17.

22. Repeat the analysis of problem 15 for the network of Fig. 9.83 with the addition of a source resistance and signal source as shown in Fig. 9.87. Plot the gain $A_{v_s} = \frac{V_o}{V_s}$ and comment on the change in low-frequency cutoff as compared to problem 18.

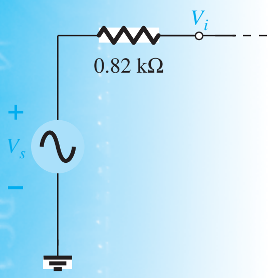


FIG. 9.84
Modification of Fig. 9.80.
Problem 19.

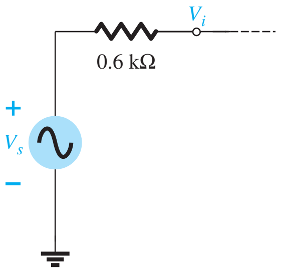


FIG. 9.85
Modification of Fig. 9.81.
Problem 20.

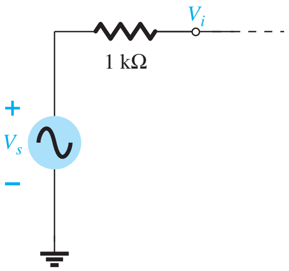


FIG. 9.86
Modification of Fig. 9.82.
Problem 21.

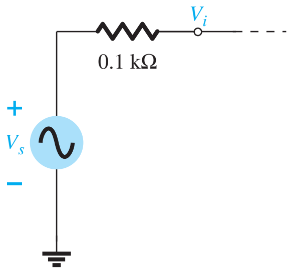


FIG. 9.87
Modification of Fig. 9.83.
Problem 22.

9.9 Low-Frequency Response—FET Amplifier

23. For the network of Fig. 9.88:

a. Determine V_{GS_Q} and I_{D_Q}.
b. Find g_{m0} and g_m.
c. Calculate the midband gain of $A_v = V_o/V_i$.
d. Determine Z_i.
e. Calculate $A_{v_s} = V_o/V_s$.
f. Determine f_{L_G}, f_{L_C}, and f_{L_S}.
g. Determine the low-cutoff frequency.
h. Sketch the asymptotes of the Bode plot defined by part (f).
i. Sketch the low-frequency response for the amplifier using the results of part (f).

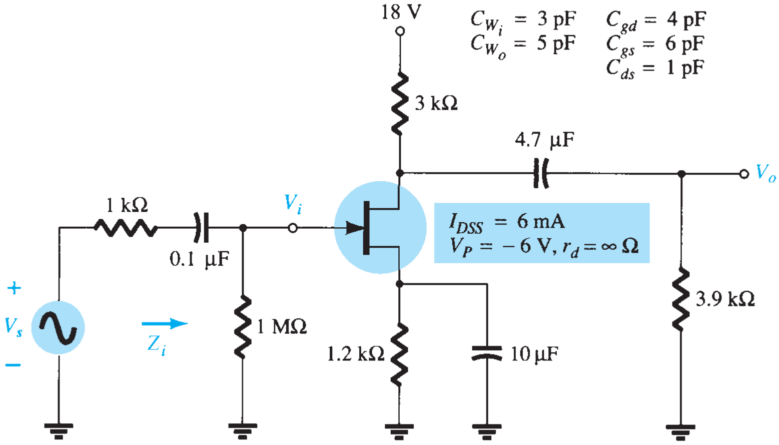

18 V
C_{W_i} = 3 pF
C_{W_o} = 5 pF
C_{gd} = 4 pF
C_{gs} = 6 pF
C_{ds} = 1 pF
3 kΩ
4.7 μF
V_o
1 kΩ
V_i
I_{DSS} = 6 mA
V_P = −6 V, $r_d = \infty\ \Omega$
0.1 μF
+
V_s
−
Z_i
1 MΩ
1.2 kΩ
10 μF
3.9 kΩ

FIG. 9.88
Problems 23, 24, 31, and 40.

***24.** Repeat the analysis of Problem 23 with $r_d = 100\ \text{k}\Omega$. Does it have an effect of any consequence on the results? If so, which elements?

***25.** Repeat the analysis of Problem 23 for the network of Fig. 9.89. What effect does the voltage-divider configuration have on the input impedance and the gain A_{v_s} compared to the biasing arrangement of Fig. 9.88?

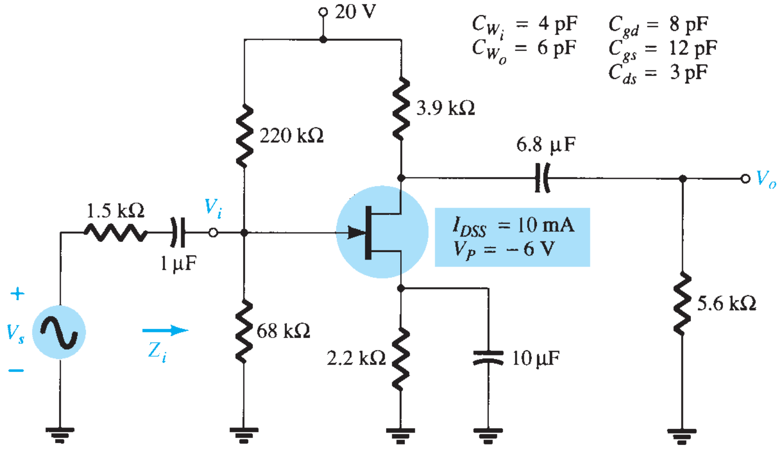

20 V
C_{W_i} = 4 pF
C_{W_o} = 6 pF
C_{gd} = 8 pF
C_{gs} = 12 pF
C_{ds} = 3 pF
3.9 kΩ
220 kΩ
6.8 μF
V_o
1.5 kΩ
V_i
I_{DSS} = 10 mA
V_P = −6 V
1 μF
+
V_s
−
Z_i
68 kΩ
2.2 kΩ
10 μF
5.6 kΩ

FIG. 9.89
Problems 25 and 32.

9.10 Miller Effect Capacitance

26. **a.** The feedback capacitance of an inverting amplifier is 10 pF. What is the Miller capacitance at the input if the gain of the amplifier is −120?
b. What is the Miller capacitance at the output of the amplifier?
c. Is it a good approximation to assume $C_{M_i} \cong |A_v|C_f$ and $C_{M_o} \cong C_f$?

9.11 High-Frequency Response—BJT Amplifier

***27.** For the network of Fig. 9.80 with R_s and V_s of Fig. 9.84:
a. Determine f_{H_i} and f_{H_o}.
b. Find f_β and f_T.
c. Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.
d. What is the gain-bandwidth product of the amplifier?

***28.** Repeat the analysis of Problem 27 for the network of Fig. 9.81 with R_s and V_s of Fig. 9.85.

***29.** Repeat the analysis of Problem 27 for the network of Fig. 9.82 with R_s and V_s of Fig. 9.86.

***30.** Repeat the analysis of Problem 27 for the network of Fig. 9.83 with R_s and V_s of Fig. 9.87.

9.12 High-Frequency Response—FET Amplifier

31. For the network of Fig. 9.88:

a. Determine g_{m0} and g_m.

b. Find A_v and A_{v_s} in the mid-frequency range.

c. Determine f_{H_i} and f_{H_o}.

d. Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

e. What is the gain-bandwidth product of the amplifier?

***32.** Repeat the analysis of Problem 31 for the network of Fig. 9.89.

9.13 Multistage Frequency Effects

33. Calculate the overall voltage gain of four identical stages of an amplifier, each having a gain of 20.

34. Calculate the overall upper 3-dB frequency for a four-stage amplifier having an individual stage value of $f_2 = 2.5$ MHz.

35. A four-stage amplifier has a lower 3-dB frequency for an individual stage of $f_1 = 40$ Hz. What is the value of f_1 for this full amplifier?

9.14 Square-Wave Testing

***36.** The application of a 10-mV, 100-kHz square wave to an amplifier resulted in the output waveform of Fig. 9.90.

a. Write the Fourier series expansion for the square wave through the ninth harmonic.

b. Determine the bandwidth of the amplifier to the accuracy available by the waveform of Fig. 9.90.

c. Calculate the low-cutoff frequency.

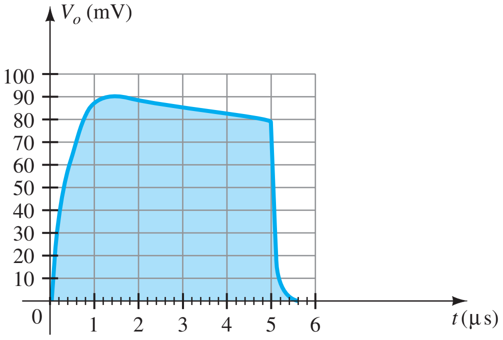


FIG. 9.90
Problem 36.

9.16 Computer Analysis

37. Using PSpice Windows, determine the frequency response of V_o/V_i for the high-pass filter of Fig. 9.45 of $R = 8.2\ \text{k}\Omega$ and $C = 4.7\ \mu\text{F}$.

38. Using PSpice Windows, determine the frequency response of V_o/V_s for the BJT amplifier of Fig. 9.87.

39. Repeat Problem 38 for the network of Fig. 9.83 using Multisim.

40. Repeat Problem 38 for the JFET configuration of Fig. 9.88 using Multisim.

10

Operational Amplifiers

CHAPTER OBJECTIVES

- Understand what a differential amplifier does
- Learn the basics of an operational amplifier
- Develop an understanding of what common mode operation is
- Describe double-ended input operation

10.1 INTRODUCTION

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 10.1 shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (−) input, respectively.

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 10.2 shows the signals connected for this operation. In Fig. 10.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 10.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure 10.3a shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 10.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.

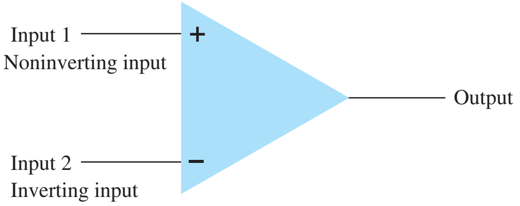
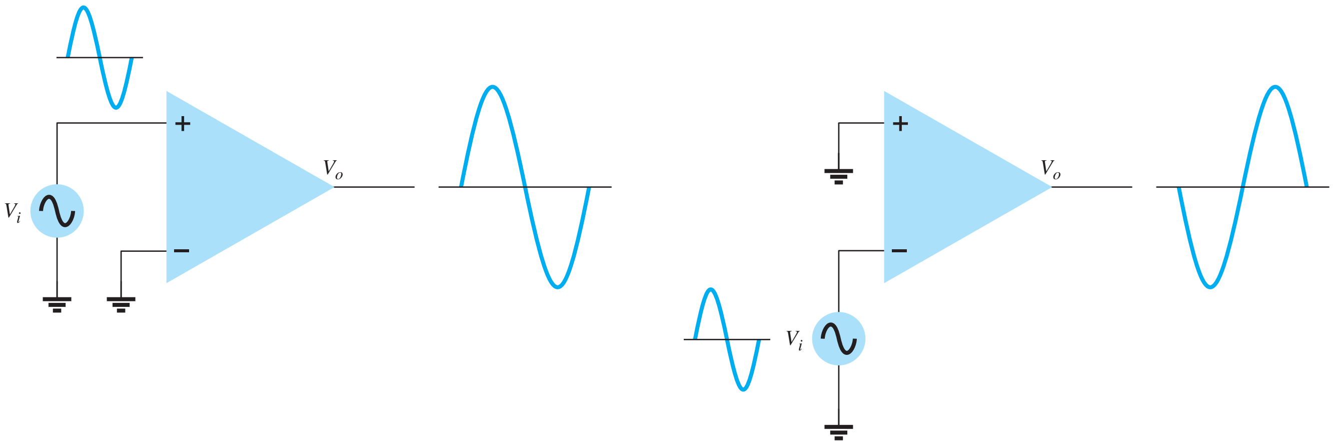
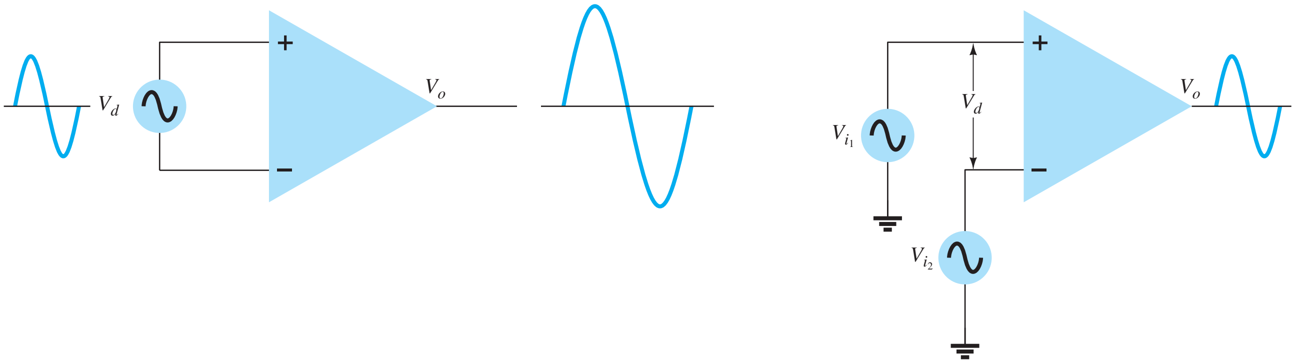


FIG. 10.1
Basic op-amp.



(a) (b)

FIG. 10.2
Single-ended operation.



(a) (b)

FIG. 10.3
Double-ended (differential) operation.

Double-Ended Output

Whereas the operation discussed so far has a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 10.4. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 10.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 10.6 shows the same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is $V_{o_1} - V_{o_2}$. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. The difference output is twice as large as either V_{o_1} or V_{o_2} because they are of opposite polarity and subtracting them results in twice their amplitude

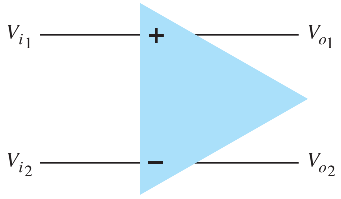


FIG. 10.4
Double-ended input with double-ended output.

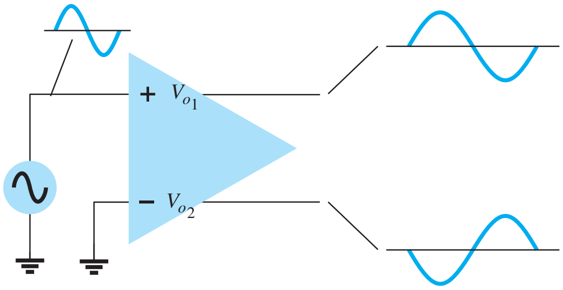


FIG. 10.5
Single-ended input with double-ended output.

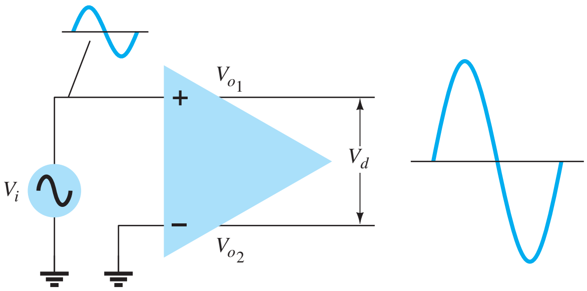


FIG. 10.6
Differential-output.

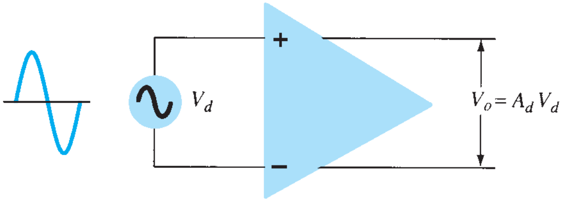


FIG. 10.7
Differential-input, differential-output operation.

[e.g., 10 V − (−10 V) = 20 V]. Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 10.8. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

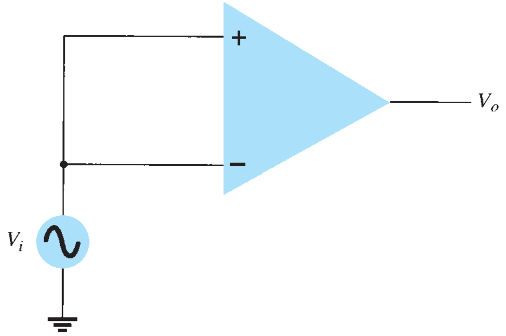


FIG. 10.8
Common-mode operation.

Common-Mode Rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection*.

10.2 DIFFERENTIAL AMPLIFIER CIRCUIT

The differential amplifier circuit is an extremely popular connection used in IC units. This connection can be described by considering the basic differential amplifier shown in Fig. 10.9. Notice that the circuit has two separate inputs and two separate outputs, and that the emitters are connected together. Whereas many differential amplifier circuits use two separate voltage supplies, the circuit can also operate using a single supply.

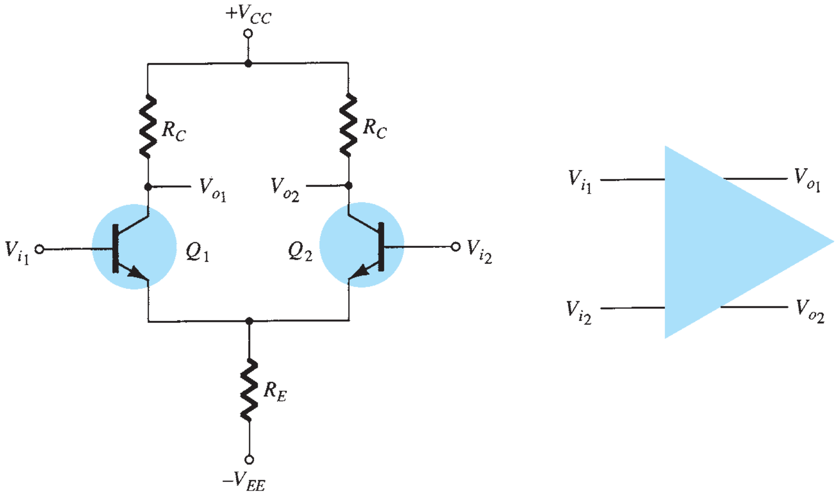


FIG. 10.9
Basic differential amplifier circuit.

A number of input signal combinations are possible:

If an input signal is applied to either input with the other input connected to ground, the operation is referred to as "single-ended."

If two opposite-polarity input signals are applied, the operation is referred to as "double-ended."

If the same input is applied to both inputs, the operation is called "common-mode."

In single-ended operation, a single input signal is applied. However, due to the common-emitter connection, the input signal operates both transistors, resulting in output from *both* collectors.

In double-ended operation, two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals at each collector, these signals canceling, so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel, and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called *common-mode rejection.*

DC Bias

Let's first consider the dc bias operation of the circuit of Fig. 10.9. With ac inputs obtained from voltage sources, the dc voltage at each input is essentially connected to 0 V, as shown in Fig. 10.10. With each base voltage at 0 V, the common-emitter dc bias voltage is

$$V_E = 0\text{ V} - V_{BE} = -0.7\text{ V}$$

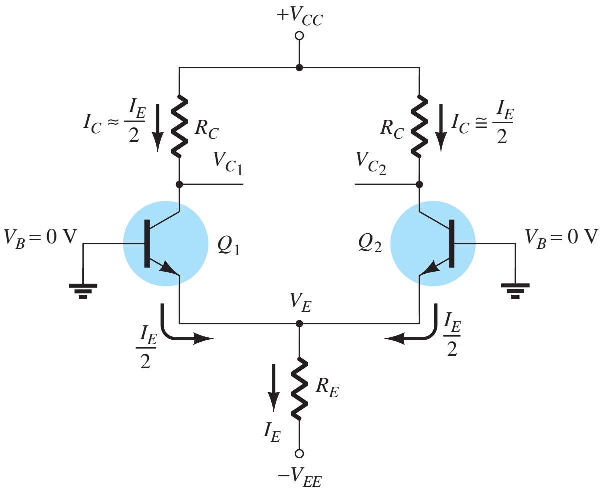

$+V_{CC}$
$I_C \approx \frac{I_E}{2}$
R_C
V_{C_1}
R_C
$I_C \cong \frac{I_E}{2}$
V_{C_2}
$V_B = 0$ V
Q_1
Q_2
$V_B = 0$ V
V_E
$\frac{I_E}{2}$
$\frac{I_E}{2}$
R_E
I_E
$-V_{EE}$

FIG. 10.10
DC bias of differential amplifier circuit.

The emitter dc bias current is then

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7\text{ V}}{R_E} \tag{10.1}$$

Assuming that the transistors are well matched (as would occur in an IC unit), we obtain

$$I_{C_1} = I_{C_2} = \frac{I_E}{2} \tag{10.2}$$

resulting in a collector voltage of

$$V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C \tag{10.3}$$

EXAMPLE 10.1 Calculate the dc voltages and currents in the circuit of Fig. 10.11.

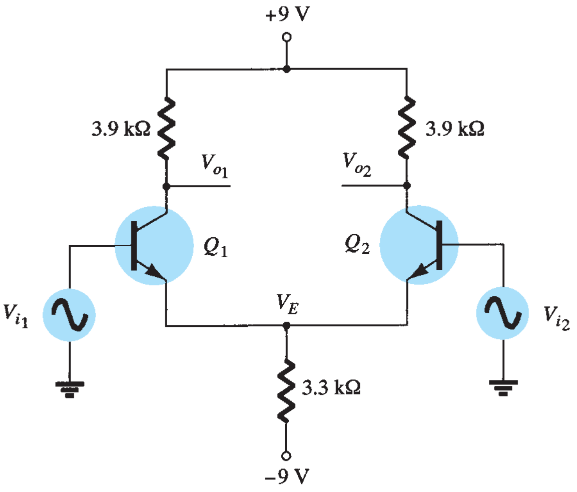

+9 V
3.9 kΩ
3.9 kΩ
V_{o_1}
V_{o_2}
Q_1
Q_2
V_{i_1}
V_E
V_{i_2}
3.3 kΩ
−9 V

FIG. 10.11
Differential amplifier circuit for Example 10.1.

Solution:

$$\text{Eq. (10.1):}\quad I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{9\text{ V} - 0.7\text{ V}}{3.3\text{ k}\Omega} \approx \mathbf{2.5\text{ mA}}$$

The collector current is then

$$\text{Eq. (10.2):}\quad I_C = \frac{I_E}{2} = \frac{2.5\text{ mA}}{2} = \mathbf{1.25\text{ mA}}$$

resulting in a collector voltage of

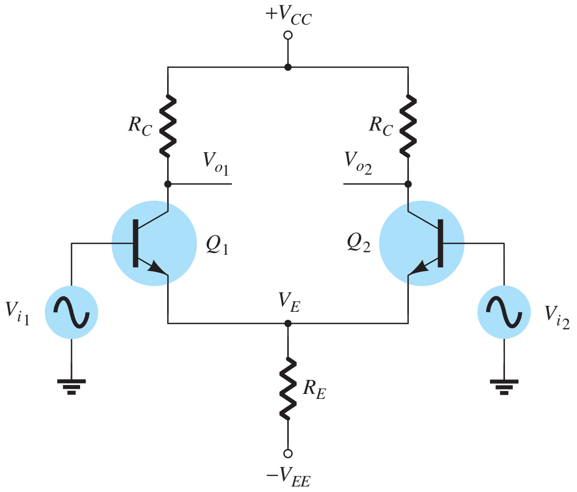
$$\text{Eq. (10.3):}\quad V_C = V_{CC} - I_C R_C = 9\text{ V} - (1.25\text{ mA})(3.9\text{ k}\Omega) \approx \mathbf{4.1\text{ V}}$$

The common-emitter voltage is thus –0.7 V, whereas the collector bias voltage is near 4.1 V for both outputs.

AC Operation of Circuit

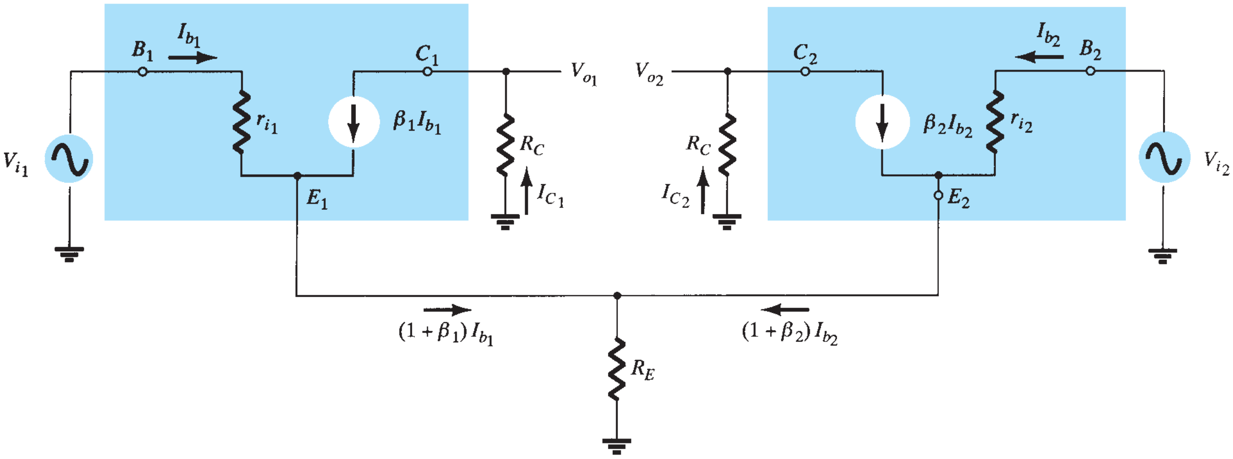
An ac connection of a differential amplifier is shown in Fig. 10.12. Separate input signals are applied as V_{i_1} and V_{i_2}, with separate outputs resulting as V_{o_1} and V_{o_2}. To carry out ac analysis, we redraw the circuit in Fig. 10.13. Each transistor is replaced by its ac equivalent.

Single-Ended AC Voltage Gain To calculate the single-ended ac voltage gain, V_o/V_i, apply signal to one input with the other connected to ground, as shown in Fig. 10.14. The



$+V_{CC}$
R_C
R_C
V_{o_1}
V_{o_2}
Q_1
Q_2
V_E
V_{i_1}
V_{i_2}
R_E
$-V_{EE}$

FIG. 10.12
AC connection of differential amplifier.



I_{b_1}
B_1
C_1
V_{o_1}
V_{o_2}
C_2
I_{b_2}
B_2
r_{i_1}
$\beta_1 I_{b_1}$
R_C
R_C
$\beta_2 I_{b_2}$
r_{i_2}
V_{i_1}
V_{i_2}
E_1
I_{C_1}
I_{C_2}
E_2
$(1+\beta_1)I_{b_1}$
$(1+\beta_2)I_{b_2}$
R_E

FIG. 10.13
AC equivalent of differential amplifier circuit.

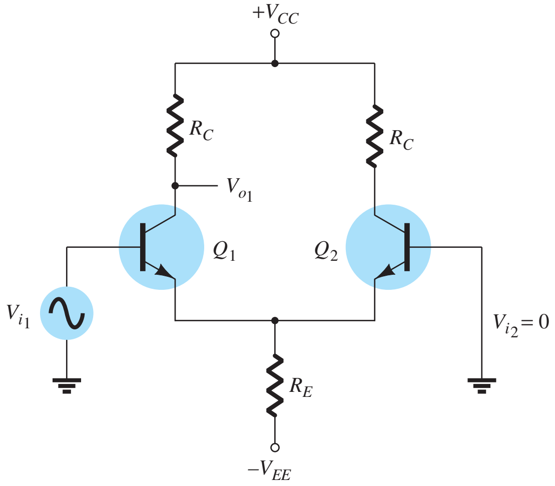

$+V_{CC}$
R_C
R_C
V_{o_1}
Q_1
Q_2
V_{i_1}
$V_{i_2} = 0$
R_E
$-V_{EE}$

FIG. 10.14

Connection to calculate $A_{V_1} = V_{o_1}/V_{i_1}$.

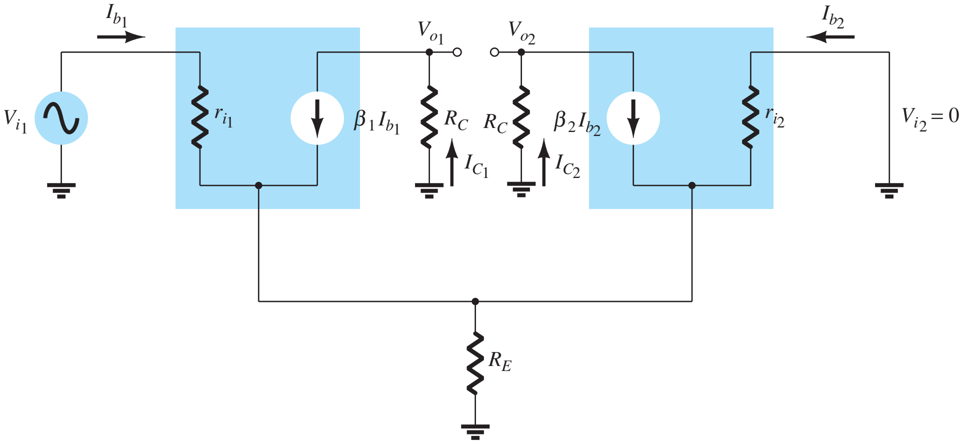

I_{b_1}
V_{o_1}
V_{o_2}
I_{b_2}
V_{i_1}
r_{i_1}
$\beta_1 I_{b_1}$
R_C
R_C
$\beta_2 I_{b_2}$
r_{i_2}
$V_{i_2} = 0$
I_{C_1}
I_{C_2}
R_E

FIG. 10.15

AC equivalent of circuit in Fig. 10.14.

ac equivalent of this connection is drawn in Fig. 10.15. The ac base current can be calculated using the base 1 input Kirchhoff voltage loop (KVL) equation. If one assumes that the two transistors are well matched, then

$$I_{b_1} = I_{b_2} = I_b$$
$$r_{i_1} = r_{i_2} = r_i = \beta r_e$$

With R_E very large (ideally infinite), the circuit for obtaining the KVL equation simplifies to that of Fig. 10.16, from which we can write

$$V_{i_1} - I_b r_i - I_b r_i = 0$$

so that

$$I_b = \frac{V_{i_1}}{2r_i} = \frac{V_i}{2\beta r_e}$$

If we also assume that

$$\beta_1 = \beta_2 = \beta$$

then

$$I_C = \beta I_b = \beta \frac{V_i}{2\beta r_e} = \frac{V_i}{2r_e}$$

and the output voltage magnitude at either collector is

$$V_o = I_C R_C = \frac{V_i}{2r_e} R_C = \frac{R_C}{2r_e} V_i$$

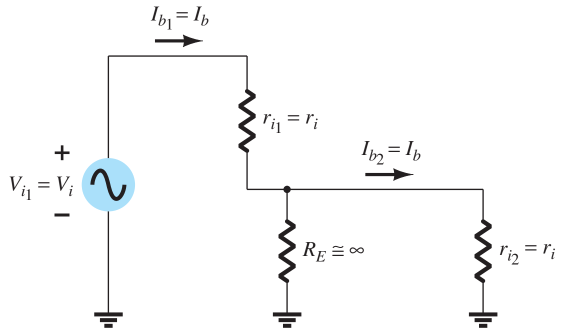

$I_{b_1} = I_b$
$r_{i_1} = r_i$
$I_{b_2} = I_b$
+
$V_{i_1} = V_i$
–
$R_E \cong \infty$
$r_{i_2} = r_i$

FIG. 10.16
Partial circuit for calculating I_b.

for which the single-ended voltage gain magnitude at either collector is

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_C}{2r_e}} \tag{10.4}$$

EXAMPLE 10.2 Calculate the single-ended output voltage V_{o_1} for the circuit of Fig. 10.17.

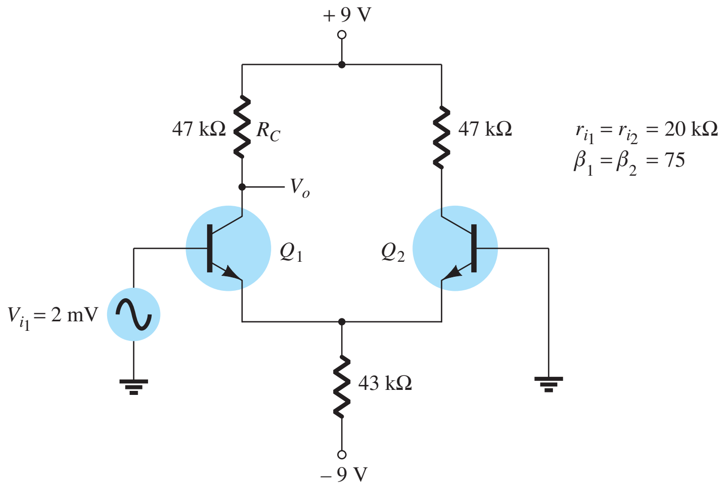

+ 9 V
47 kΩ
R_C
47 kΩ
$r_{i_1} = r_{i_2} = 20$ kΩ
$\beta_1 = \beta_2 = 75$
V_o
Q_1
Q_2
$V_{i_1} = 2$ mV
43 kΩ
– 9 V

FIG. 10.17
Circuit for Examples 10.2 and 10.3.

Solution: The dc bias calculations provide

$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{9\text{ V} - 0.7\text{ V}}{43\text{ k}\Omega} = 193\ \mu\text{A}$$

The collector dc current is then

$$I_C = \frac{I_E}{2} = 96.5\ \mu\text{A}$$

so that $V_C = V_{CC} - I_C R_C = 9\text{ V} - (96.5\ \mu\text{A})(47\text{ k}\Omega) = 4.5\text{ V}$

The value of r_e is then

$$r_e = \frac{26}{0.0965} \cong 269\ \Omega$$

The ac voltage gain magnitude can be calculated using Eq. (10.31):

$$A_v = \frac{R_C}{2r_e} = \frac{(47\text{ k}\Omega)}{2(269\ \Omega)} = 87.4$$

providing an output ac voltage of magnitude

$$V_o = A_v V_i = (87.4)(2\text{ mV}) = 174.8\text{ mV} = \mathbf{0.175\ V}$$

Double-Ended AC Voltage Gain A similar analysis can be used to show that for the condition of signals applied to both inputs, the differential voltage gain magnitude is

$$\boxed{A_d = \frac{V_o}{V_d} = \frac{R_C}{r_e}} \qquad \textbf{(10.5)}$$

where $V_d = V_{i_1} - V_{i_2}$.

Common-Mode Operation of Circuit

Whereas a differential amplifier provides large amplification of the difference signal applied to both inputs, it should also provide as small an amplification of the signal common to both inputs. An ac connection showing common input to both transistors is shown in Fig. 10.18. The ac equivalent circuit is drawn in Fig. 10.19, from which we can write

$$I_b = \frac{V_i - 2(\beta + 1)I_b R_E}{r_i}$$

which can be rewritten as

$$I_b = \frac{V_i}{r_i + 2(\beta + 1)R_E}$$

The output voltage magnitude is then

$$V_o = I_C R_C = \beta I_b R_C = \frac{\beta V_i R_C}{r_i + 2(\beta + 1)R_E}$$

providing a voltage gain magnitude of

$$\boxed{A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}} \qquad \textbf{(10.6)}$$

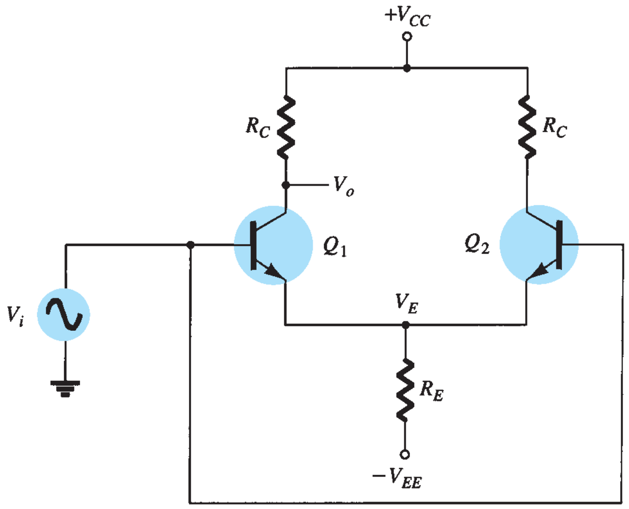


FIG. 10.18
Common-mode connection.

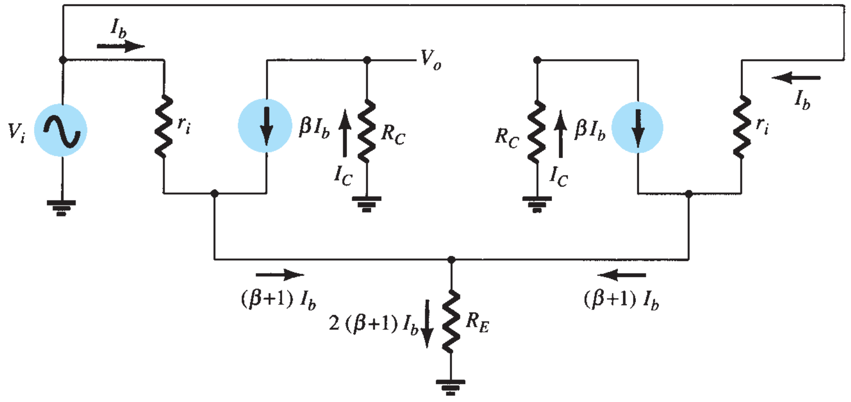


FIG. 10.19
AC circuit in common-mode connection.

EXAMPLE 10.3 Calculate the common-mode gain for the amplifier circuit of Fig. 10.17.

Solution:

$$\text{Eq. (10.6):}\quad A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\text{ k}\Omega)}{20\text{ k}\Omega + 2(76)(43\text{ k}\Omega)} = \mathbf{0.54}$$

Use of Constant-Current Source

A good differential amplifier has a very large difference gain A_d, which is much larger than the common-mode gain A_c. The common-mode rejection ability of the circuit can be considerably improved by making the common-mode gain as small as possible (ideally, 0). From Eq. (10.6), we see that the larger R_E, the smaller is A_c. One popular method for increasing the ac value of R_E is using a constant-current source circuit. Figure 10.20 shows a differential amplifier with constant-current source to provide a large value of resistance from common emitter to ac ground. The major improvement of this circuit over that in Fig. 10.9 is the much larger ac impedance for R_E obtained using the constant-current source. Figure 10.21 shows the ac equivalent circuit for the circuit of Fig. 10.20. A practical constant-current source is shown as a high impedance, in parallel with the constant current.

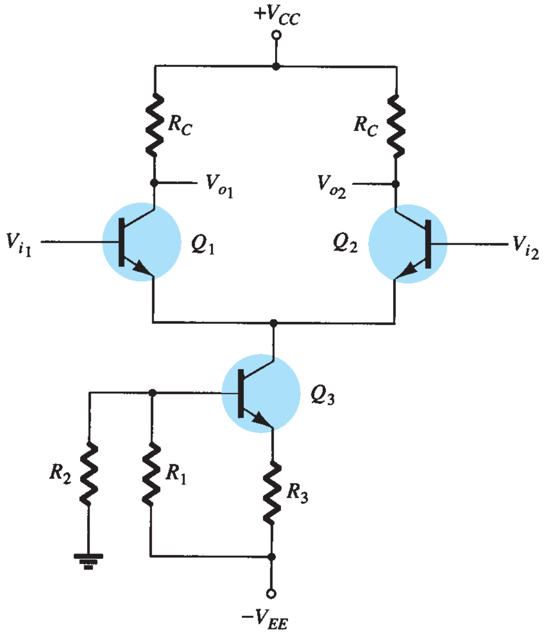


FIG. 10.20
Differential amplifier with constant-current source.

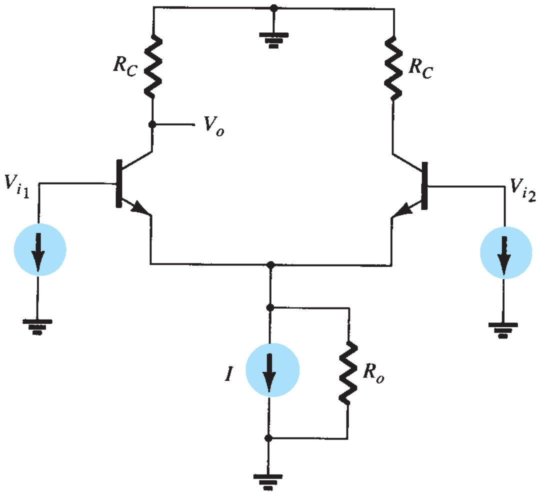


FIG. 10.21
AC equivalent of the circuit of Fig. 10.20.

EXAMPLE 10.4 Calculate the common-mode gain for the differential amplifier of Fig. 10.22.

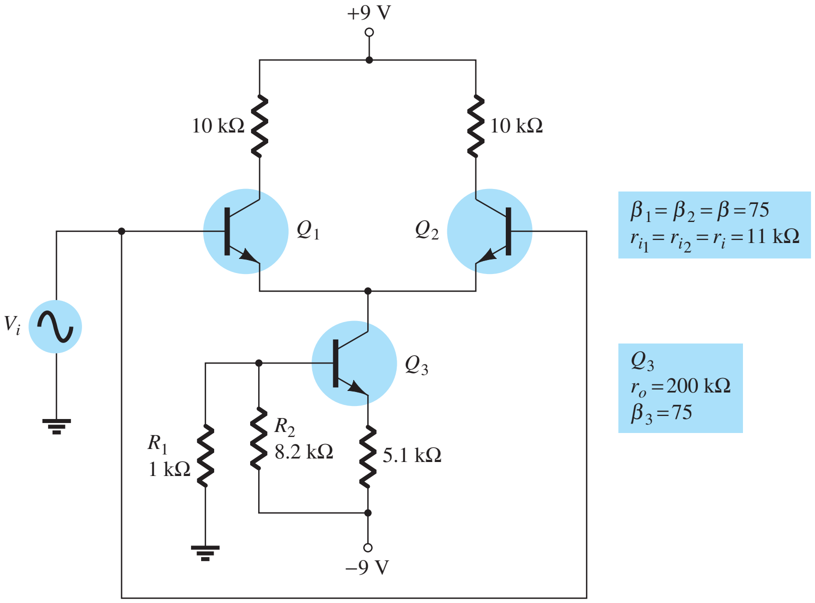


FIG. 10.22

Circuit for Example 10.4.

Solution: Using $R_E = r_o = 200\text{ k}\Omega$ gives

$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(10\text{ k}\Omega)}{11\text{ k}\Omega + 2(76)(200\text{ k}\Omega)} = \mathbf{24.7 \times 10^{-3}}$$

10.3 BiFET, BiMOS, AND CMOS DIFFERENTIAL AMPLIFIER CIRCUITS

Whereas the preceding section provided an introduction to the differential amplifier using bipolar devices, units commercially available also use JFET and MOSFET transistors to build these types of circuits. An IC unit containing a differential amplifier built using both bipolar (Bi) and junction field-effect (FET) transistors is referred to as a *BiFET circuit.* An IC unit made using both bipolar (Bi) and MOSFET (MOS) transistors is called a *BiMOS circuit.* Finally, a circuit built using opposite-type MOSFET transistors is a *CMOS circuit.*

The CMOS is a form of circuit popular in digital circuitry and uses both *n*-channel and *p*-channel enhancement MOSFET transistors (see Fig. 10.23). This complementary MOSFET or CMOS circuit uses these opposite (or complementary)-type transistors. The input V_i is applied to both gates with the output taken from the connected drains. Before going into the operation of the CMOS circuit, let's review the operation of the enhancement MOSFET transistors.

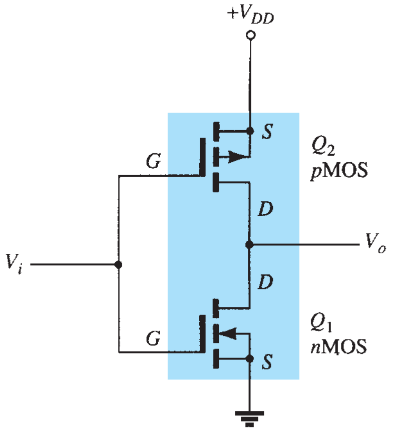


FIG. 10.23

CMOS inverter circuit.

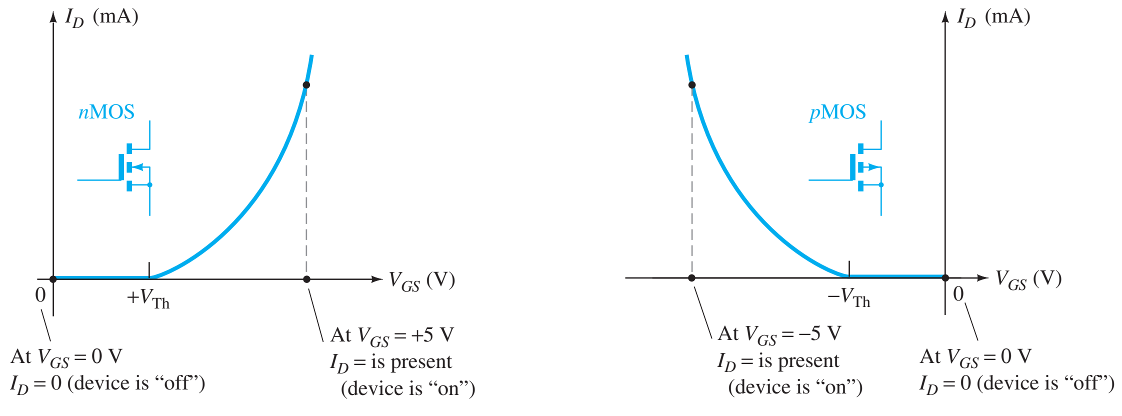
*n*MOS On/Off Operation

The drain characteristic of an *n*-channel enhancement MOSFET or *n*MOS transistor is shown in Fig. 10.24a. With 0 V applied to the gate–source, there is no drain current. Not until V_{GS} is raised past the device threshold level V_T does any current result. With an input of, say, +5 V, the *n*MOS device is fully on with current I_D present. In summary:

An input of 0 V leaves the nMOS "off," whereas an input of +5V turns the nMOS on.

*p*MOS On/Off Operation

The drain characteristic for a *p*-channel MOSFET or *p*MOS transistor is shown in Fig. 10.24b. When 0 V is applied, the device is "off" (no drain current present), whereas for an



(a) (b)

FIG. 10.24

Enhancement MOSFET characteristic showing off and on conditions: (a) nMOS; (b) pMOS.

input of −5 V (greater than the threshold voltage), the device is "on" with drain current present. In summary:

V_{GS} = 0 V leaves pMOS "off;" V_{GS} = −5 V turns pMOS on.

Consider next how the actual CMOS circuit of Fig. 10.25 operates for input of 0 V or +5 V.

0-V Input

When 0 V is applied as input to the CMOS circuit, it provides 0 V to both *n*MOS and *p*MOS gates. Figure 10.25a shows that

$$\text{For } n\text{MOS } (Q_1)\text{:} \quad V_{GS} = V_i - 0\text{ V} = 0\text{ V} - 0\text{ V} = 0\text{ V}$$

$$\text{For } p\text{MOS } (Q_2)\text{:} \quad V_{GS} = V_i - (+5\text{ V}) = 0\text{ V} - 5\text{ V} = -5\text{ V}$$

Input of 0 V to an *n*MOS transistor Q_1 leaves that device "off." The same 0-V input, however, results in the gate–source voltage of *p*MOS transistor Q_2 being −5 V (gate at 0 V is 5 V less than source at +5 V), resulting in that device turning on. The output, V_o, is then +5 V.

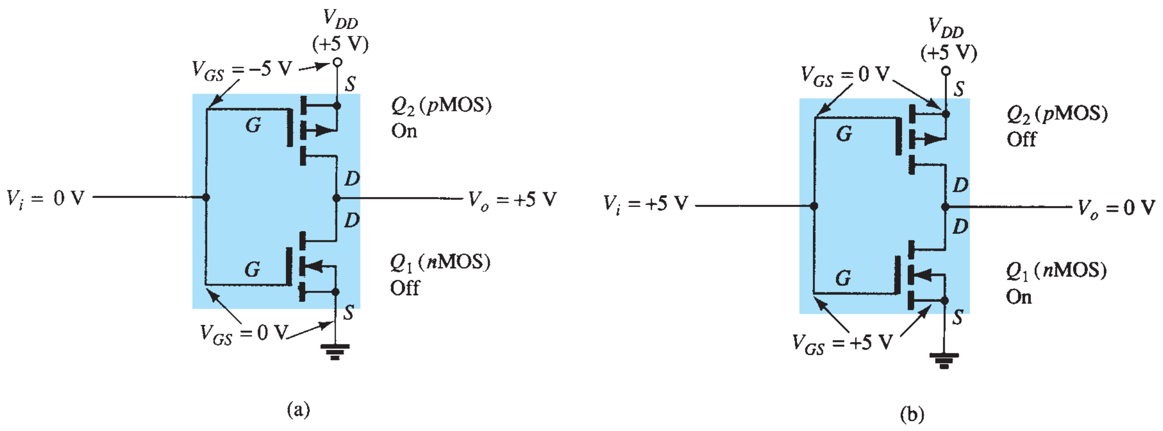
+5-V Input

When V_i = +5 V, it provides +5 V to both gates. Figure 10.25b shows that

$$\text{For } n\text{MOS } (Q_1)\text{:} \quad V_{GS} = V_i - 0\text{ V} = +5\text{ V} - 0\text{ V} = +5\text{ V}$$

$$\text{For } p\text{MOS } (Q_2)\text{:} \quad V_{GS} = V_i - (+5\text{ V}) = +5\text{ V} - 5\text{ V} = 0\text{ V}$$

This input results in transistor Q_1 being turned on and transistor Q_2 remaining off, the output then near 0 V, through conducting transistor Q_2. The CMOS connection of Fig. 10.23 provides operation as a logic inverter with V_o the opposite of V_i, as shown in Table 10.1.



(a) (b)

FIG. 10.25

Operation of CMOS circuit: (a) output +5 V; (b) output 0 V.

TABLE 10.1
Operation of CMOS Circuit

V_i (V)	Q_1	Q_2	V_o (V)
0	Off	On	+5
+5	On	Off	0

The circuits used below to show the various multidevice circuits are mostly symbolic, since the actual circuits used in ICs are much more complex. Figure 10.26 shows a BiFET circuit with JFET transistors at the inputs and bipolar transistors to provide the current source (using a current mirror circuit). The current mirror ensures that each JFET is operated at the same bias current. For ac operation, the JFET provides a high input impedance (much higher than that provided using only bipolar transistors).

Figure 10.27 shows a circuit using MOSFET input transistors and bipolar transistors for the current sources, the BiMOS unit providing even higher input impedance than the BiFET due to the use of MOSFET transistors.

Finally, a differential amplifier circuit can be built using complementary MOSFET transistors as shown in Fig. 10.28. The *p*MOS transistors provide the opposite inputs, whereas the *n*MOS transistors operate as the constant-current source. A single output is taken from

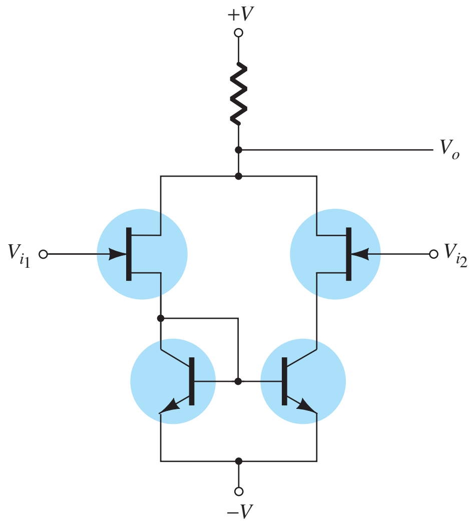


FIG. 10.26
BiFET differential amplifier circuit.

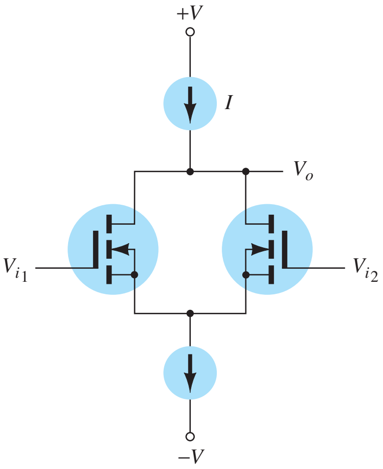


FIG. 10.27
BiMOS differential amplifier circuit.

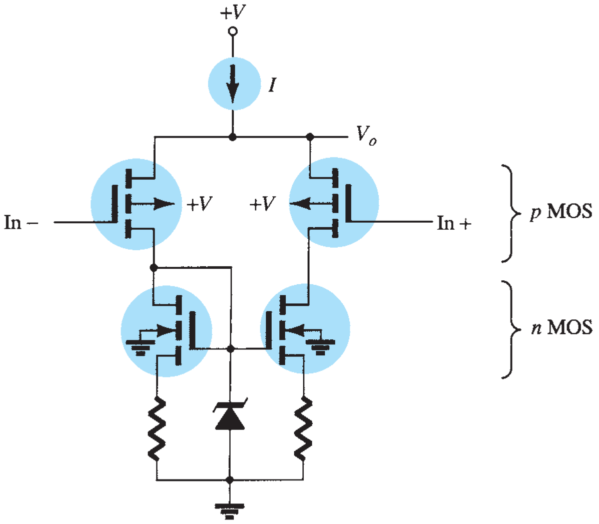


FIG. 10.28
CMOS differential amplifier.

the common point between *n*MOS and *p*MOS transistors on one side of the circuit. This type of CMOS differential amplifier is particularly well suited for battery operation due to the low power dissipation of a CMOS circuit.

10.4 OP-AMP BASICS

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100 Ω). The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output. Figure 10.29 shows a basic op-amp unit. As discussed earlier, the plus (+) input produces an output that is in phase with the signal applied, whereas an input to the minus (−) input results in an opposite-polarity output. The ac equivalent circuit of the op-amp is shown in Fig. 10.30a. As shown, the input signal applied between input terminals sees an input impedance R_i that is typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance R_o, which is typically very low. An ideal op-amp circuit, as shown in Fig. 10.30b, would have infinite input impedance, zero output impedance, and infinite voltage gain.

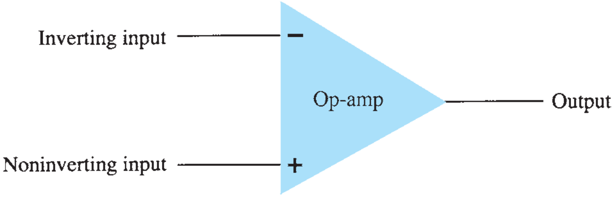
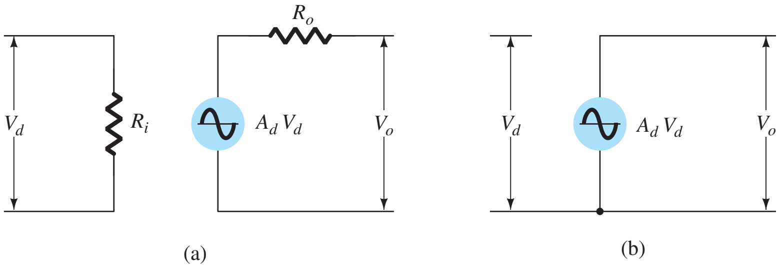


FIG. 10.29
Basic op-amp.



(a)

(b)

FIG. 10.30
AC equivalent of op-amp circuit: (a) practical; (b) ideal.

Basic Op-Amp

The basic circuit connection using an op-amp is shown in Fig. 10.31. The circuit shown provides operation as a constant-gain multiplier. An input signal V_1 is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f. The plus input is connected to ground. Since the signal V_1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 10.32a shows the op-amp replaced by its ac equivalent circuit. If we use the ideal

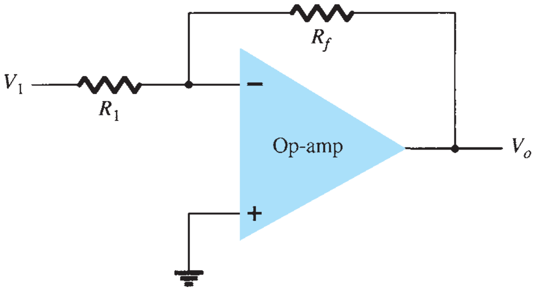
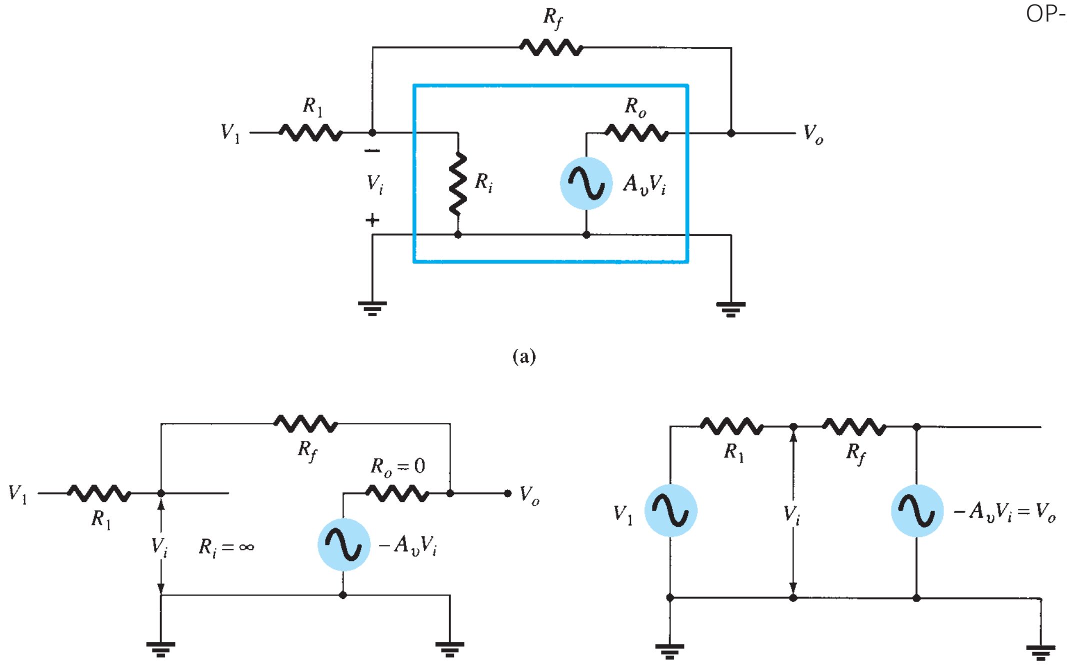


FIG. 10.31
Basic op-amp connection.



(a)

(b)

(c)

FIG. 10.32

Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

op-amp equivalent circuit, replacing R_i by an infinite resistance and R_o by a zero resistance, the ac equivalent circuit is that shown in Fig. 10.32b. The circuit is then redrawn, as shown in Fig. 10.32c, from which circuit analysis is carried out.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_vV_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f}V_1$$

For source $-A_vV_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f}V_1 + \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1}V_1 \qquad \textbf{(10.7)}$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_vR_1}V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_vV_i}{V_i} = \frac{-A_v}{V_i}\frac{R_fV_1}{A_vR_1} = -\frac{R_f}{R_1}\frac{V_1}{V_i}$$

so that

$$\boxed{\frac{V_o}{V_1} = -\frac{R_f}{R_1}} \qquad \textbf{(10.8)}$$

The result in Eq. (10.8) shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f—provided that A_v is very large.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1, the voltage gain is exactly 1.

Constant-Magnitude Gain

If R_f is some multiple of R_1, the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20{,}000$, the input voltage is

$$V_i = \frac{-V_o}{A_v} = \frac{10\text{ V}}{20{,}000} = 0.5\text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 is 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure 10.33 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

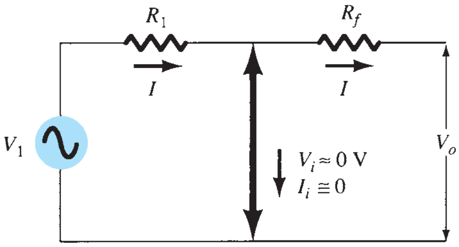


FIG. 10.33
Virtual ground in an op-amp.

The virtual ground concept, which depends on A_v being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that although the circuit of Fig. 10.33 is not physically correct, it does allow an easy means for determining the overall voltage gain.

10.5 PRACTICAL OP-AMP CIRCUITS

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this section, we cover a few of the most common of these circuit connections.

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 10.34. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (10.8), we can write

$$V_o = -\frac{R_f}{R_1} V_1$$

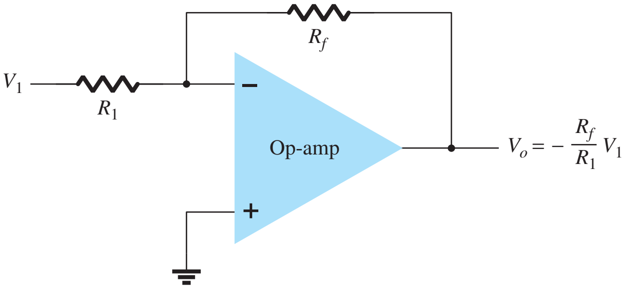


FIG. 10.34

Inverting constant-gain multiplier.

EXAMPLE 10.5 If the circuit of Fig. 10.34 has $R_1 = 100\ \text{k}\Omega$ and $R_f = 500\ \text{k}\Omega$, what output voltage results for an input of $V_1 = 2\ \text{V}$?

Solution:

$$\text{Eq. (10.8):}\quad V_o = -\frac{R_f}{R_1} V_1 = -\frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}(2\ \text{V}) = \mathbf{-10\ V}$$

Noninverting Amplifier

The connection of Fig. 10.35a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 10.35b. Note that the voltage across R_1 is V_1 since $V_i \approx 0\ \text{V}$. This must be equal to the output voltage, through a voltage divider of R_1 and R_f, so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}} \qquad \textbf{(10.9)}$$

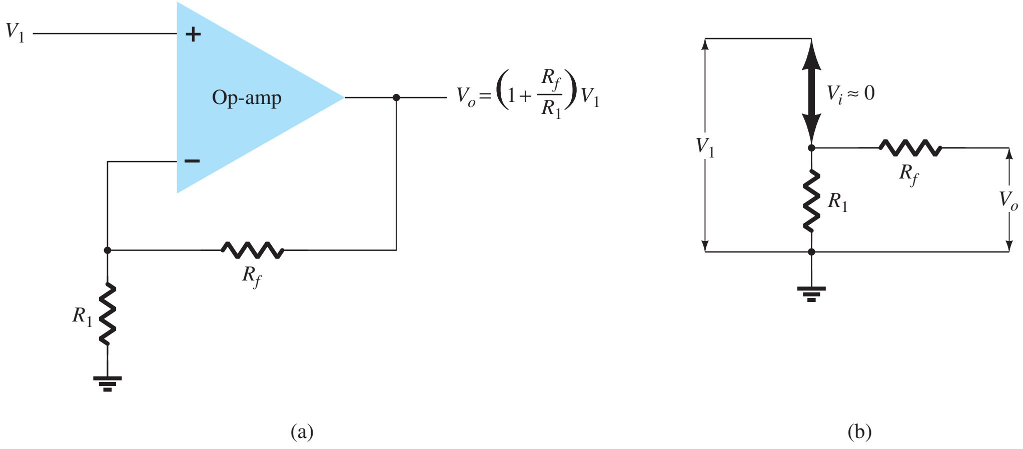


FIG. 10.35
Noninverting constant-gain multiplier.

EXAMPLE 10.6 Calculate the output voltage of a noninverting amplifier (as in Fig. 10.35) for values of $V_1 = 2\text{ V}$, $R_f = 500\text{ k}\Omega$, and $R_1 = 100\text{ k}\Omega$.

Solution:

$$\text{Eq. (10.9):}\quad V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = \left(1 + \frac{500\text{ k}\Omega}{100\text{ k}\Omega}\right)(2\text{ V}) = 6(2\text{ V}) = \mathbf{+12\text{ V}}$$

Unity Follower

The unity-follower circuit, as shown in Fig. 10.36a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 10.36b) it is clear that

$$\boxed{V_o = V_1} \tag{10.10}$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

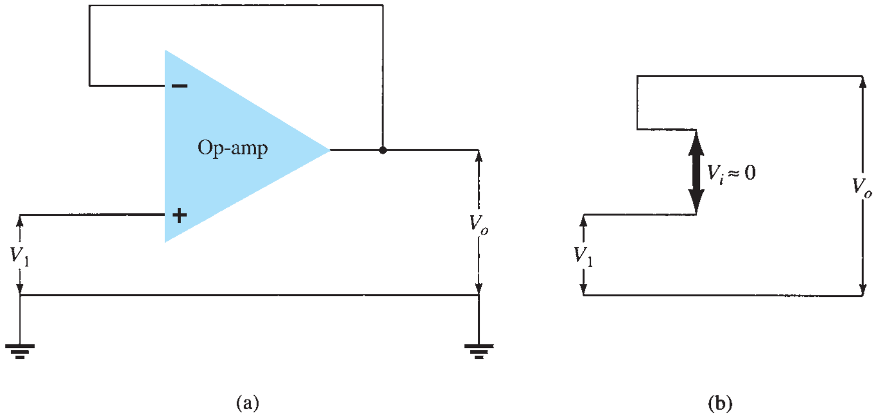


FIG. 10.36
(a) Unity follower; (b) virtual-ground equivalent circuit.

Summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 10.37a. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain

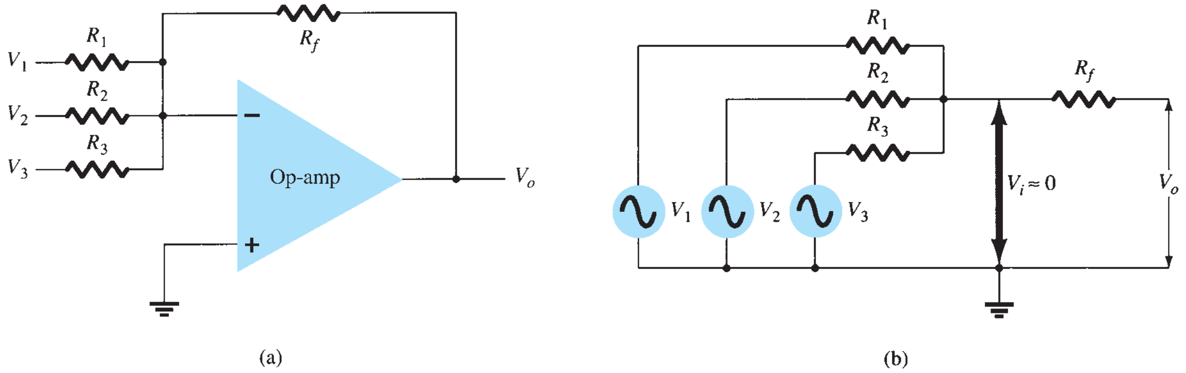


FIG. 10.37
(a) Summing amplifier; (b) virtual-ground equivalent circuit.

factor. Using the equivalent representation shown in Fig. 10.37b, we can express the output voltage in terms of the inputs as

$$\boxed{V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)} \qquad \textbf{(10.11)}$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

EXAMPLE 10.7 Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\ \text{M}\Omega$ in all cases.

a. $V_1 = +1\ \text{V}, V_2 = +2\ \text{V}, V_3 = +3\ \text{V}, R_1 = 500\ \text{k}\Omega, R_2 = 1\ \text{M}\Omega, R_3 = 1\ \text{M}\Omega.$
b. $V_1 = -2\ \text{V}, V_2 = +3\ \text{V}, V_3 = +1\ \text{V}, R_1 = 200\ \text{k}\Omega, R_2 = 500\ \text{k}\Omega, R_3 = 1\ \text{M}\Omega.$

Solution: Using Eq. (10.11), we obtain

$$\text{a.}\quad V_o = -\left[\frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+1\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+2\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+3\ \text{V})\right]$$

$$= -[2(1\ \text{V}) + 1(2\ \text{V}) + 1(3\ \text{V})] = \mathbf{-7\ V}$$

$$\text{b.}\quad V_o = -\left[\frac{1000\ \text{k}\Omega}{200\ \text{k}\Omega}(-2\ \text{V}) + \frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+3\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+1\ \text{V})\right]$$

$$= -[5(-2\ \text{V}) + 2(3\ \text{V}) + 1(1\ \text{V})] = \mathbf{+3\ V}$$

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 10.38a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 10.38b) shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0\ \text{V}$) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.[*] Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

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[*] Laplace notation allows expressing differential or integral operations, which are part of calculus, in algebraic form using the operator s. Readers unfamiliar with calculus should ignore the steps leading to Eq. (10.13) and follow the physical meaning used thereafter.

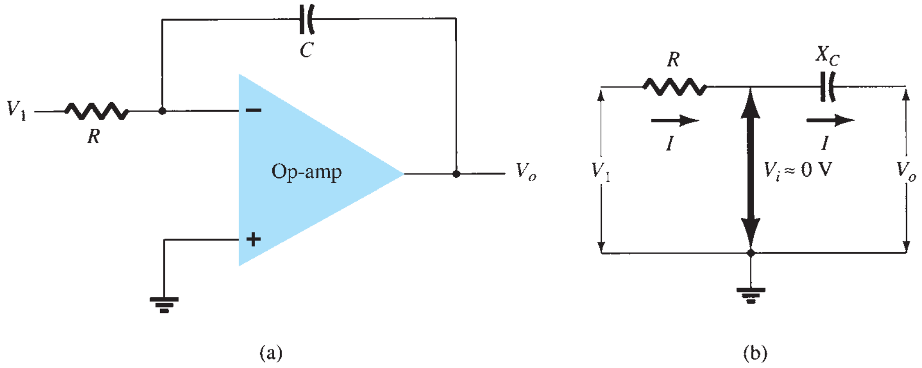


FIG. 10.38
Integrator.

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \tag{10.12}$$

This expression can be rewritten in the time domain as

$$\boxed{v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt} \tag{10.13}$$

Equation (10.13) shows that the output is the integral of the input, with an inversion and scale multiplier of $1/RC$. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

The integration operation is one of summation, summing the area under a waveform or a curve over a period of time. If a fixed voltage is applied as input to an integrator circuit, Eq. (10.13) shows that the output voltage grows over a period of time, providing a ramp voltage. Equation (10.13) can thus be understood to show that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. Although the circuit of Fig. 10.38 can operate on many varied types of input signals, the following examples will use only a fixed input voltage, resulting in a ramp output voltage.

As an example, consider an input voltage $V_1 = 1$ V to the integrator circuit of Fig. 10.39a. The scale factor of $1/RC$ is

$$-\frac{1}{RC} = \frac{1}{(1\ \text{M}\Omega)(1\ \mu\text{F})} = -1$$

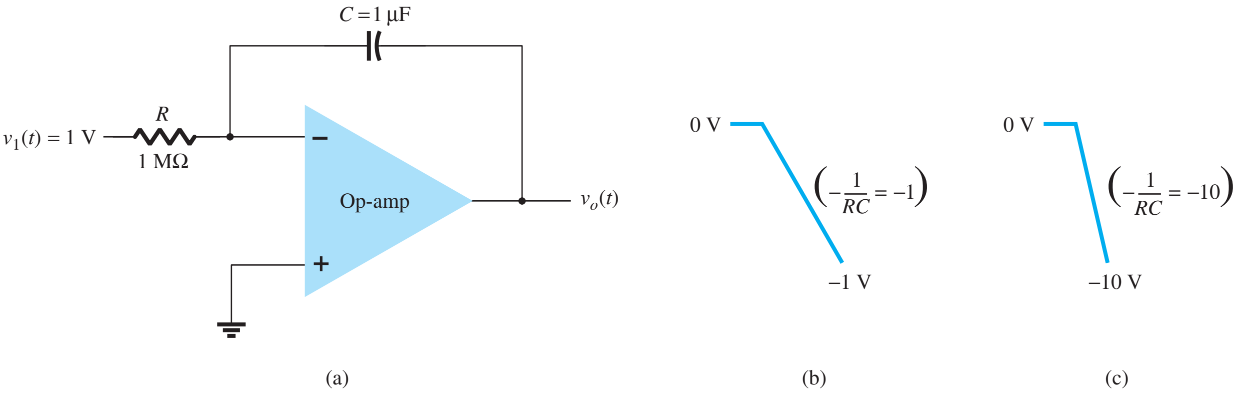

C = 1 μF
R
$v_1(t) = 1$ V
1 MΩ
Op-amp
−
+
$v_o(t)$
(a)
0 V
$\left(-\frac{1}{RC} = -1\right)$
−1 V
(b)
0 V
$\left(-\frac{1}{RC} = -10\right)$
−10 V
(c)

FIG. 10.39
Operation of integrator with step input.

so that the output is a negative ramp voltage as shown in Fig. 10.39b. If the scale factor is changed by making $R = 100\text{ k}\Omega$, for example, then

$$-\frac{1}{RC} = \frac{1}{(100\text{ k}\Omega)(1\ \mu\text{F})} = -10$$

and the output is then a steeper ramp voltage, as shown in Fig. 10.39c.

More than one input may be applied to an integrator, as shown in Fig. 10.40, with the resulting operation given by

$$v_o(t) = -\left[\frac{1}{R_1C}\int v_1(t)\,dt + \frac{1}{R_2C}\int v_2(t)\,dt + \frac{1}{R_3C}\int v_3(t)\,dt\right] \qquad \textbf{(10.14)}$$

An example of a summing integrator as used in an analog computer is given in Fig. 10.40. The actual circuit is shown with input resistors and feedback capacitor, whereas the analog-computer representation indicates only the scale factor for each input.

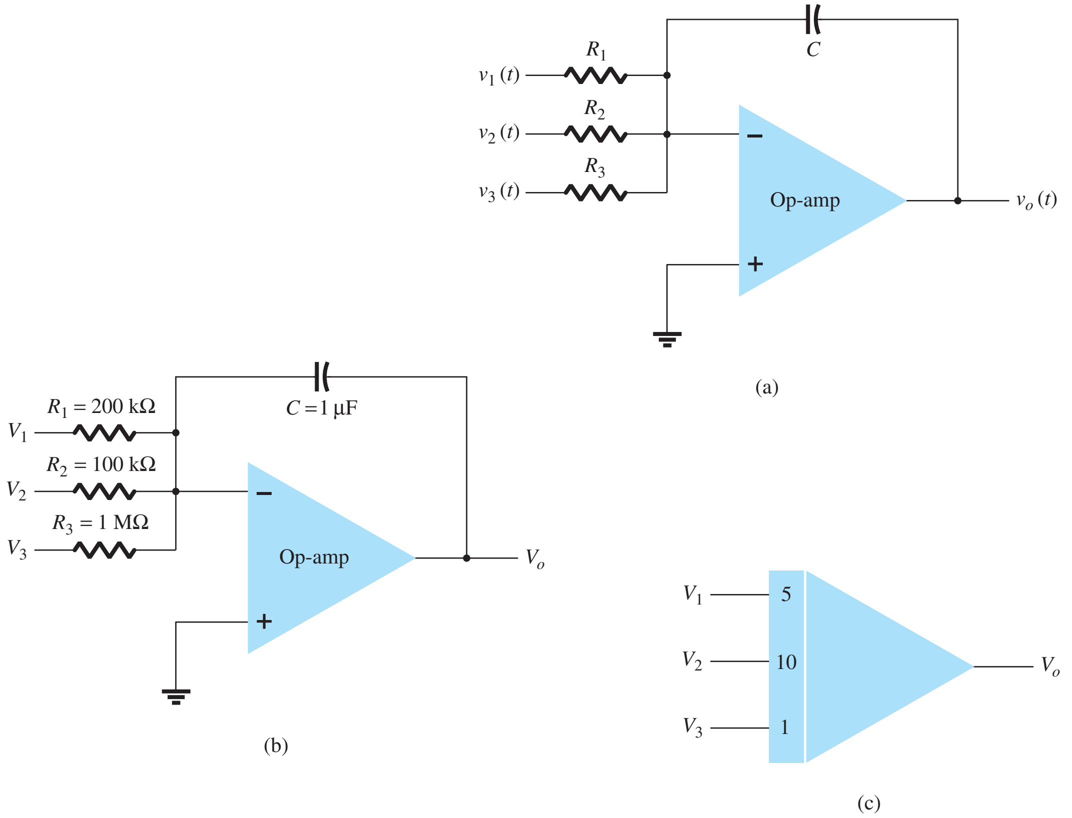


FIG. 10.40

(a) Summing-integrator circuit; (b) component values; (c) analog-computer, integrator-circuit representation.

Differentiator

A differentiator circuit is shown in Fig. 10.41. Although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$\boxed{v_o(t) = -RC\frac{dv_1(t)}{dt}} \qquad \textbf{(10.15)}$$

where the scale factor is $-RC$.

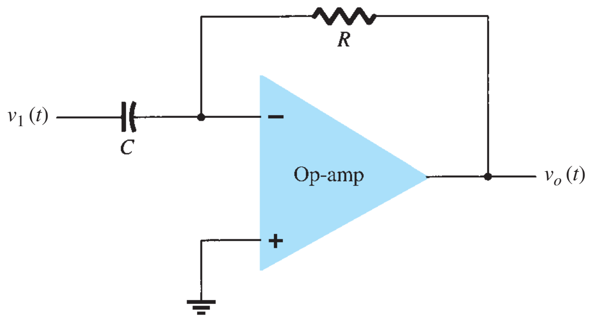


FIG. 10.41
Differentiator circuit.

10.6 OP-AMP SPECIFICATIONS—DC OFFSET PARAMETERS

Before going into various practical applications using op-amps, we should become familiar with some of the parameters used to define the operation of the unit. These specifications include both dc and transient or frequency operating features, as covered next.

Offset Currents and Voltages

Although the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal. Since the user may connect the amplifier circuit for various gain and polarity operations, however, the manufacturer specifies an input offset voltage for the op-amp. The output offset voltage is then determined by the input offset voltage and the gain of the amplifier, as connected by the user.

The output offset voltage can be shown to be affected by two separate circuit conditions: (1) an input offset voltage V_{IO} and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (−) inputs.

Input Offset Voltage V_{IO} The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. To determine the effect of this input voltage on the output, consider the connection shown in Fig. 10.42. Using $V_o = AV_i$, we can write

$$V_o = AV_i = A\left(V_{\text{IO}} - V_o\frac{R_1}{R_1 + R_f}\right)$$

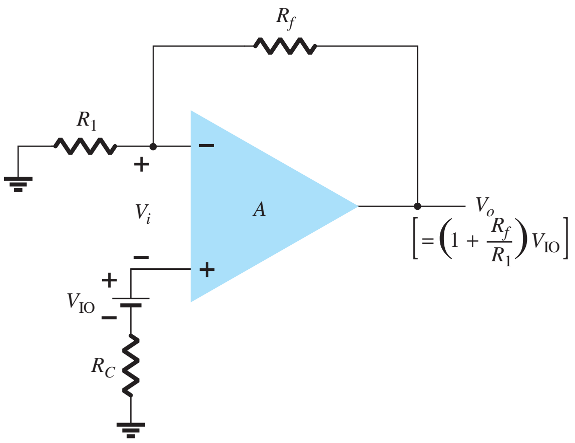

R_f
R_1
+
V_i
−
−
A
+
V_o
$\left[= \left(1 + \frac{R_f}{R_1}\right)V_{\text{IO}}\right]$
+
V_{IO}
−
R_C

FIG. 10.42
Operation showing effect of input offset voltage V_{IO}.

Solving for V_o, we get

$$V_o = V_{\text{IO}} \frac{A}{1 + A\left[R_1/(R_1 + R_f)\right]} \approx V_{\text{IO}} \frac{A}{A\left[R_1/(R_1 + R_f)\right]}$$

from which we can write

$$\boxed{V_o(\text{offset}) = V_{\text{IO}} \frac{R_1 + R_f}{R_1}} \qquad \textbf{(10.16)}$$

Equation (10.16) shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

EXAMPLE 10.8 Calculate the output offset voltage of the circuit in Fig. 10.43. The op-amp spec lists $V_{\text{IO}} = 1.2$ mV.

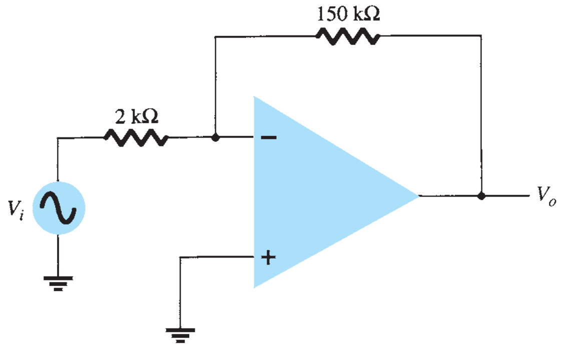


FIG. 10.43
Op-amp connection for Examples 10.8 and 10.9.

Solution:

$$\text{Eq. (10.16):}\quad V_o(\text{offset}) = V_{\text{IO}} \frac{R_1 + R_f}{R_1} = (1.2\text{ mV})\left(\frac{2\text{ k}\Omega + 150\text{ k}\Omega}{2\text{ k}\Omega}\right) = \mathbf{91.2\text{ mV}}$$

Output Offset Voltage Due to Input Offset Current I_{IO} An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For a typical op-amp connection, such as that shown in Fig. 10.44, an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops as shown in Fig. 10.45, we can determine the expression for

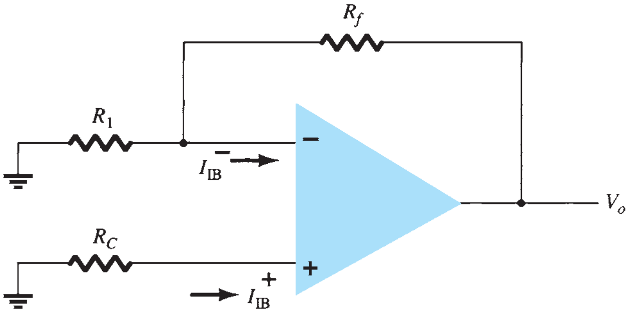


FIG. 10.44
Op-amp connection showing input bias currents.

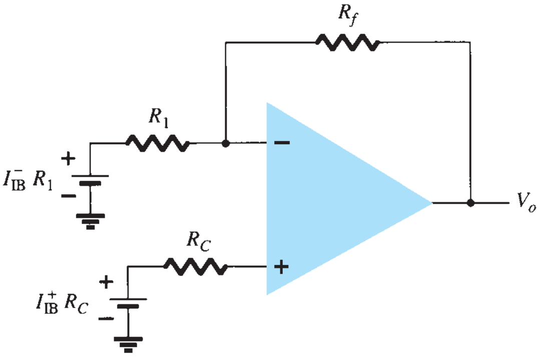


FIG. 10.45
Redrawn circuit of Fig. 10.44.

the resulting output voltage. Using superposition, we see that the output voltage due to input bias current I_{IB}^{+}, denoted by V_o^{+}, is given by

$$V_o^{+} = I_{\mathrm{IB}}^{+} R_C \left(1 + \frac{R_f}{R_1}\right)$$

whereas the output voltage due to only I_{IB}^{-}, denoted by V_o^{-}, is given by

$$V_o^{-} = I_{\mathrm{IB}}^{-} R_1 \left(-\frac{R_f}{R_1}\right)$$

for a total output offset voltage of

$$V_o(\text{offset due to } I_{\mathrm{IB}}^{+} \text{ and } I_{\mathrm{IB}}^{-}) = I_{\mathrm{IB}}^{+} R_C \left(1 + \frac{R_f}{R_1}\right) - I_{\mathrm{IB}}^{-} R_1 \frac{R_f}{R_1} \qquad \textbf{(10.17)}$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{\mathrm{IO}} = I_{\mathrm{IB}}^{+} - I_{\mathrm{IB}}^{-}$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (10.17), we can write

$$\begin{aligned} V_o(\text{offset}) &= I_{\mathrm{IB}}^{+}(R_1 + R_f) - I_{\mathrm{IB}}^{-} R_f \\ &= I_{\mathrm{IB}}^{+} R_f - I_{\mathrm{IB}}^{-} R_f = R_f (I_{\mathrm{IB}}^{+} - I_{\mathrm{IB}}^{-}) \end{aligned}$$

resulting in

$$\boxed{V_o(\text{offset due to } I_{\mathrm{IO}}) = I_{\mathrm{IO}} R_f} \qquad \textbf{(10.18)}$$

EXAMPLE 10.9 Calculate the offset voltage for the circuit of Fig. 10.43 for op-amp specification listing $I_{\mathrm{IO}} = 100$ nA.

Solution: Eq. (10.18): $V_o = I_{\mathrm{IO}} R_f = (100\text{ nA})(150\text{ k}\Omega) = \mathbf{15\ mV}$

Total Offset Due to V_{IO} and I_{IO} Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to} V_{\mathrm{IO}})| + |V_o(\text{offset due to } I_{\mathrm{IO}})| \qquad \textbf{(10.19)}$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

EXAMPLE 10.10 Calculate the total offset voltage for the circuit of Fig. 10.46 for an op-amp with specified values of input offset voltage $V_{\mathrm{IO}} = 4$ mV and input offset current $I_{\mathrm{IO}} = 150$ nA.

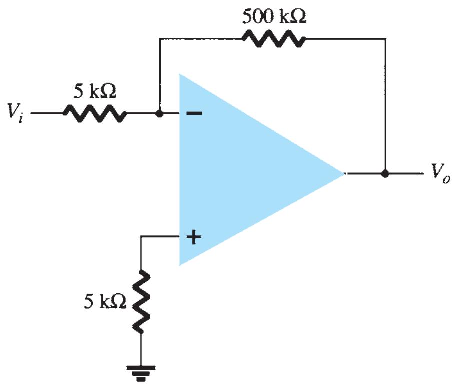


FIG. 10.46
Op-amp circuit for Example 10.10.

Solution: The offset due to V_{IO} is

$$\text{Eq. (10.16):}\quad V_o(\text{offset due to } V_{IO}) = V_{IO}\frac{R_1 + R_f}{R_1} = (4\text{ mV})\left(\frac{5\text{ k}\Omega + 500\text{ k}\Omega}{5\text{ k}\Omega}\right) = 404\text{ mV}$$

$$\text{Eq. (10.18):}\quad V_o(\text{offset due to } I_{IO}) = I_{IO}R_f = (150\text{ nA})(500\text{ k}\Omega) = 75\text{ mV}$$

resulting in a total offset

$$\text{Eq. (10.19):}\quad V_o(\text{total offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO}) = 404\text{ mV} + 75\text{ mV} = \mathbf{479\text{ mV}}$$

Input Bias Current, I_{IB} A parameter related to I_{IO} and the separate input bias currents I_{IB}^+ and I_{IB}^- is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^+ + I_{IB}^-}{2} \tag{10.20}$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB}. It can be shown that for $I_{IB}^+ > I_{IB}^-$

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} \tag{10.21}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} \tag{10.22}$$

EXAMPLE 10.11 Calculate the input bias currents at each input of an op-amp having specified values of $I_{IO} = 5\text{ nA}$ and $I_{IB} = 30\text{ nA}$.

Solution: Using Eq. (10.21), we obtain

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} = 30\text{ nA} + \frac{5\text{ nA}}{2} = \mathbf{32.5\text{ nA}}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} = 30\text{ nA} - \frac{5\text{ nA}}{2} = \mathbf{27.5\text{ nA}}$$

10.7 OP-AMP SPECIFICATIONS—FREQUENCY PARAMETERS

An op-amp is designed to be a high-gain, wide-bandwidth amplifier. This operation tends to be unstable (oscillate) due to positive feedback (see Chapter 14). To ensure stable operation, op-amps are built with internal compensation circuitry, which also causes the very high open-loop gain to diminish with increasing frequency. This gain reduction is referred to as *roll-off*. In most op-amps, roll-off occurs at a rate of 20 dB per decade (−20 dB/decade) or 6 dB per octave (−6 dB/octave). (Refer to Chapter 9 for introductory coverage of dB and frequency response.)

Note that although op-amp specifications list an open-loop voltage gain (A_{VD}), the user typically connects the op-amp using feedback resistors to reduce the circuit voltage gain to a much smaller value (closed-loop voltage gain, A_{CL}). A number of circuit improvements result from this gain reduction. First, the amplifier voltage gain is a more stable, precise value set by the external resistors; second, the input impedance of the circuit is increased over that of the op-amp alone; third, the circuit output impedance is reduced from that of the op-amp alone; and finally, the frequency response of the circuit is increased over that of the op-amp alone.

Gain–Bandwidth

Because of the internal compensation circuitry included in an op-amp, the voltage gain drops off as frequency increases. Op-amp specifications provide a description of the gain versus bandwidth. Figure 10.47 provides a plot of gain versus frequency for a typical op-amp. At low frequency down to dc operation the gain is that value listed by the manufacturer's

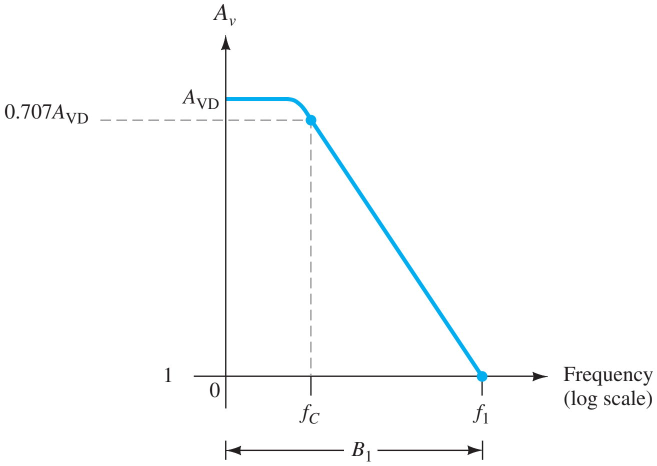


FIG. 10.47

Gain versus frequency plot.

specification A_{VD} (voltage differential gain) and is typically a very large value. As the frequency of the input signal increases, the open-loop gain drops off until it finally reaches the value of 1 (unity). The frequency at this gain value is specified by the manufacturer as the unity-gain bandwidth, B_1. Although this value is a frequency (see Fig. 10.47) at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

Another frequency of interest, as shown in Fig. 10.47, is that at which the gain drops by 3 dB (or to 0.707 the dc gain, A_{VD}), this being the cutoff frequency of the op-amp, f_C. In fact, the unity-gain frequency and cutoff frequency are related by

$$\boxed{f_1 = A_{VD} f_C} \qquad \textbf{(10.23)}$$

Equation (10.23) shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

EXAMPLE 10.12 Determine the cutoff frequency of an op-amp having specified values $B_1 = \mathbf{1\ MHz}$ and $A_{VD} = 200\ \text{V/mV}$.

Solution: Since $f_1 = B_1 = 1$ MHz, we can use Eq. (10.23) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1\ \text{MHz}}{200\ \text{V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = \mathbf{5\ Hz}$$

Slew Rate (SR)

Another parameter reflecting the op-amp's ability to handle varying signals is the slew rate, defined as

Slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/μs)

$$\boxed{\text{SR} = \frac{\Delta V_o}{\Delta t}\ \text{V}/\mu\text{s}} \quad \text{with } t \text{ in } \mu\text{s} \qquad \textbf{(10.24)}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate were to be exceeded.

---

*The closed-loop gain is that obtained with the output connected back to the input in some way.

EXAMPLE 10.13 For an op-amp having a slew rate of $\mathrm{SR} = 2\ \mathrm{V}/\mu\mathrm{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.5 V in 10 μs?

Solution: Since $V_o = A_{\mathrm{CL}}V_i$, we can use

$$\frac{\Delta V_o}{\Delta t} = A_{\mathrm{CL}}\frac{\Delta V_i}{\Delta t}$$

from which we get

$$A_{\mathrm{CL}} = \frac{\Delta V_o/\Delta t}{\Delta V_i/\Delta t} = \frac{\mathrm{SR}}{\Delta V_i/\Delta t} = \frac{2\ \mathrm{V}/\mu\mathrm{s}}{0.5\ \mathrm{V}/10\ \mu\mathrm{s}} = \mathbf{40}$$

Any closed-loop voltage gain of magnitude greater than 40 would drive the output at a rate greater than the slew rate allows, so the maximum closed-loop gain is 40.

Maximum Signal Frequency

The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K\sin(2\pi ft)$$

the maximum voltage rate of change can be shown to be

$$\text{signal maximum rate of change} = 2\pi fK\ \mathrm{V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi fK \le \mathrm{SR}$$
$$\omega K \le \mathrm{SR}$$

so that

$$\boxed{\begin{aligned} f &\le \frac{\mathrm{SR}}{2\pi K} \quad \mathrm{Hz} \\ \omega &\le \frac{\mathrm{SR}}{K} \quad \mathrm{rad/s} \end{aligned}} \qquad \textbf{(10.25)}$$

Additionally, the maximum frequency f in Eq. (10.25) is also limited by the unity-gain bandwidth.

EXAMPLE 10.14 For the signal and circuit of Fig. 10.48, determine the maximum frequency that may be used. Op-amp slew rate is $\mathrm{SR} = 0.5\ \mathrm{V}/\mu\mathrm{s}$.

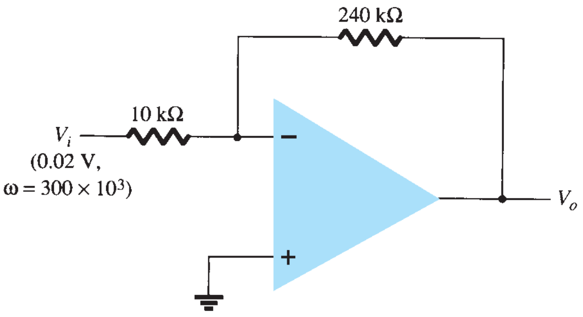


FIG. 10.48
Op-amp circuit for Example 10.14.

Solution: For a gain of magnitude

$$A_{\mathrm{CL}} = \left|\frac{R_f}{R_1}\right| = \frac{240\ \mathrm{k}\Omega}{10\ \mathrm{k}\Omega} = 24$$

the output voltage provides

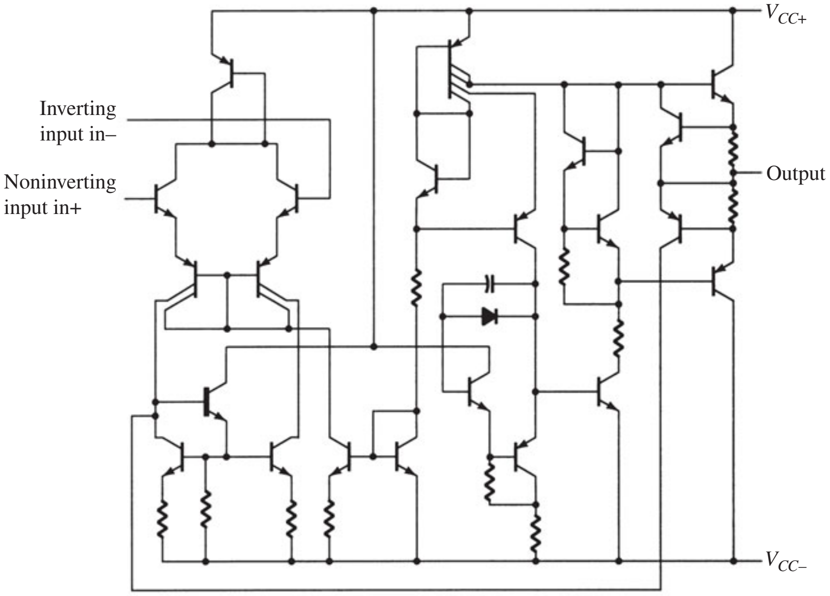
$$K = A_{\mathrm{CL}}V_i = 24(0.02\ \mathrm{V}) = 0.48\ \mathrm{V}$$

$$\text{Eq. (10.25):}\quad \omega \leq \frac{\mathrm{SR}}{K} = \frac{0.5\ \mathrm{V}/\mu\mathrm{s}}{0.48\ \mathrm{V}} = \mathbf{1.1 \times 10^6\ rad/s}$$

Since the signal frequency $\omega = 300 \times 10^3$ rad/s is less than the maximum value determined above, no output distortion will result.

10.8 OP-AMP UNIT SPECIFICATIONS

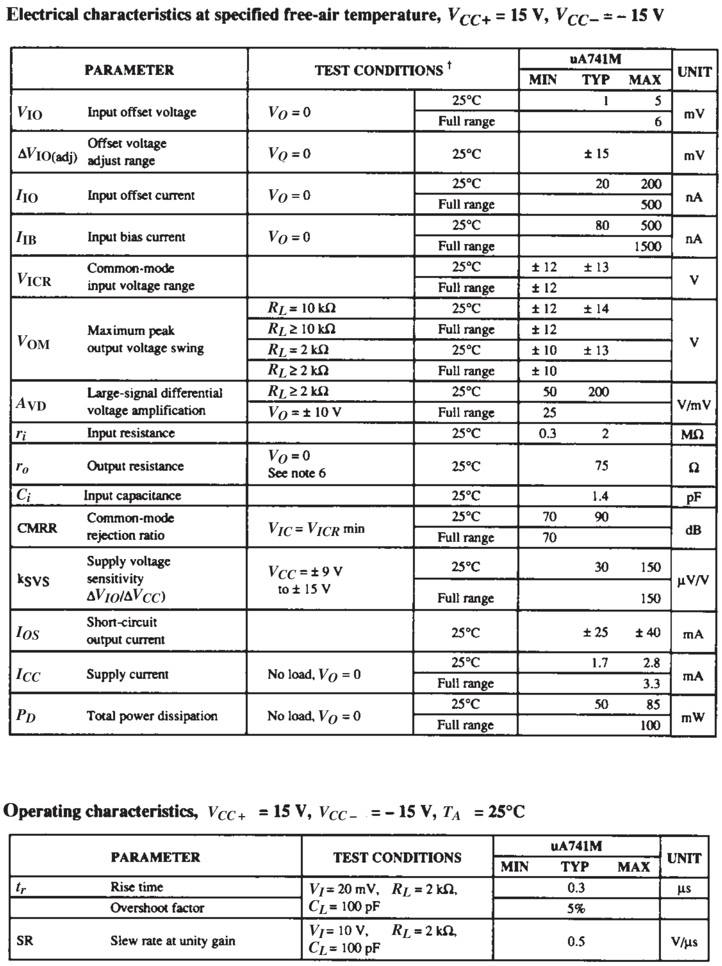
In this section, we discuss how the manufacturer's specifications are read for a typical op-amp unit. A popular bipolar op-amp IC is the 741, described by the information provided in Fig. 10.49. The op-amp is available in a number of packages, an 8-pin DIP and a 10-pin flatpack being among the more usual forms.



Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	uA741	UNIT
Supply voltage V_{CC+}	22	V
Supply voltage V_{CC-}	– 22	V
Differential input voltage	± 30	V
Input voltage any input	± 15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}	± 0.5	V
Duration of output short-circuit	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature	500	mW
Operating free-air temperature range	–40 to 85	°C
Storage temperature range	– 65 to 150	°C
Lead temperature 1,6 mm (1/16 in.) from case for 60 seconds	300	°C
Lead temperature 1,6 mm (1/16 in.) from case for 10 seconds	260	°C

FIG. 10.49
741 op-amp specifications.



Electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = – 15 V

PARAMETER		TEST CONDITIONS †		uA741M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5	mV
			Full range			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		± 15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200	nA
			Full range			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500	nA
			Full range			1500	
V_{ICR}	Common-mode input voltage range		25°C	± 12	± 13		V
			Full range	± 12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	± 12	± 14		V
		$R_L \geq 10\ k\Omega$	Full range	± 12			
		$R_L = 2\ k\Omega$	25°C	± 10	± 13		
		$R_L \geq 2\ k\Omega$	Full range	± 10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$	25°C	50	200		V/mV
		$V_O = \pm 10$ V	Full range	25			
r_i	Input resistance		25°C	0.3	2		MΩ
r_o	Output resistance	$V_O = 0$ See note 6	25°C		75		Ω
C_i	Input capacitance		25°C		1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		dB
			Full range	70			
k$_{SVS}$	Supply voltage sensitivity $\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V	25°C		30	150	µV/V
			Full range			150	
I_{OS}	Short-circuit output current		25°C		± 25	± 40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8	mA
			Full range			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85	mW
			Full range			100	

Operating characteristics, V_{CC+} = 15 V, V_{CC-} = – 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	uA741M			UNIT
			MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, $R_L = 2\ k\Omega$, C_L = 100 pF		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, $R_L = 2\ k\Omega$, C_L = 100 pF		0.5		V/µs

FIG. 10.49
Continued.

Absolute Maximum Ratings

The absolute maximum ratings provide information on what largest voltage supplies may be used, how large the input signal swing may be, and at how much power the device is capable of operating. Depending on the particular version of 741 used, the largest supply voltage is a dual supply of ±18 V or ±22 V. In addition, the IC can internally dissipate from 310 mW to 570 mW, depending on the IC package used. Table 10.2 summarizes some typical values to use in examples and problems.

TABLE 10.2
Absolute Maximum Ratings

Supply voltage	±22 V
Internal power dissipation	500 mW
Differential input voltage	±30 V
Input voltage	±15 V

EXAMPLE 10.15 Determine the current draw from a dual power supply of ±12 V if the IC dissipates 500 mW.

Solution: If we assume that each supply provides half the total power to the IC, then

$$P = VI$$

$$250\text{ mW} = 12\text{ V}(I)$$

so that each supply must provide a current of

$$I = \frac{250\ \text{mW}}{12\ \text{V}} = \mathbf{20.83\ mA}$$

Electrical Characteristics

Electrical characteristics include many of the parameters covered earlier in this chapter. The manufacturer provides some combination of typical, minimum, or maximum values for various parameters as deemed most useful. A summary is provided in Table 10.3.

V_{IO} Input offset voltage: The input offset voltage is seen to be typically 1 mV, but can go as high as 6 mV. The output offset voltage is then computed based on the circuit used. If the worst condition possible is of interest, the maximum value should be used. Typical values are those more commonly expected when using the op-amp.

I_{IO} Input offset current: The input offset current is listed to be typically 20 nA, whereas the largest value expected is 200 nA.

I_{IB} Input bias current: The input bias current is typically 80 nA and may be as large as 500 nA.

V_{ICR} Common-mode input voltage range: This parameter lists the range over which the input voltage may vary (using a supply of ±15 V), about ±12 V to ±13 V. Inputs larger in amplitude than this value will probably result in output distortion and should be avoided.

V_{OM} Maximum peak output voltage swing: This parameter lists the largest amount the output may vary (using a ±15-V supply). Depending on the circuit closed-loop gain, the input signal should be limited to keep the output from varying by an amount no larger than ±12 V in the worst case, or by ±14 V typically.

A_{VD} Large-signal differential voltage amplification: This is the open-loop voltage gain of the op-amp. Although a minimum value of 20 V/mV, or 20,000 V/V is listed, the manufacturer also lists a typical value of 200 V/mV, or 200,000 V/V.

r_i Input resistance: The input resistance of the op-amp when measured under open-loop conditions is typically 2 MΩ, but could be as little as 0.3 MΩ or 300 kΩ. In a closed-loop circuit, this input impedance can be much larger, as discussed previously.

r_o Output resistance: The op-amp output resistance is listed as typically 75 Ω. No minimum or maximum value is given by the manufacturer for this op-amp. Again, in a closed-loop circuit, the output impedance can be lower, depending on the circuit gain.

TABLE 10.3

μA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°$C

Characteristic	Minimum	Typical	Maximum	Unit
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

C_i Input capacitance: For high-frequency considerations, it is helpful to know that the input to the op-amp has typically 1.4 pF of capacitance, a generally small value compared even to stray wiring.

CMRR Common-mode rejection ratio: This parameter is seen to be typically 90 dB, but could go as low as 70 dB. Since 90 dB is equivalent to 31,622.78, the op-amp amplifies noise (common inputs) by over 30,000 times less than difference inputs.

I_{CC} Supply current: The op-amp draws a total of 2.8 mA, typically from the dual voltage supply, but the current drawn could be as little as 1.7 mA. This parameter helps the user determine the size of the voltage supply to use. It also can be used to calculate the power dissipated by the IC ($P_D = 2V_{CC}I_{CC}$).

P_D Total power dissipation: The total power dissipated by the op-amp is typically 50 mW but could go as high as 85 mW. Referring to the previous parameter, we see that the op-amp will dissipate about 50 mW when drawing about 1.7 mA using a dual 15-V supply. At smaller supply voltages, the current drawn will be less and the total power dissipated will also be less.

EXAMPLE 10.16 Using the specifications listed in Table 10.3, calculate the typical output offset voltage for the circuit connection of Fig. 10.50.

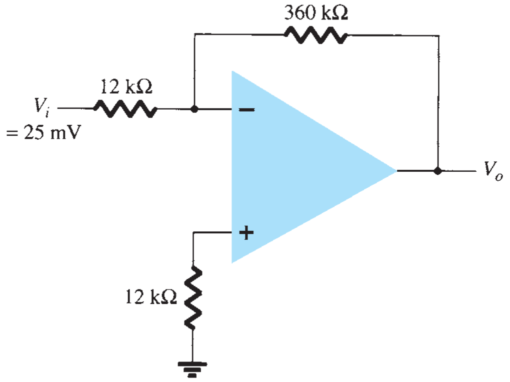


FIG. 10.50

Op-amp circuit for Examples 10.16, 10.17, and 10.19.

Solution: The output offset due to V_{IO} is calculated to be

$$\text{Eq. (10.16):}\quad V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1\text{ mV})\left(\frac{12\text{ k}\Omega + 360\text{ k}\Omega}{12\text{ k}\Omega}\right) = 31\text{ mV}$$

The output voltage due to I_{IO} is calculated to be

$$\text{Eq. (10.18):}\quad V_o(\text{offset}) = I_{IO}R_f = 20\text{ nA}\,(360\text{ k}\Omega) = 7.2\text{ mV}$$

Assuming that these two offsets are the same polarity at the output, we obtain for the total output offset voltage

$$V_o(\text{offset}) = 31\text{ mV} + 7.2\text{ mV} = \mathbf{38.2\text{ mV}}$$

EXAMPLE 10.17 For the typical characteristics of the 741 op-amp ($r_o = 75\ \Omega, A = 200\text{ k}\Omega$), calculate the following values for the circuit of Fig. 10.50:

a. A_{CL}.
b. Z_i.
c. Z_o.

Solution:

a. Eq. (10.8): $\frac{V_o}{V_i} = -\frac{R_f}{R_1} = -\frac{360\text{ k}\Omega}{12\text{ k}\Omega} = \mathbf{-30} \cong \frac{1}{\beta}$

b. $Z_i = R_1 = \mathbf{12\text{ k}\Omega}$

c. $Z_o = \frac{r_o}{(1 + \beta A)} = \frac{75\ \Omega}{1 + \left(\frac{1}{30}\right)(200\text{ k}\Omega)} = \mathbf{0.011\ \Omega}$

Operating Characteristics

Another group of values used to describe the operation of the op-amp over varying signals is provided in Table 10.4.

TABLE 10.4

Operating Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Parameter	Minimum	Typical	Maximum	Unit
B_1 Unity gain bandwidth		1		MHz
t_r Rise time		0.3		μs

EXAMPLE 10.18 Calculate the cutoff frequency of an op-amp having characteristics given in Tables 10.3 and 10.4.

Solution:

$$\text{Eq. (10.23):}\quad f_C = \frac{f_1}{A_{\text{VD}}} = \frac{B_1}{A_{\text{VD}}} = \frac{1\text{ MHz}}{20{,}000} = \mathbf{50\text{ Hz}}$$

EXAMPLE 10.19 Calculate the maximum frequency of the input signal for the circuit in Fig. 10.50 with an input of $V_i = 25$ mV.

Solution: For a closed-loop gain of $A_{\text{CL}} = 30$ and an input of $V_i = 25$ mV, the output gain factor is calculated to be

$$K = A_{\text{CL}} V_i = 30(25\text{ mV}) = 750\text{ mV} = 0.750\text{ V}$$

Using Eq. (10.25), we obtain the maximum signal frequency f_{max} as

$$f_{\text{max}} = \frac{\text{SR}}{2\pi K} = \frac{0.5\text{ V}/\mu\text{s}}{2\pi(0.750\text{ V})} = \mathbf{106\text{ kHz}}$$

Op-Amp Performance

The manufacturer provides a number of graphical descriptions to describe the performance of the op-amp. Figure 10.51 includes some typical performance curves comparing various characteristics as a function of supply voltage. The open-loop voltage gain is seen to get larger with a larger supply voltage value. Whereas the previous tabular information provided information at a particular supply voltage, the performance curve shows how the voltage gain is affected by using a range of supply voltage values.

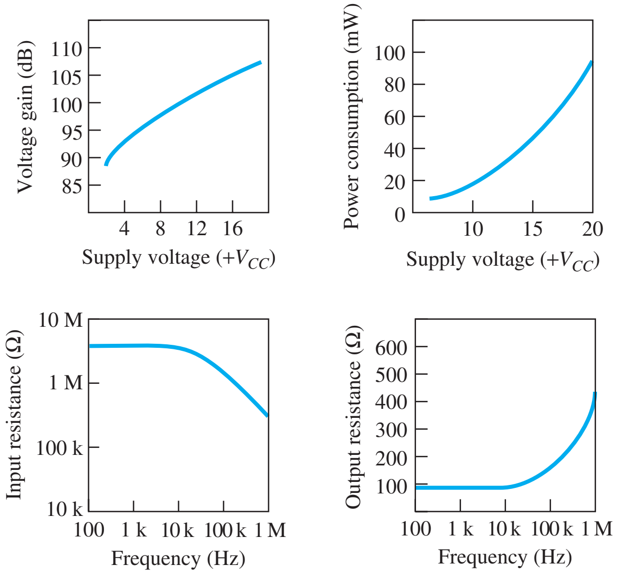


FIG. 10.51

Performance curves.

EXAMPLE 10.20 Using Fig. 10.51, determine the open-loop voltage gain for a supply voltage of $V_{CC} = \pm 12$ V.

Solution: From the curve in Fig. 10.51, $A_{VD} \approx 104$ dB. This is a linear voltage gain of

$$A_{VD}(\text{dB}) = 20 \log_{10} A_{VD}$$

$$104 \text{ dB} = 20 \log A_{VD}$$

$$A_{VD} = \text{antilog} \frac{104}{20} = \mathbf{158.5 \times 10^3}$$

Another performance curve in Fig. 10.51 shows how power consumption varies as a function of supply voltage. As shown, the power consumption increases with larger values of supply voltage. For example, whereas the power dissipation is about 50 mW at $V_{CC} = \pm 15$ V, it drops to about 5 mW with $V_{CC} = \pm 5$ V. Two other curves show how the input and output resistances are affected by frequency: The input impedance drops and the output resistance increases at higher frequency.

10.9 DIFFERENTIAL AND COMMON-MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$\boxed{V_d = V_{i_1} - V_{i_2}} \qquad \textbf{(10.26)}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$\boxed{V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2})} \tag{10.27}$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of-phase components, the resulting output can be expressed as

$$\boxed{V_o = A_d V_d + A_c V_c} \tag{10.28}$$

where V_d = difference voltage given by Eq. (10.26)
V_c = common voltage given by Eq. (10.27)
A_d = differential gain of the amplifier
A_c = common-mode gain of the amplifier

Opposite-Polarity Inputs

If opposite-polarity inputs applied to an op-amp are ideally opposite signals, $V_{i_1} = -V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.26):}\quad V_d = V_{i_1} - V_{i_2} = V_s - (-V_s) = 2V_s$$

and the resulting common voltage is

$$\text{Eq. (10.27):}\quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[V_s + (-V_s)] = 0$$

so that the resulting output voltage is

$$\text{Eq. (10.28):}\quad V_o = A_d V_d + A_c V_c = A_d(2V_s) + 0 = 2A_d V_s$$

This shows that when the inputs are an ideal opposite signal (no common element), the output is the differential gain times twice the input signal applied to one of the inputs.

Same-Polarity Inputs

If the same-polarity inputs are applied to an op-amp, $V_{i_1} = V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.26):}\quad V_d = V_{i_1} - V_{i_2} = V_s - V_s = 0$$

and the resulting common voltage is

$$\text{Eq. (10.27):}\quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(V_s + V_s) = V_s$$

so that the resulting output voltage is

$$\text{Eq. (10.28):}\quad V_o = A_d V_d + A_c V_c = A_d(0) + A_c V_s = A_c V_s$$

This shows that when the inputs are ideal in-phase signals (no difference signal), the output is the common-mode gain times the input signal V_s, which shows that only common-mode operation occurs.

Common-Mode Rejection

The solutions above provide the relationships that can be used to measure A_d and A_c in op-amp circuits.

1. *To measure A_d*: Set $V_{i_1} = -V_{i_2} = V_s = 0.5$ V, so that

   $$\text{Eq. (10.26):}\quad V_d = (V_{i_1} - V_{i_2}) = (0.5\text{ V} - (-0.5\text{ V}) = 1\text{ V}$$

   and

   $$\text{Eq. (10.27):}\quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[0.5\text{ V} + (-0.5\text{ V})] = 0\text{ V}$$

   Under these conditions the output voltage is

   $$\text{Eq. (10.28):}\quad V_o = A_d V_d + A_c V_c = A_d(1\text{ V}) + A_c(0) = A_d$$

Thus, setting the input voltages $V_{i_1} = -V_{i_2} = 0.5\text{ V}$ results in an output voltage numerically equal to the value of A_d.

2. *To measure* A_c: Set $V_{i_1} = V_{i_2} = V_s = 1\text{ V}$, so that

$$\text{Eq. (10.26):}\quad V_d = (V_{i_1} - V_{i_2}) = (1\text{ V} - 1\text{ V}) = 0\text{ V}$$

and

$$\text{Eq. (10.27):}\quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(1\text{ V} + 1\text{ V}) = 1\text{ V}$$

Under these conditions the output voltage is

$$\text{Eq. (10.28):}\quad V_o = A_dV_d + A_cV_c = A_d(0\text{ V}) + A_c(1\text{ V}) = A_c$$

Thus, setting the input voltages $V_{i_1} = V_{i_2} = 1\text{ V}$ results in an output voltage numerically equal to the value of A_c.

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\boxed{\text{CMRR} = \frac{A_d}{A_c}} \tag{10.29}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\boxed{\text{CMRR (log)} = 20\log_{10}\frac{A_d}{A_c}\quad\text{(dB)}} \tag{10.30}$$

EXAMPLE 10.21 Calculate the CMRR for the circuit measurements shown in Fig. 10.52.

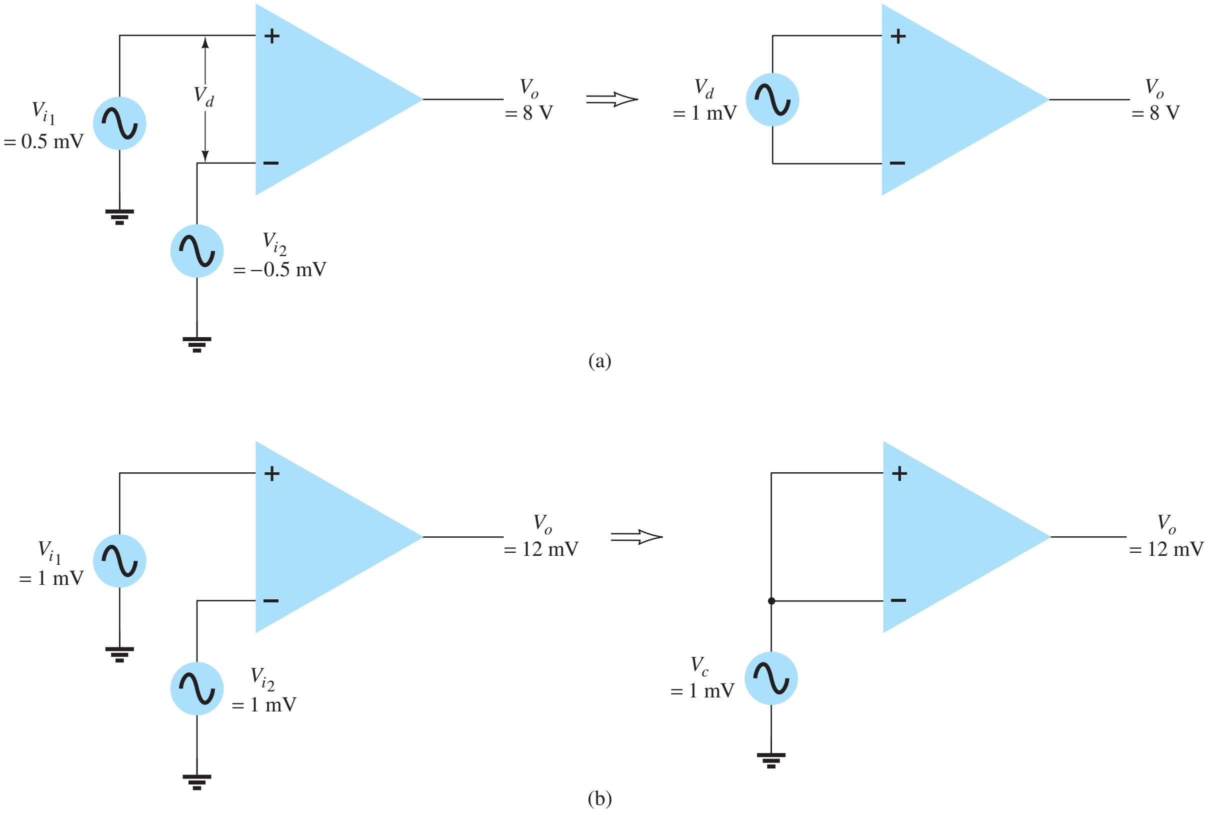


FIG. 10.52
(a) Differential and (b) common-mode operation.

Solution: From the measurement shown in Fig. 10.52a, using the procedure in step 1 above, we obtain

$$A_d = \frac{V_o}{V_d} = \frac{8\text{ V}}{1\text{ mV}} = 8000$$

The measurement shown in Fig. 10.52b, using the procedure in step 2 above, gives us

$$A_c = \frac{V_o}{V_c} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

Using Eq. (10.28), we obtain the value of CMRR,

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = \mathbf{666.7}$$

which can also be expressed as

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10}666.7 = \mathbf{56.48\ dB}$$

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain A_c is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better is the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$$\text{Eq. (12.22):}\quad V_o = A_dV_d + A_cV_c = A_dV_d\left(1 + \frac{A_cV_c}{A_dV_d}\right)$$

Using Eq. (12.24), we can write the above as

$$\boxed{V_o = A_dV_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)} \qquad \textbf{(10.31)}$$

Even when both V_d and V_c components of a signal are present, Eq. (10.31) shows that for large values of CMRR, the output voltage will be due mostly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

EXAMPLE 10.22 Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 150\ \mu\text{V}$ and $V_{i_2} = 140\ \mu\text{V}$. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is:

a. 100.
b. 10^5.

Solution:

$$\text{Eq. (10.26):}\quad V_d = V_{i_1} - V_{i_2} = (150 - 140)\ \mu\text{V} = 10\ \mu\text{V}$$

$$\text{Eq. (10.27):}\quad V_c = \frac{1}{2}(V_{i_1} + V_{i_2}) = \frac{150\ \mu\text{V} + 140\ \mu\text{V}}{2} = 145\ \mu\text{V}$$

a.

$$\text{Eq. (10.31):}\quad V_o = A_dV_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)$$

$$= (4000)(10\ \mu\text{V})\left(1 + \frac{1}{100}\frac{145\ \mu\text{V}}{10\ \mu\text{V}}\right)$$

$$= 40\text{ mV}(1.145) = \mathbf{45.8\ mV}$$

b. $$V_o = (4000)(10\ \mu\text{V})\left(1 + \frac{1}{10^5}\frac{145\ \mu\text{V}}{10\ \mu\text{V}}\right) = 40\text{ mV}(1.000145) = \mathbf{40.006\ mV}$$

Example 10.22 shows that the larger the value of CMRR, the closer is the output voltage to the difference input times the difference gain with the common-mode signal being rejected.

10.10 SUMMARY

Important Conclusions and Concepts

1. Differential operation involves the use of opposite-polarity inputs.
2. Common-mode operation involves the use of the same-polarity inputs.
3. Common-mode rejection compares the gain for differential inputs to that for common inputs.
4. An op-amp is an **op**erational **amp**lifier.
5. The basic features of an op-amp are:
   Very high input impedance (typically megohms)
   Very high voltage gain (typically a few hundred thousand and greater)
   Low output impedance (typically less than 100 Ω)
6. Virtual ground is a concept based on the practical fact that the differential input voltage between plus (+) and minus (−) inputs is nearly (virtually) 0 V—when calculated as the output voltage (at most, that of the voltage supply) divided by the very high voltage gain of the op-amp.
7. Basic op-amp connections include:
   Inverting amplifier
   Noninverting amplifier
   Unity-gain amplifier
   Summing amplifier
   Integrator amplifier
8. Op-amp specs include:
   Offset voltages and currents
   Frequency parameters
   Gain–bandwidth
   Slew rate

Equations

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c}$$

Inverting amplifier:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Noninverting amplifier:

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Unity follower:

$$V_o = V_1$$

Summing amplifier:

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Integrator amplifier:

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \qquad \text{V}/\mu\text{s}$$

10.11 COMPUTER ANALYSIS

PSpice Windows

Program 10.1—Inverting Op-Amp An inverting op-amp, shown in Fig. 10.53, is considered first. With the dc voltage display turned on, the result after running an analysis shows that for an input of 2 V and a circuit gain of −5,

$$A_v = -R_F/R_1 = -500\text{ k}\Omega/100\text{ k}\Omega = -5$$

The output is exactly −10 V:

$$V_o = A_v V_i = -5(2\text{ V}) = -10\text{ V}$$

The input to the minus terminal is −50.01 μV, which is virtually ground, or 0 V.

A practical inverting op-amp circuit is drawn in Fig. 10.54. Using the same resistor values as in Fig. 10.53 with a practical op-amp unit, the μA741, we obtain the resulting output of −9.96 V, near the ideal value of −10 V. This slight difference from the ideal is due to the actual gain and input impedance of the μA741 op-amp unit.

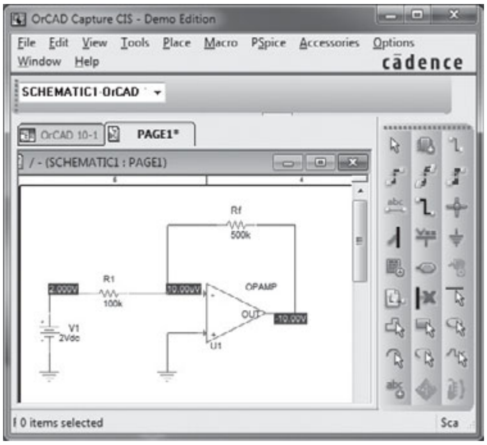
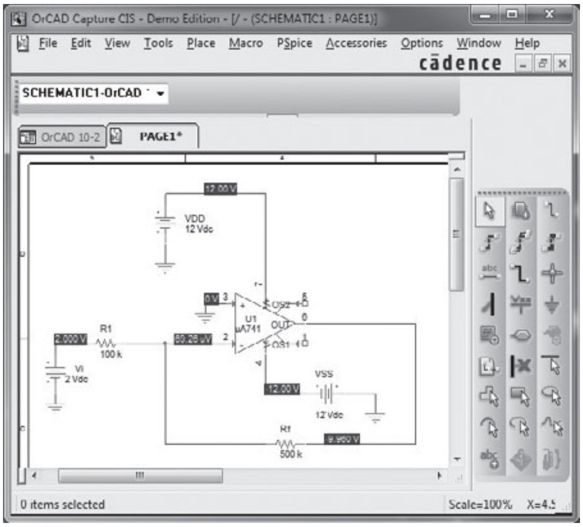

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 10-1
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
Rf
500k
R1
100k
2.000V
10.00uV
OPAMP
OUT
-10.00V
V1
2Vdc
U1
0 items selected
Sca

FIG. 10.53
Inverting op-amp using ideal model.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File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 10-2
PAGE1*
12.00 V
VDD
12 Vdc
0 V
3
U1
μA741
OS2
OUT
OS1
2
R1
100 k
2.000 V
50.28 uV
VI
2 Vdc
12.00 V
VSS
12 Vdc
Rf
500 k
9.960 V
0 items selected
Scale=100%
X=4.5

FIG. 10.54
Practical inverting op-amp circuit.

Before the analysis is done, selecting **Analysis Setup, Transfer Function,** and then **Output** of **V(RF:2)** and **Input Source** of V_i will provide the small-signal characteristics in the output listing. The circuit gain is seen to be

$$V_o/V_i = -5$$

$$\text{Input resistance at } V_i = 1 \times 10^5$$

$$\text{Output resistance at } V_o = 4.95 \times 10^{-3}$$

Program 10.2—Noninverting Op-Amp Figure 10.55 shows a noninverting op-amp circuit. The bias voltages are displayed on the figure. The theoretical gain of the amplifier circuit should be

$$A_v = (1 + R_F/R_1) = 1 + 500\text{ k}\Omega/100\text{ k}\Omega = 6$$

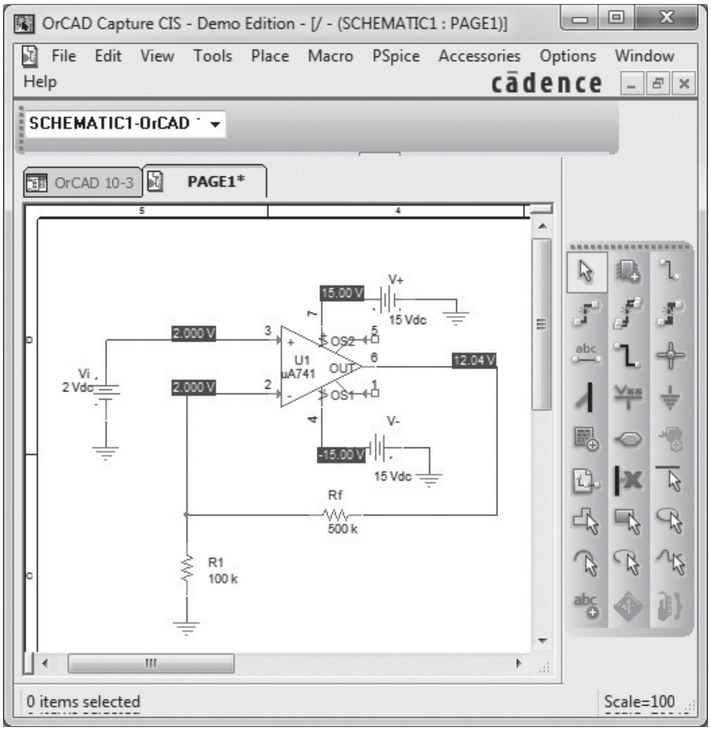
For an input of 2 V, the resulting output will be

$$V_o = A_v V_i = 5(2\text{ V}) = 10\text{ V}$$

The output is noninverted from the input.

Program 10.3—Summing Op-Amp Circuit A summing op-amp circuit such as that in Example 10.3 is shown in Fig. 10.56. Bias voltages also are displayed in Fig. 10.56, showing the resulting output at 3 V, as was calculated in Example 10.3. Notice how well the virtual ground concept works with the minus input being only 3.791 μV.

Program 10.4—Unity-Gain Op-Amp Circuit Figure 10.57 shows a unity-gain op-amp circuit with bias voltages displayed. For an input of +2 V, the output is exactly +2 V.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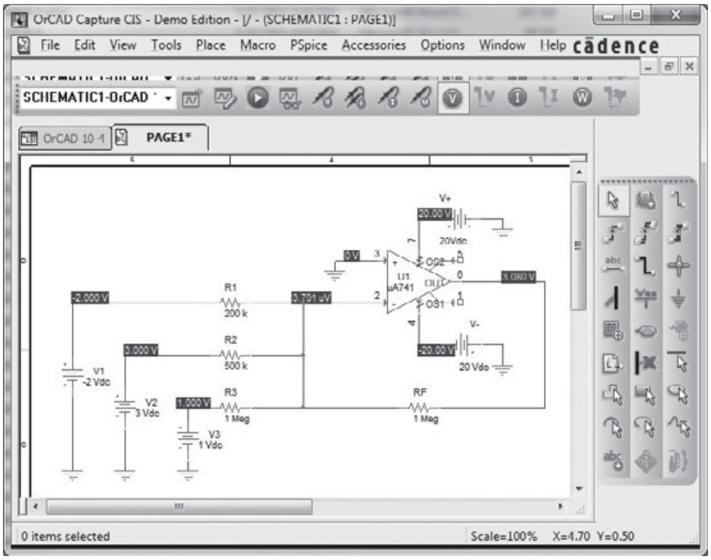
cādence
SCHEMATIC1-OrCAD
OrCAD 10-3
PAGE1*
15.00 V
V+
15 Vdc
2.000 V
3
OS2
5
7
U1
uA741
OUT
6
12.04 V
Vi
2 Vdc
2.000 V
2
OS1
1
4
V-
-15.00 V
15 Vdc
Rf
500 k
R1
100 k
0 items selected
Scale=100

FIG. 10.55

Design Center schematic for noninverting op-amp circuit.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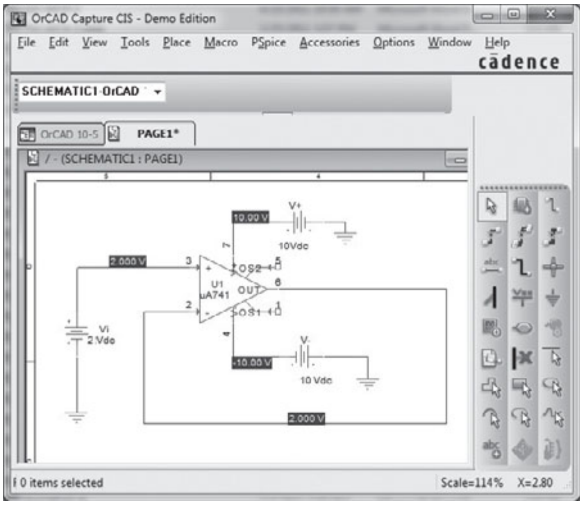
SCHEMATIC1-OrCAD
OrCAD 10-4
PAGE1*
V+
20.00 V
20Vdc
0 V
3
OS2
5
U1
uA741
OUT
0
3.080 V
R1
200 k
-2.000 V
3.701 uV
2
OS1
1
V-
-20.00 V
20 Vdc
R2
500 k
3.000 V
V1
-2 Vdc
R3
1 Meg
1.000 V
V2
3 Vdc
V3
1 Vdc
RF
1 Meg
0 items selected
Scale=100%
X=4.70 Y=0.50

FIG. 10.56

Summing amplifier for Program 10.3.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SCHEMATIC1-OrCAD
OrCAD 10-5
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
V+
10.00 V
10Vdc
2.000 V
3
OS2
5
U1
uA741
OUT
6
2
OS1
1
Vi
2 Vdc
V-
-10.00 V
10 Vdc
2.000 V
0 items selected
Scale=114%
X=2.80

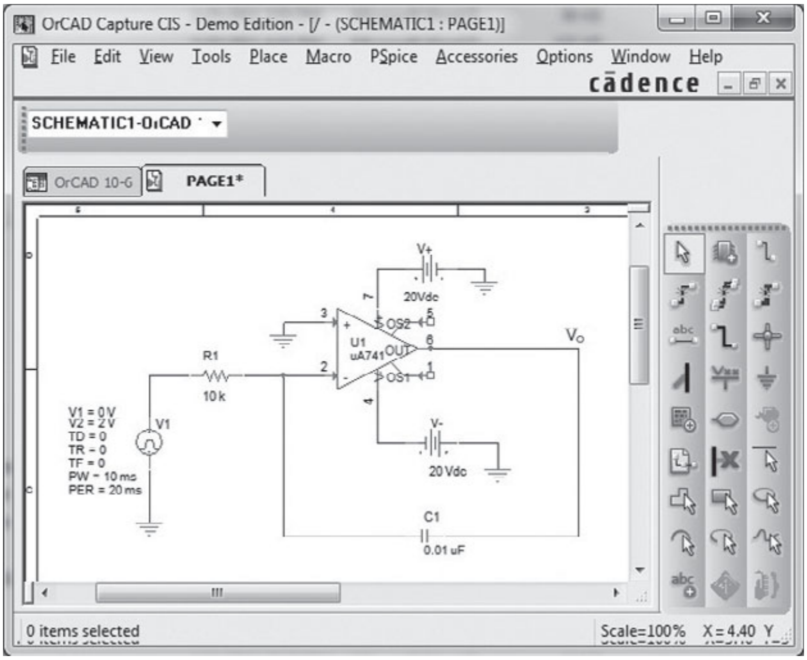
FIG. 10.57

Unity-gain amplifier.

Program 10.5—Op-Amp Integrator Circuit An op-amp integrator circuit is shown in Fig. 10.58. The input is selected as **VPULSE,** which is set to be a step input as follows: Set **ac** = 0, **dc** = 0, **V1** = 0 V, **V2** = 2 V, **TD** = 0, **TR** = 0, **TF** = 0, **PW** = 10 ms, and **PER** = 20 ms. This provides a step from 0 to 2 V, with no time delay, rise time, or fall time, having a period of 10 ms and repeating after a period of 20 ms. For this problem, the voltage rises instantly to 2 V, then stays there for a sufficiently long time for the output to drop as a ramp voltage from the maximum supply level of +20 V to the lowest level of −20 V. Theoretically, the output for the circuit of Fig. 10.58 is

$$v_o(t) = -1/RC \int v_i(t)\,dt$$

$$v_o(t) = -1/(10\text{ k}\Omega)(0.01\ \mu\text{F}) \int 2\,dt = -10{,}000 \int 2\,dt = -20{,}000t$$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File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 10-6
PAGE1*
V+
20Vdc
U1
uA741
OS2
OUT
OS1
V-
20 Vdc
Vo
R1
10 k
V1
C1
0.01 uF
0 items selected
Scale=100%
X=4.40
Y

V1 = 0V
V2 = 2V
TD = 0
TR = 0
TF = 0
PW = 10 ms
PER = 20 ms

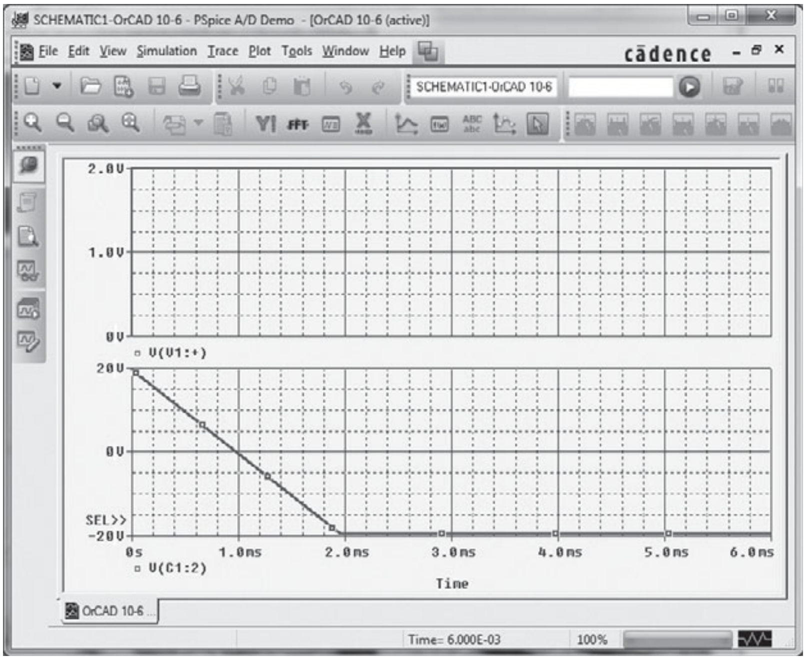
FIG. 10.58

Op-amp integrator circuit.

This is a negative ramp voltage dropping at a rate (slope) of −20,000 V/s. This ramp voltage will drop from +20 V to −20 V in

$$40\text{ V}/20{,}000 = 2 \times 10^{-3} = 2\text{ ms}$$

Figure 10.59 shows the input step waveform and the resulting output ramp waveform obtained using **PROBE.**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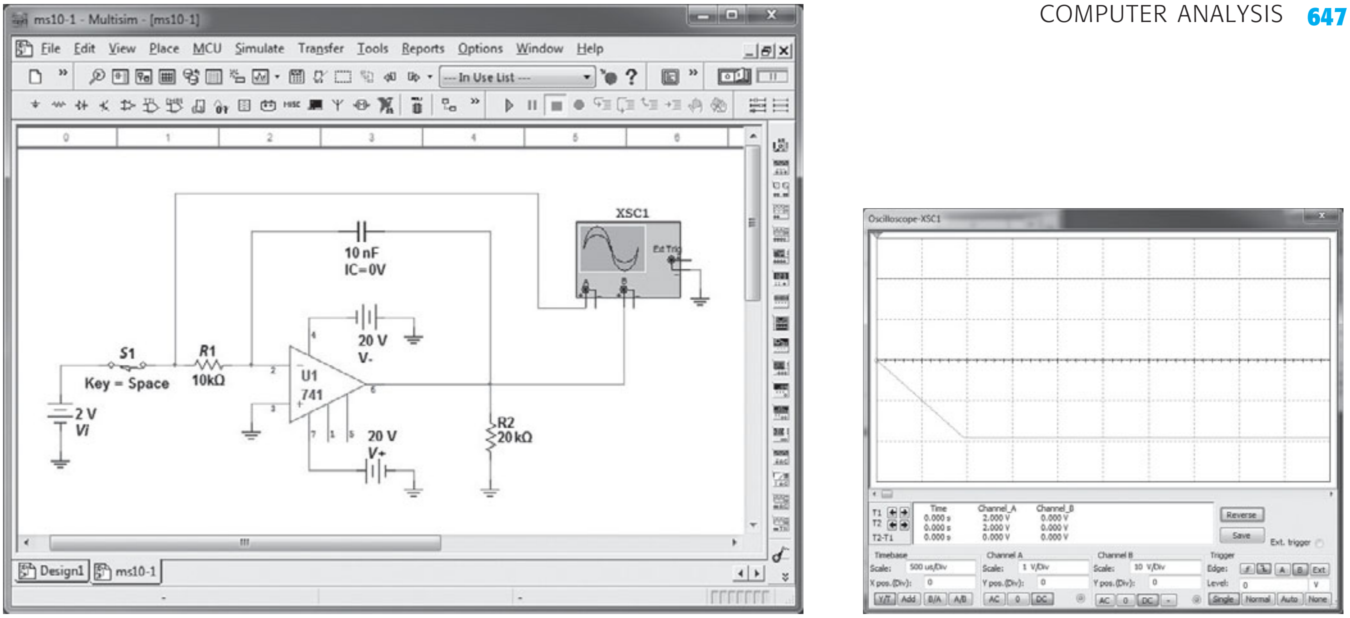
cādence
SCHEMATIC1-OrCAD 10-6
2.0V
1.0V
0V
V(V1:+)
20V
0V
SEL>>
-20V
0s
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
6.0ms
V(C1:2)
Time
OrCAD 10-6
Time= 6.000E-03
100%

FIG. 10.59

Probe waveform for integrator circuit.

Multisim

The same integrator circuit can be constructed and operated using Multisim. Figure 10.60a shows the integrator circuit built using Multisim, with an oscilloscope connected to the


ms10-1 - Multisim - [ms10-1]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
XSC1
Ext Trig
10 nF
IC=0V
20 V
V-
S1
R1
Key = Space
10kΩ
U1
741
2 V
Vi
R2
20 kΩ
20 V
V+
Design1
ms10-1
Oscilloscope-XSC1
Reverse
Save
Ext. trigger
Y/T Add B/A A/B
AC 0 DC
Single Normal Auto None

	Time	Channel_A	Channel_B
T1	0.000 s	2.000 V	0.000 V
T2	0.000 s	2.000 V	0.000 V
T2-T1	0.000 s	0.000 V	0.000 V

Timebase Scale: 500 us/Div
X pos.(Div): 0
Channel A Scale: 1 V/Div
Y pos.(Div): 0
Channel B Scale: 10 V/Div
Y pos.(Div): 0
Trigger Level: 0 V

(a)

(b)

FIG. 10.60

Multisim integrator circuit: (a) circuit; (b) waveform.

op-amp output. The oscilloscope graph obtained is shown in Fig. 10.60b, the linear output waveform going from +20 V down to −20 V in a period of about 2 ms.

Program 10.6—Multistage Op-Amp Circuit A multistage op-amp circuit is shown in Fig. 10.61. The input to stage 1 of 200 mV provides an output of 200 mV to stages 2 and 3. Stage 2 is an inverting amplifier with gain $-200\text{ k}\Omega/20\text{ k}\Omega = -10$, with an output from stage 2 of $-10(200\text{ mV}) = -2$ V. Stage 3 is a noninverting amplifier with gain of $(1 + 200\text{ k}\Omega/10\text{ k}\Omega = 21)$, resulting in an output of $21(200\text{ mV}) = 4.2$ V.

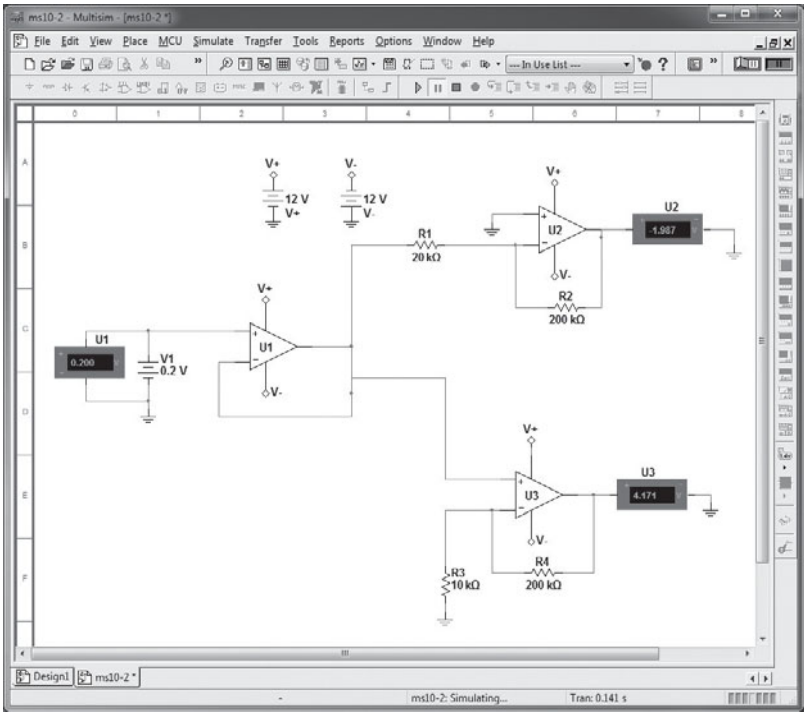

ms10-2 - Multisim - [ms10-2 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
V+
12 V
V+
V-
12 V
V-
R1
20 kΩ
U2
-1.987
R2
200 kΩ
U1
0.200
V1
0.2 V
U1
U3
4.171
R3
10 kΩ
R4
200 kΩ
Design1
ms10-2 *
ms10-2: Simulating...
Tran: 0.141 s

FIG. 10.61

Multistage op-amp circuit.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

10.5 Practical Op-Amp Circuits

1. What is the output voltage in the circuit of Fig. 10.62?

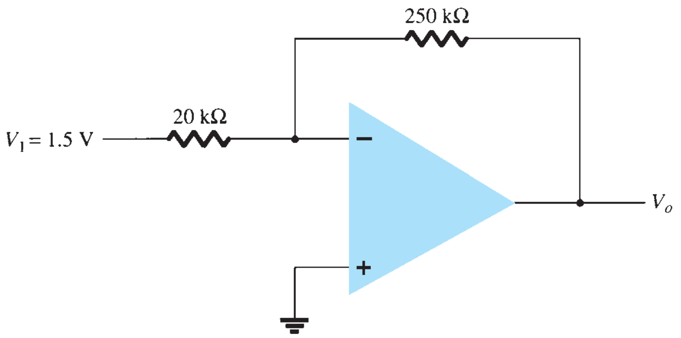

250 kΩ
20 kΩ
$V_1 = 1.5$ V
−
+
V_o

FIG. 10.62
Problems 1 and 25.

2. What is the range of the voltage-gain adjustment in the circuit of Fig. 10.63?

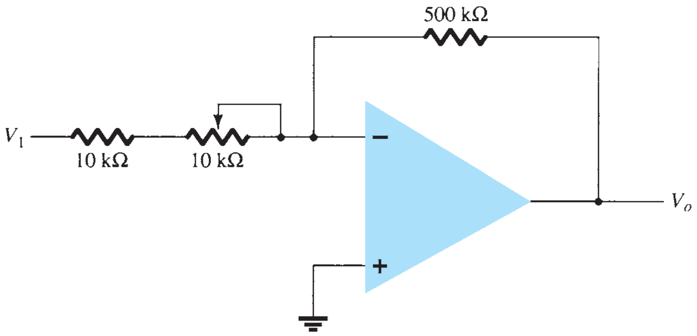

500 kΩ
V_1
10 kΩ
10 kΩ
−
+
V_o

FIG. 10.63
Problem 2.

3. What input voltage results in an output of 2 V in the circuit of Fig. 10.64?
4. What is the range of the output voltage in the circuit of Fig. 10.65 if the input can vary from 0.1 to 0.5 V?

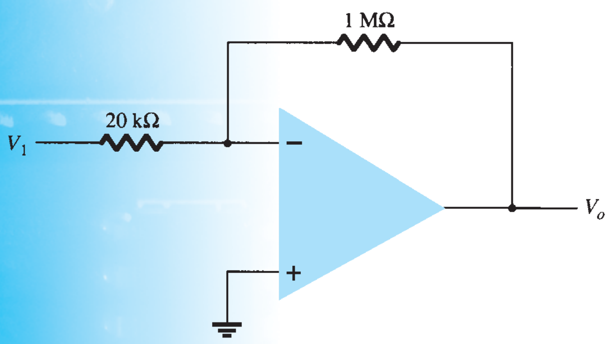

1 MΩ
20 kΩ
V_1
−
+
V_o

FIG. 10.64
Problem 3.

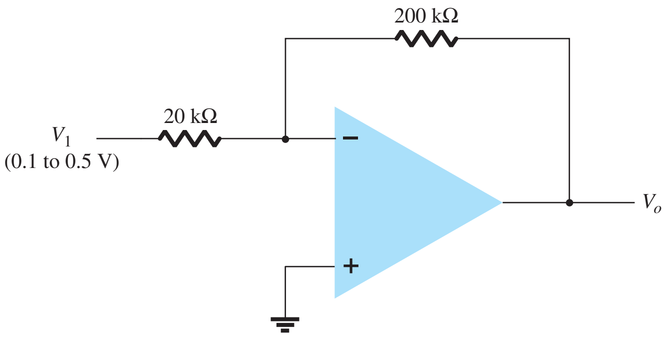
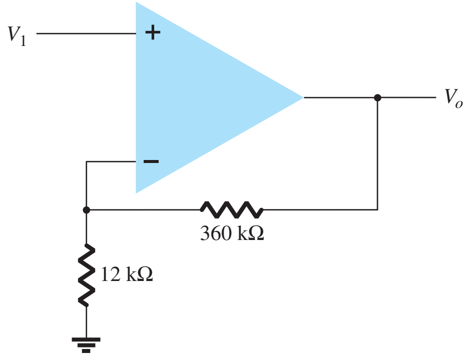

200 kΩ
20 kΩ
V_1
(0.1 to 0.5 V)
−
+
V_o

FIG. 10.65
Problem 4.



V_1
+
−
V_o
360 kΩ
12 kΩ

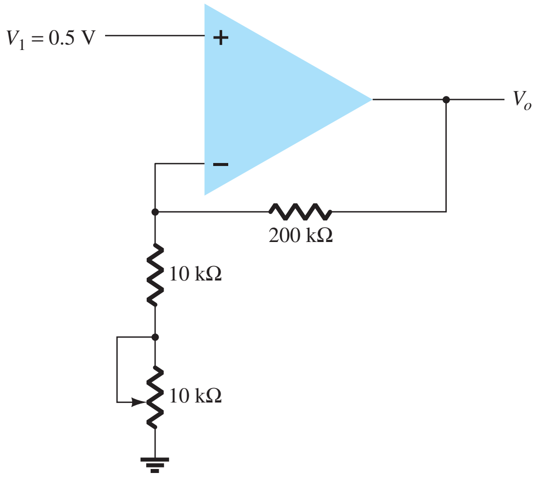
FIG. 10.66
Problems 5, 6, and 26.

5. What output voltage results in the circuit of Fig. 10.66 for an input of $V_1 = -0.3$ V?

6. What input must be applied to the input of Fig. 10.66 to result in an output of 2.4 V?

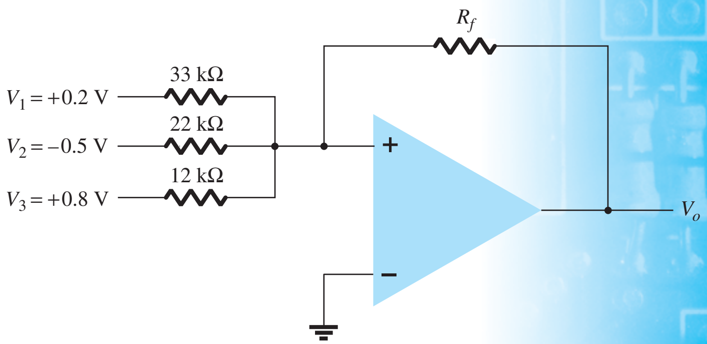
7. What range of output voltage is developed in the circuit of Fig. 10.67?

8. Calculate the output voltage developed by the circuit of Fig. 10.68 for $R_f = 330$ kΩ.



$V_1 = 0.5$ V
+
−
V_o
200 kΩ
10 kΩ
10 kΩ

FIG. 10.67
Problem 7.

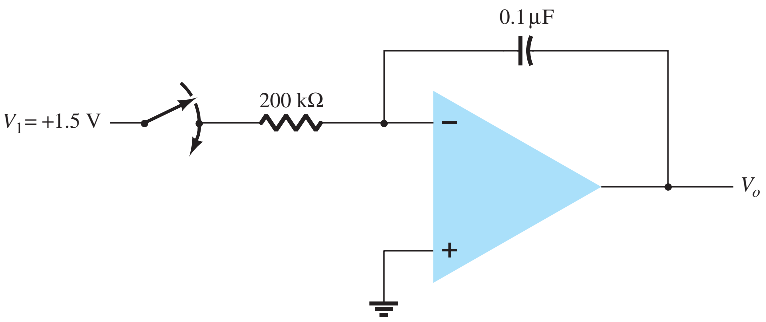


R_f
33 kΩ
$V_1 = +0.2$ V
22 kΩ
$V_2 = -0.5$ V
12 kΩ
$V_3 = +0.8$ V
+
−
V_o

FIG. 10.68
Problems 8, 9, and 27.

9. Calculate the output voltage of the circuit in Fig. 10.68 for $R_f = 68$ kΩ.

10. Sketch the output waveform resulting in Fig. 10.69.



0.1 μF
200 kΩ
$V_1 = +1.5$ V
−
+
V_o

FIG. 10.69
Problem 10.

11. What output voltage results in the circuit of Fig. 10.70 for $V_1 = +0.5$ V?

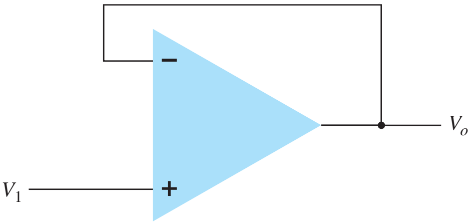
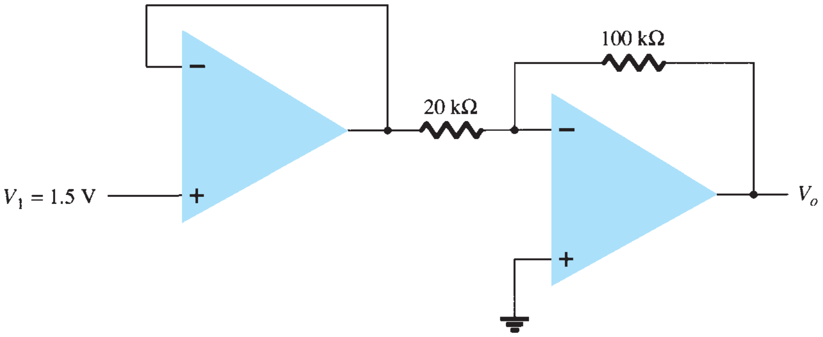


FIG. 10.70
Problem 11.

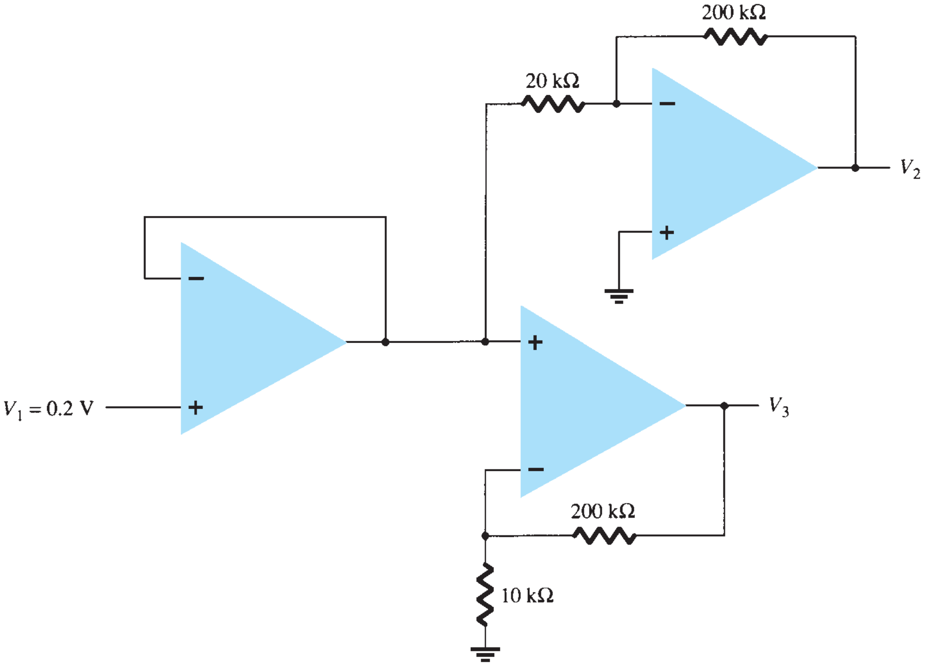
12. Calculate the output voltage for the circuit of Fig. 10.71.



$V_1 = 1.5$ V
−
+
20 kΩ
100 kΩ
−
+
V_o

FIG. 10.71
Problems 12 and 28.

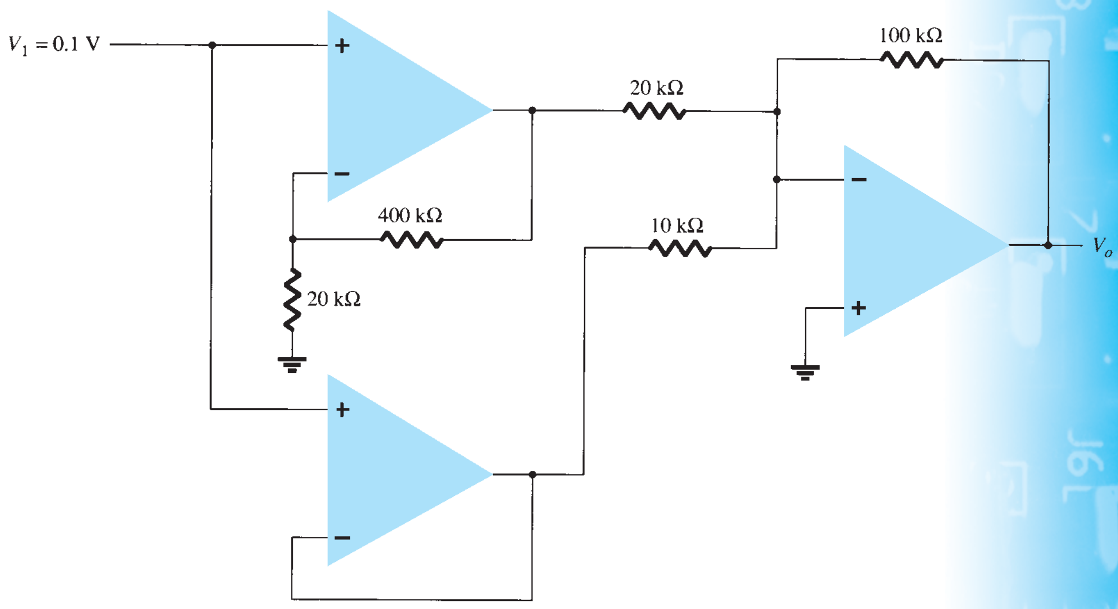
13. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 10.72.



200 kΩ
20 kΩ
−
+
V_2
−
+
$V_1 = 0.2$ V
+
−
V_3
200 kΩ
10 kΩ

FIG. 10.72
Problem 13.

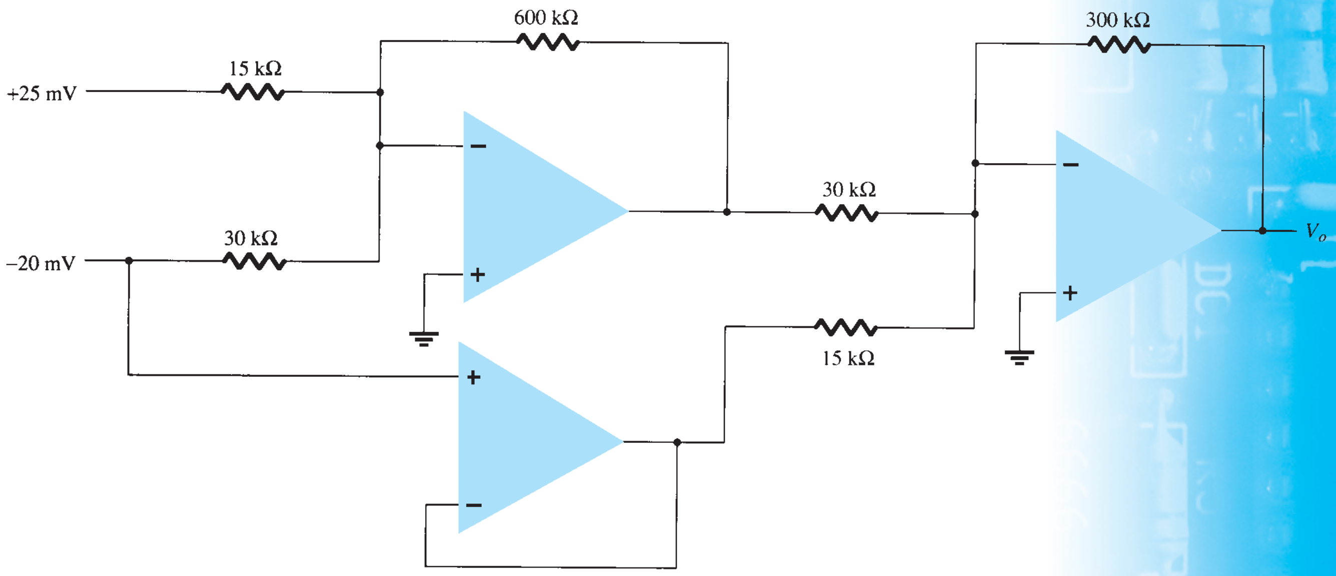
14. Calculate the output voltage, V_o, in the circuit of Fig. 10.73.



$V_1 = 0.1$ V
+
−
400 kΩ
20 kΩ
20 kΩ
100 kΩ
10 kΩ
+
−
−
+
V_o

FIG. 10.73
Problems 14 and 29.

15. Calculate V_o in the circuit of Fig. 10.74.



600 kΩ
15 kΩ
+25 mV
30 kΩ
−20 mV
−
+
+
−
30 kΩ
15 kΩ
300 kΩ
−
+
V_o

FIG. 10.74
Problems 15 and 30.

10.6 Op-Amp Specifications—DC Offset Parameters

***16.** Calculate the total offset voltage for the circuit of Fig. 10.75 for an op-amp with specified values of input offset voltage $V_{IO} = 6$ mV and input offset current $I_{IO} = 120$ nA.

***17.** Calculate the input bias current at each input of an op-amp having specified values of $I_{IO} = 4$ nA and $I_{IB} = 20$ nA.

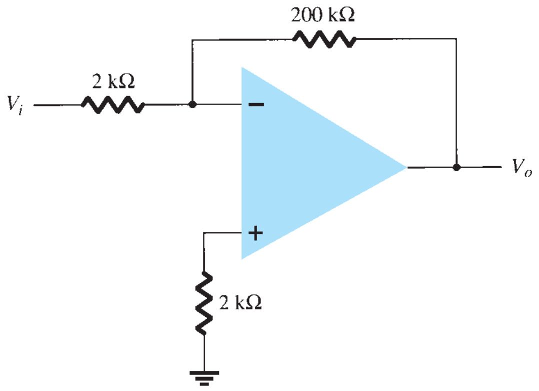


FIG. 10.75
Problems 16, 20, 21, and 22.

10.7 Op-Amp Specifications—Frequency Parameters

18. Determine the cutoff frequency of an op-amp having specified values $B_1 = 800$ kHz and $A_{VD} = 150$ V/mV.

***19.** For an op-amp having a slew rate of SR = 2.4 V/μs, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.3 V in 10 μs?

***20.** For an input of $V_1 = 50$ mV in the circuit of Fig. 10.75, determine the maximum frequency that may be used. The op-amp slew rate SR = 0.4 V/μs.

***21.** Using the specifications listed in Table 10.3, calculate the typical offset voltage for the circuit connection of Fig. 10.75.

***22.** For the typical characteristics of the 741 op-amp, calculate the following values for the circuit of Fig. 10.75:
a. A_{CL}.
b. Z_i.
c. Z_o.

10.9 Differential and Common-Mode Operation

23. Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1$ mV, $V_o = 120$ mV, $V_C = 1$ mV, and $V_o = 20$ μV.

24. Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 200$ μV and $V_{i_2} = 140$ μV. The amplifier has a differential gain of $A_d = 6000$ and the value of CMRR is:
a. 200.
b. 10^5.

10.11 Computer Analysis

***25.** Use Schematic Capture or Multisim to draw a circuit to determine the output voltage in the circuit of Fig. 10.62.

***26.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.66 for the input of $V_i = 0.5$ V.

***27.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.68 for $R_f = 68$ kΩ.

***28.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.71.

***29.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.73.

***30.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.74.

***31.** Use Schematic Capture or Multisim to obtain the output waveform for a 2-V step input to an integrator circuit, as shown in Fig. 10.39 with values of $R = 40$ kΩ and $C = 0.003$ μF.

11

Op-Amp Applications

CHAPTER OBJECTIVES

- Learn about constant gain, summing, and buffering amplifiers
- Understand how an active filter works
- Describe different types of controlled sources

11.1 CONSTANT-GAIN MULTIPLIER

One of the most common op-amp circuits is the inverting constant-gain multiplier, which provides a precise gain or amplification. Figure 11.1 shows a standard circuit connection, with the resulting gain being given by

$$\boxed{A = -\frac{R_f}{R_1}} \tag{11.1}$$

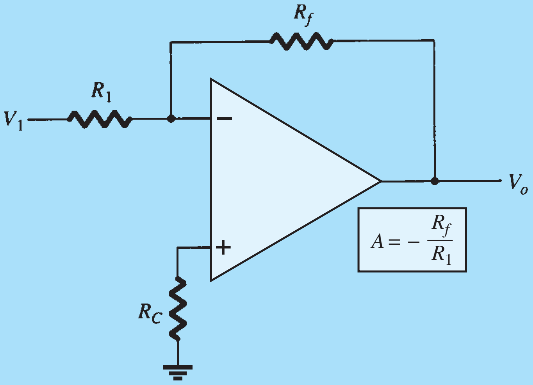


FIG. 11.1
Fixed-gain amplifier.

EXAMPLE 11.1 Determine the output voltage for the circuit of Fig. 11.2 with a sinusoidal input of 2.5 mV.

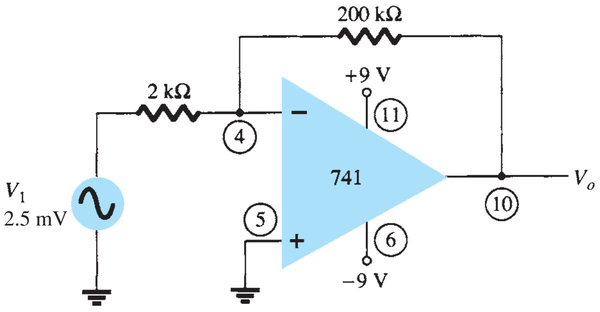


FIG. 11.2
Circuit for Example 11.1.

Solution: The circuit of Fig. 11.2 uses a 741 op-amp to provide a constant or fixed gain, calculated from Eq. (11.1) to be

$$A = -\frac{R_f}{R_1} = -\frac{200\text{ k}\Omega}{2\text{ k}\Omega} = -100$$

The output voltage is then

$$V_o = AV_i = -100(2.5\text{ mV}) = -250\text{ mV} = \mathbf{-0.25\ V}$$

A noninverting constant-gain multiplier is provided by the circuit of Fig. 11.3, with the gain given by

$$\boxed{A = 1 + \frac{R_f}{R_1}} \qquad \textbf{(11.2)}$$

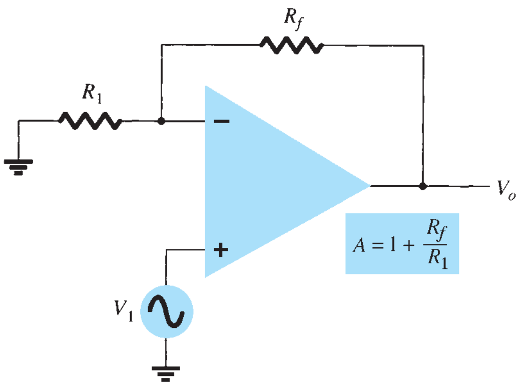


FIG. 11.3
Noninverting fixed-gain amplifier.

EXAMPLE 11.2 Calculate the output voltage from the circuit of Fig. 11.4 for an input of 120 μV.

Solution: The gain of the op-amp circuit is calculated using Eq. (11.2) to be

$$A = 1 + \frac{R_f}{R_1} = 1 + \frac{240\text{ k}\Omega}{2.4\text{ k}\Omega} = 1 + 100 = 101$$

The output voltage is then

$$V_o = AV_i = 101(120\ \mu\text{V}) = \mathbf{12.12\ mV}$$

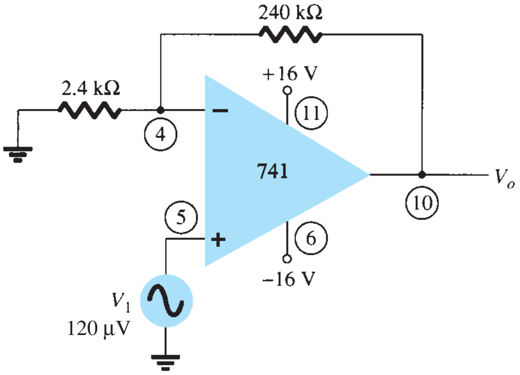


FIG. 11.4
Circuit for Example 11.2.

Multiple-Stage Gains

When a number of stages are connected in series, the overall gain is the product of the individual stage gains. Figure 11.5 shows a connection of three stages. The first stage is connected to provide noninverting gain as given by Eq. (11.1). The next two stages provide an inverting gain given by Eq. (11.1). The overall circuit gain is then noninverting and is calculated by

$$A = A_1 A_2 A_3$$

where $A_1 = 1 + R_f/R_1, A_2 = -R_f/R_2$, and $A_3 = -R_f/R_3$.

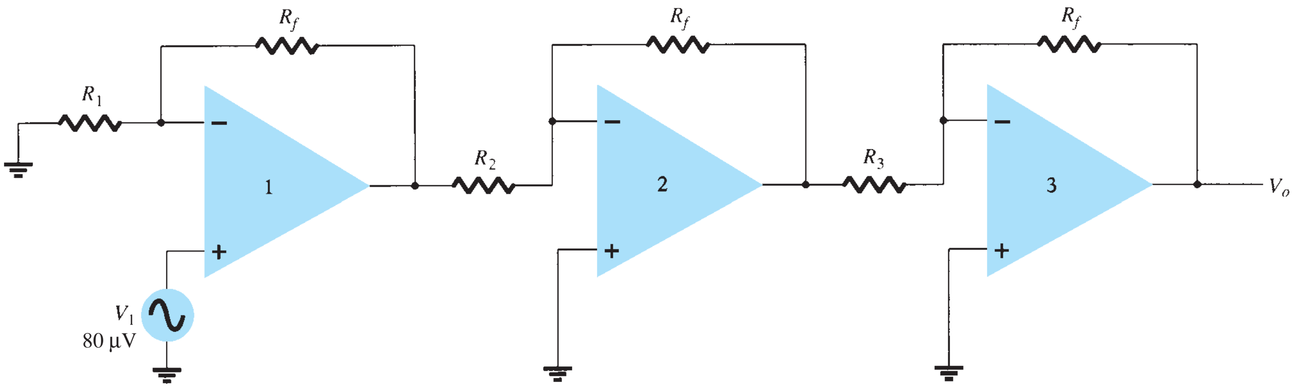


FIG. 11.5
Constant-gain connection with multiple stages.

EXAMPLE 11.3 Calculate the output voltage using the circuit of Fig. 11.5 for resistor components of value $R_f = 470\text{ k}\Omega$, $R_1 = 4.3\text{ k}\Omega$, $R_2 = 33\text{ k}\Omega$, and $R_3 = 33\text{ k}\Omega$ for an input of 80 μV.

Solution: The amplifier gain is calculated to be

$$A = A_1 A_2 A_3 = \left(1 + \frac{R_f}{R_1}\right)\left(-\frac{R_f}{R_2}\right)\left(-\frac{R_f}{R_3}\right)$$

$$= \left(1 + \frac{470\text{ k}\Omega}{4.3\text{ k}\Omega}\right)\left(-\frac{470\text{ k}\Omega}{33\text{ k}\Omega}\right)\left(-\frac{470\text{ k}\Omega}{33\text{ k}\Omega}\right)$$

$$= (110.3)(-14.2)(-14.2) = 22.2 \times 10^3$$

so that

$$V_o = AV_i = 22.2 \times 10^3 (80\ \mu\text{V}) = \mathbf{1.78\ V}$$

EXAMPLE 11.4 Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +10, −18, and −27. Use a 270-kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150 μV?

Solution: For the gain of +10,

$$A_1 = 1 + \frac{R_f}{R_1} = +10$$

$$\frac{R_f}{R_1} = 10 - 1 = 9$$

$$R_1 = \frac{R_f}{9} = \frac{270\ \text{k}\Omega}{9} = 30\ \text{k}\Omega$$

For the gain of −18,

$$A_2 = -\frac{R_f}{R_2} = -18$$

$$R_2 = \frac{R_f}{18} = \frac{270\ \text{k}\Omega}{18} = 15\ \text{k}\Omega$$

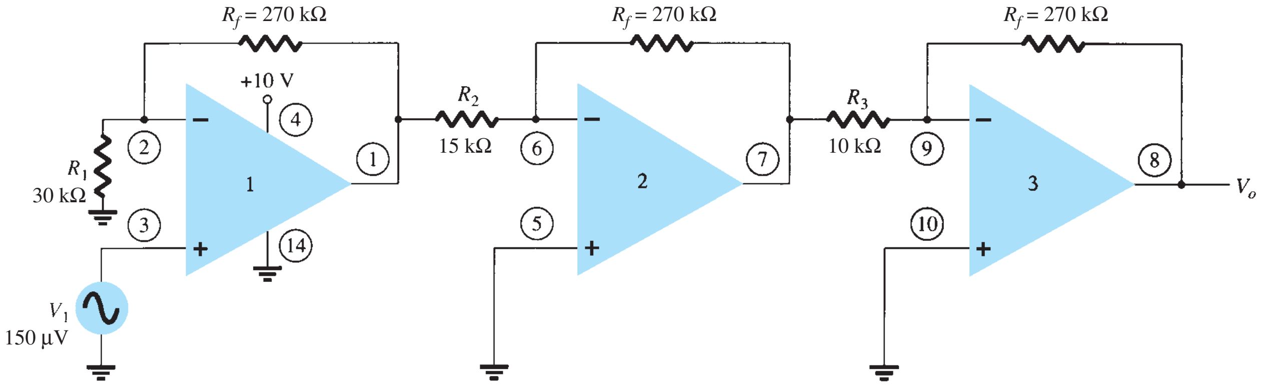
For the gain of −27,

$$A_3 = -\frac{R_f}{R_3} = -27$$

$$R_3 = \frac{R_f}{27} = \frac{270\ \text{k}\Omega}{27} = 10\ \text{k}\Omega$$

The circuit showing the pin connections and all components used is given in Fig. 11.6. For an input of $V_1 = 150\ \mu\text{V}$, the output voltage is

$$\begin{aligned} V_o &= A_1A_2A_3V_1 = (10)(-18)(-27)(150\ \mu\text{V}) = 4860(150\ \mu\text{V}) \\ &= \mathbf{0.729\ V} \end{aligned}$$



$R_f = 270\ \text{k}\Omega$
$R_f = 270\ \text{k}\Omega$
$R_f = 270\ \text{k}\Omega$
+10 V
4
R_2
R_3
2
1
15 kΩ
6
7
10 kΩ
9
8
V_o
R_1
30 kΩ
1
2
3
3
5
10
14
V_1
150 μV

FIG. 11.6
Circuit for Example 11.4 (using LM124).

A number of op-amp stages could also be used to provide separate gains, as demonstrated in the next example.

EXAMPLE 11.5 Show the connection of three op-amp stages using an LM348 IC to provide outputs that are 10, 20, and 50 times larger than the input. Use a feedback resistor of $R_f = 500\ \text{k}\Omega$ in all stages.

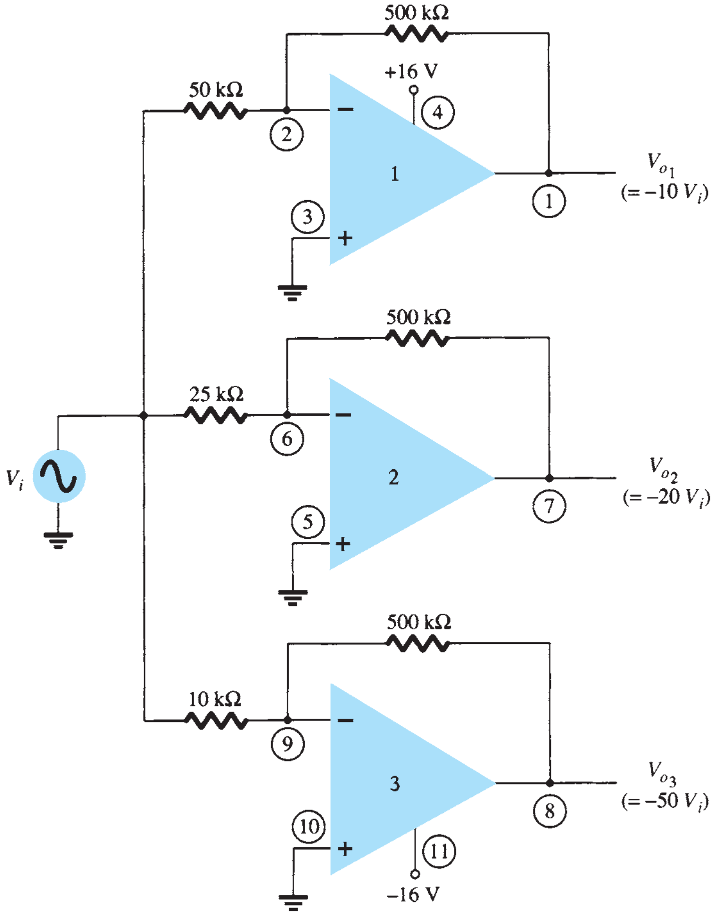
Solution: The resistor component for each stage is calculated to be

$$R_1 = -\frac{R_f}{A_1} = -\frac{500\ \text{k}\Omega}{-10} = 50\ \text{k}\Omega$$

$$R_2 = -\frac{R_f}{A_2} = -\frac{500\ \text{k}\Omega}{-20} = 25\ \text{k}\Omega$$

$$R_3 = -\frac{R_f}{A_3} = -\frac{500\ \text{k}\Omega}{-50} = 10\ \text{k}\Omega$$

The resulting circuit is drawn in Fig. 11.7.



500 kΩ
+16 V
50 kΩ
4
2
1
3
1
−
+
V_{o_1}
(= −10 V_i)
500 kΩ
25 kΩ
6
2
5
7
−
+
V_{o_2}
(= −20 V_i)
V_i
500 kΩ
10 kΩ
9
3
10
8
11
−
+
V_{o_3}
(= −50 V_i)
−16 V

FIG. 11.7

Circuit for Example 11.5 (using LM348).

11.2 VOLTAGE SUMMING

Another popular use of an op-amp is as a summing amplifier. Figure 11.8 shows the connection, with the output being the sum of the three inputs, each multiplied by a different gain. The output voltage is

$$\boxed{V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)} \qquad \textbf{(11.3)}$$

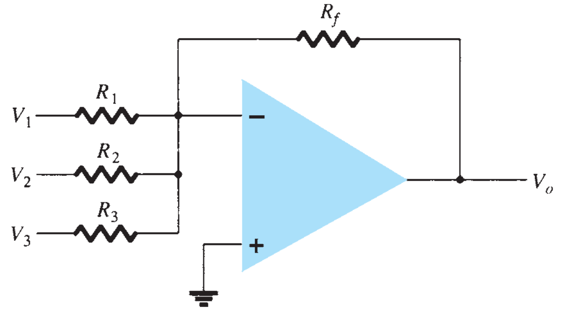

R_f
R_1
R_2
R_3
V_1
V_2
V_3
−
+
V_o

FIG. 11.8
Summing amplifier.

EXAMPLE 11.6 Calculate the output voltage for the circuit of Fig. 11.9. The inputs are $V_1 = 50 \text{ mV} \sin(1000t)$ and $V_2 = 10 \text{ mV} \sin(3000t)$.

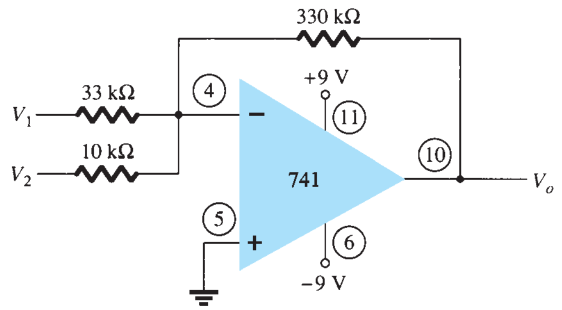

330 kΩ
33 kΩ
10 kΩ
V_1
V_2
4
+9 V
11
10
741
5
6
−9 V
−
+
V_o

FIG. 11.9
Circuit for Example 11.6.

Solution: The output voltage is

$$V_o = -\left(\frac{330 \text{ k}\Omega}{33 \text{ k}\Omega} V_1 + \frac{330 \text{ k}\Omega}{10 \text{ k}\Omega} V_2\right) = -(10\ V_1 + 33\ V_2)$$
$$= -[10(50 \text{ mV}) \sin(1000t) + 33(10 \text{ mV}) \sin(3000t)]$$
$$= \mathbf{-[0.5 \sin (1000\mathit{t}) + 0.33 \sin (3000\mathit{t})]}$$

Voltage Subtraction

Two signals can be subtracted from one another in a number of ways. Figure 11.10 shows two op-amp stages used to provide subtraction of input signals. The resulting output is given by

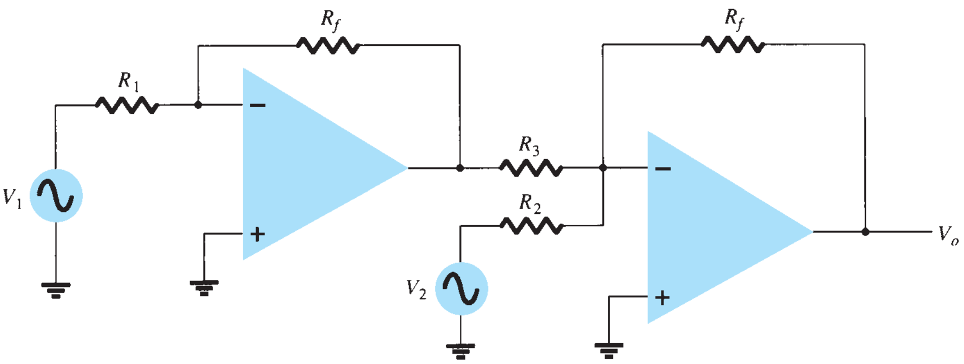

R_f
R_1
V_1
−
+
R_3
R_2
V_2
R_f
−
+
V_o

FIG. 11.10
Circuit for subtracting two signals.

$$V_o = -\left[\frac{R_f}{R_3}\left(-\frac{R_f}{R_1}V_1\right) + \frac{R_f}{R_2}V_2\right]$$

$$\boxed{V_o = -\left(\frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1}V_1\right)} \tag{11.4}$$

EXAMPLE 11.7 Determine the output for the circuit of Fig. 11.10 with components $R_f = 1\ \text{M}\Omega$, $R_1 = 100\ \text{k}\Omega$, $R_2 = 50\ \text{k}\Omega$, and $R_3 = 500\ \text{k}\Omega$.

Solution: The output voltage is calculated to be

$$V_o = -\left(\frac{1\ \text{M}\Omega}{50\ \text{k}\Omega}V_2 - \frac{1\ \text{M}\Omega}{500\ \text{k}\Omega}\frac{1\ \text{M}\Omega}{100\ \text{k}\Omega}V_1\right) = -(20\ V_2 - 20\ V_1) = \mathbf{-20(V_2 - V_1)}$$

The output is seen to be the difference of V_2 and V_1 multiplied by a gain factor of −20.

Another connection to provide subtraction of two signals is shown in Fig. 11.11. This connection uses only one op-amp stage to provide subtracting two input signals. Using superposition, we can show the output to be

$$\boxed{V_o = \frac{R_3}{R_1 + R_3}\frac{R_2 + R_4}{R_2}V_1 - \frac{R_4}{R_2}V_2} \tag{11.5}$$

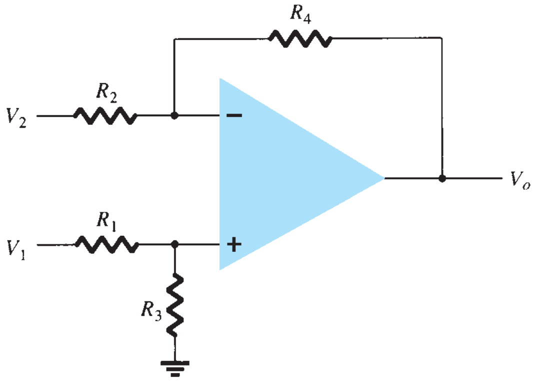


FIG. 11.11
Subtraction circuit.

EXAMPLE 11.8 Determine the output voltage for the circuit of Fig. 11.12.

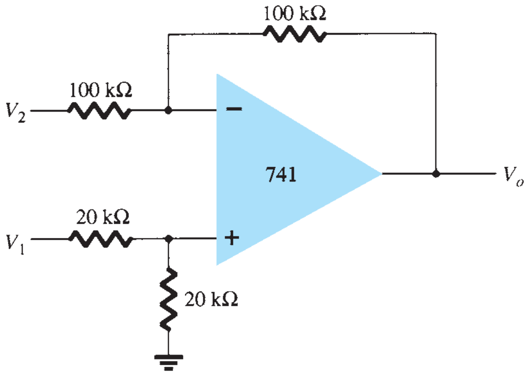


FIG. 11.12
Circuit for Example 11.8.

Solution: The resulting output voltage can be expressed as

$$V_o = \left(\frac{20\text{ k}\Omega}{20\text{ k}\Omega + 20\text{ k}\Omega}\right)\left(\frac{100\text{ k}\Omega + 100\text{ k}\Omega}{100\text{ k}\Omega}\right)V_1 - \frac{100\text{ k}\Omega}{100\text{ k}\Omega}V_2$$
$$= V_1 - V_2$$

The resulting output voltage is seen to be the difference of the two input voltages.

11.3 VOLTAGE BUFFER

A voltage buffer circuit provides a means of isolating an input signal from a load by using a stage having unity voltage gain, with no phase or polarity inversion, and acting as an ideal circuit with very high input impedance and low output impedance. Figure 11.13 shows an op-amp connected to provide this buffer amplifier operation. The output voltage is determined by

$$\boxed{V_o = V_1} \tag{11.6}$$

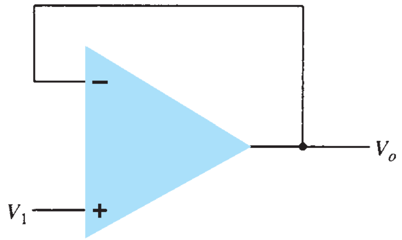


FIG. 11.13
Unity-gain (buffer) amplifier.

Figure 11.14 shows how an input signal can be provided to two separate outputs. The advantage of this connection is that the load connected across one output has no (or little) effect on the other output. In effect, the outputs are buffered or isolated from each other.

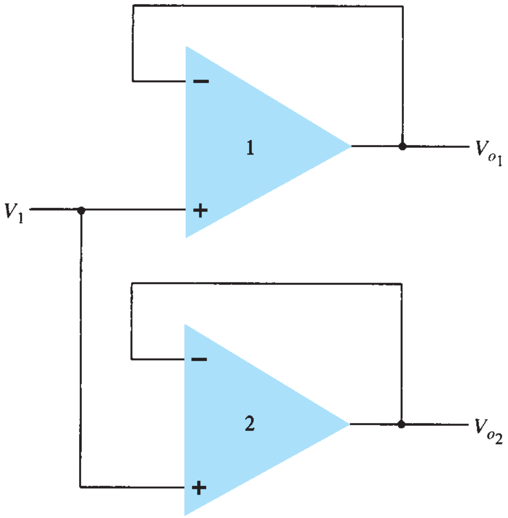


FIG. 11.14
Use of buffer amplifier to provide output signals.

EXAMPLE 11.9 Show the connection of a 741 as a unity-gain circuit.

Solution: The connection is shown in Fig. 11.15.

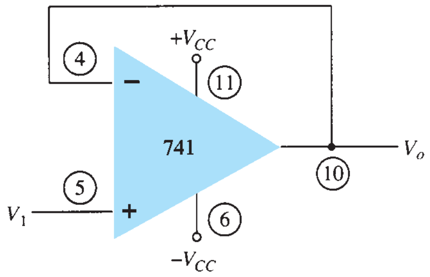


FIG. 11.15
Connection for Example 11.9.

11.4 CONTROLLED SOURCES

Operational amplifiers can be used to form various types of controlled sources. An input voltage can be used to control an output voltage or current, or an input current can be used to control an output voltage or current. These types of connections are suitable for use in various instrumentation circuits. A form of each type of controlled source is provided next.

Voltage-Controlled Voltage Source

An ideal form of a voltage source whose output V_o is controlled by an input voltage V_1 is shown in Fig. 11.16. The output voltage is seen to be dependent on the input voltage (times a scale factor k). This type of circuit can be built using an op-amp as shown in Fig. 11.17. Two versions of the circuit are shown, one using the inverting input, the other the noninverting input. For the connection of Fig. 11.17a, the output voltage is

$$\boxed{V_o = -\frac{R_f}{R_1}V_1 = kV_1} \tag{11.7}$$

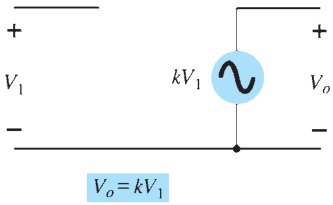
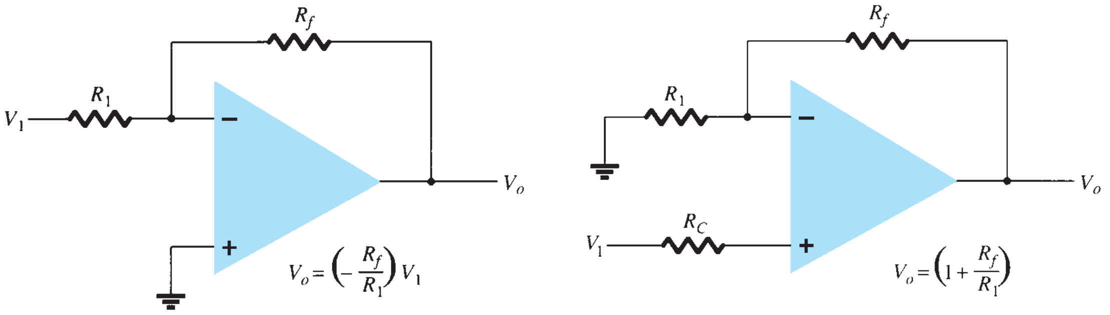


FIG. 11.16
Ideal voltage-controlled voltage source.



R_f
R_1
V_1
–
+
V_o
$V_o = \left(-\frac{R_f}{R_1}\right)V_1$
R_f
R_1
–
R_C
V_1
+
V_o
$V_o = \left(1 + \frac{R_f}{R_1}\right)$

(a) (b)

FIG. 11.17
Practical voltage-controlled voltage source circuits.

whereas that of Fig. 11.17b results in

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = kV_1} \qquad \textbf{(11.8)}$$

Voltage-Controlled Current Source

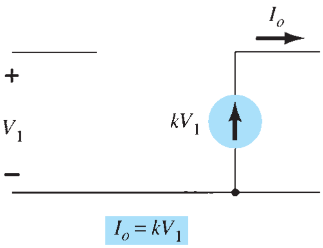


FIG. 11.18
Ideal voltage-controlled current source.

An ideal form of circuit providing an output current controlled by an input voltage is that of Fig. 11.18. The output current is dependent on the input voltage. A practical circuit can be built, as in Fig. 11.19, with the output current through load resistor R_L controlled by the input voltage V_1. The current through load resistor R_L can be seen to be

$$\boxed{I_o = \frac{V_1}{R_1} = kV_1} \qquad \textbf{(11.9)}$$

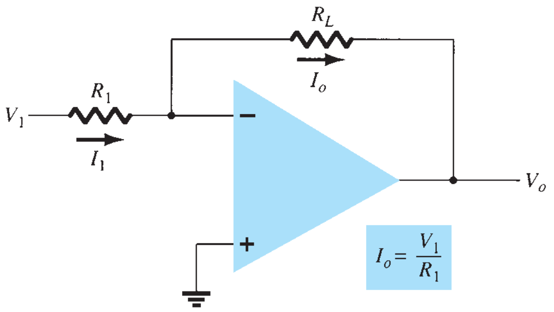


FIG. 11.19
Practical voltage-controlled current source.

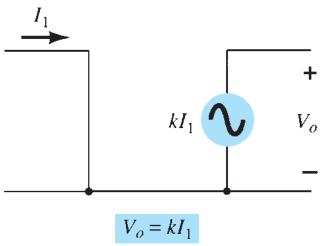


FIG. 11.20
Ideal current-controlled voltage source.

Current-Controlled Voltage Source

An ideal form of a voltage source controlled by an input current is shown in Fig. 11.20. The output voltage is dependent on the input current. A practical form of the circuit is built using an op-amp as shown in Fig. 11.21. The output voltage is seen to be

$$\boxed{V_o = -I_1R_L = kI_1} \qquad \textbf{(11.10)}$$

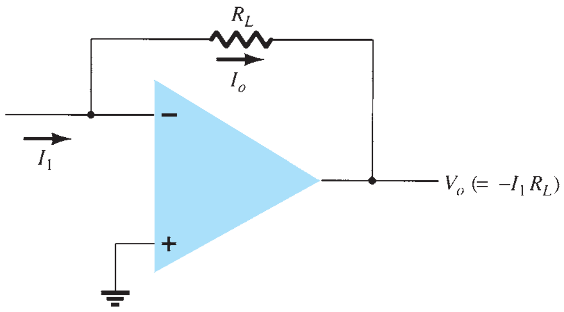


FIG. 11.21
Practical form of current-controlled voltage source.

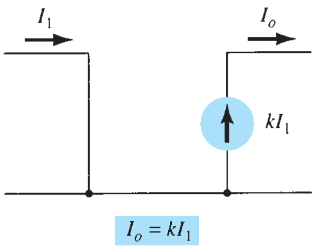


FIG. 11.22
Ideal current-controlled current source.

Current-Controlled Current Source

An ideal form of a circuit providing an output current dependent on an input current is shown in Fig. 11.22. In this type of circuit, an output current is provided dependent on the input current. A practical form of the circuit is shown in Fig. 11.23. The input current I_1 can be shown to result in the output current I_o so that

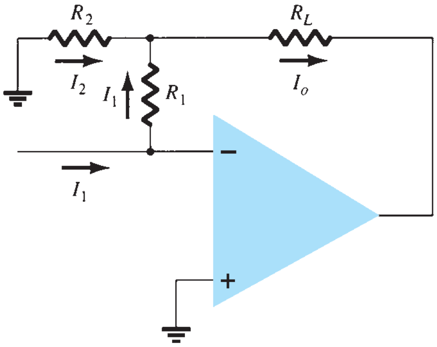

R_2
R_L
I_2
I_1
R_1
I_o
I_1
–
+

FIG. 11.23
Practical form of current-controlled current source.

$$\boxed{I_o = I_1 + I_2 = I_1 + \frac{I_1R_1}{R_2} = \left(1 + \frac{R_1}{R_2}\right)I_1 = kI_1} \tag{11.11}$$

EXAMPLE 11.10

a. For the circuit of Fig. 11.24a, calculate I_L.
b. For the circuit of Fig. 11.24b, calculate V_o.

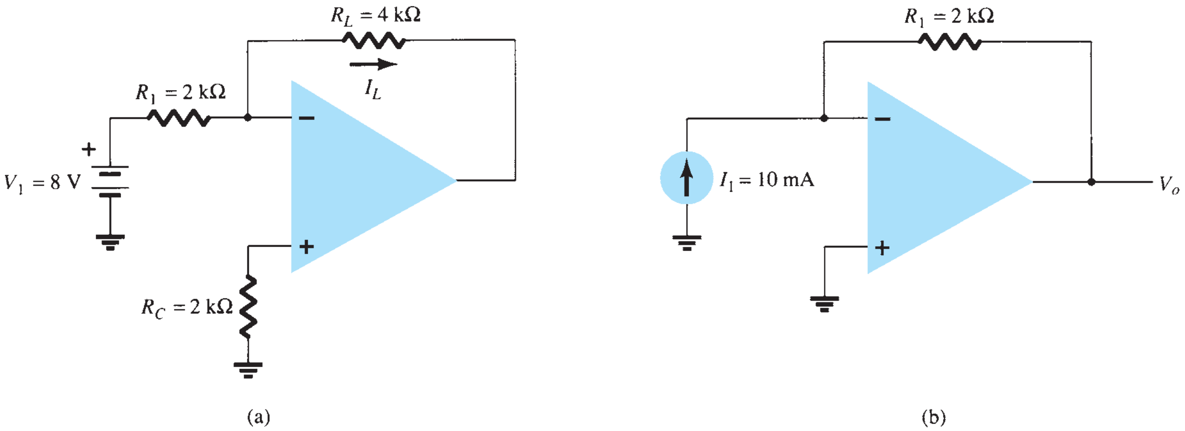

$R_L = 4\text{ k}\Omega$
I_L
$R_1 = 2\text{ k}\Omega$
+
$V_1 = 8\text{ V}$
–
+
$R_C = 2\text{ k}\Omega$
(a)
$R_1 = 2\text{ k}\Omega$
$I_1 = 10\text{ mA}$
–
+
V_o
(b)

FIG. 11.24
Circuits for Example 11.10.

Solution:

a. For the circuit of Fig. 11.24a,

$$I_L = \frac{V_1}{R_1} = \frac{8\text{ V}}{2\text{ k}\Omega} = \mathbf{4\text{ mA}}$$

b. For the circuit of Fig. 11.24b,

$$V_o = -I_1R_1 = -(10\text{ mA})(2\text{ k}\Omega) = \mathbf{-20\text{ V}}$$

11.5 INSTRUMENTATION CIRCUITS

A popular area of op-amp application is in instrumentation circuits such as dc or ac voltmeters. A few typical circuits will demonstrate how op-amps can be used.

dc Millivoltmeter

Figure 11.25 shows a 741 op-amp used as the basic amplifier in a dc millivoltmeter. The amplifier provides a meter with high input impedance and scale factors dependent only on resistor value and accuracy. Notice that the meter reading represents millivolts of signal at the circuit input. An analysis of the op-amp circuit provides the circuit transfer function

$$\left|\frac{I_o}{V_1}\right| = \frac{R_f}{R_1}\left(\frac{1}{R_S}\right) = \left(\frac{100\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{10\text{ mV}}$$

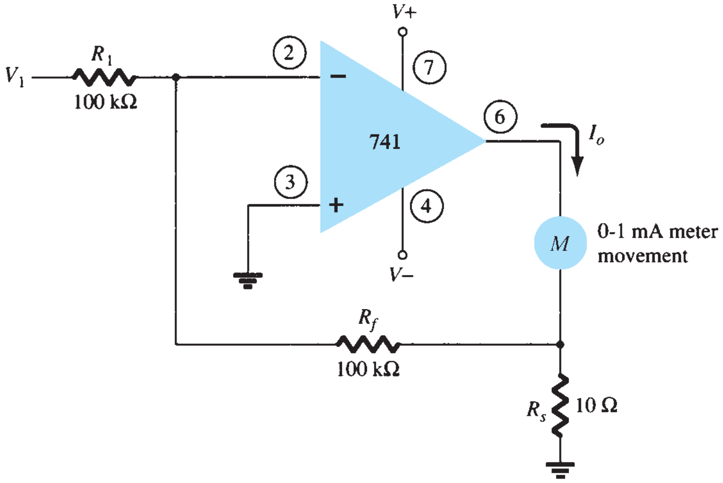


FIG. 11.25
Op-amp dc millivoltmeter.

Thus, an input of 10 mV will result in a current through the meter of 1 mA. If the input is 5 mV, the current through the meter will be 0.5 mA, which is half-scale deflection. Changing R_f to 200 kΩ, for example, would result in a circuit scale factor of

$$\left|\frac{I_o}{V_1}\right| = \left(\frac{200\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{5\text{ mV}}$$

showing that the meter now reads 5 mV, full scale. It should be kept in mind that building such a millivoltmeter requires purchasing an op-amp, a few resistors, diodes, capacitors, and a meter movement.

ac Millivoltmeter

Another example of an instrumentation circuit is the ac millivoltmeter shown in Fig. 11.26. The circuit transfer function is

$$\left|\frac{I_o}{V_1}\right| = \frac{R_f}{R_1}\left(\frac{1}{R_S}\right) = \left(\frac{100\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{10\text{ mV}}$$

which appears the same as the dc millivoltmeter, except that in this case the signal handled is an ac signal. The meter indication provides a full-scale deflection for an ac input voltage of 10 mV, whereas an ac input of 5 mV will result in half-scale deflection with the meter reading interpreted in millivolt units.

Display Driver

Figure 11.27 shows op-amp circuits that can be used to drive a lamp display or LED display. When the noninverting input to the circuit in Fig. 11.27a goes above the inverting input, the output at terminal 1 goes to the positive saturation level (near +5 V in this example) and the lamp is driven "on" when transistor Q_1 conducts. As shown in the circuit, the output of the op-amp provides 30 mA of current to the base of transistor Q_1, which then drives 600 mA through a suitably selected transistor (with $\beta > 20$) capable of handling that amount of current. Figure 11.27b shows an op-amp circuit that can supply 20 mA to drive an LED display when the noninverting input goes positive compared to the inverting input.

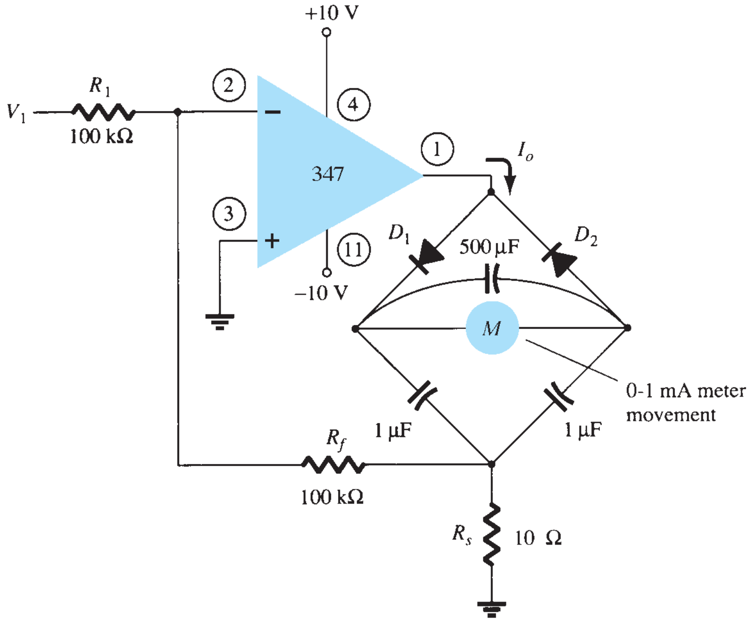
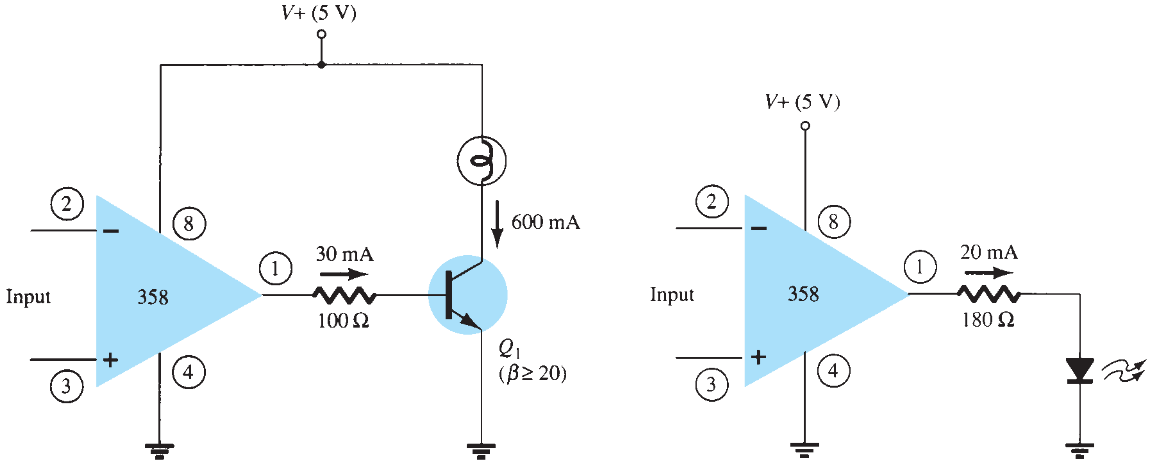

+10 V
R_1
V_1
100 kΩ
②
④
347
①
I_o
③
⑪
−10 V
D_1
500 μF
D_2
M
0-1 mA meter movement
R_f
1 μF
1 μF
100 kΩ
R_s
10 Ω

FIG. 11.26
AC millivoltmeter using op-amp.


V+ (5 V)
②
⑧
Input
358
①
30 mA
100 Ω
600 mA
Q_1
($\beta \geq 20$)
③
④
V+ (5 V)
②
⑧
Input
358
①
20 mA
180 Ω
③
④

(a)

(b)

FIG. 11.27
Display driver circuits: (a) lamp driver; (b) LED driver.

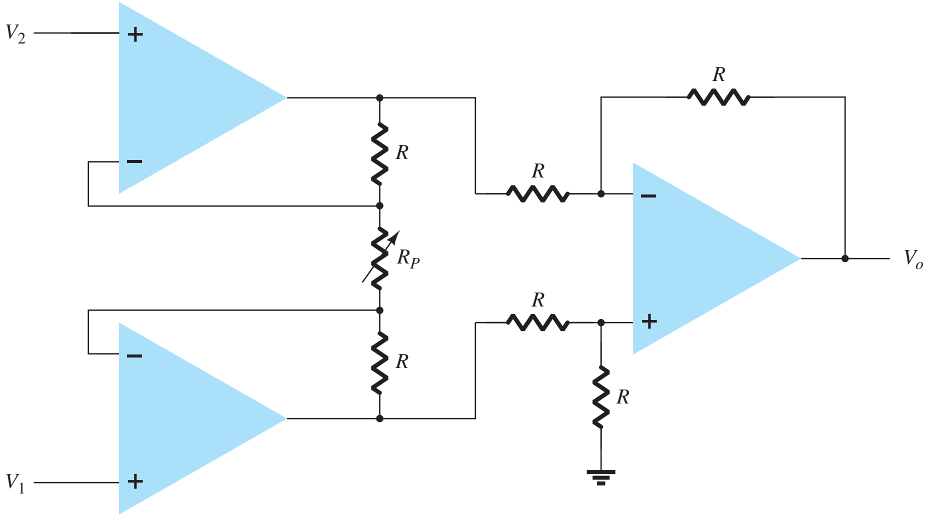
Instrumentation Amplifier

A circuit providing an output based on the difference between two inputs (times a scale factor) is shown in Fig. 11.28. A potentiometer is provided to permit adjusting the scale factor of the circuit. Whereas three op-amps are used, a single-quad op-amp IC is all that is necessary (other than the resistor components). The output voltage can be shown to be

$$\frac{V_o}{V_1 - V_2} = 1 + \frac{2R}{R_P}$$

so that the output can be obtained from

$$\boxed{V_o = \left(1 + \frac{2R}{R_P}\right)(V_1 - V_2) = k(V_1 - V_2)} \qquad \textbf{(11.12)}$$

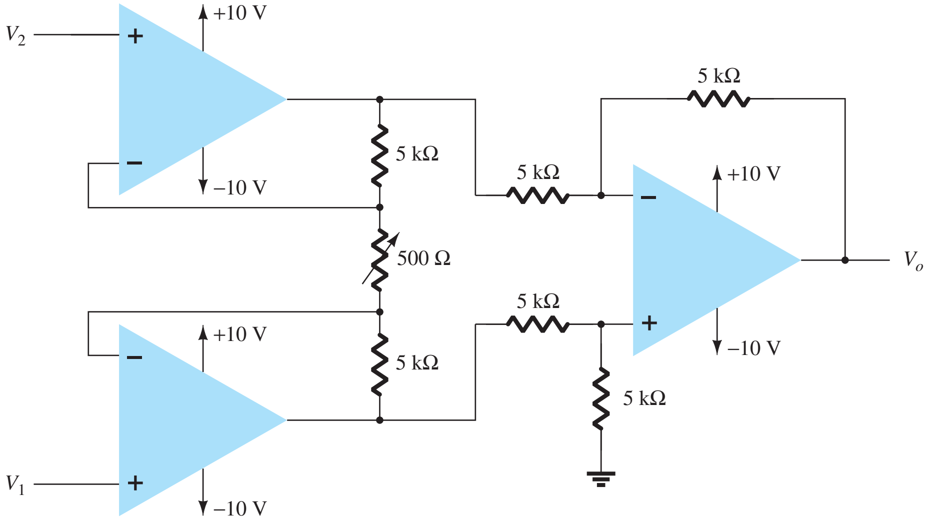


V_2
+
−
R
R_P
R
−
+
V_1
R
R
R
−
+
R
V_o

FIG. 11.28

Instrumentation amplifier.

EXAMPLE 11.11 Calculate the output voltage expression for the circuit of Fig. 11.29.



V_2
+
−
+10 V
−10 V
5 kΩ
500 Ω
5 kΩ
−
+
+10 V
−10 V
V_1
5 kΩ
5 kΩ
5 kΩ
5 kΩ
+10 V
−10 V
−
+
V_o

FIG. 11.29

Circuit for Example 11.11.

Solution: The output voltage can then be expressed using Eq. (11.12) as

$$V_o = \left(1 + \frac{2R}{R_P}\right)(V_1 - V_2) = \left[1 + \frac{2(5000)}{500}\right](V_1 - V_2)$$

$$= \mathbf{21(V_1 - V_2)}$$

11.6 ACTIVE FILTERS

A popular application uses op-amps to build active filter circuits. A filter circuit can be constructed using passive components: resistors and capacitors. An active filter additionally uses an amplifier to provide voltage amplification and signal isolation or buffering.

A filter that provides a constant output from dc up to a cutoff frequency f_{OH} and then passes no signal above that frequency is called an ideal low-pass filter. The ideal response of a low-pass filter is shown in Fig. 11.30a. A filter that provides or passes signals above a cutoff frequency f_{OL} is a high-pass filter, as idealized in Fig. 11.30b. When the filter circuit passes signals that are above one ideal cutoff frequency and below a second cutoff frequency, it is called a bandpass filter, as idealized in Fig. 11.30c.

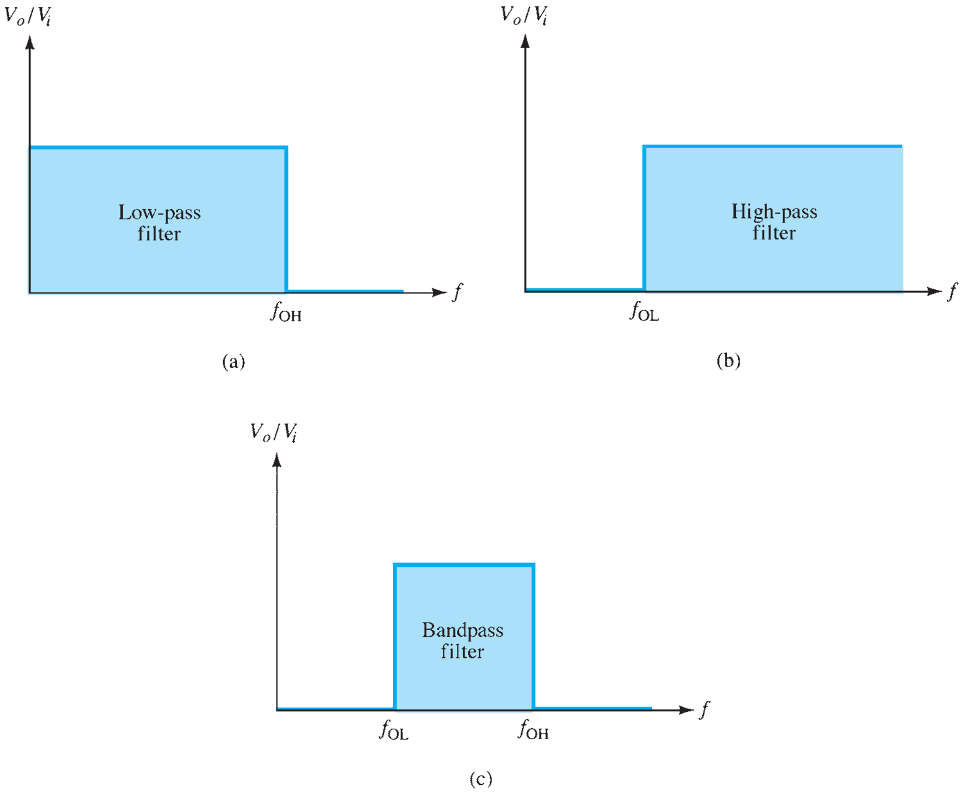


FIG. 11.30

Ideal filter response: (a) low-pass; (b) high-pass; (c) bandpass.

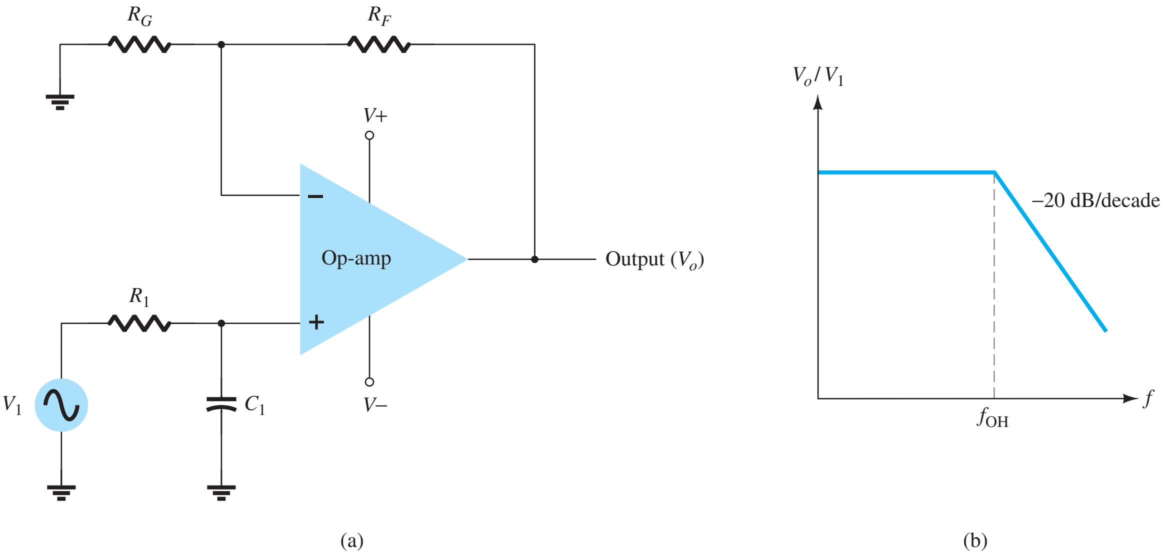
Low-Pass Filter

A first-order, low-pass filter using a single resistor and capacitor as in Fig. 11.31a has a practical slope of −20 dB per decade, as shown in Fig. 11.31b (rather than the ideal response of Fig. 11.30a). The voltage gain below the cutoff frequency is constant at

$$\boxed{A_v = 1 + \frac{R_F}{R_G}} \tag{11.13}$$

at a cutoff frequency of

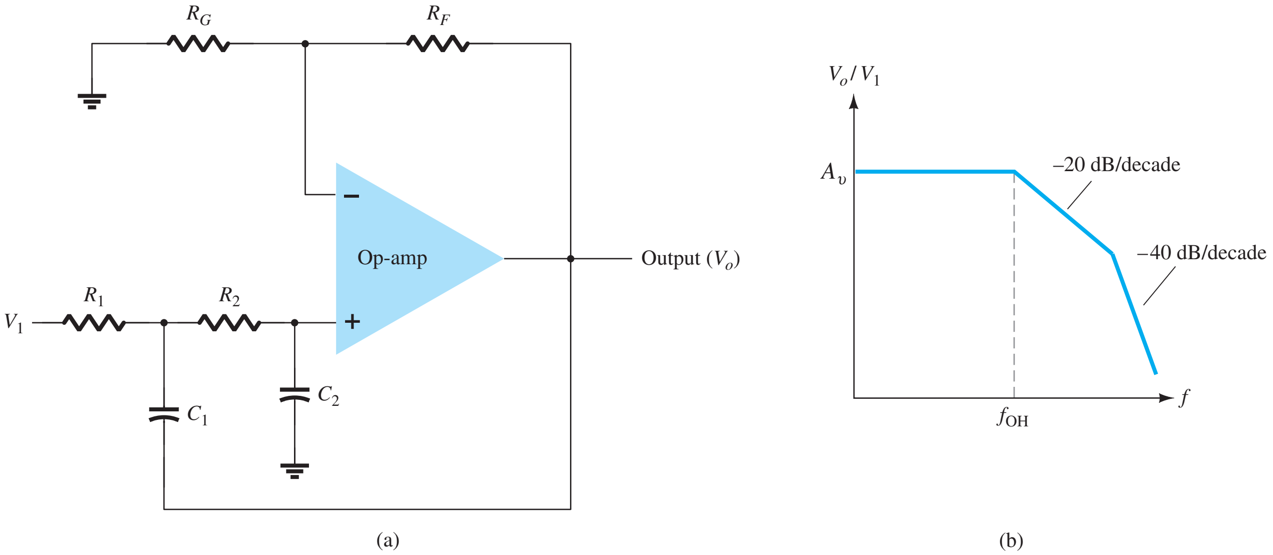
$$\boxed{f_{OH} = \frac{1}{2\pi R_1 C_1}} \tag{11.14}$$



R_G
R_F
$V+$
–
Op-amp
+
Output (V_o)
R_1
V_1
C_1
$V-$
(a)
V_o/V_1
–20 dB/decade
f_{OH}
f
(b)

FIG. 11.31
First-order low-pass active filter.

Connecting two sections of filter as in Fig. 11.32 results in a second-order low-pass filter with cutoff at -40 dB per decade—closer to the ideal characteristic of Fig. 11.30a. The circuit voltage gain and the cutoff frequency are the same for the second-order circuit as for the first-order filter circuit, except that the filter response drops at a faster rate for a second-order filter circuit.



R_G
R_F
–
Op-amp
+
Output (V_o)
V_1
R_1
R_2
C_1
C_2
(a)
V_o/V_1
A_v
–20 dB/decade
–40 dB/decade
f_{OH}
f
(b)

FIG. 11.32
Second-order low-pass active filter.

EXAMPLE 11.12 Calculate the cutoff frequency of a first-order low-pass filter for $R_1 = 1.2\ \text{k}\Omega$ and $C_1 = 0.02\ \mu\text{F}$.

Solution:

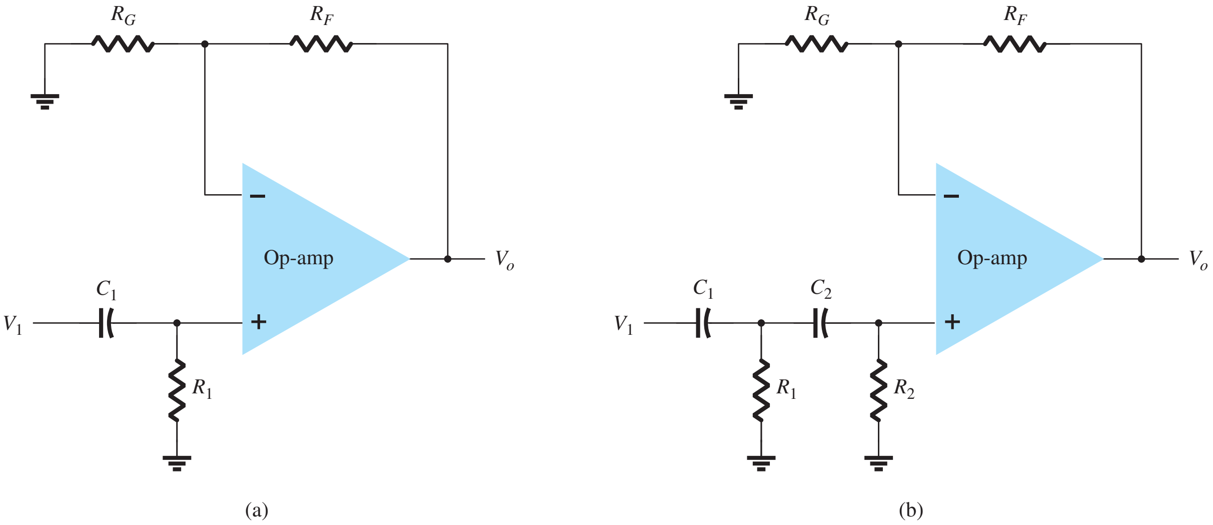
$$f_{OH} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(1.2 \times 10^3)(0.02 \times 10^{-6})} = \mathbf{6.63\ kHz}$$

High-Pass Active Filter

First- and second-order high-pass active filters can be built as shown in Fig. 11.33. The amplifier gain is calculated using Eq. (11.13). The amplifier cutoff frequency is

$$\boxed{f_{\mathrm{OL}} = \frac{1}{2\pi R_1 C_1}} \qquad \textbf{(11.15)}$$

with a second-order filter $R_1 = R_2$, and $C_1 = C_2$ results in the same cutoff frequency as in Eq. (11.15).



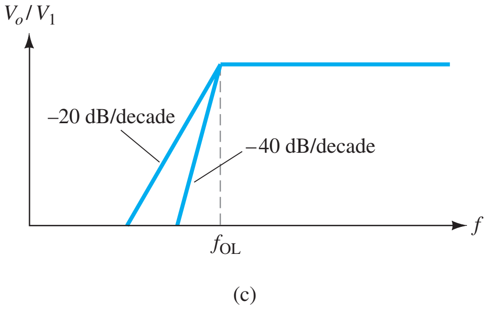


FIG. 11.33
High-pass filter: (a) first order; (b) second order; (c) response plot.

EXAMPLE 11.13 Calculate the cutoff frequency of a second-order high-pass filter as in Fig. 11.33b for $R_1 = R_2 = 2.1\ \mathrm{k\Omega}$, $C_1 = C_2 = 0.05\ \mu\mathrm{F}$, and $R_G = 10\ \mathrm{k\Omega}$, $R_F = 50\ \mathrm{k\Omega}$.

Solution:

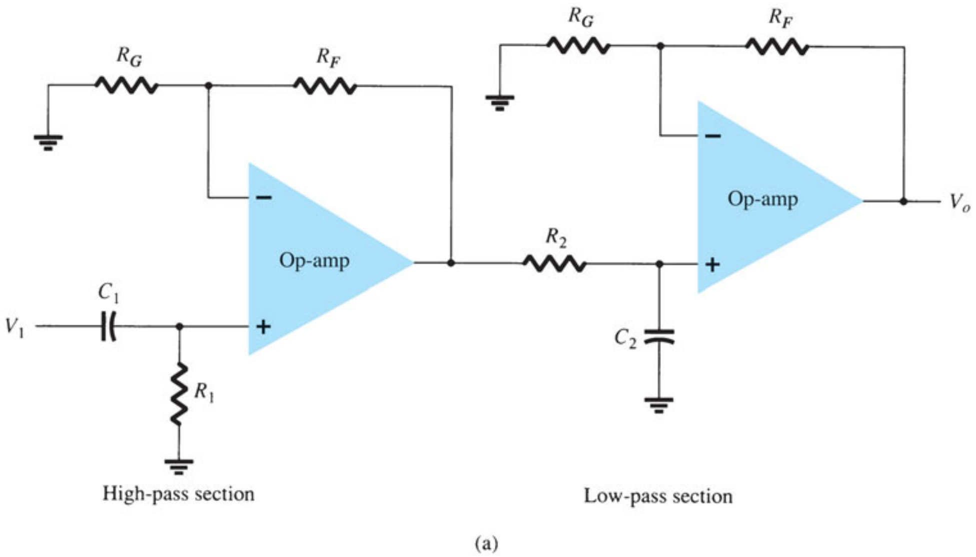
$$\text{Eq. (11.13):} \quad A_v = 1 + \frac{R_F}{R_G} = 1 + \frac{50\ \mathrm{k\Omega}}{10\ \mathrm{k\Omega}} = 6$$

The cutoff frequency is then

$$\text{Eq. (11.15):} \quad f_{\mathrm{OL}} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(2.1 \times 10^3)(0.05 \times 10^{-6})} \approx \mathbf{1.5\ kHz}$$

Bandpass Filter

Figure 11.34 shows a bandpass filter using two stages, the first a high-pass filter and the second a low-pass filter, the combined operation being the desired bandpass response.



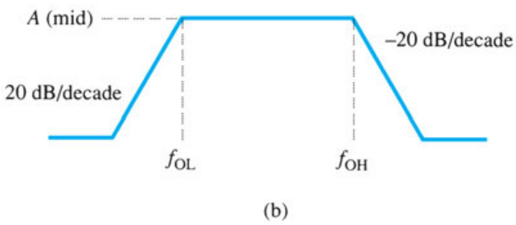


FIG. 11.34
Bandpass active filter.

EXAMPLE 11.14 Calculate the cutoff frequencies of the bandpass filter circuit of Fig. 11.34 with $R_1 = R_2 = 10\text{ k}\Omega$, $C_1 = 0.1\ \mu\text{F}$, and $C_2 = 0.002\ \mu\text{F}$.

Solution:

$$f_{OL} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(10 \times 10^3)(0.1 \times 10^{-6})} = \mathbf{159.15\ Hz}$$

$$f_{OH} = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi(10 \times 10^3)(0.002 \times 10^{-6})} = \mathbf{7.96\ kHz}$$

11.7 SUMMARY

Equations

Constant-gain multiplier:

$$A = -\frac{R_f}{R_1}$$

Noninverting constant-gain multiplier:

$$A = 1 + \frac{R_f}{R_1}$$

Voltage-summing amplifier:

$$A = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

Voltage buffer:

$$V_o = V_1$$

Low-pass active filter cutoff frequency:

$$f_{\text{OH}} = \frac{1}{2\pi R_1 C_1}$$

High-pass active filter cutoff frequency:

$$f_{\text{OL}} = \frac{1}{2\pi R_1 C_1}$$

11.8 COMPUTER ANALYSIS

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems will be used to display the resulting dc bias or, using **PROBE**, to display resulting waveforms. As always, first use **Schematic** drawing to draw the circuit diagram and set the desired analysis, then use **Simulation** to analyze the circuit. Finally, examine the resulting **Output** or use **PROBE** to view various waveforms.

Program 11.1—Summing Op-Amp

A summing op-amp using a 741 IC is shown in the OrCAD schematic in Fig. 11.35. Three dc voltage inputs are summed, with a resulting output dc voltage determined as follows:

$$\begin{aligned} V_o &= -[(100\,\text{k}\Omega/20\,\text{k}\Omega)(+2\text{ V}) + (100\,\text{k}\Omega/50\,\text{k}\Omega)(-3\text{ V}) \\ &\qquad + (100\,\text{k}\Omega/10\,\text{k}\Omega(+1\text{ V})] \\ &= -[(10\text{ V}) + (-6\text{ V}) + (10\text{ V})] = -[20\text{ V} - 6\text{ V}] = -14\text{ V} \end{aligned}$$

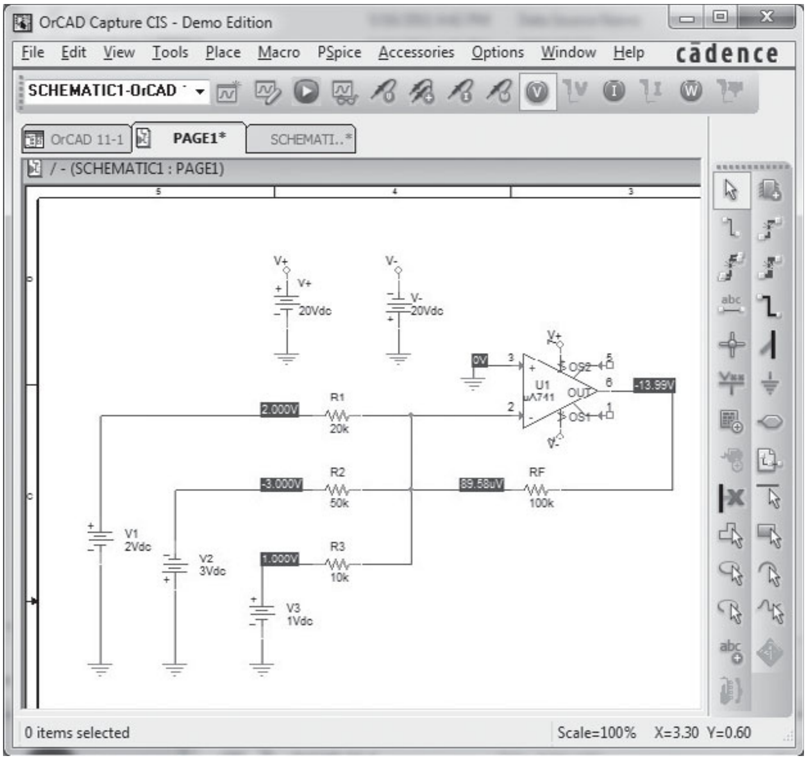

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 11-1
PAGE1*
SCHEMATI..*
/ - (SCHEMATIC1 : PAGE1)
V+
V+
20Vdc
V-
V-
20Vdc
V+
0V
3
U1
uA741
OS2
5
OUT
6
-13.99V
2
OS1
1
V-
2.000V
R1
20k
-3.000V
R2
50k
89.58uV
RF
100k
1.000V
R3
10k
V1
2Vdc
V2
3Vdc
V3
1Vdc
0 items selected
Scale=100%
X=3.30 Y=0.60

FIG. 11.35

Summing amplifier using a μA741 op-amp.

The steps in drawing the circuit and doing the analysis are as follows. Using **Get New Part**:

Select **μA741**.
Select **R** and repeatedly place three input resistors and one feedback resistor; set resistor values and change resistor names, if desired.
Select **VDC** and place three input voltages and two supply voltages; set voltage values and change voltage names, if desired.
Select **GLOBAL** (global connector) and use to identify supply voltages and make connection to op-amp power input terminals (4 and 7).

Now that the circuit is drawn and all part names and values set as in Fig. 11.35, press the **Simulation** (Run PSpice) button to have PSpice analyze the circuit. Since no specific analysis has been chosen, only the dc bias will be carried out.

Press the **Enable Bias Voltage Display** button to see the dc voltages at various points in the circuit. The bias voltages displayed in Fig. 11.35 show the output to be -13.99 V (compared to the calculated value of -14 V above).

Program 11.2—Op-Amp DC Voltmeter

A dc voltmeter built using a μA741 op-amp is provided by the OrCAD schematic of Fig. 11.36. From the material presented in Section 11.5, the transfer function of the circuit is

$$I_o/V_1 = (R_F/R_1)(1/R_S) = (1\ \text{M}\Omega/1\ \text{M}\Omega)(1/10\ \text{k}\Omega)$$

The full-scale setting of this voltmeter (for I_o full scale at 1 mA) is then

$$V_1(\text{full scale}) = (10\ \text{k}\Omega)(1\ \text{mA}) = 10\ \text{V}$$

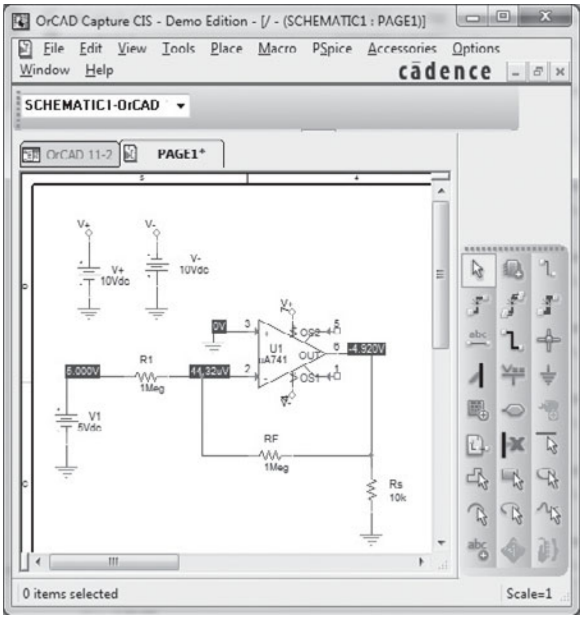

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options
Window Help
cadence
SCHEMATIC1-OrCAD
OrCAD 11-2
PAGE1*
V+
V-
V+
10Vdc
V-
10Vdc
V+
0V
3
OS2
5
U1
μA741
OUT
6
-4.920V
5.000V
R1
1Meg
44.32uV
2
OS1
1
V-
V1
5Vdc
RF
1Meg
Rs
10k
0 items selected
Scale=1

FIG. 11.36
Op-amp dc voltmeter.

Thus, an input of 10 V will result in a meter current of 1 mA—the full-scale deflection of the meter. Any input less then 10 V will result in a proportionately smaller meter deflection.

The steps in drawing the circuit and doing the analysis are as follows. Using **Get New Part**:

Select **μA741.**
Select **R** and repeatedly place input resistor, feedback resistor, and meter setting resistor; set resistor values and change resistor names, if desired.
Select **VDC** and place input voltage and two supply voltages; set voltage values and change voltage names, if desired.

Select **GLOBAL** (global connector) and use to identify supply voltages and make connection to op-amp power input terminals (4 and 7).
Select **IPROBE** and use as meter movement.

Now that the circuit is drawn and all part names and values set as in Fig. 11.36, press the **Simulation** button (Run PSpice) to have PSpice analyze the circuit. Since no specific analysis has been chosen, only the dc bias will be carried out.

Figure 11.36 shows that an input of 5 V will result in a current of 0.5 mA, with the meter reading of 0.5 being read as 5 V (since 1 mA full scale will occur for 10 V input).

Program 11.3—Low-Pass Active Filter

Figure 11.37 shows the schematic of a low-pass active filter. This first-order filter circuit passes frequencies from dc up to the cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{OH} = 1/(2\pi R_1 C_1)$$

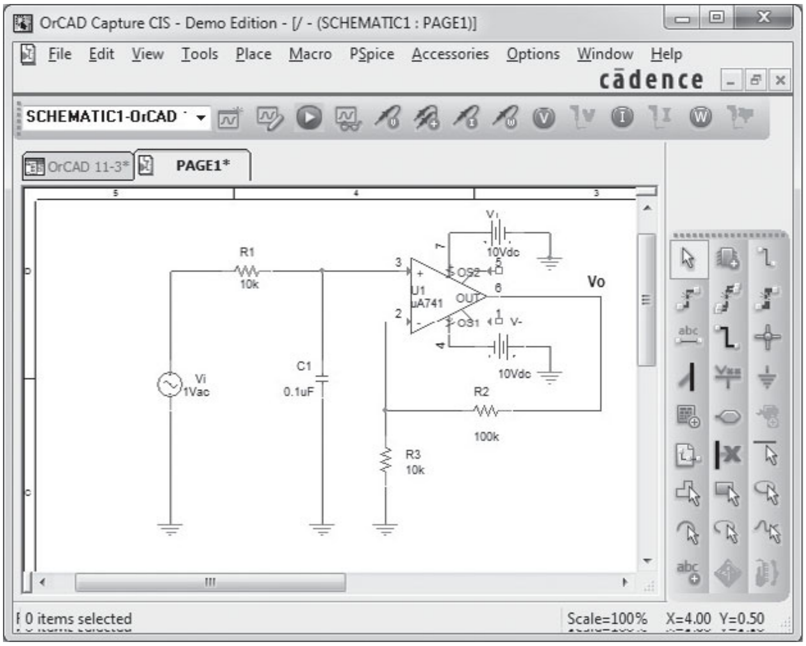

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 11-3*
PAGE1*
R1
10k
V+
10Vdc
U1
uA741
OS2
OUT
OS1
V-
Vo
Vi
1Vac
C1
0.1uF
10Vdc
R2
100k
R3
10k
0 items selected
Scale=100%
X=4.00 Y=0.50

FIG. 11.37
Low-pass active filter.

For the circuit of Fig. 11.37, this is

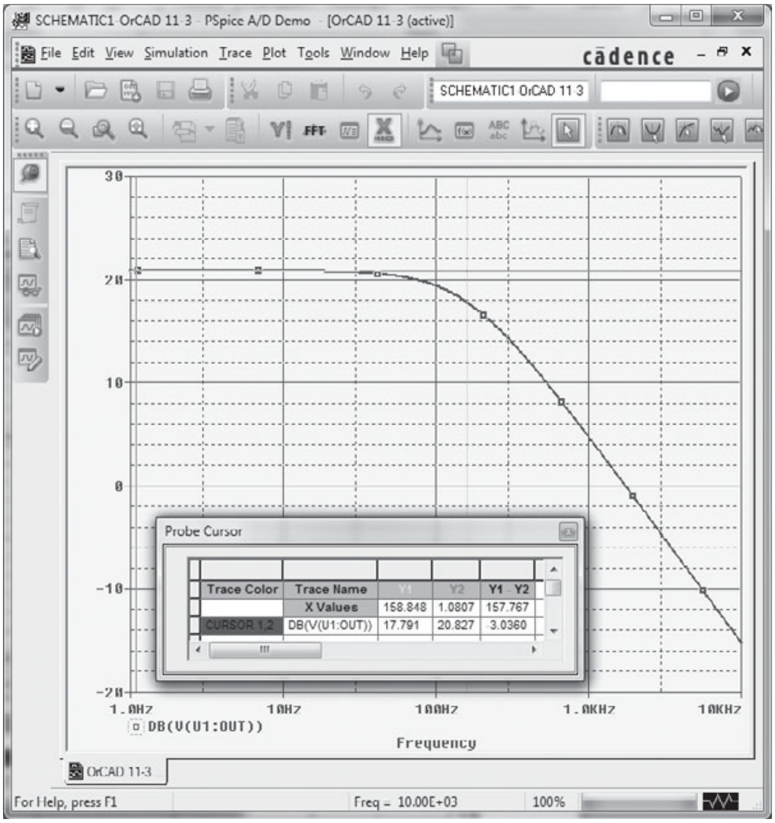
$$f_{OH} = 1/(2\pi R_1 C_1) = 1/(2\pi \cdot 10\ \text{k}\Omega \cdot 0.1\ \mu\text{F}) = 159\ \text{Hz}$$

Figure 11.38 shows the result obtained using the **Analysis Setup-AC frequency** and then choosing an ac sweep of 100 points per decade from 1 Hz to 10 kHz. After running the analysis, the **Analysis Graph** is created as shown in Fig. 11.38. The cutoff frequency obtained is seen to be 158.8, very close to that calculated above.

Program 11.4—High-Pass Active Filter

Figure 11.39 shows the schematic of a high-pass active filter. This first-order filter circuit passes frequencies above a cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{OL} = 1/(2\pi R_1 C_1)$$


SCHEMATIC1-OrCAD 11-3 - PSpice A/D Demo - [OrCAD 11-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1 OrCAD 11-3
30
20
10
0
-10
-20
1.0Hz
10Hz
100Hz
1.0KHz
10KHz
DB(V(U1:OUT))
Frequency
OrCAD 11-3
For Help, press F1
Freq = 10.00E+03
100%

Probe Cursor

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	158.848	1.0807	157.767
CURSOR 1,2	DB(V(U1:OUT))	17.791	20.827	-3.0360

FIG. 11.38
AC analysis of low-pass filter.

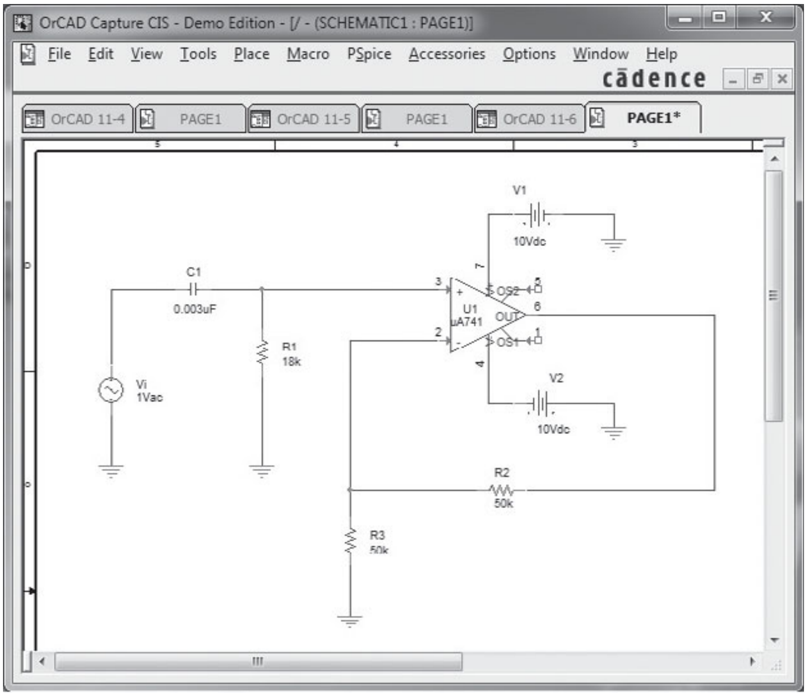
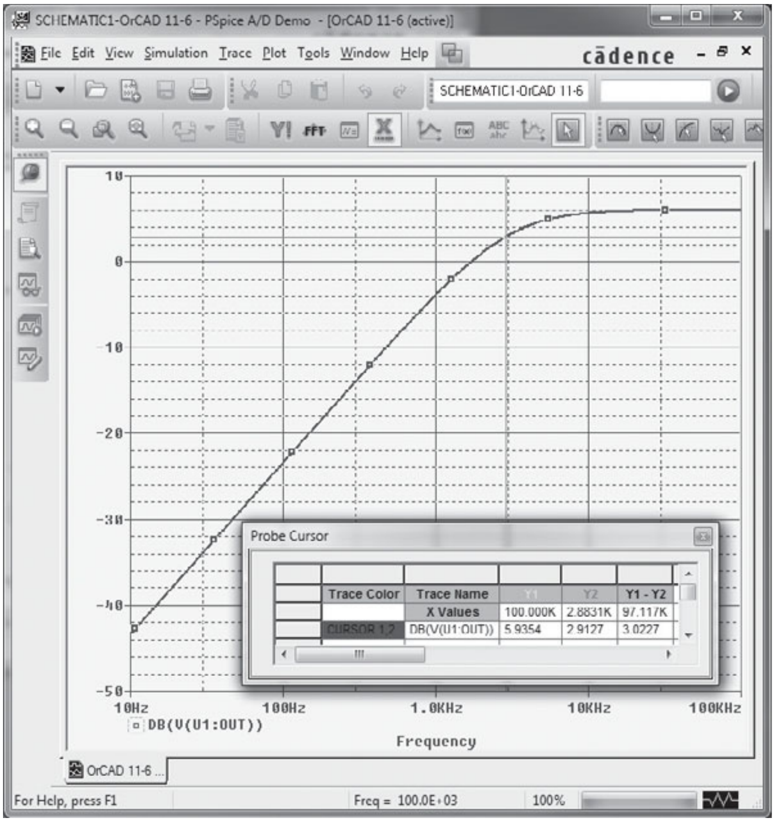

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
OrCAD 11-4
PAGE1
OrCAD 11-5
PAGE1
OrCAD 11-6
PAGE1*
V1
10Vdc
C1
0.003uF
R1
18k
Vi
1Vac
U1
uA741
OUT
OS2
OS1
V2
10Vdc
R2
50k
R3
50k

FIG. 11.39
High-pass active filter.

For the circuit of Fig. 11.39, this is

$$f_{OH} = 1/(2\pi R_1C_1) = 1/(2\pi \cdot 18\text{ k}\Omega \cdot 0.003\ \mu\text{F}) = 2.95\text{ kHz}$$

The **Analysis** is set for an ac sweep of 100 points per decade from 10 Hz to 100 kHz. After running the analysis, the output showing the output voltage in dB units is that shown in Fig. 11.40. The cutoff frequency obtained is seen to be 2.9 kHz, very close to that calculated above.


SCHEMATIC1-OrCAD 11-6 - PSpice A/D Demo - [OrCAD 11-6 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 11-6
10
0
-10
-20
-30
-40
-50
10Hz
100Hz
1.0KHz
10KHz
100KHz
DB(V(U1:OUT))
Frequency
Probe Cursor
OrCAD 11-6 ...
For Help, press F1
Freq = 100.0E+03
100%

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	100.000K	2.8831K	97.117K
CURSOR 1,2	DB(V(U1:OUT))	5.9354	2.9127	3.0227

FIG. 11.40

dB output plot for the active high-pass filter circuit of Fig. 11.39.

Program 11.5—Second-Order High-Pass Active Filter

Figure 11.41 shows the schematic of a second-order high-pass active filter using Orcad. This second-order filter circuit passes frequencies above a cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{\mathrm{OL}} = 1/(2\pi R_1 C_1)$$

For the circuit of Fig. 11.41, this is

$$f_{\mathrm{OL}} = 1/(2\pi R_1 C_1) = 1/(2\pi \cdot 18\ \mathrm{k}\Omega \cdot 0.0022\ \mu\mathrm{F}) = 4\ \mathrm{kHz}$$

The **Analysis Setup** is set for an ac sweep of 20 points per decade from 100 Hz to 100 kHz, as shown in Fig. 11.42. After running the analysis, we find the **PROBE** output showing

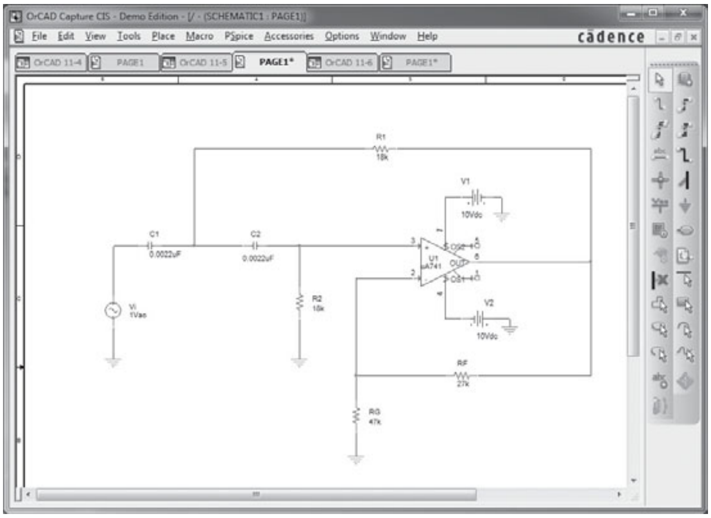
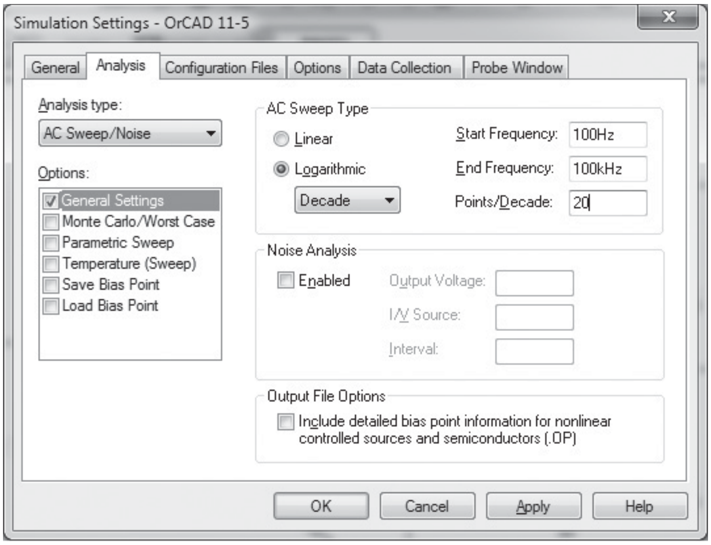

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
OrCAD 11-4
PAGE1
OrCAD 11-5
PAGE1*
OrCAD 11-6
PAGE1*
R1
18k
V1
10Vdc
C1
0.0022uF
C2
0.0022uF
3
2
U1
uA741
OS2
OUT
OS1
7
4
5
6
1
R2
18k
Vi
1Vac
V2
10Vdc
RF
27k
RG
47k

FIG. 11.41

Second-order high-pass filter.


Simulation Settings - OrCAD 11-5
General
Analysis
Configuration Files
Options
Data Collection
Probe Window
OK
Cancel
Apply
Help

Analysis type: AC Sweep/Noise

Options:
☑ General Settings
☐ Monte Carlo/Worst Case
☐ Parametric Sweep
☐ Temperature (Sweep)
☐ Save Bias Point
☐ Load Bias Point

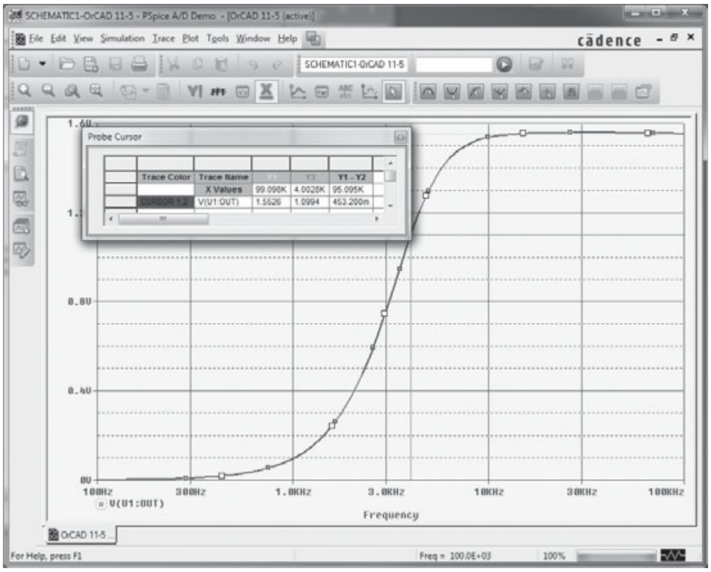
AC Sweep Type
○ Linear
● Logarithmic
Decade
Start Frequency: 100Hz
End Frequency: 100kHz
Points/Decade: 20

Noise Analysis
☐ Enabled
Output Voltage:
I/V Source:
Interval:

Output File Options
☐ Include detailed bias point information for nonlinear controlled sources and semiconductors (.OP)

FIG. 11.42

Analysis setup for Fig. 11.41.


SCHEMATIC1-OrCAD 11-5 - PSpice A/D Demo - [OrCAD 11-5 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 11-5
1.6V
1.2V
0.8V
0.4V
0V
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
V(U1:OUT)
Frequency
OrCAD 11-5

Probe Cursor

	Trace Color	Trace Name	Y1	Y2	Y1 - Y2
		X Values	99.098K	4.0028K	95.095K
	CURSOR 1,2	V(U1:OUT)	1.5526	1.0994	453.200m

For Help, press F1
Freq = 100.0E+03
100%

FIG. 11.43

Probe plot of V_o for second-order high-pass active filter.

the output voltage (V_o) as in Fig. 11.43. The cutoff frequency obtained using **Cursor** is seen to be **fL** = 4 kHz, the same as that calculated above.

Figure 11.44 provides the plot of the dB gain versus frequency, showing that over a decade (from about 300 Hz to about 3 Hz), the gain changes by about 40 dB—as expected for a second-order filter.

Program 11.6—Bandpass Active Filter

Figure 11.45 shows a bandpass active filter circuit. Using the values of Example 11.14, we obtain the bandpass frequencies

$$f_{OL} = 1/(2\pi R_1 C_1) = 1/(2\pi \cdot 10\,\text{k}\Omega \cdot 0.1\,\mu\text{F}) = 159\text{ Hz}$$

$$f_{OH} = 1/(2\pi R_2 C_2) = 1/(2\pi \cdot 10\,\text{k}\Omega \cdot 0.002\,\mu\text{F}) = 7.96\text{ kHz}$$

The sweep is set at 10 points per decade from 10 Hz to 1 MHz. The plot of V_o in Fig. 11.46 shows the low-cutoff frequency at about 181.1 Hz. The cutoff frequencies are measured at the voltage 0.707 (7.8423 V) $\cong$ 6 V. The upper cutoff frequency is about 8.2 kHz, using the cursor on the upper 0.707 voltage point. These values match those calculated above quite well.

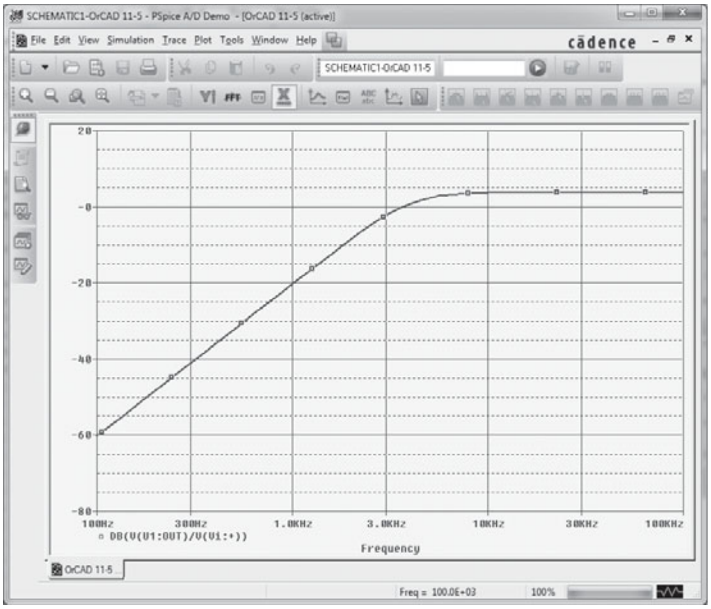

SCHEMATIC1-OrCAD 11-5 - PSpice A/D Demo - [OrCAD 11-5 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 11-5
20
-0
-20
-40
-60
-80
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
DB(V(U1:OUT)/V(Vi:+))
Frequency
OrCAD 11-5
Freq = 100.0E+03
100%

FIG. 11.44

Plot of dB (V_o/V_i) for a second-order high-pass active filter.

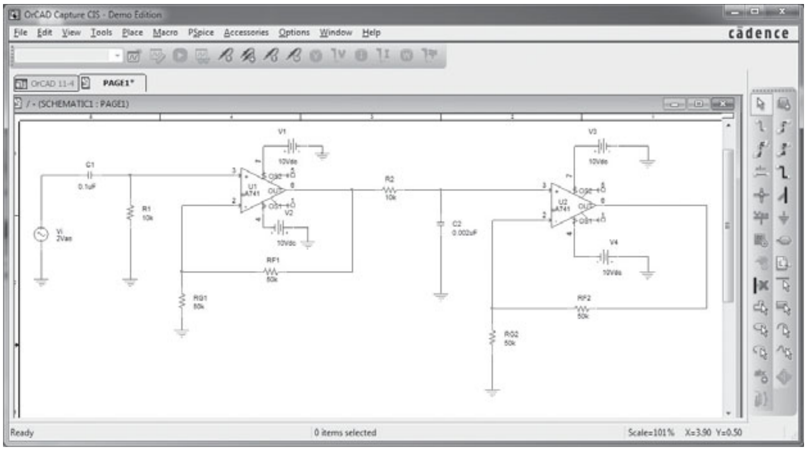
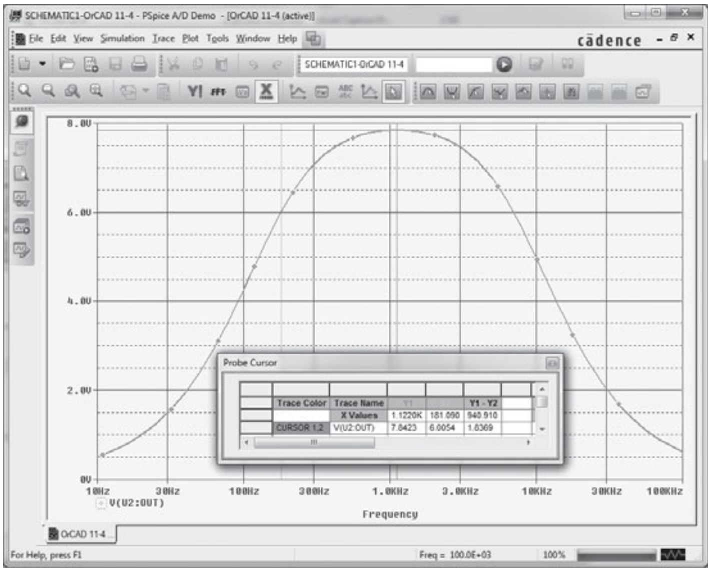

OrCAD Capture CIS - Demo Edition
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
OrCAD 11-4
PAGE1*
/ - (SCHEMATIC1 : PAGE1)
V1
10Vdc
C1
0.1uF
R1
10k
Vi
2Vac
U1
uA741
R2
10k
C2
0.002uF
RF1
50k
RG1
50k
V2
10Vdc
V3
10Vdc
U2
uA741
V4
10Vdc
RF2
50k
RG2
50k
Ready
0 items selected
Scale=101%
X=3.90 Y=0.50

FIG. 11.45

Bandpass active filter.


SCHEMATIC1-OrCAD 11-4 - PSpice A/D Demo - [OrCAD 11-4 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 11-4
8.0V
6.0V
4.0V
2.0V
0V
10Hz
30Hz
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
V(U2:OUT)
Frequency
Probe Cursor
OrCAD 11-4
For Help, press F1
Freq = 100.0E+03
100%

Trace Color	Trace Name	Y1		Y1 - Y2
	X Values	1.1220K	181.090	940.910
CURSOR 1,2	V(U2:OUT)	7.8423	6.0054	1.8369

FIG. 11.46

Probe plot of bandpass active filter.

PROBLEMS

**Note*: Asterisks indicate more difficult problems.

11.1 Constant-Gain Multiplier

1. Calculate the output voltage for the circuit of Fig. 11.47 for an input of $V_i = 3.5$ mV rms.
2. Calculate the output voltage of the circuit of Fig. 11.48 for an input of 150 mV rms.

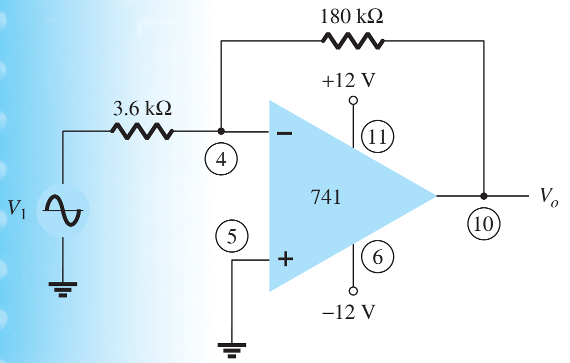

180 kΩ
3.6 kΩ
+12 V
11
4
5
741
10
6
−12 V
V_1
V_o
−
+

FIG. 11.47
Problem 1.

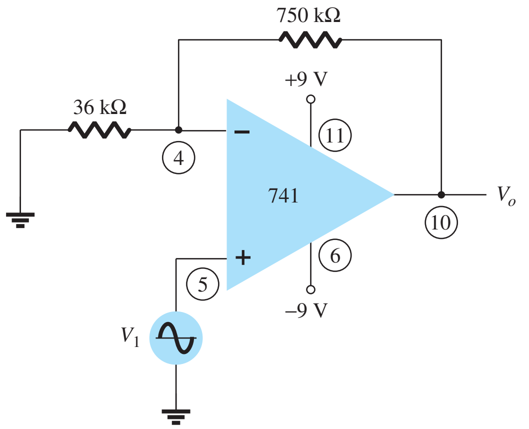

750 kΩ
+9 V
36 kΩ
11
4
741
10
V_o
6
5
−9 V
V_1
−
+

FIG. 11.48
Problem 2.

*3. Calculate the output voltage in the circuit of Fig. 11.49.

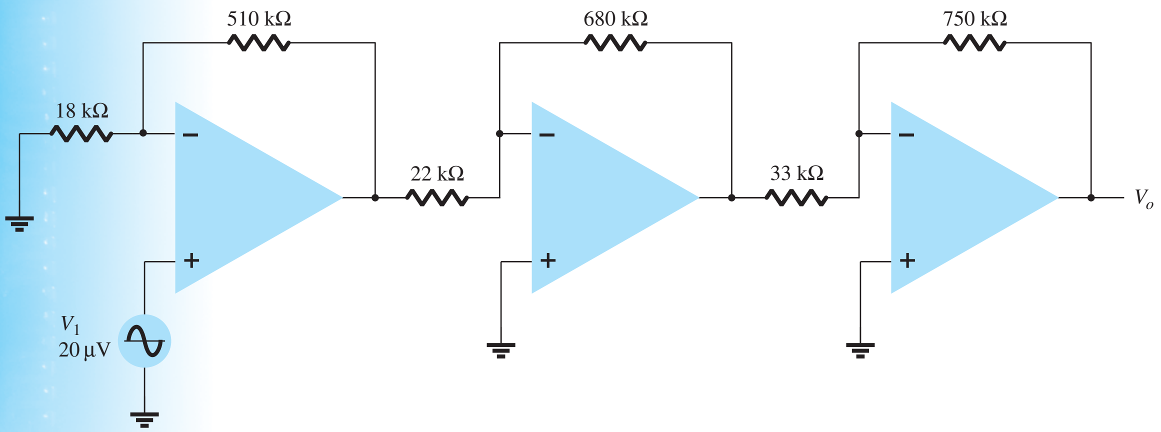

510 kΩ
680 kΩ
750 kΩ
18 kΩ
22 kΩ
33 kΩ
V_o
V_1
20 μV
−
+
−
+
−
+

FIG. 11.49
Problem 3.

*4. Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +15, −22, and −30. Use a 420-kΩ feedback resistor for all stages. What output voltage results for an input of $V_1 = 80\ \mu$V?

5. Show the connection of two op-amp stages using an LM358 IC to provide outputs that are 15 and −30 times larger than the input. Use a feedback resistor, $R_F = 150$ kΩ, in all stages.

11.2 Voltage Summing

6. Calculate the output voltage for the circuit of Fig. 11.50 with inputs of $V_1 = 40$ mV rms and $V_2 = 20$ mV rms.
7. Determine the output voltage for the circuit of Fig. 11.51.
8. Determine the output voltage for the circuit of Fig. 11.52.

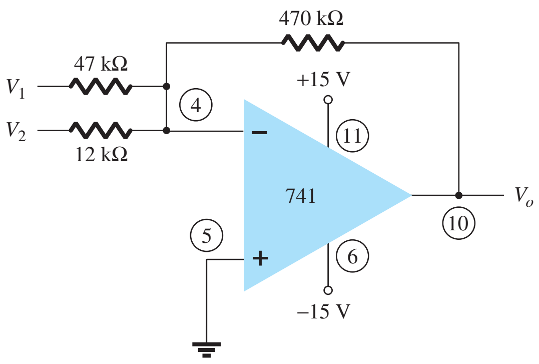

470 kΩ
47 kΩ
V_1
V_2
12 kΩ
+15 V
4
11
741
V_o
10
5
6
−15 V

FIG. 11.50
Problem 6.

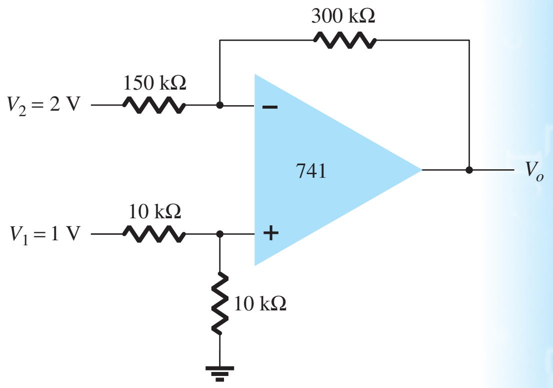

300 kΩ
150 kΩ
$V_2 = 2$ V
741
V_o
10 kΩ
$V_1 = 1$ V
10 kΩ

FIG. 11.51
Problem 7.

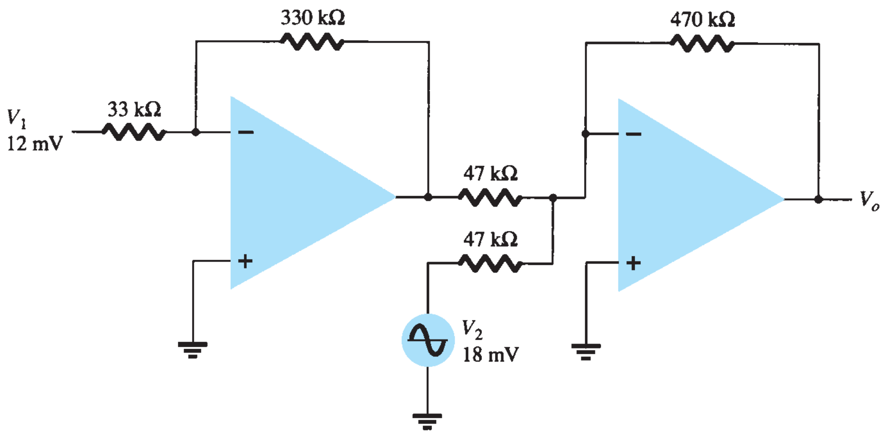

330 kΩ
470 kΩ
V_1
12 mV
33 kΩ
47 kΩ
47 kΩ
V_o
V_2
18 mV

FIG. 11.52
Problem 8.

11.3 Voltage Buffer

9. Show the connection (including pin information) of an LM124 IC stage connected as a unity-gain amplifier.

10. Show the connection (including pin information) of two LM358 stages connected as unity-gain amplifiers to provide the same output.

11.4 Controlled Sources

11. For the circuit of Fig. 11.53, calculate I_L.

12. Calculate V_o for the circuit of Fig. 11.54.

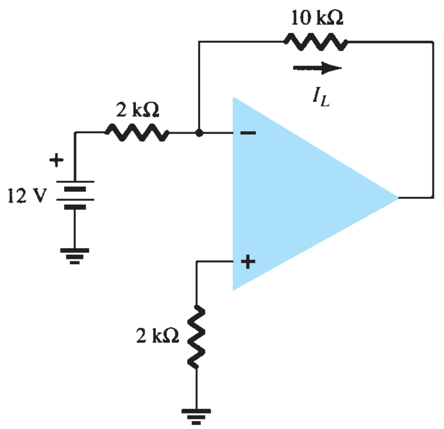

10 kΩ
I_L
2 kΩ
12 V
2 kΩ

FIG. 11.53
Problem 11.

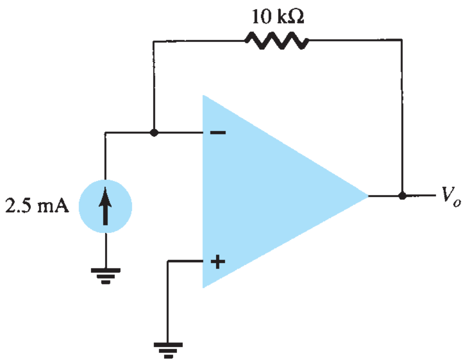
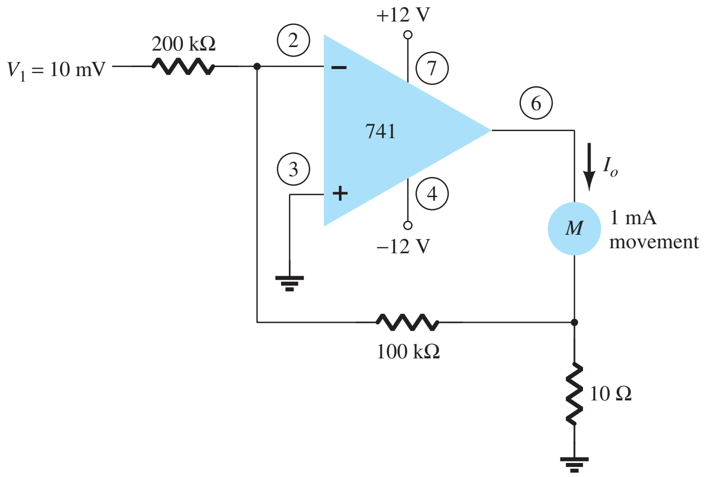

10 kΩ
2.5 mA
V_o

FIG. 11.54
Problem 12.

11.5 Instrumentation Circuits

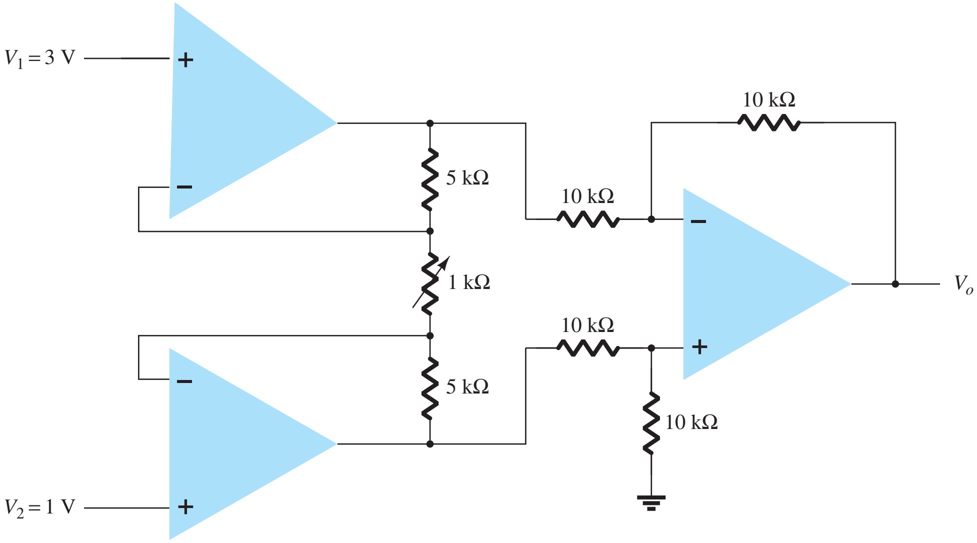
13. Calculate the output current I_o in the circuit of Fig. 11.55.



$V_1 = 10$ mV
200 kΩ
2
3
741
+12 V
7
4
−12 V
6
I_o
M
1 mA movement
100 kΩ
10 Ω

FIG. 11.55
Problem 13.

***14.** Calculate V_o in the circuit of Fig. 11.56.



$V_1 = 3$ V
$V_2 = 1$ V
5 kΩ
1 kΩ
5 kΩ
10 kΩ
10 kΩ
10 kΩ
10 kΩ
V_o

FIG. 11.56
Problem 14.

11.6 Active Filters

15. Calculate the cutoff frequency of a first-order low-pass filter in the circuit of Fig. 11.57.

16. Calculate the cutoff frequency of the high-pass filter circuit in Fig. 11.58.

17. Calculate the lower and upper cutoff frequencies of the bandpass filter circuit in Fig. 11.59.

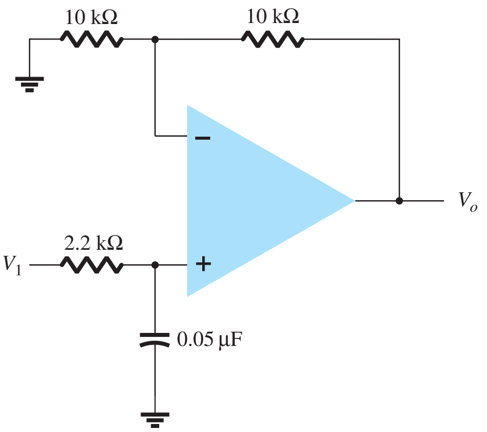

10 kΩ
10 kΩ
V_o
2.2 kΩ
V_1
0.05 μF

FIG. 11.57
Problem 15.

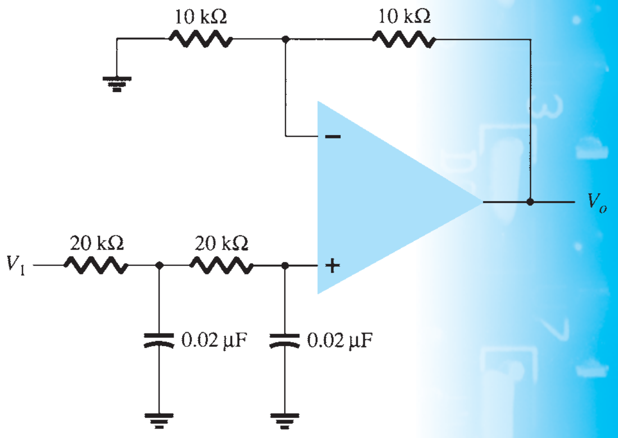

10 kΩ
10 kΩ
V_o
20 kΩ
20 kΩ
V_1
0.02 μF
0.02 μF

FIG. 11.58
Problem 16.

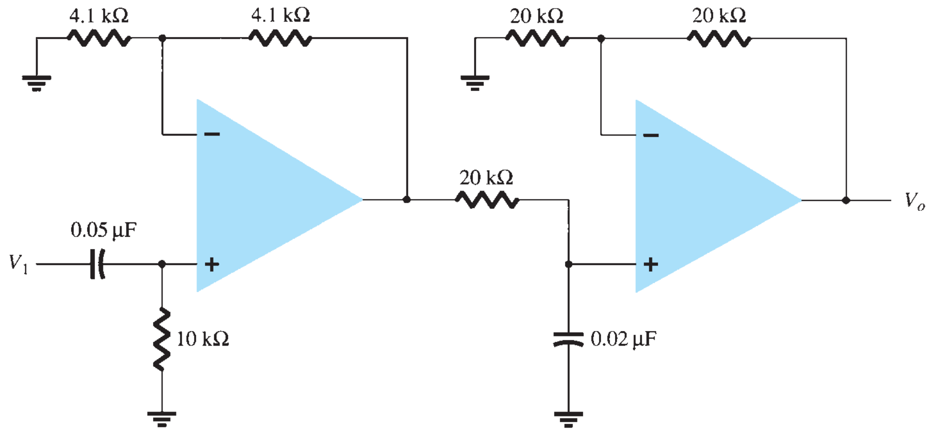

4.1 kΩ
4.1 kΩ
20 kΩ
20 kΩ
20 kΩ
V_o
0.05 μF
V_1
10 kΩ
0.02 μF

FIG. 11.59
Problem 17.

11.8 Computer Analysis

***18.** Use Design Center to draw the schematic of Fig. 11.60 and determine V_o.

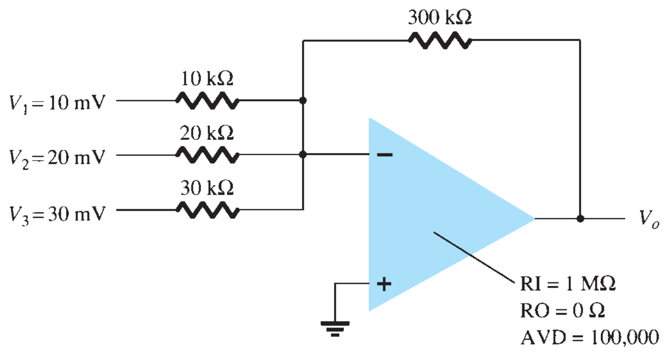
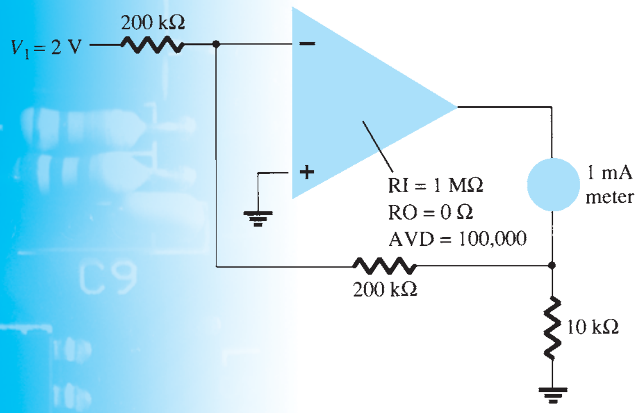

300 kΩ
10 kΩ
$V_1 = 10$ mV
20 kΩ
$V_2 = 20$ mV
30 kΩ
$V_3 = 30$ mV
V_o
RI = 1 MΩ
RO = 0 Ω
AVD = 100,000

FIG. 11.60
Problem 18.

***19.** Use Design Center to calculate I(VSENSE) in the circuit of Fig. 11.61.

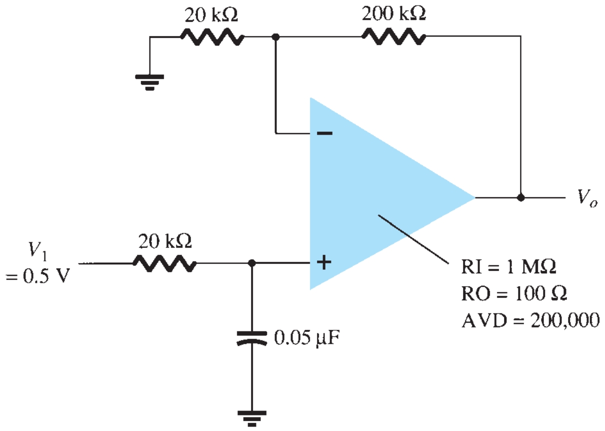
***20.** Use Multisim to plot the response of the low-pass filter circuit in Fig. 11.62.

***21.** Use Multisim to plot the response of the high-pass filter circuit in Fig. 11.63.



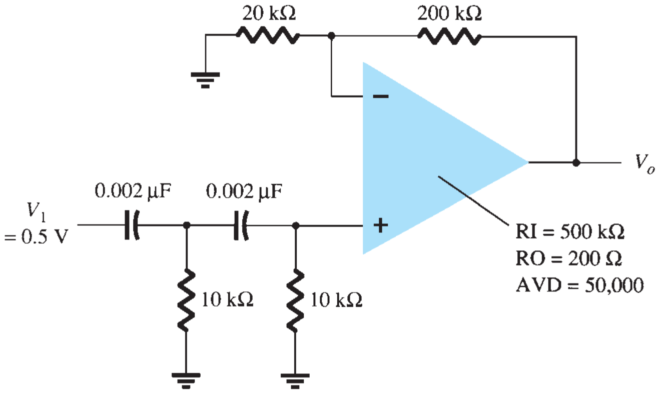
$V_1 = 2$ V
200 kΩ
−
+
RI = 1 MΩ
RO = 0 Ω
AVD = 100,000
1 mA
meter
200 kΩ
10 kΩ

FIG. 11.61
Problem 19.



20 kΩ
200 kΩ
−
V_o
V_1
= 0.5 V
20 kΩ
+
RI = 1 MΩ
RO = 100 Ω
AVD = 200,000
0.05 μF

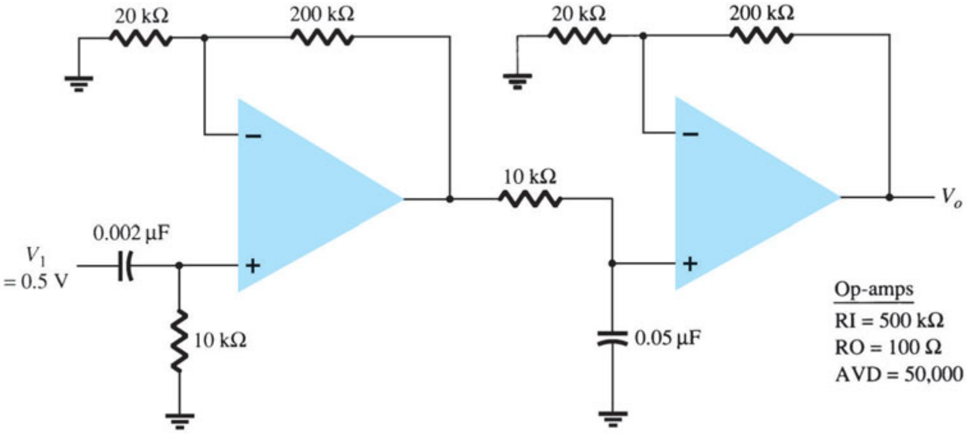
FIG. 11.62
Problem 20.



20 kΩ
200 kΩ
−
V_o
0.002 μF
0.002 μF
V_1
= 0.5 V
+
RI = 500 kΩ
RO = 200 Ω
AVD = 50,000
10 kΩ
10 kΩ

FIG. 11.63
Problem 21.

***22.** Use Design Center to plot the response of the bandpass filter circuit in Fig. 11.64.



20 kΩ
200 kΩ
20 kΩ
200 kΩ
−
−
10 kΩ
V_o
0.002 μF
V_1
= 0.5 V
+
+
10 kΩ
0.05 μF
Op-amps
RI = 500 kΩ
RO = 100 Ω
AVD = 50,000

FIG. 11.64
Problem 22.

12

Power Amplifiers

CHAPTER OBJECTIVES

- The differences between classes A, AB, and C amplifiers
- What causes amplifier distortion
- Efficiency of various classes of amplifiers
- Power calculations for various class amplifiers

12.1 INTRODUCTION—DEFINITIONS AND AMPLIFIER TYPES

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device). In small-signal amplifiers, the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. In Chapter 12, we concentrate on amplifier circuits used to handle large-voltage signals at moderate to high current levels. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal. A brief description of amplifier classes is provided next.

Class A: The output signal varies for a full 360° of the input signal. Figure12.1a shows that this requires the *Q*-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

Class B: A class B circuit provides an output signal varying over one-half the input signal cycle, or for 180° of signal, as shown in Fig. 12.1b. The dc bias point for class B is at 0 V, with the output then varying from this bias point for a half-cycle. Obviously, the

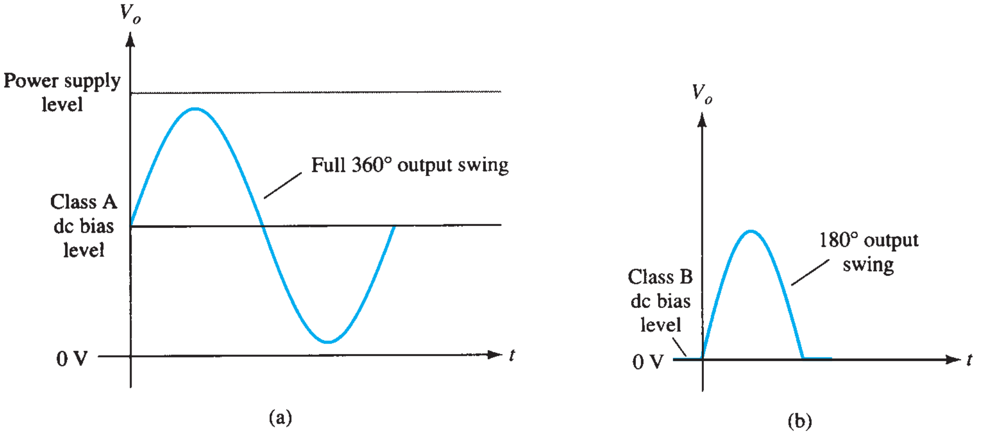


FIG. 12.1
Amplifier operating classes.

output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half-cycle and another to provide operation on the negative-output half-cycle—are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as *push–pull operation*, which is discussed later in this chapter. Note that class B operation by itself creates a very distorted output signal since reproduction of the input takes place for only 180° of the output signal swing.

Class AB: An amplifier may be biased at a dc level above the zero-base-current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push–pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero-base-current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

Class C: The output of a class C amplifier is biased for operation at less than 180° of the cycle and will operate only with a tuned (resonant) circuit, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

Class D: This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample-and-hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is "on" (using power) only for short intervals and the overall efficiency can practically be very high, as described next.

Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%. Table 12.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In class B operation, a push–pull connection is obtained using either a transformer coupling

TABLE 12.1

Comparison of Amplifier Classes

	Class A	 AB	 B	 C[a]	 D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

[a] *Class C is usually not used for delivering large amounts of power, and thus the efficiency is not given here.*

or by using complementary (or quasi-complementary) operation with *npn* and *pnp* transistors to provide operation on opposite-polarity cycles. Although transformer operation can provide opposite-cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package. Circuits and examples are provided later in this chapter.

12.2 SERIES-FED CLASS A AMPLIFIER

The simple fixed-bias circuit connection shown in Fig. 12.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

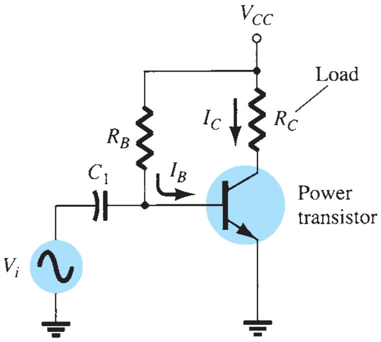


FIG. 12.2

Series-fed class A large-signal amplifier.

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\text{ V}}{R_B} \qquad \textbf{(12.1)}$$

with the collector current then being

$$I_C = \beta I_B \qquad \textbf{(12.2)}$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C \qquad \textbf{(12.3)}$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 12.3. A dc load line is drawn using the

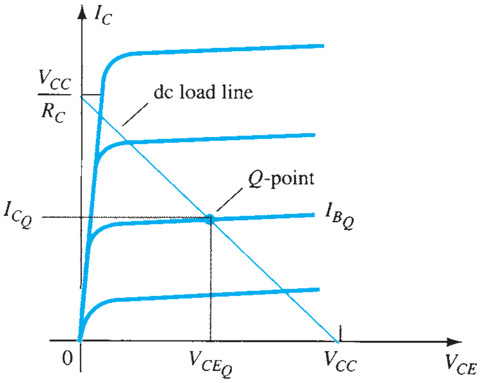


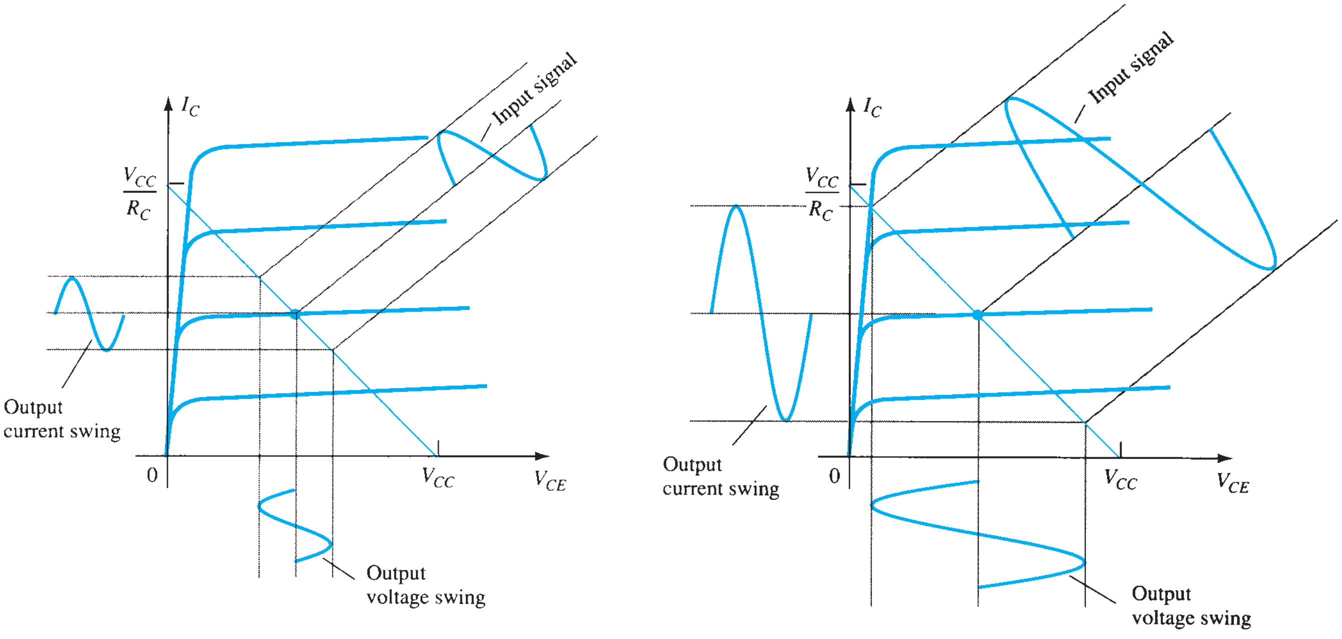
FIG. 12.3

Transistor characteristic showing load line and Q-point.

values of V_{CC} and R_C. The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q-point) for the circuit. The quiescent-point values are those calculated using Eqs. (12.1) through (12.3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and V_{CC}/R_C), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the Q-point set at this optimum bias point, the power considerations for the circuit of Fig. 12.2 are determined as described next.

AC Operation

When an input ac signal is applied to the amplifier of Fig. 12.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 12.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC}/R_C at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC}.



(a)

(b)

FIG. 12.4

Amplifier input and output signal variation.

Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current I_{C_Q}. The power then drawn from the supply is

$$\boxed{P_i(\text{dc}) = V_{CC}I_{C_Q}} \qquad \textbf{(12.4)}$$

Even with an ac signal applied, the average current drawn from the supply remains equal to the quiescent current I_{C_Q}, so that Eq. (12.4) represents the input power supplied to the class A series-fed amplifier.

Output Power The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load R_C in the circuit of Fig. 12.2. The ac signal V_i causes the base current to vary around the dc bias current and the collector current around its quiescent level I_{C_Q}. As shown in Fig. 12.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using RMS signals. The ac power delivered to the load (R_C) may be expressed using

$$\boxed{P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms})} \tag{12.5}$$

$$\boxed{P_o(\text{ac}) = I_C^2(\text{rms})R_C} \tag{12.6}$$

$$\boxed{P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C}} \tag{12.7}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\boxed{\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%} \tag{12.8}$$

Maximum Efficiency For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (12.7) yields

$$\begin{aligned}\text{maximum } P_o(\text{ac}) &= \frac{V_{CC}(V_{CC}/R_C)}{8}\\ &= \frac{V_{CC}^2}{8R_C}\end{aligned}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

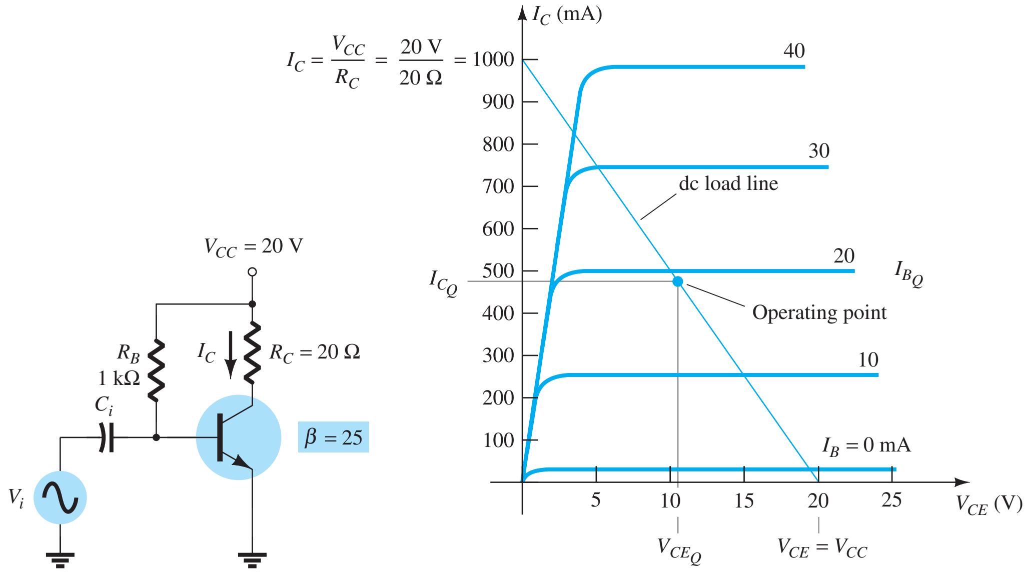
$$\begin{aligned}\text{maximum } P_i(\text{dc}) &= V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2}\\ &= \frac{V_{CC}^2}{2R_C}\end{aligned}$$

We can then use Eq. (12.8) to calculate the maximum efficiency:

$$\begin{aligned}\text{maximum }\%\ \eta &= \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\%\\ &= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\%\\ &= 25\%\end{aligned}$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

EXAMPLE 12.1 Calculate the input power, output power, and efficiency of the amplifier circuit in Fig. 12.5 for an input voltage that results in a base current of 10 mA peak.


$V_{CC} = 20$ V
R_B
1 kΩ
C_i
I_C
$R_C = 20\ \Omega$
$\beta = 25$
V_i
I_C (mA)
$I_C = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{20\ \Omega} = 1000$
900
800
700
600
500
400
300
200
100
40
30
dc load line
20
I_{B_Q}
I_{C_Q}
Operating point
10
$I_B = 0$ mA
5
10
15
20
25
V_{CE} (V)
V_{CE_Q}
$V_{CE} = V_{CC}$

(a) (b)

FIG. 12.5

Operation of a series-fed circuit for Example 12.1.

Solution: Using Eqs. (12.1) through (12.3), we can determine the Q-point to be

$$I_{B_Q} = \frac{V_{CC} - 0.7\text{ V}}{R_B} = \frac{20\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 19.3\text{ mA}$$

$$I_{C_Q} = \beta I_B = 25(19.3\text{ mA}) = 482.5\text{ mA} \cong 0.48\text{ A}$$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20\text{ V} - (0.48\ \Omega)(20\ \Omega) = 10.4\text{ V}$$

This bias point is marked on the transistor collector characteristic of Fig. 12.5b. The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 12.5b by connecting $V_{CE} = V_{CC} = 20$ V with $I_C = V_{CC}/R_C = 1000$ mA $= 1$ A, as shown. When the input ac base current increases from its dc bias level, the collector current rises by

$$I_C(\text{p}) = \beta I_B(\text{p}) = 25(10\text{ mA peak}) = 250\text{ mA peak}$$

Using Eq. (12.6) yields

$$P_o(\text{ac}) = I^2_C(rms)R_C = \frac{I^2_C(\text{p})}{2}R_C = \frac{(250 \times 10^{-3}\text{ A})^2}{2}(20\ \Omega) = \mathbf{0.625\ W}$$

Using Eq. (12.4) results in

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (20\text{ V})(0.48\text{ A}) = \mathbf{9.6\ W}$$

The amplifier's power efficiency can then be calculated using Eq. (12.8):

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.625\text{ W}}{9.6\text{ W}} \times 100\% = \mathbf{6.5\%}$$

12.3 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 12.6. This is a simple circuit form to use in presenting a few basic concepts. More practical circuit versions are covered later.

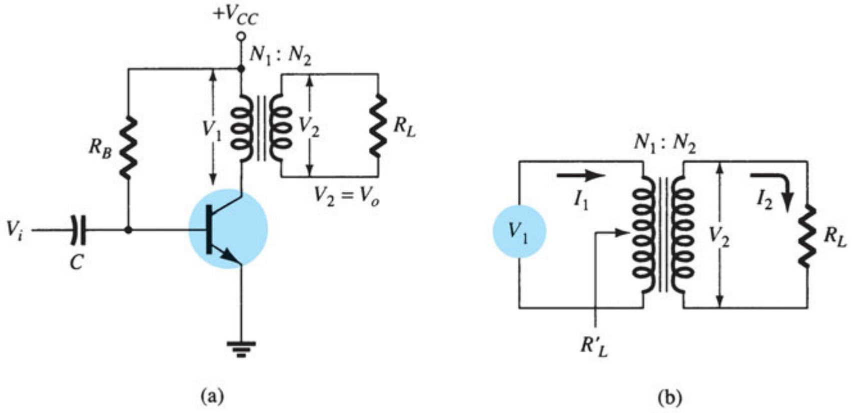


FIG. 12.6

Transformer-coupled audio power amplifier.

Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented next.

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

Voltage Transformation As shown in Fig. 12.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by

$$\boxed{\frac{V_2}{V_1} = \frac{N_2}{N_1}} \tag{12.9}$$

Equation (12.9) shows that if the number of turns of wire on the secondary side is larger than the number on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

Current Transformation The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by

$$\boxed{\frac{I_2}{I_1} = \frac{N_1}{N_2}} \tag{12.10}$$

This relationship is shown in Fig. 12.7b. If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

Impedance Transformation Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed. As shown in Fig. 12.7c, an impedance R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R'_L). This can be shown as follows:

$$\frac{R_L}{R'_L} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2}{I_2}\frac{I_1}{V_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{N_2 N_2}{N_1 N_1} = \left(\frac{N_2}{N_1}\right)^2$$

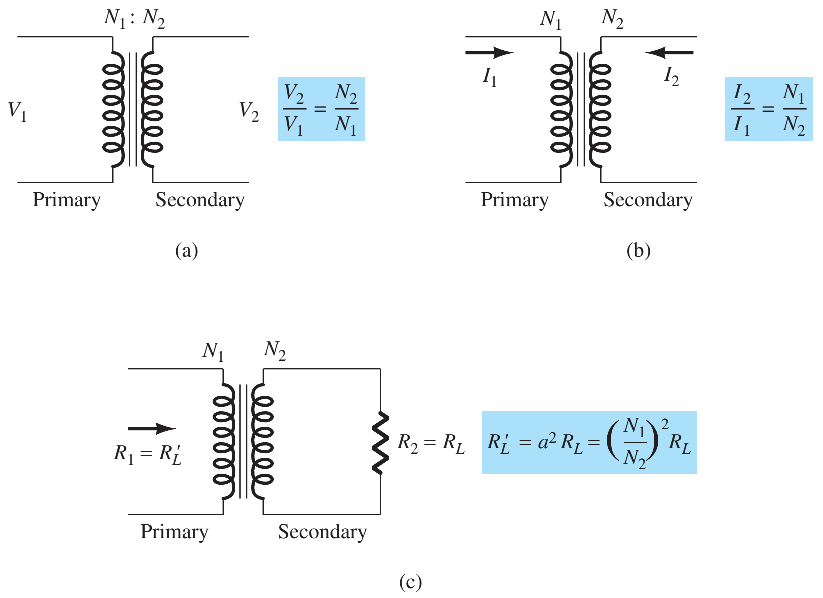

$N_1 : N_2$
V_1
V_2
$\frac{V_2}{V_1} = \frac{N_2}{N_1}$
Primary
Secondary
(a)
N_1
N_2
I_1
I_2
$\frac{I_2}{I_1} = \frac{N_1}{N_2}$
Primary
Secondary
(b)
N_1
N_2
$R_1 = R_L'$
$R_2 = R_L$
$R_L' = a^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$
Primary
Secondary
(c)

FIG. 12.7

Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

If we define $a = N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes

$$\boxed{\frac{R_L'}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2} \qquad \textbf{(12.11)}$$

We can express the load resistance reflected to the primary side as

$$\boxed{R_1 = a^2 R_2} \quad \text{or} \quad \boxed{R_L' = a^2 R_L} \qquad \textbf{(12.12)}$$

where R_L' is the reflected impedance. As shown in Eq. (12.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

EXAMPLE 12.2 Calculate the effective resistance seen looking into the primary of a 15:1 transformer connected to an 8-Ω load.

Solution: Eq. (12.22):

$$R_L' = a^2 R_L = (15)^2(8\ \Omega) = 1800\ \Omega = \mathbf{1.8\ k\Omega}$$

EXAMPLE 12.3 What transformer turns ratio is required to match a 16-Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ?

Solution: Eq. (12.11):

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{R_L'}{R_L} = \frac{10\ \text{k}\Omega}{16\ \Omega} = 625$$

$$\frac{N_1}{N_2} = \sqrt{625} = \mathbf{25:1}$$

Operation of Amplifier Stage

DC Load Line The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 12.6. Typically, this dc resistance is small (ideally 0 Ω) and, as shown in Fig. 12.8, a 0-Ω dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the 0-Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CE_Q} = V_{CC}$.

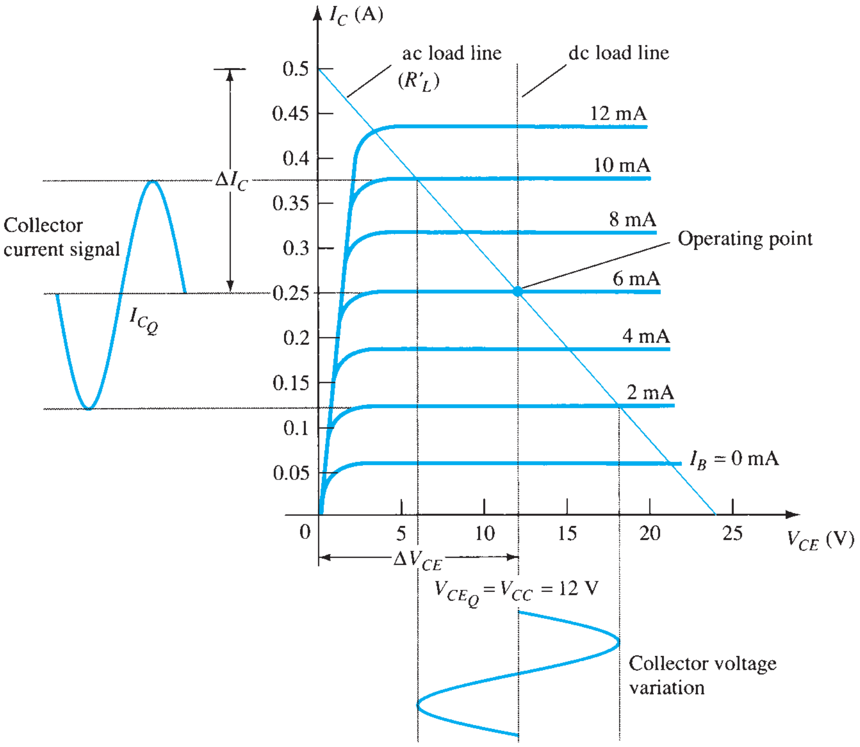


FIG. 12.8

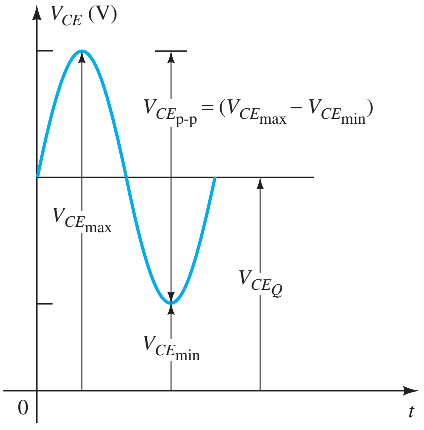
Load lines for class A transformer-coupled amplifier.

Quiescent Operating Point The operating point in the characteristic curve of Fig.12.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than the maximum of 50%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

AC Load Line To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance (R'_L) is calculated using Eq. (12.12) using the value of the load connected across the secondary (R_L) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to $-1/R'_L$ (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of V_{CC}. In fact, the voltage developed across the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

Signal Swing and Output AC Power Figure 12.9 shows the voltage and current signal swings from the circuit of Fig. 12.6. From the signal variations shown in Fig. 12.9, the values of the peak-to-peak signal swings are

$$V_{CE}(\text{p-p}) = V_{CE_{\max}} - V_{CE_{\min}}$$
$$I_C(\text{p-p}) = I_{C_{\max}} - I_{C_{\min}}$$



(a) (b)

FIG. 12.9
Graphical operation of transformer-coupled class A amplifier.

The ac power developed across the transformer primary can then be calculated using

$$\boxed{P_o(\text{ac}) = \frac{(V_{CE_{\max}} - V_{CE_{\min}})(I_{C_{\max}} - I_{C_{\min}})}{8}} \qquad \textbf{(12.13)}$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), we find that the power delivered by the secondary to the load is approximately that calculated using Eq. (12.13). The output ac power can also be determined using the voltage delivered to the load.

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (12.9):

$$V_L = V_2 = \frac{N_2}{N_1}V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

and equals the power calculated using Eq. (12.5c).

Using Eq. (12.10) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2}I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms})R_L$$

EXAMPLE 12.4 Calculate the ac power delivered to the 8-Ω speaker for the circuit of Fig. 12.10. The circuit component values result in a dc base current of 6 mA, and the input signal (V_i) results in a peak base current swing of 4 mA.

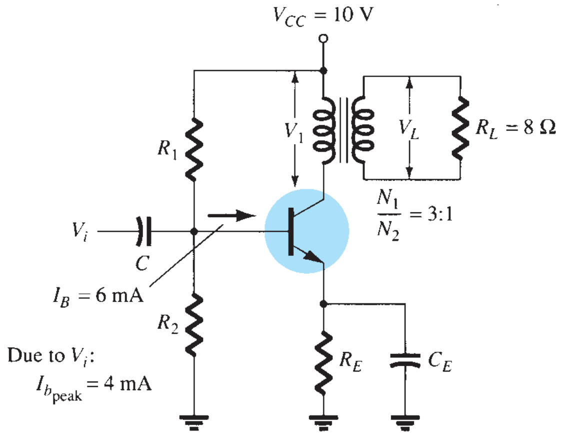


FIG. 12.10

Transformer-coupled class A amplifier for Example 12.4.

Solution: The dc load line is drawn vertically (see Fig. 12.11) from the voltage point:

$$V_{CE_Q} = V_{CC} = 10\ \text{V}$$

For $I_B = 6$ mA, the operating point on Fig. 12.11 is

$$V_{CE_Q} = 10\ \text{V} \quad \text{and} \quad I_{C_Q} = 140\ \text{mA}$$

The effective ac resistance seen at the primary is

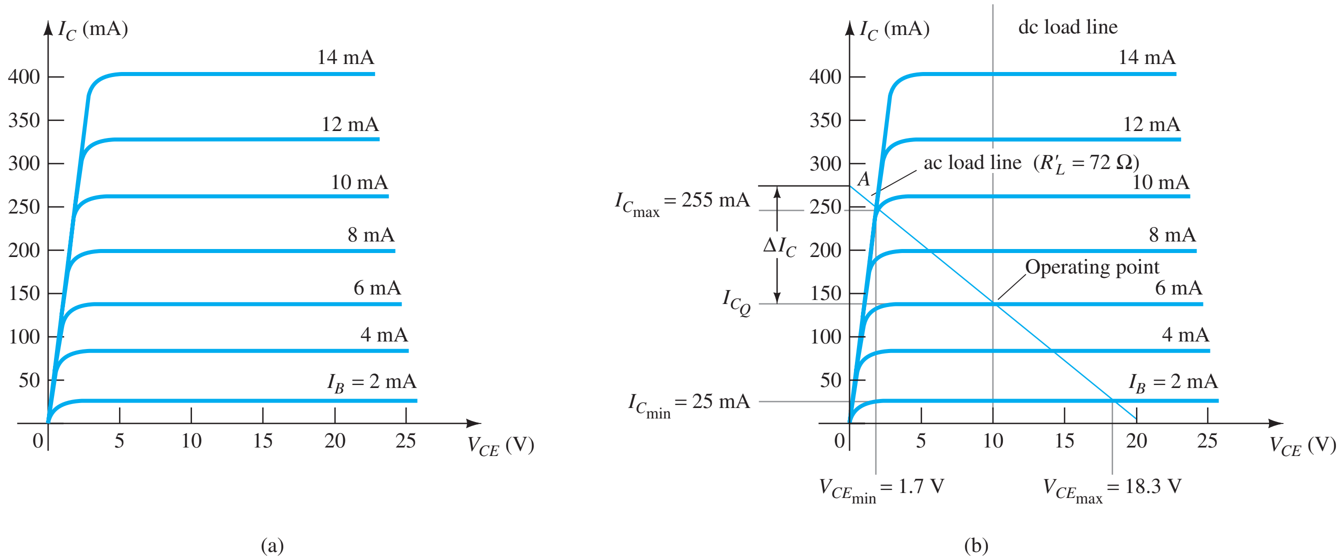
$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = (3)^2(8) = 72\ \Omega$$

The ac load line can then be drawn of slope $-1/72$ going through the indicated operating point. To help draw the load line, consider the following procedure. For a current swing of

$$I_C = \frac{V_{CE}}{R'_L} = \frac{10\ \text{V}}{72\ \Omega} = 139\ \text{mA}$$

mark a point A:

$$I_{CE_Q} + I_C = 140\ \text{mA} + 139\ \text{mA} = 279\ \text{mA along the } y\text{-axis}$$



(a)

(b)

FIG. 12.11

Transformer-coupled class A transistor characteristic for Examples 12.4 and 12.5: (a) device characteristic; (b) dc and ac load lines.

Connect point A through the Q-point to obtain the ac load line. For the given base current swing of 4 mA peak, the maximum and minimum collector current and collector–emitter voltage obtained from Fig. 12.11 are, respectively,

$$V_{CE_{\min}} = 1.7\text{ V} \qquad I_{C_{\min}} = 25\text{ mA}$$
$$V_{CE_{\max}} = 18.3\text{ V} \qquad I_{C_{\max}} = 255\text{ mA}$$

The ac power delivered to the load can then be calculated using Eq. (12.13):

$$P_o(\text{ac}) = \frac{(V_{CE_{\max}} - V_{CE_{\min}})(I_{C_{\max}} - I_{C_{\min}})}{8}$$
$$= \frac{(18.3\text{ V} - 1.7\text{ V})(255\text{ mA} - 25\text{ mA})}{8} = \mathbf{0.477\ W}$$

Efficiency

So far we have considered calculating the ac power delivered to the load. We next consider the input power from the battery, power losses in the amplifier, and the overall power efficiency of the transformer-coupled class A amplifier.

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$\boxed{P_i(\text{dc}) = V_{CC}I_{C_Q}} \tag{12.14}$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$\boxed{P_Q = P_i(\text{dc}) - P_o(\text{ac})} \tag{12.15}$$

where P_Q is the power dissipated as heat. Although the equation is simple, it is nevertheless significant when operating a class A amplifier. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates the least power when the load is drawing maximum power from the circuit.

EXAMPLE 12.5 For the circuit of Fig. 12.10 and results of Example 12.4, calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 12.4.

Solution: Eq. (12.14):

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (10\text{ V})(140\text{ mA}) = \mathbf{1.4\ W}$$

Eq. (12.15):

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4\text{ W} - 0.477\text{ W} = \mathbf{0.92\ W}$$

The efficiency of the amplifier is then

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477\text{ W}}{1.4\text{ W}} \times 100\% = \mathbf{34.1\%}$$

Maximum Theoretical Efficiency For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\boxed{\% \eta = 50\left(\frac{V_{CE_{\max}} - V_{CE_{\min}}}{V_{CE_{\max}} + V_{CE_{\min}}}\right)^2 \%} \qquad \textbf{(12.16)}$$

The larger the value of $V_{CE_{\max}}$ and the smaller the value of $V_{CE_{\min}}$, the closer the efficiency approaches the theoretical limit of 50%.

EXAMPLE 12.6 Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

a. $V(\text{p}) = 12\text{ V}$.
b. $V(\text{p}) = 6\text{ V}$.
c. $V(\text{p}) = 2\text{ V}$.

Solution:

a. Since $V_{CE_Q} = V_{CC} = 12\text{ V}$, the maximum and minimum of the voltage swing are, respectively,

$$V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 12\text{ V} = 24\text{ V}$$
$$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 12\text{ V} = 0\text{ V}$$

resulting in

$$\% \eta = 50\left(\frac{24\text{ V} - 0\text{ V}}{24\text{ V} + 0\text{ V}}\right)^2 \% = \mathbf{50\%}$$

b.

$$V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 6\text{ V} = 18\text{ V}$$
$$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 6\text{ V} = 6\text{ V}$$

resulting in

$$\% \eta = 50\left(\frac{18\text{ V} - 6\text{ V}}{18\text{ V} + 6\text{ V}}\right)^2 \% = \mathbf{12.5\%}$$

c.

$$V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 2\text{ V} = 14\text{ V}$$
$$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 2\text{ V} = 10\text{ V}$$

resulting in

$$\% \eta = 50\left(\frac{14\text{ V} - 10\text{ V}}{14\text{ V} + 10\text{ V}}\right)^2 \% = \mathbf{1.39\%}$$

Notice how dramatically the amplifier efficiency drops from a maximum of 50% for $V(\text{p}) = V_{CC}$ to slightly over 1% for $V(\text{p}) = 2\text{ V}$.

12.4 CLASS B AMPLIFIER OPERATION

Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. This is essentially no bias, and the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push–pull circuit*. Figure 12.12 shows a diagram for push–pull operation. An ac input signal is applied to the push–pull circuit, with each half operating on alternate half-cycles, the load then

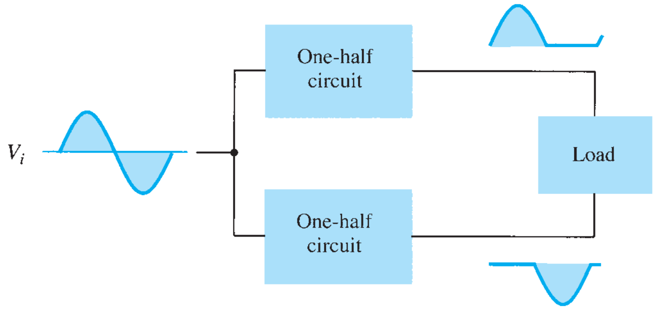

V_i
One-half circuit
One-half circuit
Load

FIG. 12.12

Block representation of push–pull operation.

receiving a signal for the full ac cycle. The power transistors used in the push–pull circuit are capable of delivering the desired power to the load, and the class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; see Fig. 12.13) that provides the input or dc power. The amount of this input power can be calculated using

$$\boxed{P_i(\text{dc}) = V_{CC}I_{\text{dc}}} \tag{12.17}$$

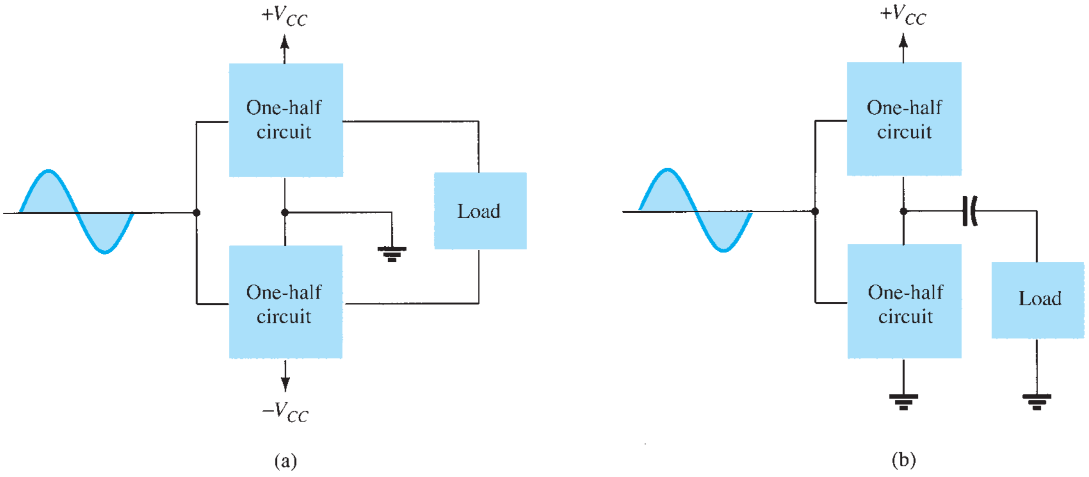

$+V_{CC}$
One-half circuit
One-half circuit
Load
$-V_{CC}$
(a)
$+V_{CC}$
One-half circuit
One-half circuit
Load
(b)

FIG. 12.13

Connection of push–pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.

where I_{dc} is the average or dc current drawn from the power supplies. In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, whereas that drawn from two power supplies has the form of a half-wave rectified signal from each supply. In either case, the value of the average current drawn can be expressed as

$$\boxed{I_{\text{dc}} = \frac{2}{\pi}I(\text{p})} \tag{12.18}$$

where $I(\text{p})$ is the peak value of the output current waveform. Using Eq. (12.18) in the power input equation (12.17) results in

$$\boxed{P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi}I(\text{p})\right)} \tag{12.19}$$

Output (AC) Power

The power delivered to the load (usually referred to as a resistance R_L) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$\boxed{P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L}} \tag{12.20}$$

If one is using an oscilloscope, the measured peak or peak-to-peak output voltage can be used:

$$\boxed{P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L}} \tag{12.21}$$

The larger the rms or peak output voltage, the larger is the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Using Eqs. (12.19) and (12.21) in the efficiency equation above results in

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4}\frac{V_L(\text{p})}{V_{CC}} \times 100\% \tag{12.22}$$

[using $I(\text{p}) = V_L(\text{p})/R_L$]. Equation (12.22) shows that the larger the peak voltage, the higher is the circuit efficiency, up to a maximum value when $V_L(\text{p}) = V_{CC}$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power Dissipated by Output Transistors The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

$$P_{2Q} = P_i(\text{dc}) - P_o(\text{ac}) \tag{12.23}$$

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \tag{12.24}$$

EXAMPLE 12.7 For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of $V_{CC} = 30$ V, determine the input power, output power, and circuit efficiency.

Solution: A 20-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(\mathrm{p}) = \frac{V_L(\mathrm{p})}{R_L} = \frac{20\ \mathrm{V}}{16\ \Omega} = 1.25\ \mathrm{A}$$

The dc value of the current drawn from the power supply is then

$$I_{\mathrm{dc}} = \frac{2}{\pi} I_L(\mathrm{p}) = \frac{2}{\pi}(1.25\ \mathrm{A}) = 0.796\ \mathrm{A}$$

and the input power delivered by the supply voltage is

$$P_i(\mathrm{dc}) = V_{CC} I_{\mathrm{dc}} = (30\ \mathrm{V})(0.796\ \mathrm{A}) = \mathbf{23.9\ W}$$

The output power delivered to the load is

$$P_o(\mathrm{ac}) = \frac{V_L^2(\mathrm{p})}{2R_L} = \frac{(20\ \mathrm{V})^2}{2(16\ \Omega)} = \mathbf{12.5\ W}$$

for a resulting efficiency of

$$\%\ \eta = \frac{P_o(\mathrm{ac})}{P_i(\mathrm{dc})} \times 100\% = \frac{12.5\ \mathrm{W}}{23.9\ \mathrm{W}} \times 100\% = \mathbf{52.3\%}$$

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when $V_L(\mathrm{p}) = V_{CC}$:

$$\boxed{\text{maximum } P_o(\mathrm{ac}) = \frac{V_{CC}^2}{2R_L}} \qquad \mathbf{(12.25)}$$

The corresponding peak ac current $I(\mathrm{p})$ is then

$$I(\mathrm{p}) = \frac{V_{CC}}{R_L}$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{\mathrm{dc}} = \frac{2}{\pi} I(\mathrm{p}) = \frac{2V_{CC}}{\pi R_L}$$

Using this current to calculate the maximum value of input power results in

$$\boxed{\text{maximum } P_i(\mathrm{dc}) = V_{CC}\,(\text{maximum } I_{\mathrm{dc}}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}} \qquad \mathbf{(12.26)}$$

The maximum circuit efficiency for class B operation is then

$$\text{maximum } \%\ \eta = \frac{P_o(\mathrm{ac})}{P_i(\mathrm{dc})} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\%$$

$$= \frac{\pi}{4} \times 100\% = \mathbf{78.54\%} \qquad \mathbf{(12.27)}$$

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(\mathrm{p}) = 0.636 V_{CC} \qquad \left(= \frac{2}{\pi} V_{CC}\right)$$

for a maximum transistor power dissipation of

$$\boxed{\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}} \qquad \mathbf{(12.28)}$$

EXAMPLE 12.8 For a class B amplifier using a supply of $V_{CC} = 30$ V and driving a load of 16 Ω, determine the maximum input power, output power, and transistor dissipation.

Solution: The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{2(16\ \Omega)} = \mathbf{28.125\ W}$$

The maximum input power drawn from the voltage supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30\text{ V})^2}{\pi(16\ \Omega)} = \mathbf{35.81\ W}$$

The circuit efficiency is then

$$\text{maximum } \%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125\text{ W}}{35.81\text{ W}} \times 100\% = 78.54\%$$

as expected. The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30\text{ V})^2}{\pi^2 16\ \Omega}\right] = \mathbf{5.7\ W}$$

Under maximum conditions a pair of transistors each handling 5.7 W at most can deliver 28.125 W to a 16-Ω load while drawing 35.81 W from the supply.

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L}$$

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = V_{CC}\left[\frac{2V_L(\text{p})}{\pi R_L}\right]$$

so that

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}\,[(2/\pi)(V_L(\text{p})/R_L)]} \times 100\%$$

$$\%\,\eta = 78.54\frac{V_L(\text{p})}{V_{CC}}\% \tag{12.29}$$

EXAMPLE 12.9 Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 24$ V with peak output voltages of:

a. $V_L(\text{p}) = 22$ V.
b. $V_L(\text{p}) = 6$ V.

Solution: Using Eq. (12.29) gives

a. $\%\,\eta = 78.54\dfrac{V_L(\text{p})}{V_{CC}}\% = 78.54\left(\dfrac{22\text{ V}}{24\text{ V}}\right) = \mathbf{72\%}$

b. $\%\,\eta = 78.54\left(\dfrac{6\text{ V}}{24\text{ V}}\right)\% = \mathbf{19.6\%}$

Notice that a voltage near the maximum [22 V in part (a)] results in an efficiency near the maximum, whereas a small voltage swing [6 V in part (b)] still provides an efficiency near 20%. Similar power supply and signal swings would have resulted in much poorer efficiency in a class A amplifier.

12.5 CLASS B AMPLIFIER CIRCUITS

A number of circuit arrangements for obtaining class B operation are possible. We will consider the advantages and disadvantages of a number of the more popular circuits in this section. The input signals to the amplifier could be a single signal, the circuit then providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite-polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, and the transformer-coupled amplifier has been very popular for a long time. Opposite-polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite-polarity signals. An opposite-polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *n*MOS and *p*MOS).

Figure 12.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 12.14a shows a center-tapped transformer to provide opposite-phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite

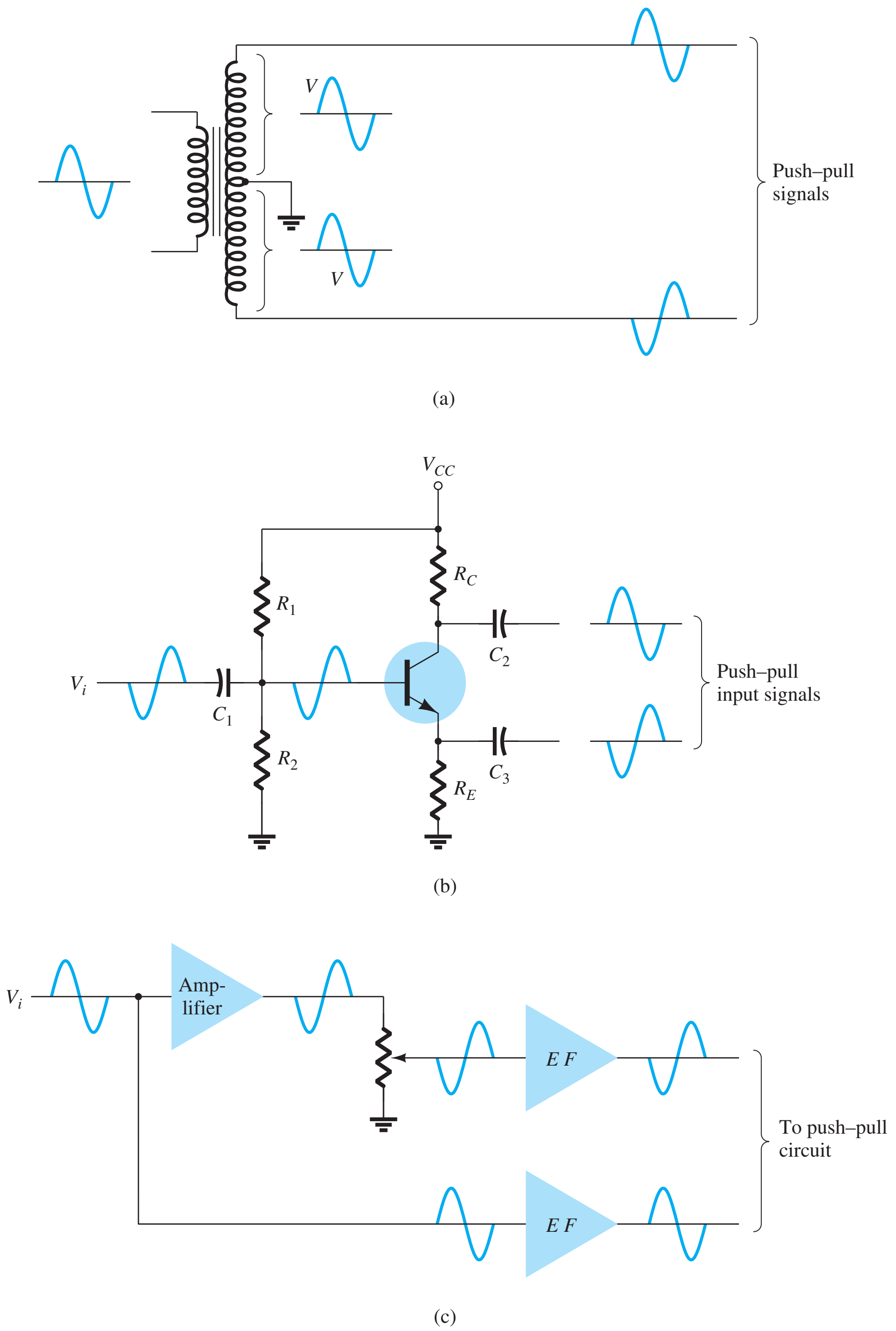


FIG. 12.14
Phase-splitter circuits.

in phase and of the same magnitude. The circuit of Fig. 12.14b uses a BJT stage with in-phase output from the emitter and opposite-phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a noninverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

Transformer-Coupled Push–Pull Circuits

The circuit of Fig. 12.15 uses a center-tapped input transformer to produce opposite-polarity signals to the two transistor inputs and an output transformer to drive the load in a push–pull mode of operation described next.

During the first half-cycle of operation, transistor Q_1 is driven into conduction, whereas transistor Q_2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q_2 conducts, whereas Q_1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.

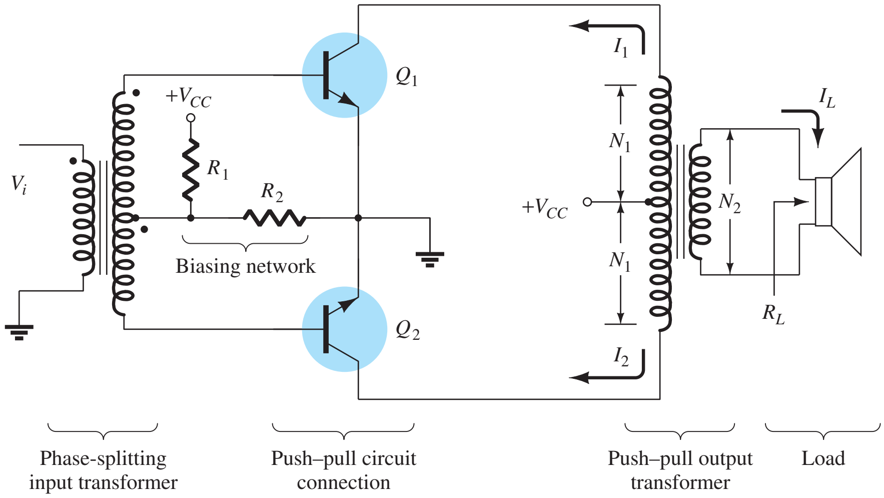
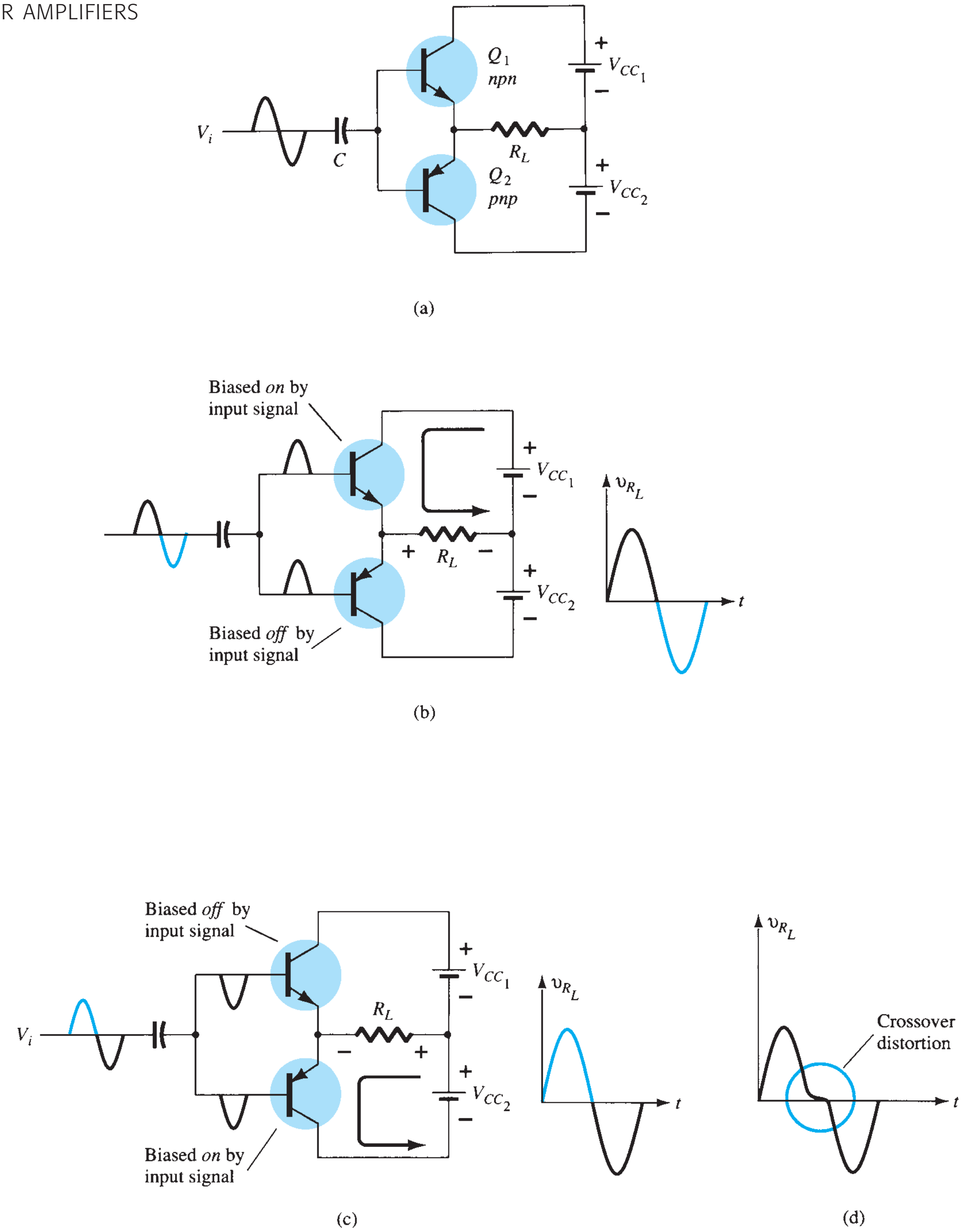


FIG. 12.15
Push–pull circuit.

Complementary-Symmetry Circuits

Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 12.16a. Whereas a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 12.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 12.16c.

During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 12.16d). *Crossover distortion* refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off so that the output voltage does not follow the input around the zero-voltage condition. Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.


V_i
C
Q_1
npn
Q_2
pnp
R_L
V_{CC_1}
V_{CC_2}
+
−
Biased *on* by input signal
Biased *off* by input signal
v_{R_L}
t
Biased *off* by input signal
Biased *on* by input signal
Crossover distortion

(a)

(b)

(c)

(d)

FIG. 12.16

Complementary-symmetry push–pull circuit.

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 12.17. Note that the load is driven as the output of an emitter-follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-connected transistors to provide higher output current and lower output resistance.

Quasi-Complementary Push–Pull Amplifier

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push–pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same matched *npn* transistors for the output is provided by a

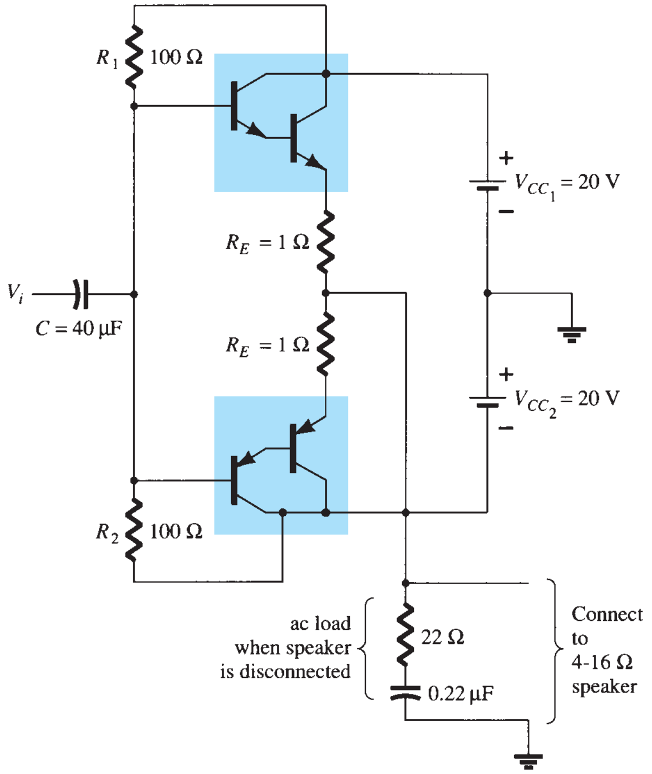

R_1
100 Ω
V_{CC_1} = 20 V
R_E = 1 Ω
V_i
C = 40 µF
R_E = 1 Ω
V_{CC_2} = 20 V
R_2
100 Ω
ac load
when speaker
is disconnected
22 Ω
0.22 µF
Connect
to
4-16 Ω
speaker

FIG. 12.17

Complementary-symmetry push–pull circuit using Darlington transistors.

quasi-complementary circuit, as shown in Fig. 12.18. The push–pull operation is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor

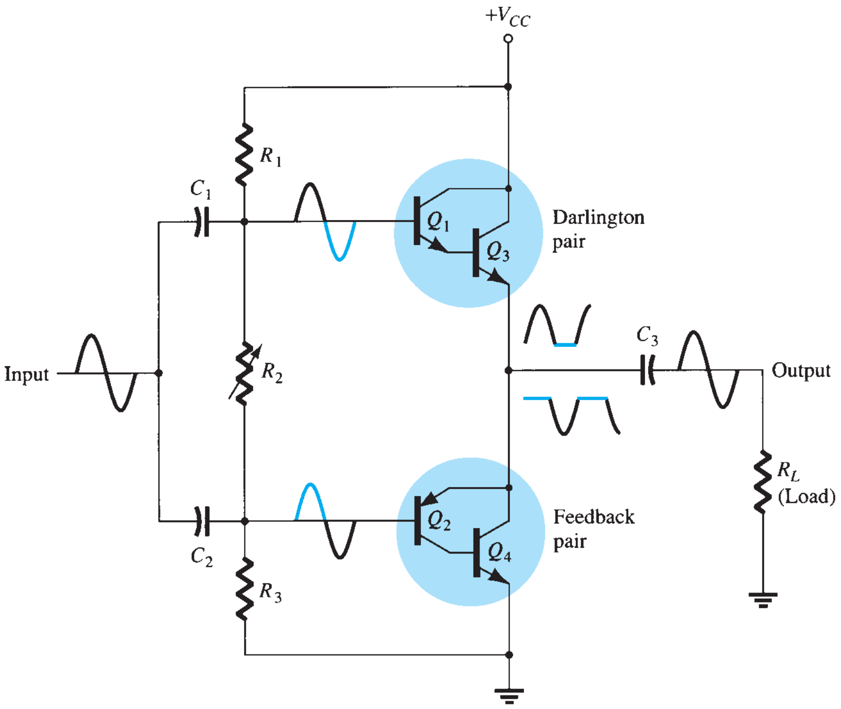

$+V_{CC}$
R_1
C_1
Q_1
Q_3
Darlington
pair
Input
R_2
C_3
Output
R_L
(Load)
Q_2
Q_4
Feedback
pair
C_2
R_3

FIG. 12.18

Quasi-complementary push–pull transformerless power amplifier.

R_2 can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push–pull stage then results in a full cycle output to the load. The quasi-complementary push–pull amplifier is the most popular form of power amplifier.

EXAMPLE 12.10 For the circuit of Fig. 12.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.

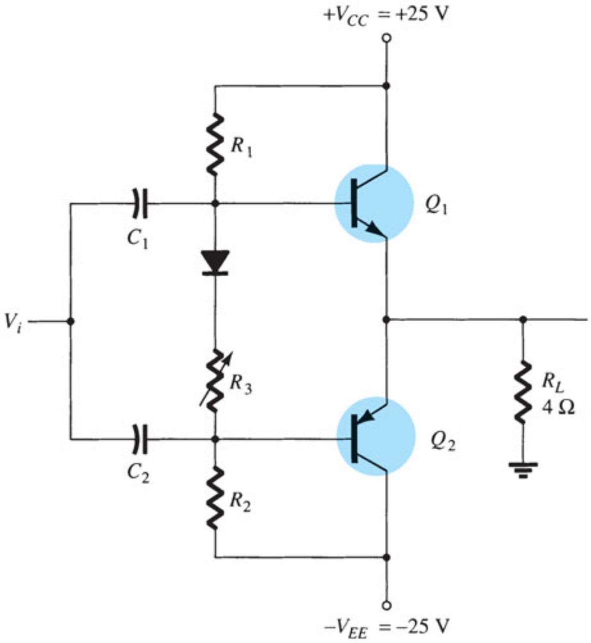


FIG. 12.19

Class B power amplifier for Examples 12.10 to 12.12.

Solution: The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\,V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(\text{p}) = 17\text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = \mathbf{36.125\ W}$$

The peak load current is

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\ \Omega} = 4.25\text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi}I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = (25\text{ V})(2.71\text{ A}) = \mathbf{67.75\ W}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\text{ W} - 36.125\text{ W}}{2} = \mathbf{15.8\ W}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125\text{ W}}{67.75\text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 12.11 For the circuit of Fig. 12.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and power dissipated by the output transistors at this voltage.

Solution: The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25\text{ V})^2}{\pi 4\ \Omega} = \mathbf{99.47\ W}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25\text{ V})^2}{2(4\ \Omega)} = \mathbf{78.125\ W}$$

[Note that the maximum efficiency is achieved:

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125\text{ W}}{99.47\text{ W}}100\% = 78.54\%]$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25\text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47\text{ W} - 78.125\text{ W} = \mathbf{21.3\ W}$$

EXAMPLE 12.12 For the circuit of Fig. 12.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution: The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25\text{ V})^2}{\pi^2 4\ \Omega} = \mathbf{31.66\ W}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(\text{p}) = 0.636(25\text{ V}) = \mathbf{15.9\ V}$$

(Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, whereas at $V_L = 25$ V they only had to dissipate 21.3 W.)

12.6 AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs, the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics*. For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz (2 × 1 kHz), 3 kHz (3 × 1 kHz), 4 kHz (4 × 1 kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency*; those at integer multiples are the *harmonics*. The 2-kHz component is therefore called a *second harmonic*, that at 3 kHz is the *third harmonic*, and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude A_1 and the nth frequency component has an amplitude A_n, a harmonic distortion can be defined as

$$\boxed{\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\%} \qquad \textbf{(12.30)}$$

The fundamental component is typically larger than any harmonic component.

EXAMPLE 12.13 Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution: Using Eq. (12.30) yields

$$\%\ D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{10\%}$$

$$\%\ D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{4\%}$$

$$\%\ D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{2\%}$$

Total Harmonic Distortion When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\%\ \text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\% \qquad \textbf{(12.31)}$$

where THD is total harmonic distortion.

EXAMPLE 12.14 Calculate the total harmonic distortion for the amplitude components given in Example 12.13.

Solution: Using the computed values of $D_2 = 0.10, D_3 = 0.04$, and $D_4 = 0.02$ in Eq. (12.31), we obtain

$$\begin{aligned}\%\ \text{THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= \mathbf{10.95\%}\end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

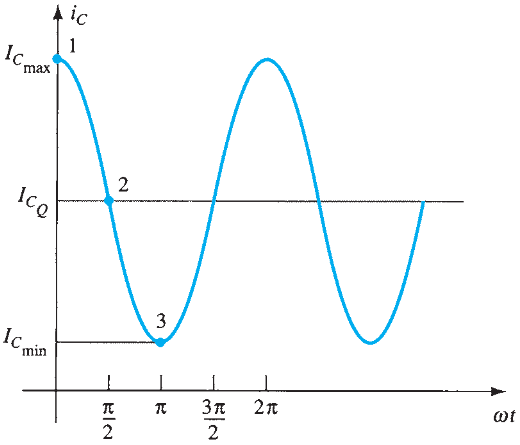


FIG. 12.20
Waveform for obtaining second harmonic distortion.

Second Harmonic Distortion Figure 12.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The signal shown indicates that some distortion is present. An equation that approximately describes the distorted signal waveform is

$$i_C \approx I_{C_Q} + I_0 + I_1 \cos \omega t + I_2 \cos \omega t \tag{12.32}$$

The current waveform contains the original quiescent current I_{C_Q}, which occurs with zero input signal; an additional dc current I_0, due to the nonzero average of the distorted signal; the fundamental component of the distorted ac signal I_1; and a second harmonic component I_2, at twice the fundamental frequency. Although other harmonics are also present, only the second is considered here. Equating the resulting current from Eq. (12.32) at a few points in the cycle to that shown on the current waveform provides the following three relations:

At point 1 ($\omega t = 0$),

$$i_C = I_{C_{\max}} = I_{C_Q} + I_0 + I_1 \cos 0 + I_2 \cos 0$$
$$I_{C_{\max}} = I_{C_Q} + I_0 + I_1 + I_2$$

At point 2 ($\omega t = \pi/2$),

$$i_C = I_{C_Q} = I_{C_Q} + I_0 + I_1 \cos\frac{\pi}{2} + I_2 \cos\frac{2\pi}{2}$$
$$I_{C_Q} = I_{C_Q} + I_0 - I_2$$

At point 3 ($\omega t = \pi$),

$$i_C = I_{C_{\min}} = I_{C_Q} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$
$$I_{C_{\min}} = I_{C_Q} + I_0 - I_1 + I_2$$

Solving the preceding three equations simultaneously gives the following results:

$$I_0 = I_2 = \frac{I_{C_{\max}} + I_{C_{\min}} - 2I_{C_Q}}{4}, \qquad I_1 = \frac{I_{C_{\max}} - I_{C_{\min}}}{2}$$

Referring to Eq. (12.30), we can express the definition of second harmonic distortion as

$$D_2 = \left|\frac{I_2}{I_1}\right| \times 100\%$$

Inserting the values of I_1 and I_2 determined above gives

$$D_2 = \left|\frac{\frac{1}{2}(I_{C_{\max}} + I_{C_{\min}}) - I_{C_Q}}{I_{C_{\max}} - I_{C_{\min}}}\right| \times 100\% \tag{12.33}$$

In a similar manner, the second harmonic distortion can be expressed in terms of measured collector–emitter voltages:

$$D_2 = \left|\frac{\frac{1}{2}(V_{CE_{\max}} + V_{CE_{\min}}) - V_{CE_Q}}{V_{CE_{\max}} - V_{CE_{\min}}}\right| \times 100\% \tag{12.34}$$

EXAMPLE 12.15 Calculate the second harmonic distortion if an output waveform displayed on an oscilloscope provides the following measurements:

a. $V_{CE_{\min}} = 1\text{ V}, V_{CE_{\max}} = 22\text{ V}, V_{CE_Q} = 12\text{ V}.$
b. $V_{CE_{\min}} = 4\text{ V}, V_{CE_{\max}} = 20\text{ V}, V_{CE_Q} = 12\text{ V}.$

Solution: Using Eq. (12.34), we get

a. $$D_2 = \left|\frac{\frac{1}{2}(22\text{ V} + 1\text{ V}) - 12\text{ V}}{22\text{ V} - 1\text{ V}}\right| \times 100\% = \mathbf{2.38\%}$$

b. $$D_2 = \left|\frac{\frac{1}{2}(20\text{ V} + 4\text{ V}) - 12\text{ V}}{20\text{ V} - 4\text{ V}}\right| \times 100\% = \mathbf{0\%} \qquad \text{(no distortion)}$$

Power of a Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor R_C due to the fundamental component of the distorted signal is

$$P_1 = \frac{I_1^2 R_C}{2} \tag{12.35}$$

The total power due to all the harmonic components of the distorted signal can then be calculated using

$$P = (I_1^2 + I_2^2 + I_3^2 + \cdots)\frac{R_C}{2} \tag{12.36}$$

The total power can also be expressed in terms of the total harmonic distortion,

$$P = (1 + D_2^2 + D_3^2 + \cdots)I_1^2\frac{R_C}{2} = (1 + \text{THD}^2)P_1 \tag{12.37}$$

EXAMPLE 12.16 For a harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$, and $D_4 = 0.01$, with $I_1 = 4\text{ A}$ and $R_C = 8\ \Omega$, calculate the total harmonic distortion, fundamental power component, and total power.

Solution: The total harmonic distortion is

$$\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.1)^2 + (0.02)^2 + (0.01)^2} \approx \mathbf{0.1}$$

The fundamental power, using Eq. (12.35), is

$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(4\text{ A})^2(8\ \Omega)}{2} = \mathbf{64\ W}$$

The total power calculated using Eq. (12.37) is then

$$P = (1 + \text{THD}^2)P_1 = [1 + (0.1)^2]64 = (1.01)64 = \mathbf{64.64\ W}$$

(Note that the total power is due mainly to the fundamental component even with 10% second harmonic distortion.)

Graphical Description of Harmonic Components of a Distorted Signal

A distorted waveform such as that which occurs in class B operation can be represented using Fourier analysis as a fundamental with harmonic components. Figure 12.21a shows a positive half-cycle such as the type that would result in one side of a class B amplifier. Using Fourier analysis techniques, we can obtain the fundamental component of the distorted signal as shown in Fig. 12.21b. Similarly, the second and third harmonic components can be obtained and are shown in Fig. 12.21c and d, respectively. Using the Fourier technique, we can construct the distorted waveform by adding the fundamental and harmonic components, as shown in Fig. 12.21e. In general, any periodic distorted waveform can be represented by adding a fundamental component and all harmonic components, each of varying amplitude and at various phase angles.

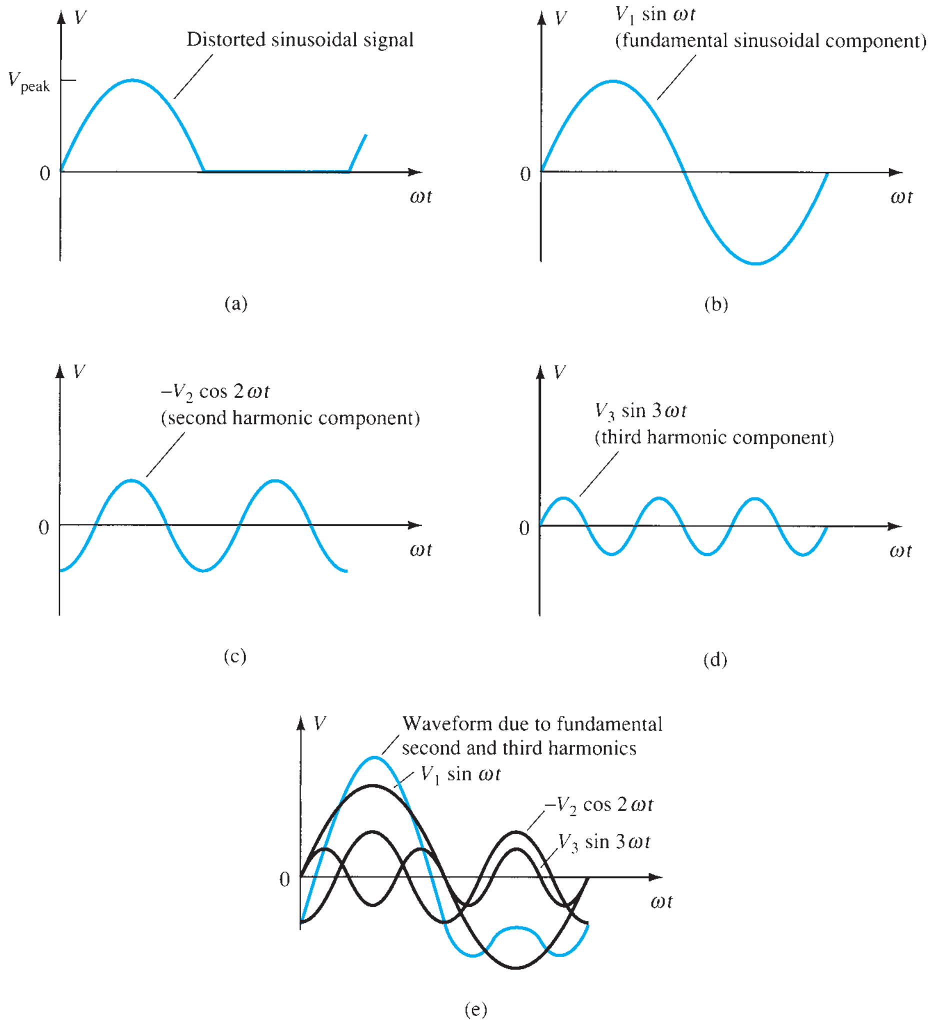


FIG. 12.21

Graphical representation of a distorted signal through the use of harmonic components.

12.7 POWER TRANSISTOR HEAT SINKING

Although integrated circuits are used for small-signal and low-power applications, most high-power applications still require individual power transistors. Improvements in production techniques have provided higher power ratings in small-sized packaging cases, have increased the maximum transistor breakdown voltage, and have provided faster-switching power transistors.

The maximum power handled by a particular device and the temperature of the transistor junctions are related since the power dissipated by the device causes an increase in temperature at the junction of the device. Obviously, a 100-W transistor will provide more power capability than a 10-W transistor. On the other hand, proper heat-sinking techniques will allow operation of a device at about one-half its maximum power rating.

Of the two types of bipolar transistors—germanium and silicon—silicon transistors provide greater maximum temperature ratings. Typically, the maximum junction temperature of these types of power transistors is as follows:

Silicon: 150–200°C
Germanium: 100–110°C

For many applications the average power dissipated may be approximated by

$$P_D = V_{CE} I_C \tag{12.38}$$

This power dissipation, however, is allowed only up to a maximum temperature. Above this temperature, the device power dissipation capacity must be reduced (or derated) so that at higher case temperatures the power-handling capacity is reduced, down to 0 W at the device maximum case temperature.

The greater the power handled by the transistor, the higher is the case temperature. Actually, the limiting factor in power handling by a particular transistor is the temperature of the device's collector junction. Power transistors are mounted in large metal cases to provide a large area from which the heat generated by the device may radiate (be transferred). Even so, operating a transistor directly into air (mounting it on a plastic board, for example) severely limits the device power rating. If, instead (as is usual practice), the device is mounted on some form of heat sink, its power-handling capacity can approach the rated maximum value more closely. A few heat sinks are shown in Fig. 12.22. When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temperature to a much lower value than would result without the heat sink. Even with an infinite heat sink (which, of course, is not available), for which the case temperature is held at the ambient (air) temperature, the junction will be heated above the case temperature and a maximum power rating must be considered.

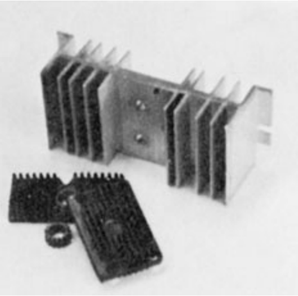


FIG. 12.22
Typical power heat sinks.

Since even a good heat sink cannot hold the transistor case temperature at ambient (which, by the way, could be more than 25°C if the transistor circuit is in a confined area where other devices are also radiating a good amount of heat), it is necessary to derate the amount of maximum power allowed for a particular transistor as a function of increased case temperature.

Figure 12.23 shows a typical power derating curve for a silicon transistor. The curve shows that the manufacturer will specify an upper temperature point (not necessarily 25°C), after which a linear derating takes place. For silicon, the maximum power that should be handled by the device does not reduce to 0 W until the case temperature is 200°C.

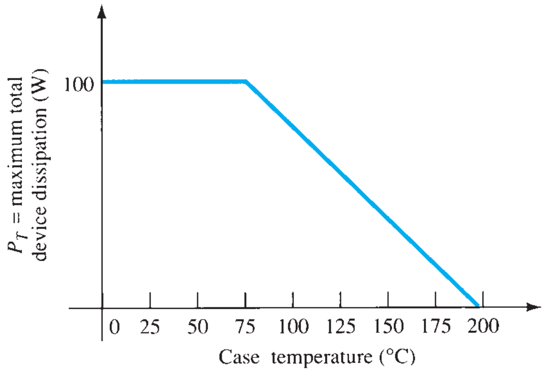


FIG. 12.23
Typical power derating curve for silicon transistors.

It is not necessary to provide a derating curve since the same information could be given simply as a listed derating factor on the device specification sheet. Stated mathematically, we have

$$P_D(\text{temp}_1) = P_D(\text{temp}_0) - (\text{Temp}_1 - \text{Temp}_0)(\text{derating factor}) \tag{12.39}$$

where the value of Temp_0 is the temperature at which derating should begin, the value of Temp_1 is the particular temperature of interest (above the value Temp_0), $P_D(\text{temp}_0)$ and $P_D(\text{temp}_1)$ are the maximum power dissipations at the temperatures specified, and the derating factor is the value given by the manufacturer in units of watts (or milliwatts) per degree of temperature.

EXAMPLE 12.17 Determine what maximum dissipation will be allowed for an 80-W silicon transistor (rated at 25°C) if derating is required above 25°C by a derating factor of 0.5 W/°C at a case temperature of 125°C.

Solution:

$$\begin{aligned} P_D(125°\text{C}) &= P_D(25°\text{C}) - (125°\text{C} - 25°\text{C})(0.5\ \text{W}/°\text{C}) \\ &= 80\ \text{W} - 100°\text{C}(0.5\ \text{W}/°\text{C}) = \mathbf{30\ W} \end{aligned}$$

It is interesting to note what power rating results from using a power transistor without a heat sink. For example, a silicon transistor rated at 100 W at (or below) 100°C is rated only 4 W at (or below) 25°C, the free-air temperature. Thus, operated without a heat sink, the device can handle a maximum of only 4 W at the room temperature of 25°C. Using a heat sink large enough to hold the case temperature to 100°C at 100 W allows operating at the maximum power rating.

Thermal Analogy of a Power Transistor

Selection of a suitable heat sink requires a considerable amount of detail that is not appropriate to our present basic considerations of the power transistor. However, more detail about the thermal characteristics of the transistor and its relation to the power dissipation of the transistor may help provide a clearer understanding of power as limited by temperature. The following discussion should prove useful.

A picture of how the junction temperature T_J, case temperature T_C, and ambient (air) temperature T_A are related by the device heat-handling capacity—a temperature coefficient usually called thermal resistance—is presented in the thermal–electrical analogy shown in Fig. 12.24.

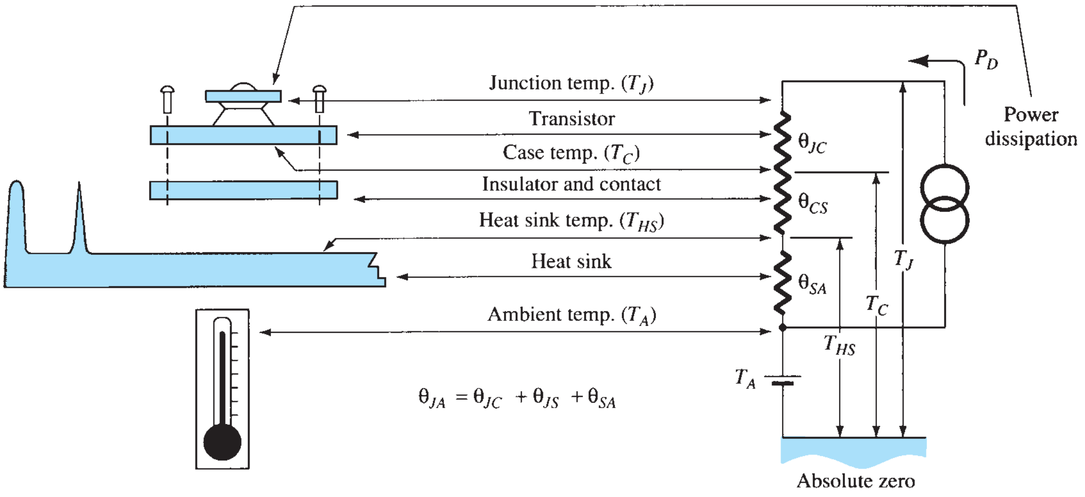


FIG. 12.24

Thermal-to-electrical analogy.

In providing a thermal–electrical analogy, the term *thermal resistance* is used to describe heat effects by an electrical term. The terms in Fig. 12.24 are defined as follows:

θ_{JA} = total thermal resistance (junction to ambient)
θ_{JC} = transistor thermal resistance (junction to case)
θ_{CS} = insulator thermal resistance (case to heat sink)
θ_{SA} = heat-sink thermal resistance (heat sink to ambient)

Using the electrical analogy for thermal resistances, we can write

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}} \qquad \textbf{(12.40)}$$

The analogy can also be used in applying Kirchhoff's law to obtain

$$T_J = P_D\theta_{JA} + T_A \qquad \textbf{(12.41)}$$

The last relation shows that the junction temperature "floats" on the ambient temperature, and that the higher the ambient temperature, the lower is the allowed value of device power dissipation.

The thermal factor θ provides information about how much temperature drop (or rise) results for a given amount of power dissipation. For example, the value of θ_{JC} is usually about 0.5°C/W. This means that for a power dissipation of 50 W, the difference in temperature between case temperature (as measured by a thermocouple) and the inside junction temperature is only

$$T_J - T_C = \theta_{JC} P_D = (0.5°\text{C/W})(50\text{ W}) = 25°\text{C}$$

Thus, if the heat sink can hold the case at, say, 50°C, the junction is then only at 75°C. This is a relatively small temperature difference, especially at lower power-dissipation levels.

The value of thermal resistance from junction to free air (using no heat sink) is, typically,

$$\theta_{JA} = 40°\text{C/W} \qquad \text{(into free air)}$$

For this thermal resistance, only 1 W of power dissipation results in a junction temperature 40°C greater than the ambient.

A heat sink can now be seen to provide a low thermal resistance between case and air—much less than the 40°C/W value of the transistor case alone. Using a heat sink having

$$\theta_{SA} = 2°\text{C/W}$$

and with an insulating thermal resistance (from case to heat sink) of

$$\theta_{CS} = 0.8°\text{C/W}$$

and finally, for the transistor,

$$\theta_{CJ} = 0.5°\text{C/W}$$

we obtain

$$\begin{aligned}\theta_{JA} &= \theta_{SA} + \theta_{CS} + \theta_{CJ} \\ &= 2.0°\text{C/W} + 0.8°\text{C/W} + 0.5°\text{C/W} = 3.3°\text{C/W}\end{aligned}$$

So, with a heat sink, the thermal resistance between air and the junction is only 3.3°C/W, compared to 40°C/W for the transistor operating directly into free air. Using the value of θ_{JA} above for a transistor operated at, say, 2 W, we calculate

$$T_J - T_A = \theta_{JA} P_D = (3.3°\text{C/W})(2\text{ W}) = 6.6°\text{C}$$

In other words, the use of a heat sink in this example provides only a 6.6°C increase in junction temperature as compared to an 80°C rise without a heat sink.

EXAMPLE 12.18 A silicon power transistor is operated with a heat sink ($\theta_{SA} = 1.5°\text{C/W}$). The transistor, rated at 150 W (25°C), has $\theta_{JC} = 0.5°\text{C/W}$, and the mounting insulation has $\theta_{CS} = 0.6°\text{C/W}$. What maximum power can be dissipated if the ambient temperature is 40°C and $T_{J_{\max}} = 200°\text{C}$?

Solution:

$$P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{200°\text{C} - 40°\text{C}}{0.5°\text{C/W} + 0.6°\text{C/W} + 1.5°\text{C/W}} \approx \mathbf{61.5\ W}$$

12.8 CLASS C AND CLASS D AMPLIFIERS

Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, although not used as audio amplifiers, do find use in tuned circuits as in communications.

Class C Amplifier

A class C amplifier, such as that shown in Fig. 12.25, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.

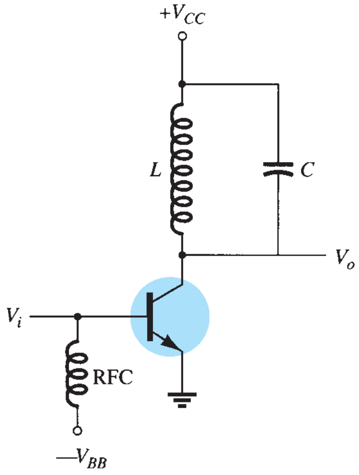


FIG. 12.25
Class C amplifier circuit.

Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back into a sinusoidal-type signal to recover the original signal. Fig. 12.26 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced. Although the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.

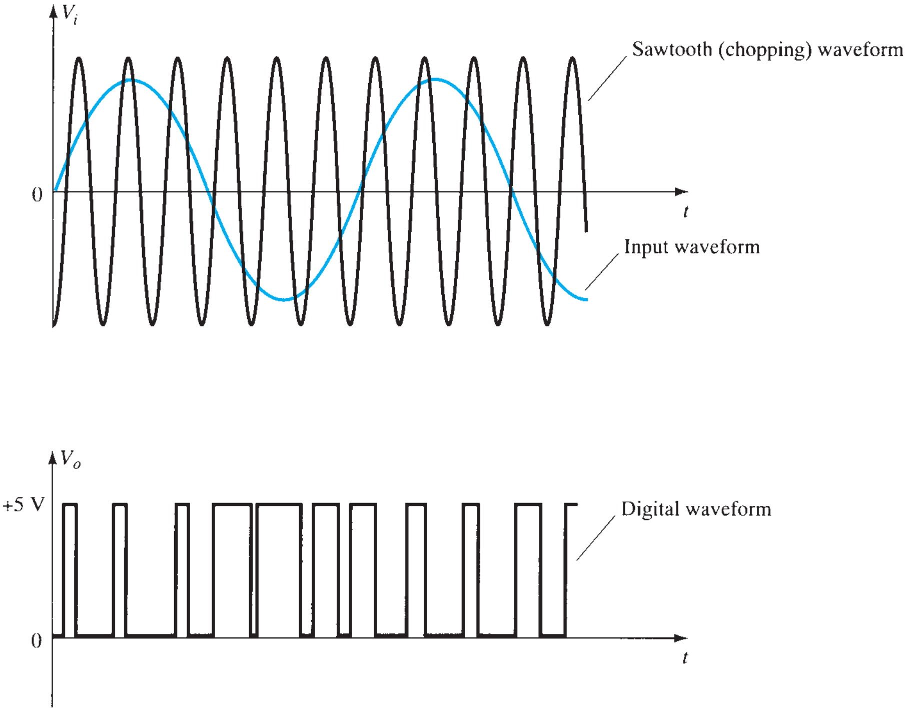


FIG. 12.26
Chopping of a sinusoidal waveform to produce a digital waveform.

Figure 12.27 shows a block diagram of the unit needed to amplify the class D signal and then convert back into the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to their low "on" voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.

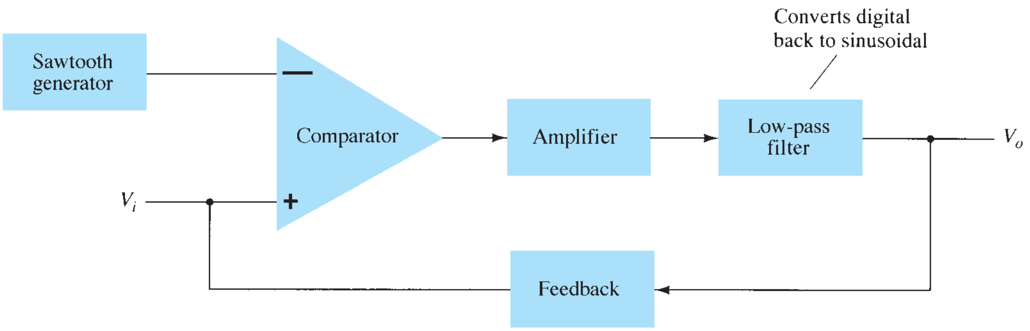


FIG. 12.27
Block diagram of class D amplifier.

12.9 SUMMARY

Important Conclusions and Concepts

1. Amplifier classes:
   Class A—the output stage conducts for a full 360° (a full waveform cycle).
   Class B—the output stages each conduct for 180° (together providing a full cycle).
   Class AB—the output stages each conduct between 180° and 360° (providing a full cycle at less efficiency).
   Class C—the output stage conducts for less than 180° (used in tuned circuits).
   Class D—has operation using digital or pulsed signals.
2. Amplifier efficiency:
   Class A—maximum efficiency of 25% (without transformer) and 50% (with transformer).
   Class B—maximum efficiency of 78.5%.
3. Power considerations:
   a. Input power is provided by the dc power supply.
   b. Output power is that delivered to the load.
   c. Power dissipated by active devices is essentially the difference between the input and output powers.
4. Push–pull (complementary) operation is typically the opposite of that of devices with one on at a time—one "pushing" for half the cycle and the other "pulling" for half the cycle.
5. **Harmonic distortion** refers to the nonsinusoidal nature of a periodic waveform—the distortion being defined as that at the periodic frequency and multiples of that frequency.
6. **Heat sink** refers to the use of metal cases or frames and fans to remove the heat gen–erated in a circuit element.

Equations

$$P_i(\text{dc}) = V_{CC}I_{CQ}$$

$$\begin{aligned} P_o(\text{ac}) &= V_{CE}(\text{rms})I_C(\text{rms}) \\ &= I_C^2(\text{rms})R_C \\ &= \frac{V_C^2(\text{rms})}{R_C} \end{aligned}$$

$$\begin{aligned} P_o(\text{ac}) &= \frac{V_{CE}(\text{p})I_C(\text{p})}{2} \\ &= \frac{I_C^2(\text{p})}{2R_C} \\ &= \frac{V_{CE}^2(\text{p})}{2R_C} \end{aligned}$$

$$\begin{aligned} P_o(\text{ac}) &= \frac{V_{CE}(\text{p-p})I_C(\text{p-p})}{8} \\ &= \frac{I_C^2(\text{p-p})}{8}R_C \\ &= \frac{V_{CE}^2(\text{p-p})}{8R_C} \end{aligned}$$

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Transformer action:

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Class B operation:

$$I_{\text{dc}} = \frac{2}{\pi} I(\text{p})$$

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi} I(\text{p})\right)$$

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L}$$

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}$$

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{\text{dc}}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}$$

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

Harmonic distortion:

$$\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

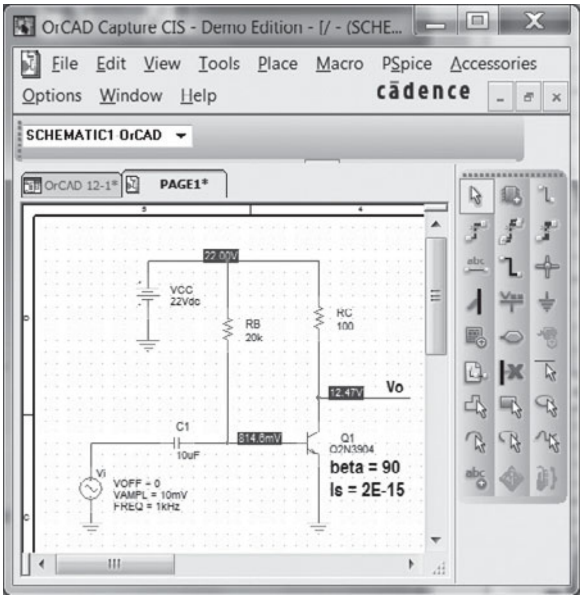
Heat sink:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

12.10 COMPUTER ANALYSIS

Program 12.1—Series-Fed Class A Amplifier

Using Design Center, we draw the circuit of a series-fed class A amplifier as shown in Fig. 12.28. Figure 12.29 shows some of the analysis output. Edit the transistor model for values of only **BF** = 90 and **IS** = 2E-15. This keeps the transistor model more ideal so that PSpice calculations better match those below.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cādence
SCHEMATIC1 OrCAD
OrCAD 12-1*
PAGE1*
22.00V
VCC
22Vdc
RB
20k
RC
100
12.47V
Vo
C1
10uF
814.6mV
Q1
Q2N3904
beta = 90
Is = 2E-15
Vi
VOFF = 0
VAMPL = 10mV
FREQ = 1kHz

FIG. 12.28

Series-fed class A amplifier.

The dc bias of the collector voltage is shown to be

$$V_c(\text{dc}) = 12.47 \text{ V}$$

With transistor beta set to 90, the ac gain is calculated as follows:

$$I_E = I_c = 95 \text{ mA (from analysis output of PSpice)}$$

$$r_e = 26 \text{ mV}/95 \text{ mA} = 0.27\ \Omega$$

```
Series-fed Class-A Amplifier

****      CIRCUIT DESCRIPTION
******************************************************************************
****      BJT MODEL PARAMETERS
          Q2N3904
          NPN
     IS   2.000000E-15
     BF   90

****      SMALL SIGNAL BIAS SOLUTION
******************************************************************************
 NODE      VOLTAGE   NODE      VOLTAGE   NODE      VOLTAGE   NODE      VOLTAGE
 (N00210)  .8146     (N00214)  0.0000    (N00232)  22.0000   (N00286)  12.4670

   VOLTAGE SOURCE CURRENTS
   NAME      CURRENT
   V_VCC     -9.639E-02
   V_Vi       0.000E+00

TOTAL POWER DISSIPATION   2.12E+00  WATTS
```

FIG. 12.29

Analysis output for the circuit of Fig. 12.28.

For a gain of

$$A_v = -R_c/r_e = -100/0.27 = -370$$

The output voltage is then

$$V_o = A_v V_i = (-370) \cdot 10\text{ mV} = -3.7\text{ V(peak)}$$

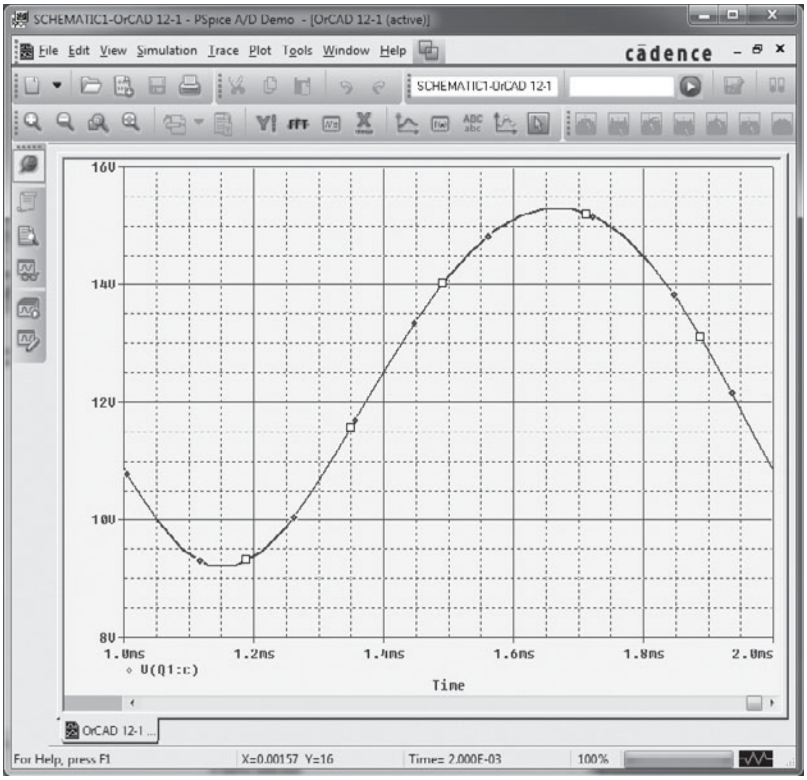
The output waveform obtained using **probe** is shown in Fig. 12.30. For a peak-to-peak output of

$$V_o(\text{p-p}) = 15.6\text{ V} - 8.75\text{ V} = 6.85\text{ V}$$

the peak output is

$$V_o(\text{p}) = 6.85\text{ V}/2 = 3.4\text{ V}$$

which compares well with that calculated below.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File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 12-1
16V
14V
12V
10V
8V
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
◇ V(Q1:c)
Time
OrCAD 12-1 ...
For Help, press F1
X=0.00157 Y=16
Time= 2.000E-03
100%

FIG. 12.30

Probe output for the circuit of Fig. 12.28.

From the circuit output analysis, the input power is

$$P_i = V_{CC}I_C = (22\text{ V}) \cdot (95\text{ mA}) = 2.09\text{ W}$$

From the probe ac data, the output power is

$$P_o(\text{ac}) = V_o(\text{p-p})^2/[8 \cdot R_L] = (6.85)^2/[8 \cdot 100] = 58\text{ mW}$$

The efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (58\text{ mW}/2.09\text{ W}) \cdot 100\% = 2.8\%$$

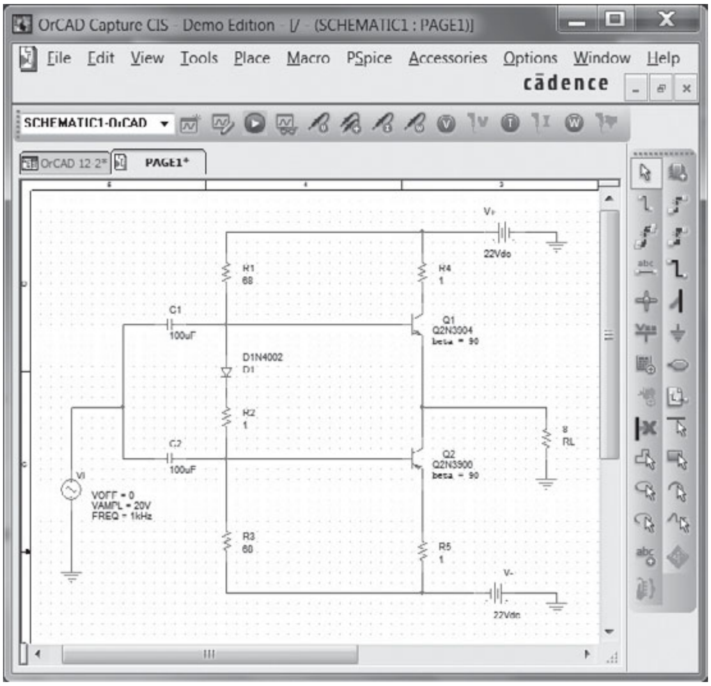
A larger input signal would increase the ac power delivered to the load and increase the efficiency (the maximum being 25%).

Program 12.2—Quasi-Complementary Push–Pull Amplifier

Figure 12.31 shows a quasi-complementary push–pull class B power amplifier. For the input of $V_i = 20\text{ V(p)}$, the output waveform obtained using **probe** is shown in Fig. 12.32.

The resulting ac output voltage is seen to be

$$V_o(\text{p-p}) = 33.7\text{ V}$$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SCHEMATIC1-OrCAD
OrCAD 12-2*
PAGE1*
V+
22Vdc
R1
68
R4
1
C1
100uF
Q1
Q2N3904
beta = 90
D1N4002
D1
R2
1
8
RL
C2
100uF
Q2
Q2N3906
beta = 90
VI
VOFF = 0
VAMPL = 20V
FREQ = 1kHz
R3
68
R5
1
V-
22Vdc

FIG. 12.31

Quasi-complementary class B power amplifier.

so that

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (33.7\text{ V})^2/(8 \cdot 8\ \Omega) = 17.7\text{ W}$$

The input power for that amplitude signal is

$$\begin{aligned} P_i &= V_{CC}I_{\text{dc}} = V_{CC}\,[(2/\pi)(V_o(\text{p-p})/2)/R_L] \\ &= (22\text{ V}) \cdot [(2/\pi)(33.7\text{ V}/2)/8] = 29.5\text{ W} \end{aligned}$$

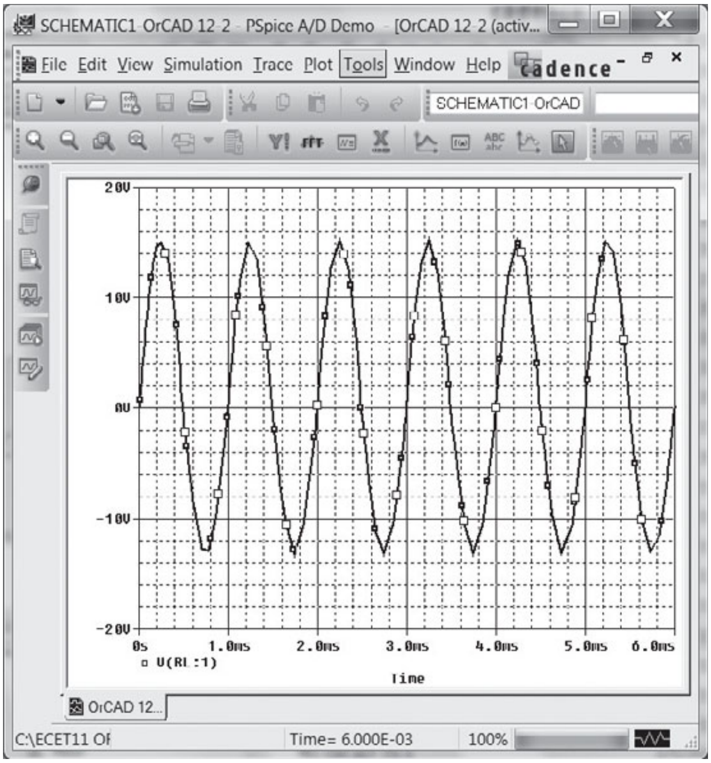
The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (17.7\text{ W}/29.5\text{ W}) \cdot 100\% = 60\%$$

Program 12.3—Op-Amp Push–Pull Amplifier

Figure 12.33 shows an op-amp push–pull amplifier providing ac output to an 8-Ω load. As shown, the op-amp provides a gain of

$$A_v = -R_F/R_1 = -47\text{ k}\Omega/18\text{ k}\Omega = -2.6$$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cadence
SCHEMATIC1-OrCAD
20V
10V
0V
-10V
-20V
0s
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
6.0ms
□ V(RL:1)
Time
OrCAD 12...
C:\ECET11 OF
Time= 6.000E-03
100%

FIG. 12.32

Probe output of the circuit in Fig. 12.31.

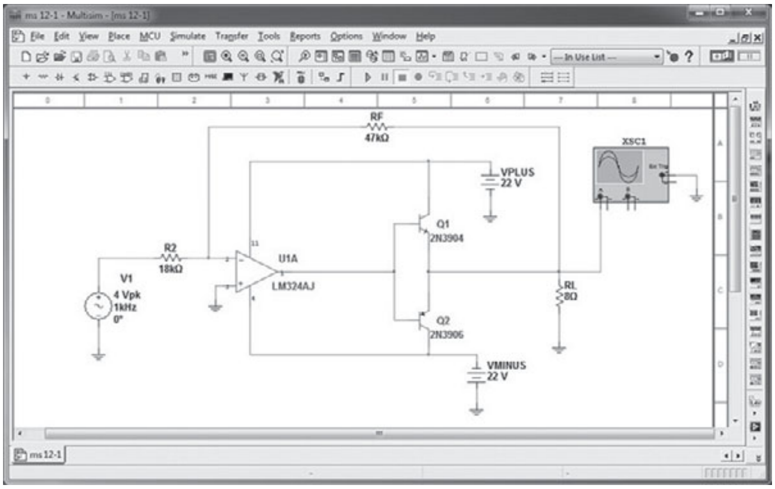

ms 12-1 - Multisim - [ms 12-1]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
RF
47kΩ
XSC1
VPLUS
22 V
Q1
2N3904
R2
18kΩ
U1A
LM324AJ
V1
4 Vpk
1kHz
0°
RL
8Ω
Q2
2N3906
VMINUS
22 V
ms 12-1

FIG. 12.33

Op-amp class B amplifier.

For the input $V_i = 1$ V, the output is

$$V_o(\text{p}) = A_v V_i = -2.6 \cdot (1\text{ V}) = -2.6\text{ V}$$

Figure 12.34 shows the oscilloscope display of the output voltage.

The output power is then calculated to be

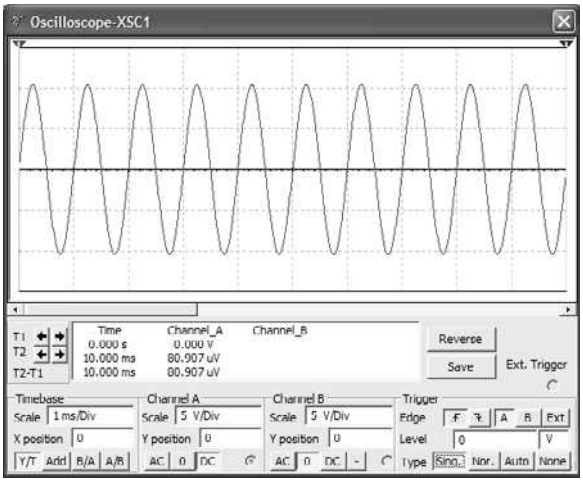
$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (20.4\text{ V})^2/(8 \cdot 8\ \Omega) = 6.5\text{ W}$$

The input power for that amplitude signal is

$$\begin{aligned} P_i &= V_{CC} I_{\text{dc}} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)/R_L] \\ &= (12\text{ V}) \cdot [(2/\pi) \cdot (20.4\text{ V}/2)/8] = 9.7\text{ W} \end{aligned}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (6.5\text{ W}/9.7\text{ W}) \cdot 100\% = 67\%$$



	Time	Channel_A	Channel_B
T1	0.000 s	0.000 V	
T2	10.000 ms	80.907 uV	
T2-T1	10.000 ms	80.907 uV	

Timebase
Scale 1 ms/Div
X position 0

Channel A
Scale 5 V/Div
Y position 0

Channel B
Scale 5 V/Div
Y position 0

Trigger
Level 0 V

FIG. 12.34

Probe output for the circuit of Fig. 12.33.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

12.2 Series-Fed Class A Amplifier

1. Calculate the input and output power for the circuit of Fig. 12.35. The input signal results in a base current of 5 mA rms.

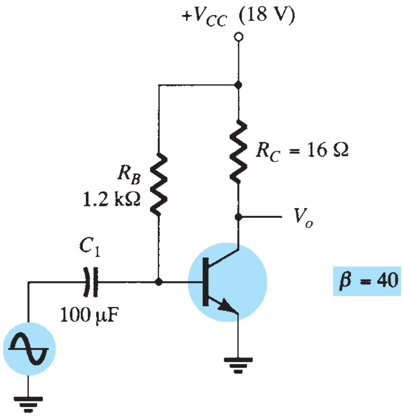


FIG. 12.35

Problems 1 to 4 and 26.

2. Calculate the input power dissipated by the circuit of Fig. 12.35 if R_B is changed to 1.5 kΩ.
3. What maximum output power can be delivered by the circuit of Fig. 12.35 if R_B is changed to 1.5 kΩ?
4. If the circuit of Fig. 12.35 is biased at its center voltage and center collector operating point, what is the input power for a maximum output power of 1.5 W?

12.3 Transformer-Coupled Class A Amplifier

5. A class A transformer-coupled amplifier uses a 25:1 transformer to drive a 4-Ω load. Calculate the effective ac load (seen by the transistor connected to the larger turns side of the transformer).
6. What turns ratio transformer is needed to couple to an 8-Ω load so that it appears as an 8-kΩ effective load?
7. Calculate the transformer turns ratio required to connect four parallel 16-Ω speakers so that they appear as an 8-kΩ effective load.

***8.** A transformer-coupled class A amplifier drives a 16-Ω speaker through a 3.87:1 transformer. Using a power supply of $V_{CC} = 36$ V, the circuit delivers 2 W to the load. Calculate:
   - **a.** P(ac) across transformer primary.
   - **b.** V_L(ac).
   - **c.** V(ac) at transformer primary.
   - **d.** The rms values of load and primary current.

9. Calculate the efficiency of the circuit of Problem 8 if the bias current is $I_{C_Q} = 150$ mA.

10. Draw the circuit diagram of a class A transformer-coupled amplifier using an *npn* transistor.

12.4 Class B Amplifier Operation

11. Draw the circuit diagram of a class B *npn* push–pull power amplifier using transformer-coupled input.

12. For a class B amplifier providing a 22-V peak signal to an 8-Ω load and a power supply of $V_{CC} = 25$ V, determine:
   - **a.** Input power.
   - **b.** Output power.
   - **c.** Circuit efficiency.

13. For a class B amplifier with $V_{CC} = 25$ V driving an 8-Ω load, determine:
   - **a.** Maximum input power.
   - **b.** Maximum output power.
   - **c.** Maximum circuit efficiency.

***14.** Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 22$ V driving a 4-Ω load with peak output voltages of:
   - **a.** $V_L(\mathrm{p}) = 20$ V.
   - **b.** $V_L(\mathrm{p}) = 4$ V.

12.5 Class B Amplifier Circuits

15. Sketch the circuit diagram of a quasi-complementary amplifier, showing voltage waveforms in the circuit.

16. For the class B power amplifier of Fig. 12.36, calculate:
   - **a.** Maximum P_o(ac).
   - **b.** Maximum P_i(dc).
   - **c.** Maximum %η.
   - **d.** Maximum power dissipated by both transistors.

***17.** If the input voltage to the power amplifier of Fig. 12.36 is 8-V rms, calculate:
   - **a.** P_i(dc).
   - **b.** P_o(ac).

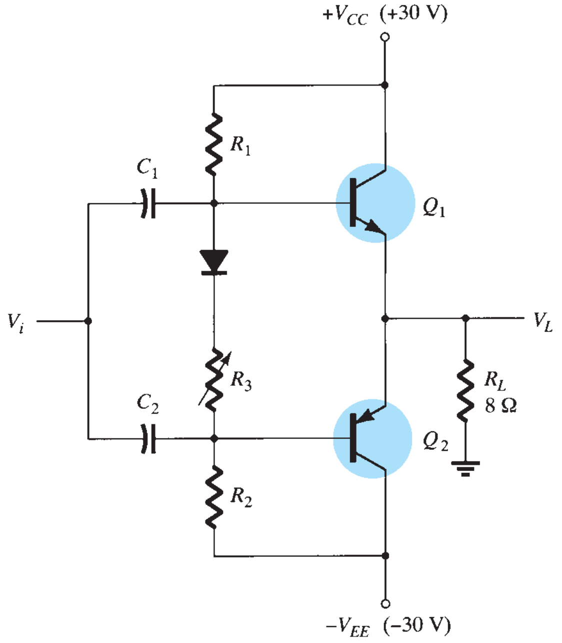


FIG. 12.36
Problems 16, 17, and 27.

c. %η.

d. Power dissipated by both power output transistors.

***18.** For the power amplifier of Fig. 12.37, calculate:

a. P_o(ac).

b. P_i(dc).

c. %η.

d. Power dissipated by both output transistors.

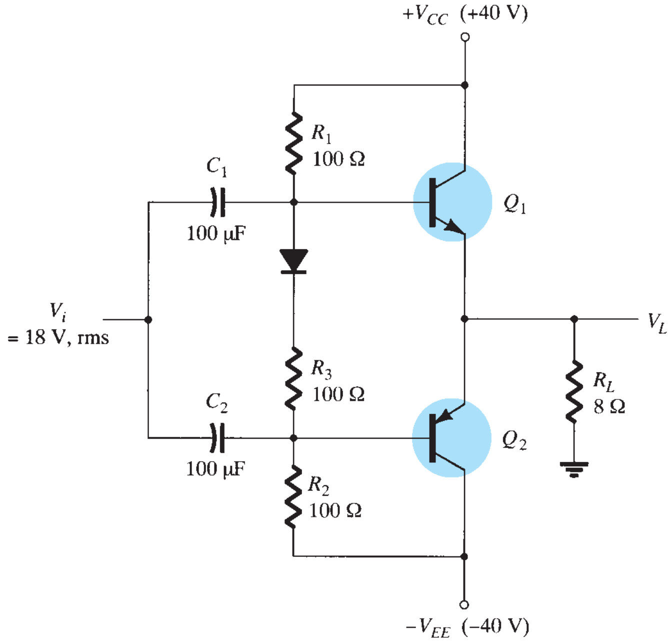


FIG. 12.37
Problem 18.

12.6 Amplifier Distortion

19. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.1 V, second harmonic amplitude of 0.3 V, third harmonic component of 0.1 V, and fourth harmonic component of 0.05 V.

20. Calculate the total harmonic distortion for the amplitude components of Problem 19.

21. Calculate the second harmonic distortion for an output waveform having measured values of $V_{CE_{\text{min}}} = 2.4$ V, $V_{CE_Q} = 10$ V, and $V_{CE_{\text{max}}} = 20$ V.

22. For distortion readings of $D_2 = 0.15, D_3 = 0.01$, and $D_4 = 0.05$, with $I_1 = 3.3$ A and $R_C = 4\ \Omega$, calculate the total harmonic distortion fundamental power component and total power.

12.7 Power Transistor Heat Sinking

23. Determine the maximum dissipation allowed for a 100-W silicon transistor (rated at 25°C) for a derating factor of 0.6 W/°C at a case temperature of 150°C.

***24.** A 160-W silicon power transistor operated with a heat sink ($\theta_{SA} = 1.5°\text{C/W}$) has $\theta_{JC} = 0.5°\text{C/W}$ and a mounting insulation of $\theta_{CS} = 0.8°\text{C/W}$. What maximum power can be handled by the transistor at an ambient temperature of 80°C? (The junction temperature should not exceed 200°C.)

25. What maximum power can a silicon transistor ($T_{J_{\text{max}}} = 200°\text{C}$) dissipate into free air at an ambient temperature of 80°C?

12.9 Computer Applications

***26.** Use Design Center to draw the schematic of Fig. 12.35 with $V_i = 9.1$ mV.

***27.** Use Design Center to draw the schematic of Fig. 12.36 with $V_i = 25$ V(p). Determine the circuit efficiency.

***28.** Use Multisim to draw the schematic of an op-amp class B amplifier as in Fig. 12.33. Use $R_1 = 10\ \text{k}\Omega, R_F = 50\ \text{k}\Omega$, and $V_i = 2.5$ V(p). Determine the circuit efficiency.

13

Linear-Digital ICs

CHAPTER OBJECTIVES

- About analog-to-digital conversion
- About digital-to-analog conversion
- Operation of a timer circuit
- Operation of phase-locked loops

13.1 INTRODUCTION

Although there are many ICs containing only digital circuits and many that contain only linear circuits, there are a number of units that contain both linear and digital circuits. Among the linear/digital ICs are comparator circuits, digital/analog converters, interface circuits, timer circuits, voltage-controlled oscillator (VCO) circuits, and phase-locked loops (PLLs).

The comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing whether the input voltage exceeded the reference voltage.

Circuits that convert digital signals into an analog or linear voltage and those that convert a linear voltage into a digital value are popular in aerospace equipment, automotive equipment, and compact disk (CD) players, among many other applications.

Interface circuits are used to enable connecting signals of different digital voltage levels, from different types of output devices, or from different impedances so that both the driver stage and the receiver stage operate properly.

Timer ICs provide linear and digital circuits to use in various timing operations, as in a car alarm, a home timer to turn lights on or off, and a circuit in electromechanical equipment to provide proper timing to match the intended unit operation. The 555 timer has long been a popular IC unit. A voltage-controlled oscillator provides an output clock signal whose frequency can be varied or adjusted by an input voltage. One popular application of a VCO is in a phase-locked loop unit, as used in various communication transmitters and receivers.

13.2 COMPARATOR UNIT OPERATION

A comparator circuit accepts input of linear voltages and provides a digital output that indicates when one input is less than or greater than the second. A basic comparator circuit can be represented as in Fig. 13.1a. The output is a digital signal that stays at a high voltage

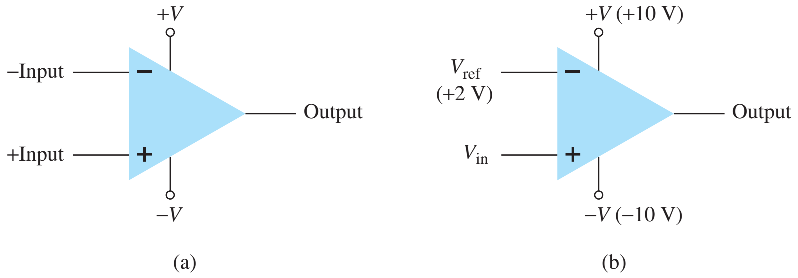


FIG. 13.1

Comparator unit: (a) basic unit; (b) typical application.

level when the noninverting (+) input is greater than the voltage at the inverting (−) input and switches to a lower voltage level when the noninverting input voltage goes below the inverting input voltage.

Figure 13.1b shows a typical connection with one input (the inverting input in this example) connected to a reference voltage of 2 V, the non-inverting input terminal connected as the input signal voltage. As long as V_{in} is less than the reference voltage level of +2 V, the output remains at a low voltage level (near −10 V). When the input rises just above +2 V, the output quickly switches to a high-voltage level (near +10 V). Thus the high output indicates that the input signal is greater than +2 V.

Because the internal circuit used to build a comparator contains essentially an op-amp circuit with very high voltage gain, we can examine the operation of a comparator using a 741 op-amp, as shown in Fig. 13.2. With reference input (at pin 2) set to 0 V, a sinusoidal signal applied to the noninverting input (pin 3) will cause the output to switch between its two output states, as shown in Fig. 13.2b. The input V_i going even a fraction of a millivolt above the 0-V reference level will be amplified by the very high voltage gain (typically over 100,000), so that the output rises to its positive output saturation level and remains there, while the input stays above $V_{ref} = 0$ V. When the input drops just below the 0-V reference level, the output is driven to its lower saturation level and stays there, while the input remains below $V_{ref} = 0$ V. Figure 13.2b clearly shows that the input signal is linear, whereas the output is digital.

In general use, the reference voltage need not be 0 V but can be any desired positive or negative voltage. Also, the reference voltage may be connected to either plus or minus input and the input signal then applied to the other input.

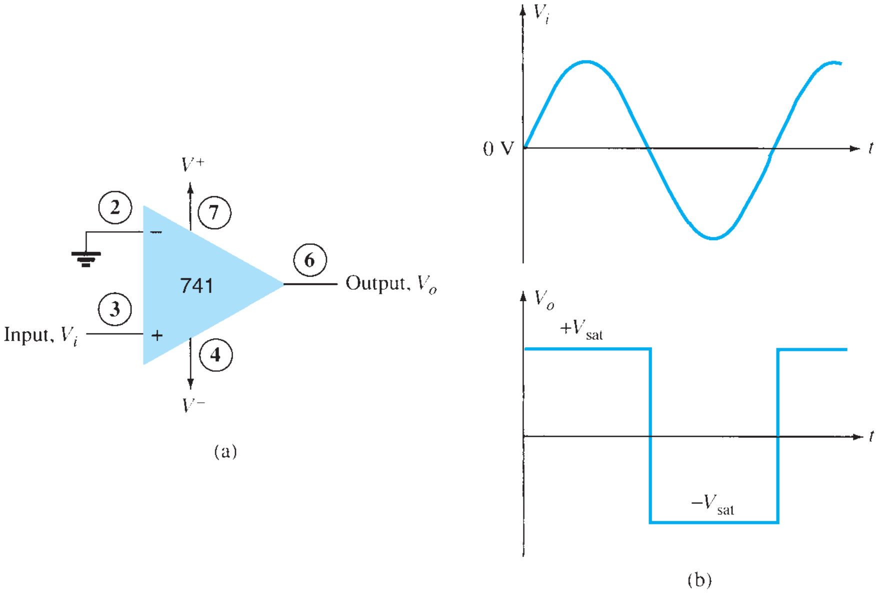


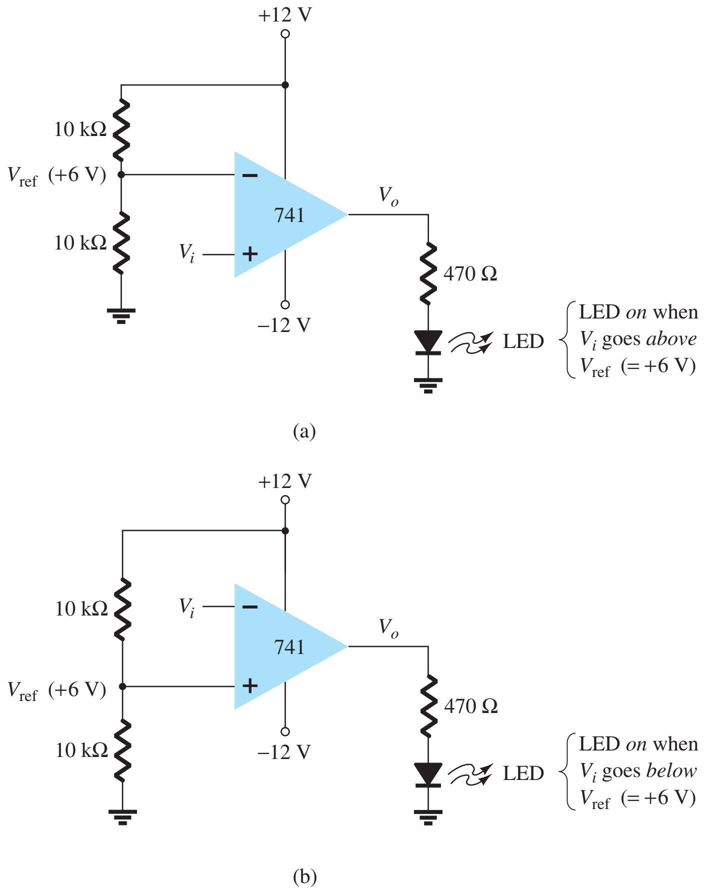
FIG. 13.2

Operation of a 741 op-amp as a comparator.

Use of Op-Amp as Comparator

Figure 13.3a shows a circuit operating with a positive reference voltage connected to the inverting input and the output connected to an indicator LED. The reference voltage level is set at

$$V_{\text{ref}} = \frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega}(+12\ \text{V}) = +6\ \text{V}$$



(a)

(b)

FIG. 13.3
A 741 op-amp used as a comparator.

Since the reference voltage is connected to the inverting input, the output will switch to its positive saturation level when the input V_i goes more positive than the +6-V reference voltage level. The output V_o then drives the LED on as an indication that the input is more positive than the reference level.

As an alternative connection, the reference voltage could be connected to the noninverting input as shown in Fig. 13.3b. With this connection, the input signal going below the reference level would cause the output to drive the LED on. The LED can thus be made to go on when the input signal goes above or below the reference level, depending on which input is connected as signal input and which as reference input.

Using Comparator IC Units

Although op-amps can be used as comparator circuits, separate IC comparator units are more suitable. Some of the improvements built into a comparator IC are faster switching between the two output levels, built-in noise immunity to prevent the output from oscillating when the input passes by the reference level, and outputs capable of directly driving a variety of loads. A few popular IC comparators are covered next, describing their pin connections and how they may be used.

311 Comparator The 311 voltage comparator shown in Fig. 13.4 contains a comparator circuit that can operate as well from dual power supplies of ±15 V as from a single +5-V supply (as used in digital logic circuits). The output can provide a voltage at one of two distinct levels or can be used to drive a lamp or a relay. Notice that the output is taken from a bipolar transistor to allow driving a variety of loads. The unit also has balance and strobe inputs, the strobe input allowing gating of the output. A few examples will show how this comparator unit can be used in some common applications.

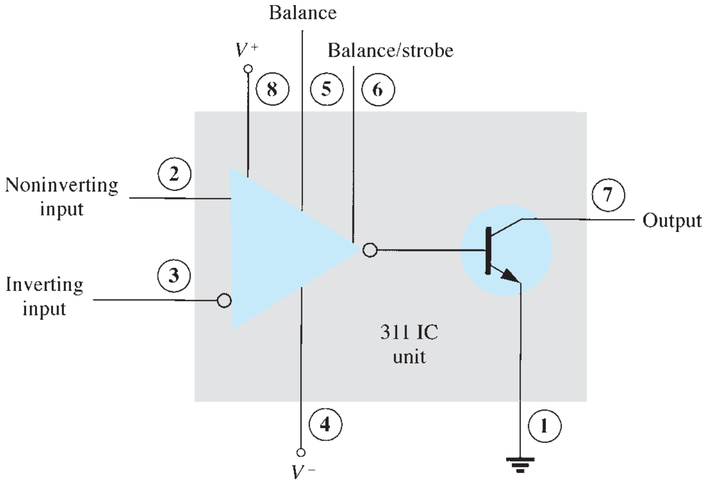


FIG. 13.4

A 311 comparator (eight-pin DIP unit).

A zero-crossing detector that senses (detects) the input voltage crossing through 0 V is shown using the 311 IC in Fig. 13.5. The inverting input is connected to ground (the reference voltage). The input signal going positive drives the output transistor on, with the output then going low (−10 V in this case). The input signal going negative (below 0 V) will drive the output transistor off, the output then going high (to +10 V). The output is thus an indication of whether the input is above or below 0 V. When the input is any positive voltage, the output is low, whereas any negative voltage will result in the output going to a high voltage level.

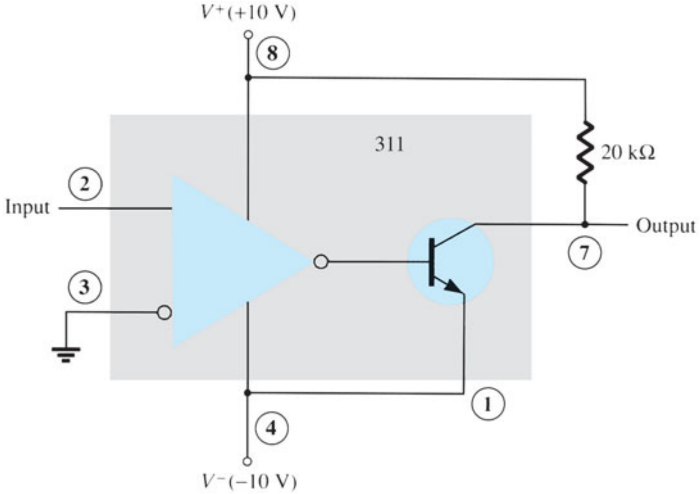


FIG. 13.5

Zero-crossing detector using a 311 IC.

Figure 13.6 shows how a 311 comparator can be used with strobing. In this example, the output will go high when the input goes above the reference level—but only if the TTL strobe input is off (or 0 V). If the TTL strobe input goes high, it drives the 311 strobe input at pin 6 low, causing the output to remain in the "off" state (with output high) regardless of the input signal. In effect, the output remains high unless strobed. If strobed, the output then acts normally, switching from high to low depending on the input signal level. In operation, the comparator output will respond to the input signal only during the time the strobe signal allows such operation.

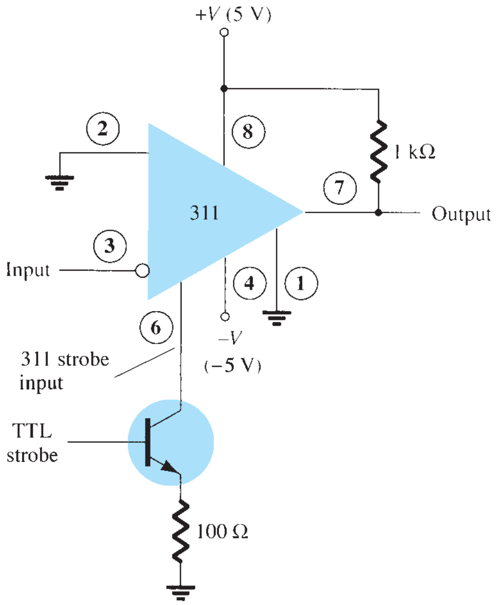


FIG. 13.6
Operation of a 311 comparator with strobe input.

Figure 13.7 shows the comparator output driving a relay. When the input goes below 0 V, driving the output low, the relay is activated, closing the normally open (N.O.) contacts at that time. These contacts can then be connected to operate a large variety of devices. For example, a buzzer or a bell wired to the contacts can be driven on whenever the input voltage drops below 0 V. As long as the voltage is present at the input terminal, the buzzer will remain off.

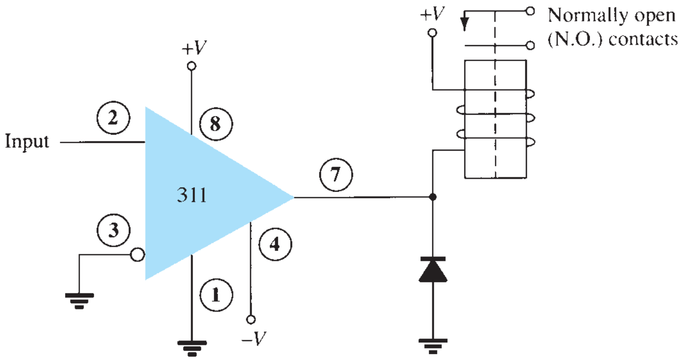


FIG. 13.7
Operation of a 311 comparator with relay output.

339 Comparator The 339 IC is a quad comparator containing four independent voltage comparator circuits connected to external pins as shown in Fig. 13.8. Each comparator has inverting and noninverting inputs and a single output. The supply voltage applied to a pair of pins powers all four comparators. Even if one wishes to use one comparator, all four will be drawing power.

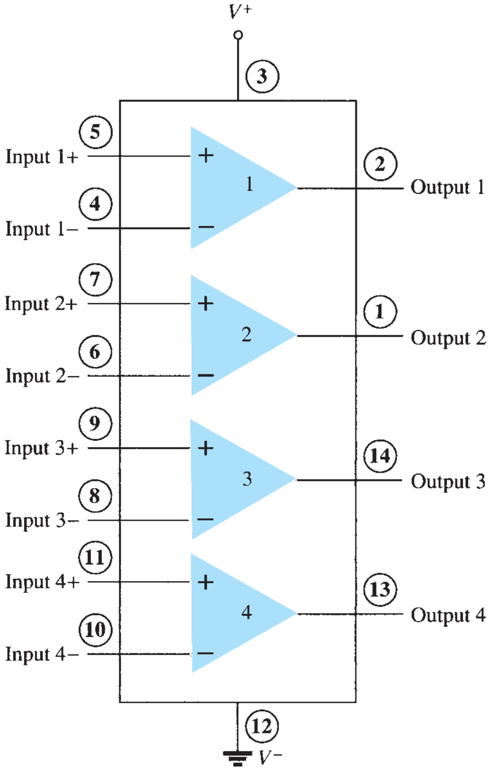

V+
3
5
Input 1+
4
Input 1−
1
2
Output 1
7
Input 2+
6
Input 2−
2
1
Output 2
9
Input 3+
8
Input 3−
3
14
Output 3
11
Input 4+
10
Input 4−
4
13
Output 4
12
V−

FIG. 13.8
Quad comparator IC (339).

To see how these comparator circuits can be used, Fig. 13.9 shows one of the 339 comparator circuits connected as a zero-crossing detector. Whenever the input signal goes above 0 V, the output switches to V^+. The input switches to V^- only when the input goes below 0 V. The circled numbers show the IC pins.

A reference level other than 0 V can also be used, and either input terminal could be used as the reference, the other terminal then being connected to the input signal. The operation of one of the comparator circuits is described next.

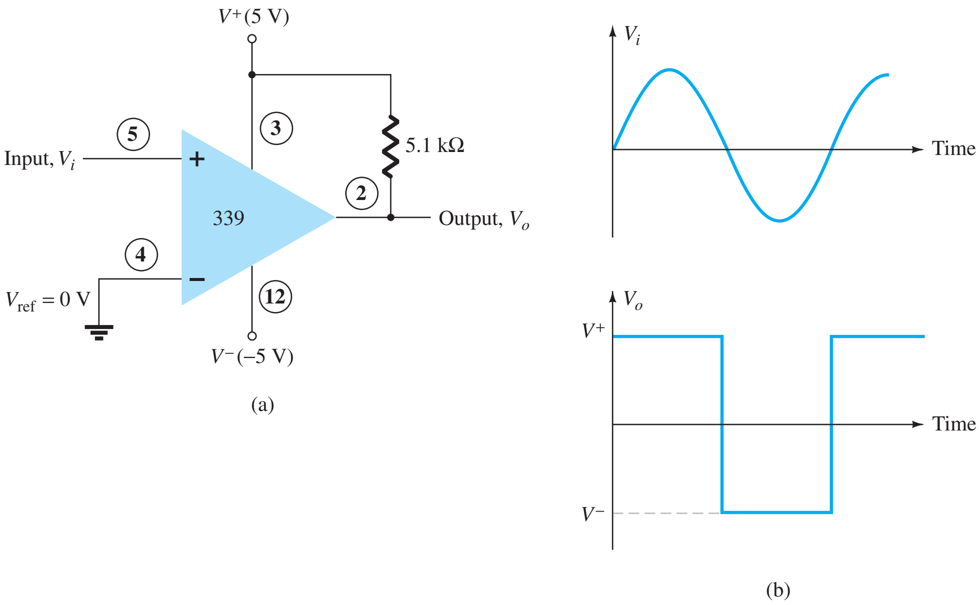
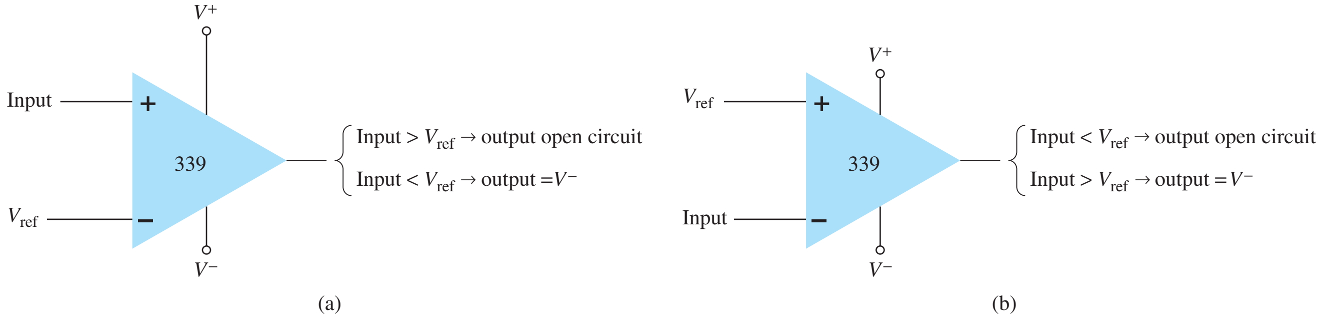

V+(5 V)
3
5.1 kΩ
5
Input, V_i
339
2
Output, V_o
4
V_{ref} = 0 V
12
V−(−5 V)
(a)
V_i
Time
V_o
V+
Time
V−
(b)

FIG. 13.9
Operation of one 339 comparator circuit as a zero-crossing detector.

The differential input voltage (difference voltage across input terminals) going positive drives the output transistor off (open circuit), whereas a negative differential input voltage drives the output transistor on—the output is then at the supply low level.

If the negative input is set at a reference level V_{ref}, and if the positive input goes above V_{ref}, this results in a positive differential input with output driven to the open-circuit state. When the noninverting input goes below V_{ref}, resulting in a negative differential input, the output will be driven to V^-.

If the positive input is set at the reference level, the inverting input going below V_{ref} results in the output open circuit, whereas the inverting input going above V_{ref} results in the output at V^-. This operation is summarized in Fig. 13.10.


V^+
Input
+
339
V_{ref}
−
V^-
Input > V_{ref} → output open circuit
Input < V_{ref} → output = V^-
V^+
V_{ref}
+
339
Input
−
V^-
Input < V_{ref} → output open circuit
Input > V_{ref} → output = V^-

(a) (b)

FIG. 13.10

Operation of a 339 comparator circuit with reference input: (a) minus input; (b) plus input.

Since the output of one of these comparator circuits is from an open-circuit collector, applications in which the outputs from more than one circuit can be wire-ORed are possible. Figure 13.11 shows two comparator circuits connected with common output and also with common input. Comparator 1 has a +5-V reference voltage input connected to the

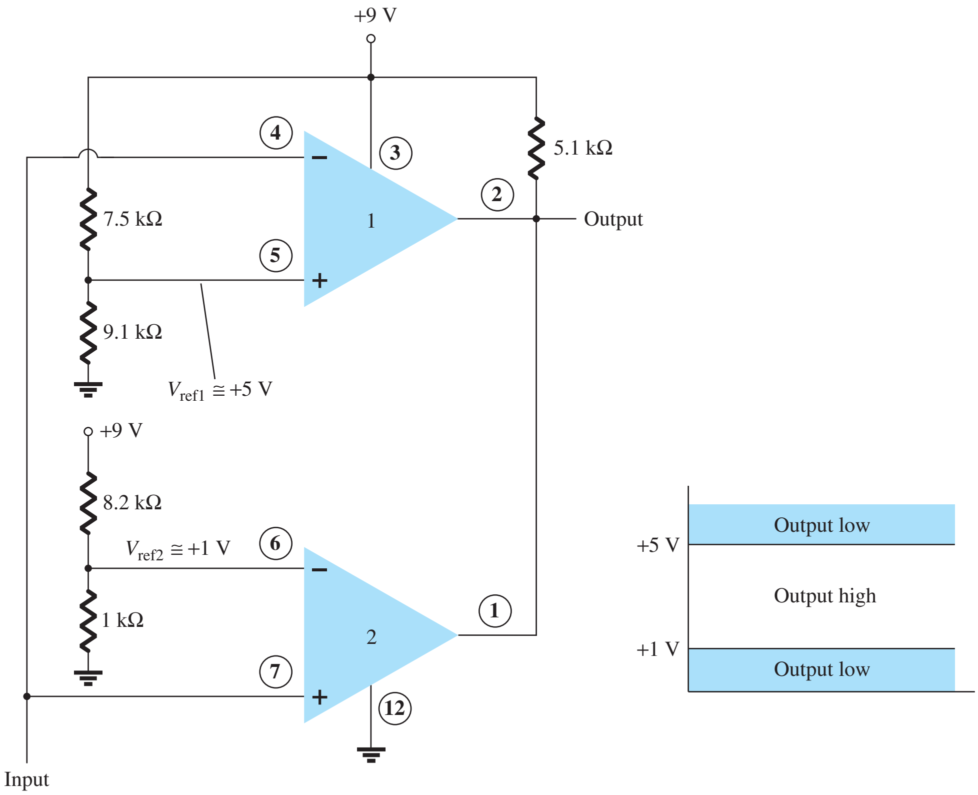

+9 V
④
③
5.1 kΩ
−
②
7.5 kΩ
1
Output
⑤
+
9.1 kΩ
$V_{\text{ref1}} \cong +5$ V
+9 V
8.2 kΩ
$V_{\text{ref2}} \cong +1$ V
⑥
−
1 kΩ
2
①
⑦
+
⑫
Input
+5 V
+1 V
Output low
Output high
Output low

FIG. 13.11

Operation of two 339 comparator circuits as a window detector.

noninverting input. The output will be driven low by comparator 1 when the input signal goes above +5 V. Comparator 2 has a reference voltage of +1 V connected to the inverting input. The output of comparator 2 will be driven low when the input signal goes below +1 V. In total, the output will go low whenever the input is below +1 V or above +5 V, as shown in Fig. 13.11, the overall operation being that of a voltage window detector. The high output indicates that the input is within a voltage window of +1 to +5 V (these values being set by the reference voltage levels used).

13.3 DIGITAL–ANALOG CONVERTERS

Many voltages and currents in electronics vary continuously over some range of values. In digital circuitry the signals are at either one of two levels, representing the binary values of 1 or 0. An analog–digital converter (ADC) obtains a digital value representing an input analog voltage, whereas a digital–analog converter (DAC) changes a digital value back into an analog voltage.

Digital-to-Analog Conversion

Ladder Network Conversion Digital-to-analog conversion can be achieved using a number of different methods. One popular scheme uses a network of resistors called a *ladder network.* A ladder network accepts inputs of binary values at, typically, 0 V or V_{ref} and provides an output voltage proportional to the binary input value. Figure 13.12a shows a ladder network with four input voltages, representing 4 bits of digital data and a dc voltage output. The output voltage is proportional to the digital input value as given by the relation

$$\boxed{V_o = \frac{D_0 \times 2^0 + D_1 \times 2^1 \times D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{\text{ref}}} \qquad \textbf{(13.1)}$$

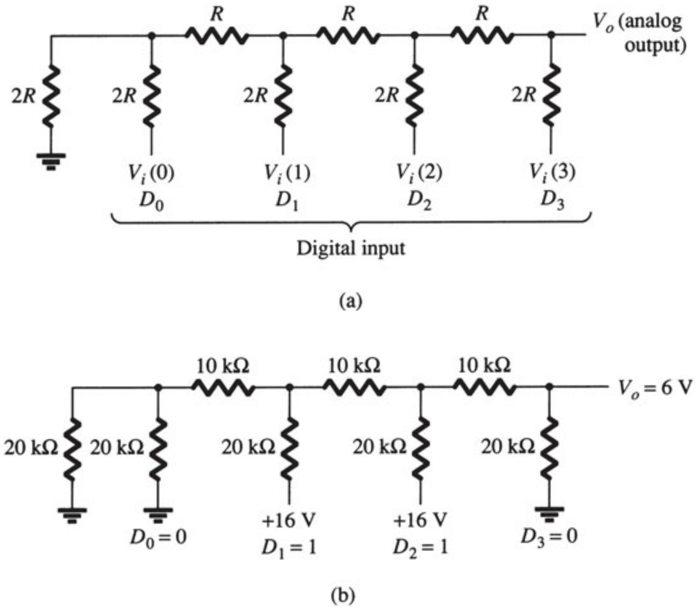


FIG. 13.12

Four-stage ladder network used as a DAC: (a) basic circuit; (b) circuit example with 0110 input.

In the example shown in Fig. 13.12b, the resulting output voltage is

$$V_o = \frac{0 \times 1 + 1 \times 2 + 1 \times 4 + 0 \times 8}{16}(16\text{ V}) = 6\text{ V}$$

Therefore, 0110_2 digital converts to 6 V analog.

The function of the ladder network is to convert the 16 possible binary values from 0000 to 1111 into one of 16 voltage levels in steps of $V_{\text{ref}}/16$. Using more sections of the ladder allows us to have more binary inputs and a greater quantization for each step. For example, a 10-stage ladder network could extend the number of voltage steps or the voltage resolution to $V_{\text{ref}}/2^{10}$, or $V_{\text{ref}}/1024$. A reference voltage of $V_{\text{ref}} = 10\text{ V}$ would then provide output voltage steps of 10 V/1024, or approximately 10 mV. More ladder stages provide greater voltage resolution. In general, the voltage resolution for n ladder stages is

$$\boxed{\frac{V_{\text{ref}}}{2^n}} \tag{13.2}$$

Figure 13.13 shows a block diagram of a typical DAC using a ladder network. The ladder network, referred to in the diagram as an *R-2R ladder*, is sandwiched between the reference current supply and current switches connected to each binary input, the resulting output current being proportional to the input binary value. The binary input turns on selected legs of the ladder, the output current being a weighted summing of the reference current. Connecting the output current through a resistor will produce an analog voltage if desired.

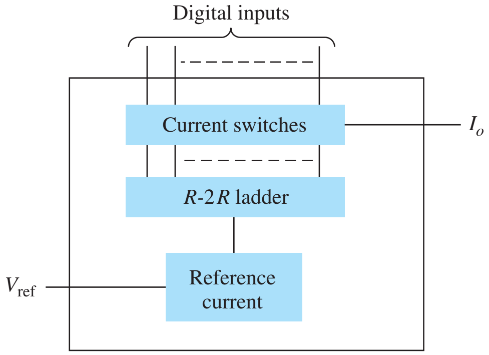


FIG. 13.13
DAC IC using R-2R ladder network.

Analog-to-Digital Conversion

Dual-Slope Conversion A popular method for converting an analog voltage into a digital value is the dual-slope method. Figure 13.14a shows a block diagram of the basic dual-slope converter. The analog voltage to be converted is applied through an electronic switch to an integrator or ramp-generator circuit (essentially a constant current charging a capacitor to produce a linear ramp voltage). The digital output is obtained from a counter operated during both positive and negative slope intervals of the integrator.

The method of conversion proceeds as follows. For a fixed time interval (usually the full count range of the counter), the analog voltage connected to the integrator raises the voltage at the comparator input to some positive level. Figure 13.14b shows that at the end of the fixed time interval the voltage from the integrator is greater for the larger input voltage. At the end of the fixed count interval, the count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage. The integrator output (or capacitor input) then decreases at a fixed rate. The counter advances during this time, whereas the integrator's output decreases at a fixed rate until it drops below the comparator reference voltage, at which time the control logic receives a signal (the comparator output) to stop the count. The digital value stored in the counter is then the digital output of the converter.

Using the same clock and integrator to perform the conversion during positive and negative slope intervals tends to compensate for clock frequency drift and integrator accuracy limitations. Setting the reference input value and clock rate can scale the counter output as desired. The counter can be a binary, BCD, or other form of digital counter, if desired.

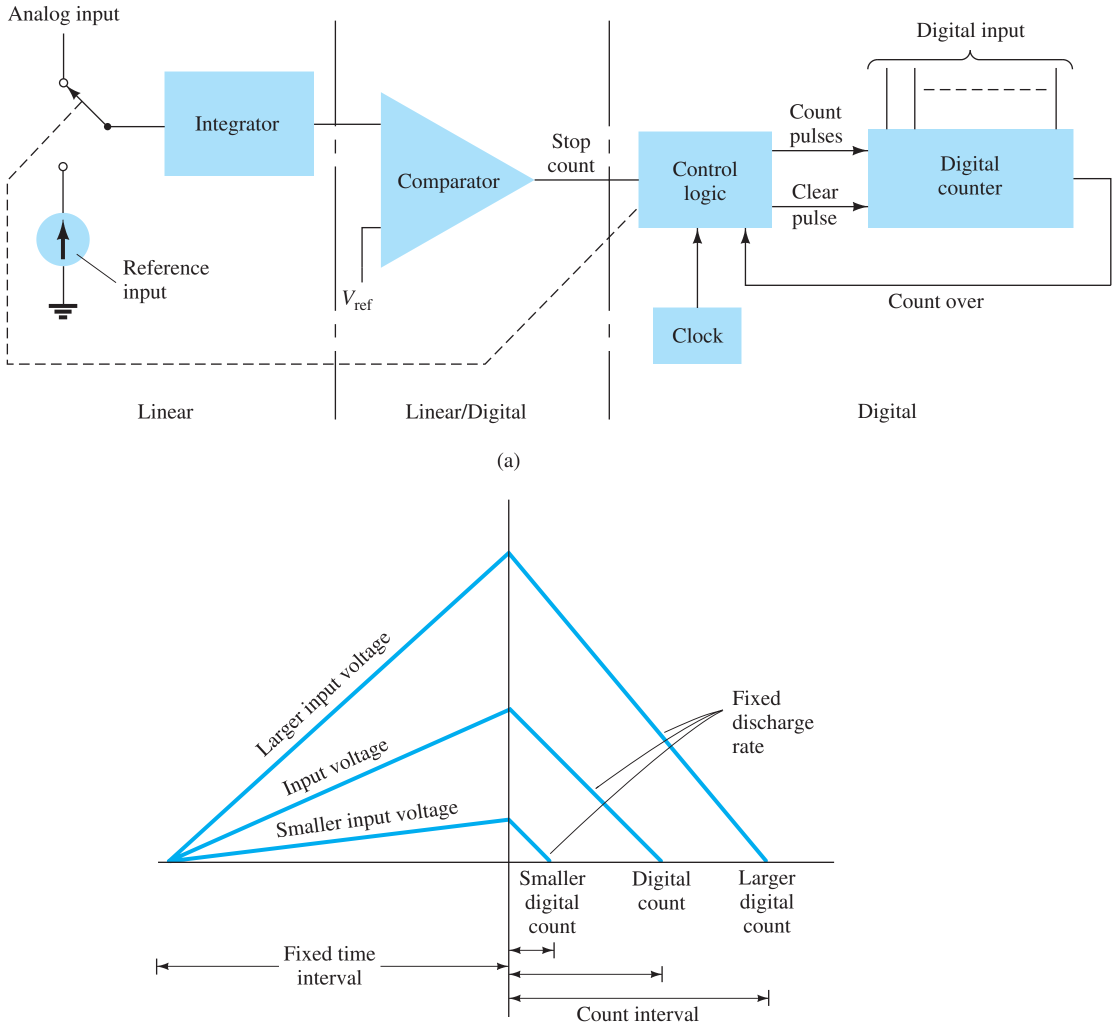

Analog input
Integrator
Reference input
Comparator
V_{ref}
Stop count
Control logic
Clock
Count pulses
Clear pulse
Digital input
Digital counter
Count over
Linear
Linear/Digital
Digital
(a)
Larger input voltage
Input voltage
Smaller input voltage
Fixed discharge rate
Smaller digital count
Digital count
Larger digital count
Fixed time interval
Count interval
(b)

FIG. 13.14

Analog-to-digital conversion using dual-slope method: (a) logic diagram; (b) waveform.

Ladder-Network Conversion Another popular method of analog-to-digital conversion uses a ladder network along with counter and comparator circuits (see Fig. 13.15). A digital counter advances from a zero count while a ladder network driven by the counter outputs a staircase voltage, as shown in Fig. 13.15b, which increases one voltage increment for each count step. A comparator circuit, receiving both staircase voltage and analog input voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage. The counter value at that time is the digital output.

The amount of voltage change stepped by the staircase signal depends on the number of count bits used. A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V steps each count by a voltage of

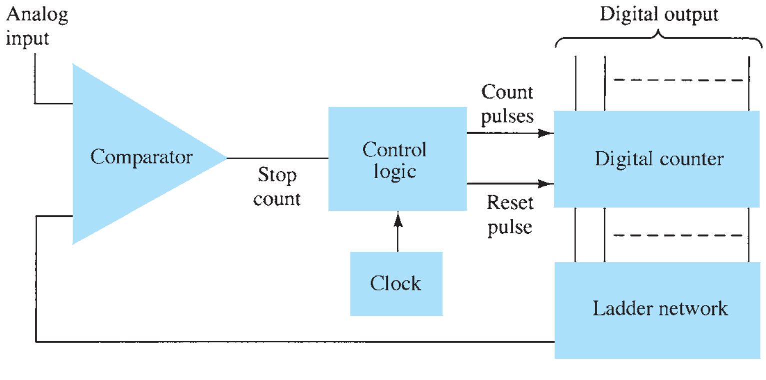
$$\frac{V_{\text{ref}}}{2^{12}} = \frac{10\text{ V}}{4096} = 2.4\text{ mV}$$

This results in a conversion resolution of 2.4 mV. The clock rate of the counter affects the time required to carry out a conversion. A clock rate of 1 MHz operating a 12-stage counter needs a maximum conversion time of

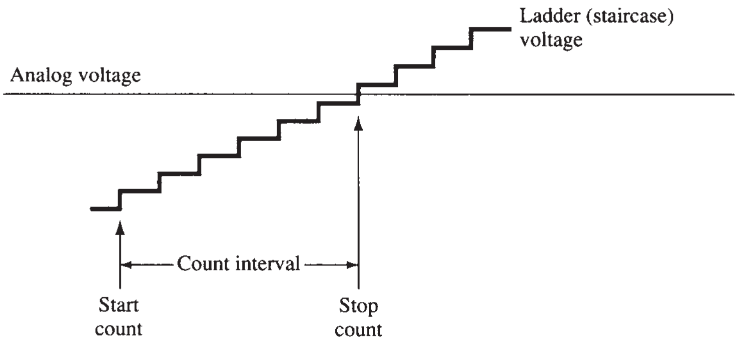
$$4096 \times 1\ \mu\text{s} = 4096\ \mu\text{s} \approx 4.1\text{ ms}$$

The minimum number of conversions that could be carried out each second is then

$$\text{number of conversions} = 1/4.1\text{ ms} \approx 244\text{ conversions/second}$$


Analog input
Comparator
Stop count
Control logic
Clock
Count pulses
Reset pulse
Digital output
Digital counter
Ladder network

(a)


Ladder (staircase) voltage
Analog voltage
Count interval
Start count
Stop count

(b)

FIG. 13.15

Analog-to-digital conversion using ladder network: (a) logic diagram; (b) waveform.

Since on the average, with some conversions requiring little count time and others near-maximum count time, a conversion time of 4.1 ms/2 = 2.05 ms is needed, and the average number of conversions is 2 × 244 = 488 conversions/second. A slower clock rate would result in fewer conversions per second. A converter using fewer count stages (and less conversion resolution) would carry out more conversions per second. The conversion accuracy depends on the accuracy of the comparator.

13.4 TIMER IC UNIT OPERATION

Another popular analog–digital integrated circuit is the versatile 555 timer. The IC is made of a combination of linear comparators and digital flip-flops as described in Fig. 13.16. The entire circuit is usually housed in an eight-pin package as specified in Fig. 13.16. A series connection of three resistors sets the reference voltage levels to the two comparators at $2V_{CC}/3$ and $V_{CC}/3$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output amplifier stage. The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor.

Astable Operation

One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. The following analysis of the operation of the 555 as an astable circuit includes details of the different parts of the unit and how the various inputs and outputs are used. Figure 13.17 shows an astable circuit built using an external resistor and capacitor to set the timing interval of the output signal.

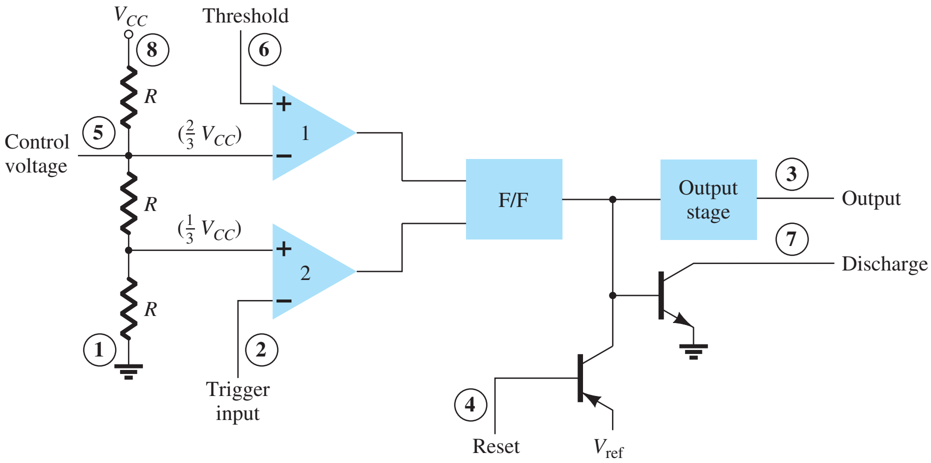

V_{CC}
8
Threshold
6
R
Control voltage
5
$(\frac{2}{3}V_{CC})$
+
1
−
R
$(\frac{1}{3}V_{CC})$
+
2
−
R
1
2
Trigger input
F/F
Output stage
3
Output
7
Discharge
4
Reset
V_{ref}

FIG. 13.16
Details of 555 timer IC.

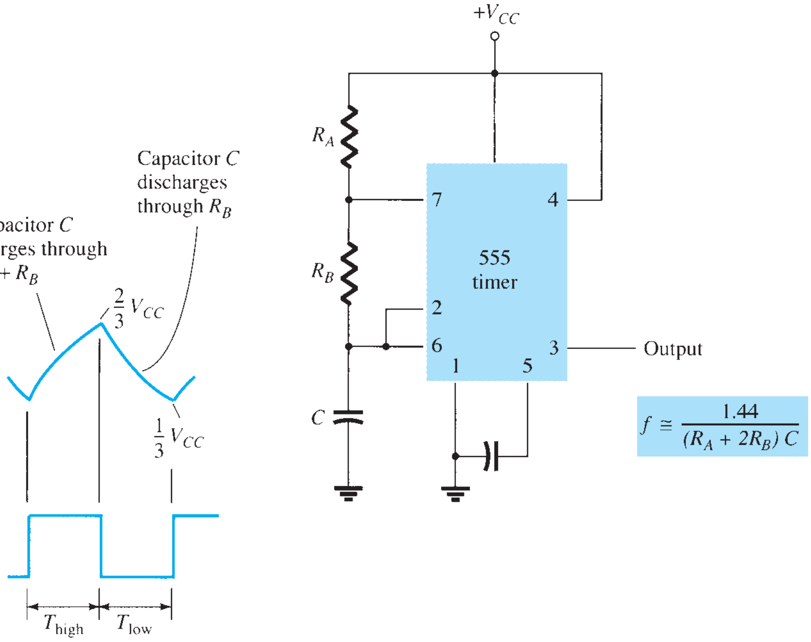

$+V_{CC}$
R_A
R_B
C
7
4
555 timer
2
6
3
1
5
Output
$f \cong \frac{1.44}{(R_A + 2R_B)C}$
Capacitor C discharges through R_B
Capacitor C charges through $R_A + R_B$
$\frac{2}{3}V_{CC}$
$\frac{1}{3}V_{CC}$
T_{high}
T_{low}

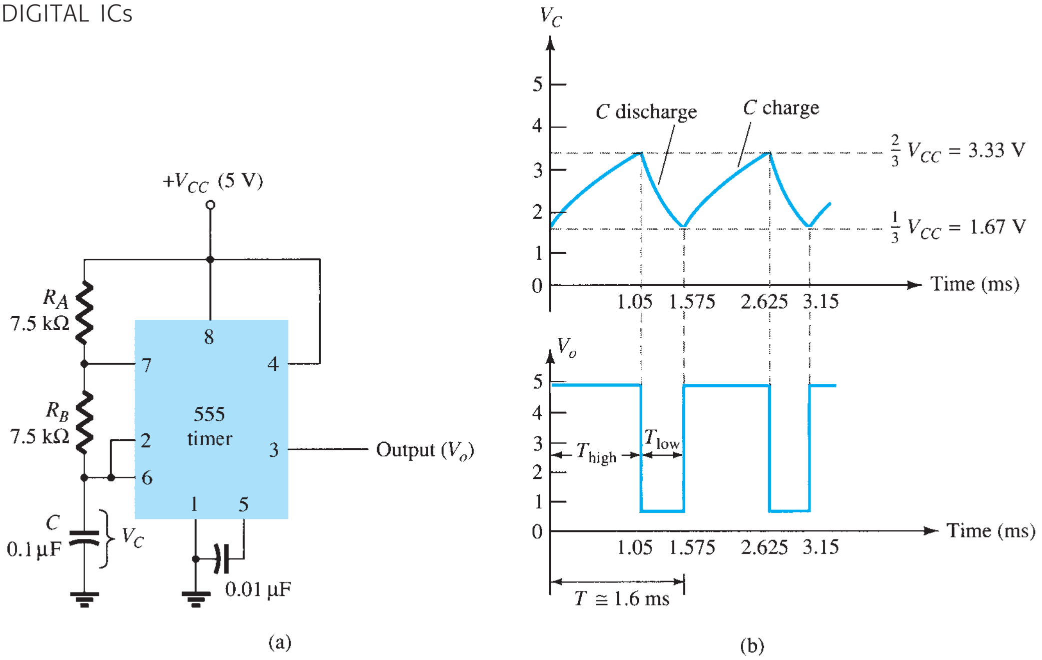
FIG. 13.17
Astable multivibrator using 555 IC.

Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to Fig. 13.17, we see that the capacitor voltage rises until it goes above $2V_{CC}/3$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level ($V_{CC}/3$). The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B toward V_{CC}.

Figure 13.18a shows the capacitor and output waveforms resulting from the astable circuit. Calculation of the time intervals during which the output is high and low can be made using the relations

$$\boxed{T_{high} \approx 0.7(R_A + R_B)C} \tag{13.3}$$

$$\boxed{T_{low} \approx 0.7R_BC} \tag{13.4}$$



+VCC (5 V)
RA 7.5 kΩ
RB 7.5 kΩ
C 0.1 µF
VC
8
7
4
2
6
3
1
5
555 timer
Output (Vo)
0.01 µF
(a)
VC
C discharge
C charge
2/3 VCC = 3.33 V
1/3 VCC = 1.67 V
Time (ms)
1.05
1.575
2.625
3.15
Vo
Thigh
Tlow
T ≅ 1.6 ms
0
1
2
3
4
5
(b)

FIG. 13.18

Astable multivibrator for Example 13.1: (a) circuit; (b) waveforms.

The total period is

$$T = \text{period} = T_{\text{high}} + T_{\text{low}} \tag{13.5}$$

The frequency of the astable circuit is then calculated using*

$$\boxed{f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B)C}} \tag{13.6}$$

EXAMPLE 13.1 Determine the frequency and draw the output waveform for the circuit of Fig. 13.18a.

Solution: Using Eqs. (13.3) through (13.6) yields

$$\begin{aligned} T_{\text{high}} &= 0.7(R_A + R_B)C = 0.7(7.5 \times 10^3 + 7.5 \times 10^3)(0.1 \times 10^{-6}) \\ &= 1.05 \text{ ms} \\ T_{\text{low}} &= 0.7R_BC = 0.7(7.5 \times 10^3)(0.1 \times 10^{-6}) = 0.525 \text{ ms} \\ T &= T_{\text{high}} + T_{\text{low}} = 1.05 \text{ ms} + 0.525 \text{ ms} = 1.575 \text{ ms} \\ f &= \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} \approx \mathbf{635\ Hz} \end{aligned}$$

The waveforms are drawn in Fig. 13.18b.

---

*The period can be directly calculated from

$$T = 0.693(R_A + 2R_B)C \approx 0.7(R_A + 2R_B)C$$

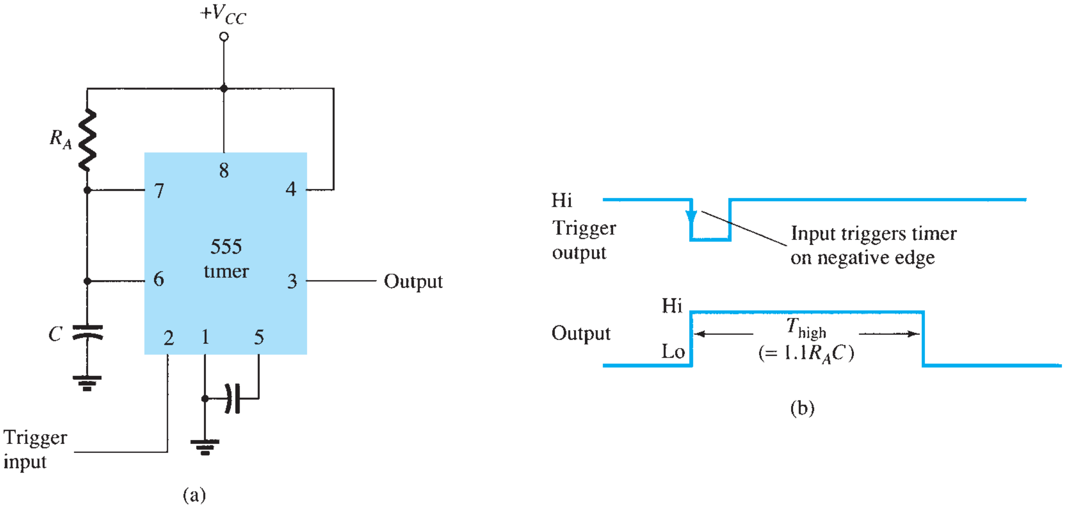
and the frequency from

$$f \approx \frac{1.44}{(R_A + 2R_B)C}$$

Monostable Operation

The 555 timer can also be used as a one-shot or monostable multivibrator circuit, as shown in Fig. 13.19. When the trigger input signal goes negative, it triggers the one-shot, with output at pin 3 then going high for a time period given by

$$T_{\text{high}} = 1.1R_AC \tag{13.7}$$



+V_{CC}
R_A
8
7
4
555
timer
6
3
Output
C
2
1
5
Trigger
input
(a)
Hi
Trigger
output
Input triggers timer
on negative edge
Hi
Output
Lo
T_{high}
(= 1.1R_AC)
(b)

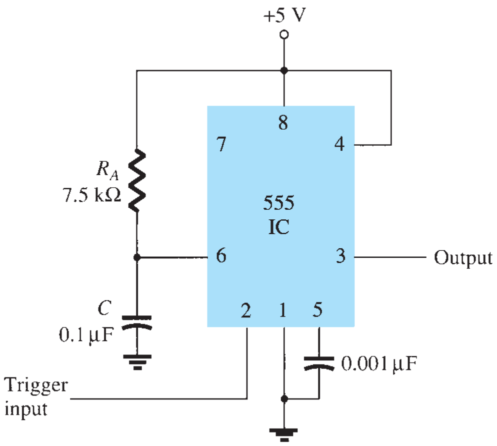
FIG. 13.19

Operation of 555 timer as a one-shot: (a) circuit; (b) waveforms.

Referring back to Fig. 13.16, we see that the negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high. Capacitor C charges toward V_{CC} through resistor R_A. During the charge interval, the output remains high. When the voltage across the capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers the flip-flop, with output going low. The discharge transistor also goes low, causing the capacitor to remain at near 0 V until triggered again.

Figure 13.19b shows the input trigger signal and the resulting output waveform for the 555 timer operated as a one-shot. Time periods for this circuit can range from microseconds to many seconds, making this IC useful for a range of applications.

EXAMPLE 13.2 Determine the period of the output waveform for the circuit of Fig. 13.20 when triggered by a negative pulse.



+5 V
8
7
4
R_A
7.5 kΩ
555
IC
6
3
Output
C
0.1 μF
2
1
5
0.001 μF
Trigger
input

FIG. 13.20

Monostable circuit for Example 13.2.

Solution: Using Eq. (13.7), we obtain

$$T_{\text{high}} = 1.1R_AC = 1.1(7.5 \times 10^3)(0.1 \times 10^{-6}) = \mathbf{0.825\ ms}$$

13.5 VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage. An example of a VCO is the 566 IC unit, which contains circuitry to generate both square-wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage. Figure 13.21a shows that the 566 contains current sources to charge and discharge an external capacitor C_1 at a rate set by external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is used to switch the current sources between charging and discharging the capacitor, and the triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers.

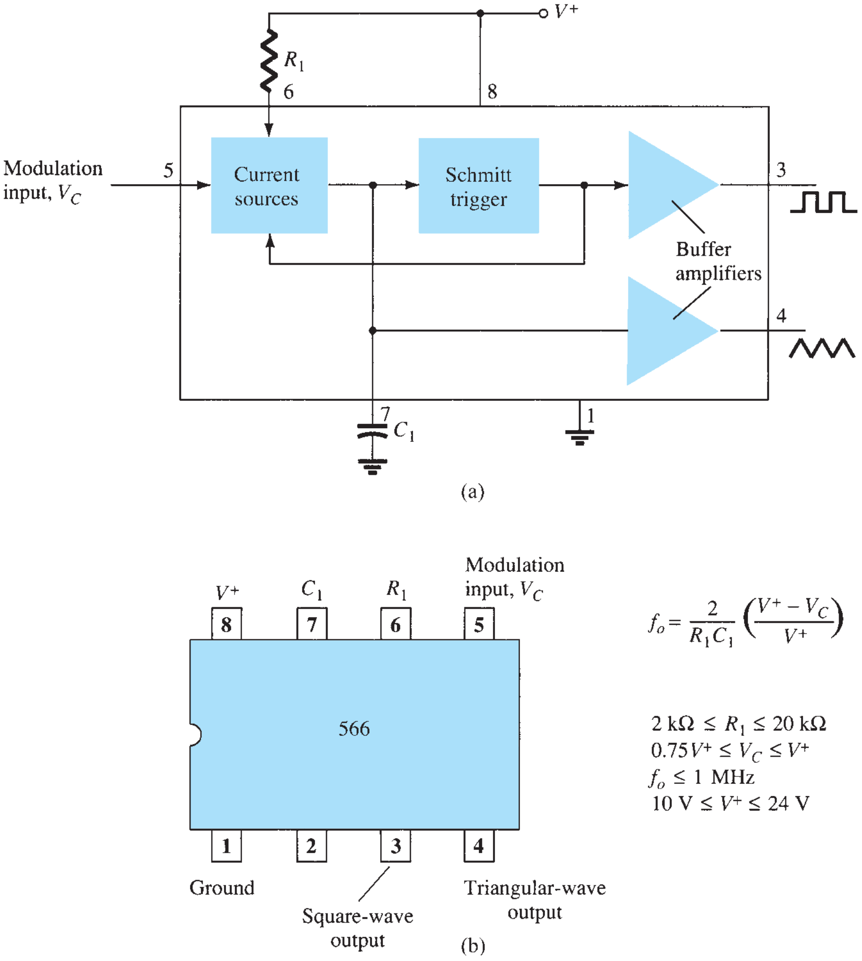

V+
R1
6
8
Modulation input, VC
5
Current sources
Schmitt trigger
3
Buffer amplifiers
4
7
C1
1
(a)
V+
C1
R1
Modulation input, VC
8
7
6
5
566
1
2
3
4
Ground
Square-wave output
Triangular-wave output
(b)
fo = 2/(R1C1) ((V+ − VC)/V+)
2 kΩ ≤ R1 ≤ 20 kΩ
0.75V+ ≤ VC ≤ V+
fo ≤ 1 MHz
10 V ≤ V+ ≤ 24 V

FIG. 13.21

A 566 function generator: (a) block diagram; (b) pin configuration and summary of operating data.

Figure 13.21b shows the pin connection of the 566 unit and a summary of formula and value limitations. The oscillator can be programmed over a 10-to-1 frequency range by proper selection of an external resistor and capacitor, and then modulated over a 10-to-1 frequency range by a control voltage V_C.

A free-running or center-operating frequency f_o can be calculated from

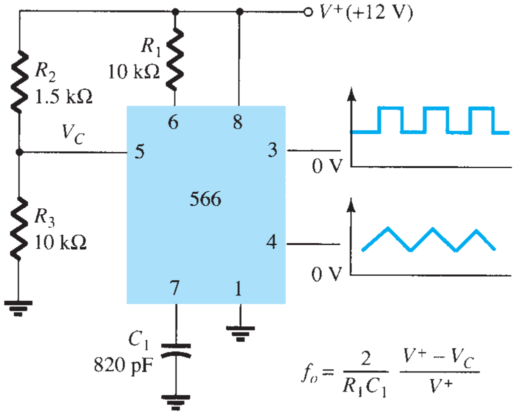
$$\boxed{f_o = \frac{2}{R_1C_1}\left(\frac{V^+ - V_C}{V^+}\right)} \qquad \textbf{(13.8)}$$

with the following practical circuit value restrictions:

1. R_1 should be within the range $2\,\text{k}\Omega \leq R_1 \leq 20\,\text{k}\Omega$.
2. V_C should be within the range $\frac{3}{4}V^+ \leq V_C \leq V^+$.
3. f_o should be below 1 MHz.
4. V^+ should range between 10 V and 24 V.

Figure 13.22 shows an example in which the 566 function generator is used to provide both square-wave and triangular-wave signals at a fixed frequency set by R_1, C_1, and V_C. A resistor divider R_2 and R_3 sets the dc modulating voltage at a fixed value

$$V_C = \frac{R_3}{R_2 + R_3}V^+ = \frac{10\,\text{k}\Omega}{1.5\,\text{k}\Omega + 10\,\text{k}\Omega}(12\text{ V}) = 10.4\text{ V}$$



V^+(+12 V)
R_1
10 kΩ
R_2
1.5 kΩ
V_C
6
8
5
3
0 V
566
R_3
10 kΩ
4
0 V
7
1
C_1
820 pF
$f_o = \frac{2}{R_1C_1}\frac{V^+ - V_C}{V^+}$

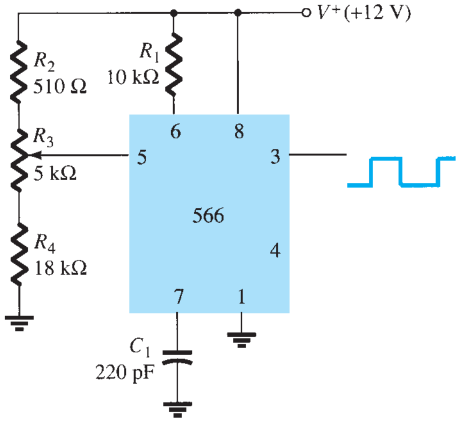
FIG. 13.22

Connection of a 566 VCO unit.

(which falls properly in the voltage range $0.75V^+ = 9$ V and $V^+ = 12$ V). Using Eq. (13.8) yields

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})}\left(\frac{12 - 10.4}{12}\right) \approx 32.5\text{ kHz}$$

The circuit of Fig. 13.23 shows how the output square-wave frequency can be adjusted using the input voltage V_C to vary the signal frequency. Potentiometer R_3 allows varying V_C



V^+(+12 V)
R_1
10 kΩ
R_2
510 Ω
R_3
5 kΩ
6
8
5
3
566
R_4
18 kΩ
4
7
1
C_1
220 pF

FIG. 13.23

Connection of a 566 as a VCO unit.

from about 9 V to near 12 V, over the full 10-to-1 frequency range. With the potentiometer wiper set at the top, the control voltage is

$$V_C = \frac{R_3 + R_4}{R_2 + R_3 + R_4}(V^+) = \frac{5\text{ k}\Omega + 18\text{ k}\Omega}{510\ \Omega + 5\text{ k}\Omega + 18\text{ k}\Omega}(+12\text{ V}) = 11.74\text{ V}$$

resulting in a lower output frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 11.74}{12}\right) \approx 19.7\text{ kHz}$$

With the wiper arm of R_3 set at the bottom, the control voltage is

$$V_C = \frac{R_4}{R_2 + R_3 + R_4}(V^+) = \frac{18\text{ k}\Omega}{510\ \Omega + 5\text{ k}\Omega + 18\text{ k}\Omega}(+12\text{ V}) = 9.19\text{ V}$$

resulting in an upper frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 9.19}{12}\right) \approx 212.9\text{ kHz}$$

The frequency of the output square wave can then be varied using potentiometer R_3 over a frequency range of at least 10 to 1.

Rather than varying a potentiometer setting to change the value of V_C, an input modulating voltage V_{in} can be applied as shown in Fig. 13.24. The voltage divider sets V_C at about 10.4 V. An input ac voltage of about 1.4 V peak can drive V_C around the bias point between voltages of 9 V and 11.8 V, causing the output frequency to vary over about a 10-to-1 range. The input signal V_{in} thus frequency-modulates the output voltage around the center frequency set by the bias value of $V_C = 10.4$ V ($f_o = 121.2$ kHz).

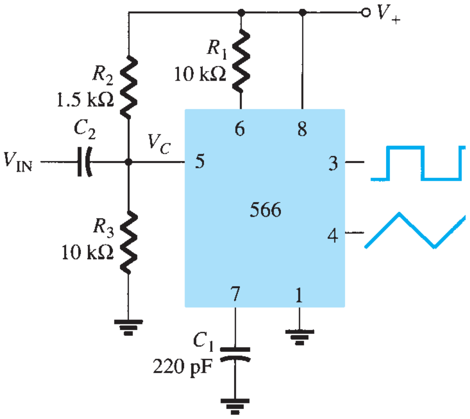


FIG. 13.24

Operation of a VCO with frequency-modulating input.

13.6 PHASE-LOCKED LOOP

A phase-locked loop (PLL) is an electronic circuit that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator connected as shown in Fig. 13.25. Common applications of a PLL include (1) frequency synthesizers that provide multiples of a reference signal frequency [e.g., the carrier frequency for the multiple channels of a citizens band (CB) unit or marine-radio-band unit can be generated using a single-crystal-controlled frequency and its multiples generated using a PLL], (2) FM demodulation networks for FM operation with excellent linearity between the input signal frequency and the PLL output voltage, (3) demodulation of the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (FSK) operation, and (4) a wide variety of areas including modems, telemetry receivers and transmitters, tone decoders, AM detectors, and tracking filters.

An input signal V_i and that from a VCO, V_o, are compared by a phase comparator (refer to Fig. 13.25), providing an output voltage V_e that represents the phase difference between the two signals. This voltage is then fed to a low-pass filter, which provides an output voltage (amplified if necessary) that can be taken as the output voltage from the PLL and is

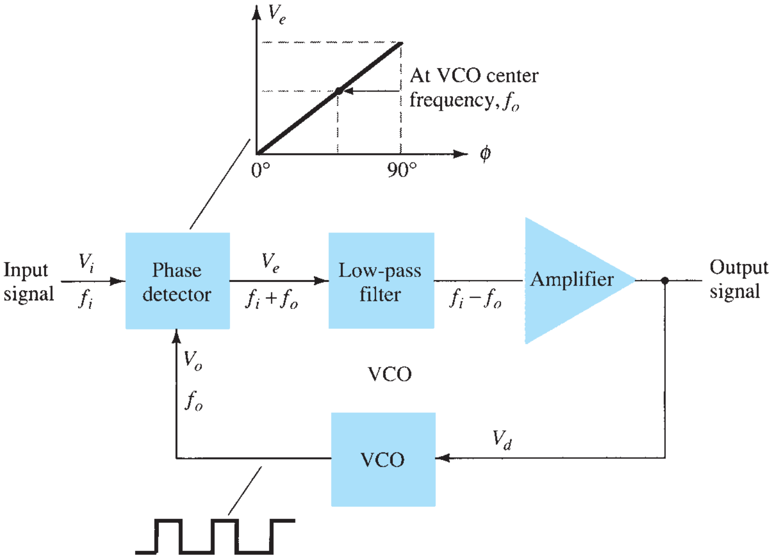


FIG. 13.25

Block diagram of basic phase-locked loop (PLL).

used internally as the voltage to modulate the VCO's frequency. The closed-loop operation of the circuit is to maintain the VCO frequency locked to that of the input signal frequency.

Basic PLL Operation

The basic operation of a PLL circuit can be explained using the circuit of Fig. 13.25 as reference. We will first consider the operation of the various circuits in the phase-locked loop when the loop is operating in lock (the input signal frequency and the VCO frequency are the same). When the input signal frequency is the same as that from the VCO to the comparator, the voltage V_d taken as output is the value needed to hold the VCO in lock with the input signal. The VCO then provides output of a fixed-amplitude square-wave signal at the frequency of the input. Best operation is obtained if the VCO center frequency f_o is set with the dc bias voltage midway in its linear operating range. The amplifier allows this adjustment in dc voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the comparator are of the same frequency, although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO. Changes in the input signal frequency then result in change in the dc voltage to the VCO. Within a capture-and-lock frequency range, the dc voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the phase comparator contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower frequency component of the signal, so that the loop can obtain lock between input and VCO signals.

Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the frequency range centered about the VCO free-running frequency f_o over which the loop can acquire lock with the input signal. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the *lock range.*

Applications

The PLL can be used in a wide variety of applications, including (1) frequency demodulation, (2) frequency synthesis, and (3) FSK decoders. Examples of each of these follow.

Frequency Demodulation FM demodulation or detection can be directly achieved using the PLL circuit. If the PLL center frequency is selected or designed at the FM carrier frequency, the filtered or output voltage of the circuit of Fig. 13.25 is the desired demodulated voltage, varying in value in proportion to the variation of the signal frequency. The PLL circuit thus operates as a complete intermediate-frequency (IF) strip, limiter, and demodulator as used in FM receivers.

One popular PLL unit is the 565, shown in Fig. 13.26a. The 565 contains a phase detector, an amplifier, and a voltage-controlled oscillator, which are only partially connected internally. An external resistor and capacitor R_1 and C_1, respectively, are used to set the free-running or center frequency of the VCO. Another external capacitor, C_2, is used to set the low-pass filter passband, and the VCO output must be connected back as input to the phase detector to close the PLL loop. The 565 typically uses two power supplies, V^+ and V^-.

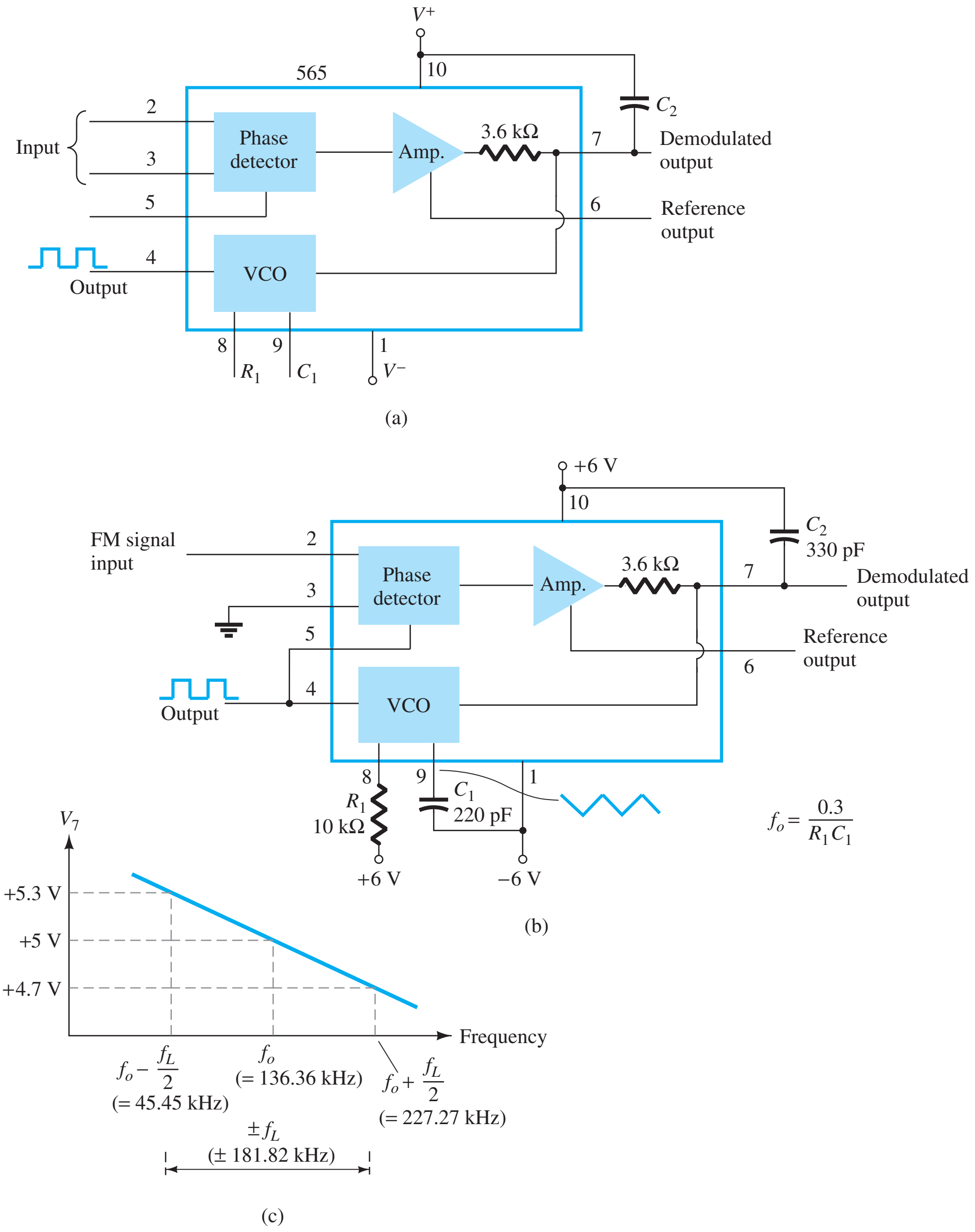

V^+
565
10
C_2
Input
2
3
5
4
Phase detector
Amp.
3.6 kΩ
7
Demodulated output
6
Reference output
VCO
Output
8
9
1
R_1
C_1
V^-
(a)
+6 V
10
C_2
330 pF
FM signal input
2
3
5
4
Phase detector
Amp.
3.6 kΩ
7
Demodulated output
Reference output
6
VCO
Output
8
9
1
R_1
10 kΩ
C_1
220 pF
+6 V
−6 V
$f_o = \frac{0.3}{R_1C_1}$
(b)
V_7
+5.3 V
+5 V
+4.7 V
Frequency
$f_o - \frac{f_L}{2}$
(= 45.45 kHz)
f_o
(= 136.36 kHz)
$f_o + \frac{f_L}{2}$
(= 227.27 kHz)
$\pm f_L$
(± 181.82 kHz)
(c)

FIG. 13.26

Phase-locked loop (PLL): (a) basic block diagram; (b) PLL connected as a frequency demodulator: (c) output voltage versus frequency plot.

Figure 13.26b shows the PLL connected to work as an FM demodulator. Resistor R_1 and capacitor C_1 set the free-running frequency f_o as follows:

$$\boxed{f_o = \frac{0.3}{R_1C_1}} \tag{13.9}$$

$$= \frac{0.3}{(10 \times 10^3)(220 \times 10^{-12})} = 136.36 \text{ kHz}$$

with limitation $2\text{ k}\Omega \leq R_1 \leq 20\text{ k}\Omega$. The lock range is

$$f_L = \pm\frac{8f_o}{V}$$

$$= \pm\frac{8(136.36 \times 10^3)}{6} = \pm 181.8\text{ kHz}$$

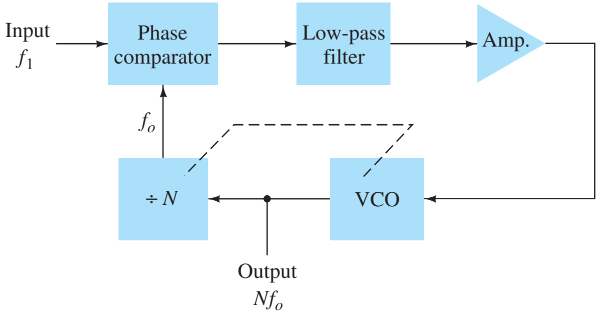
for supply voltages $V = \pm 6$ V. The capture range is

$$f_C = \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_2C_2}}$$

$$= \pm\frac{1}{2\pi}\sqrt{\frac{2\pi(181.8 \times 10^3)}{(3.6 \times 10^3)(330 \times 10^{-12})}} = 156.1\text{ kHz}$$

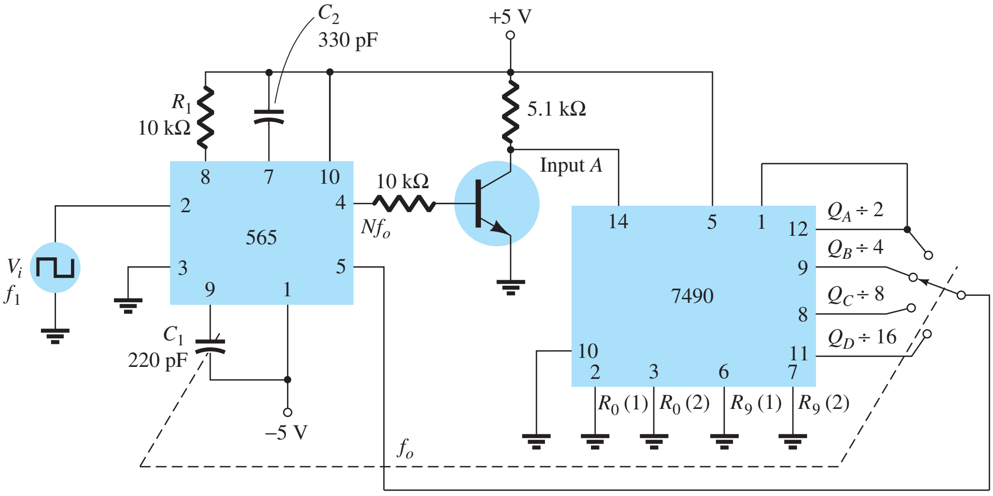
The signal at pin 4 is a 136.36-kHz square wave. An input within the lock range of 181.8 kHz will result in the output at pin 7 varying around its dc voltage level set with input signal at f_o. Figure 13.26c shows the output at pin 7 as a function of the input signal frequency. The dc voltage at pin 7 is linearly related to the input signal frequency within the frequency range $f_L = 181.8$ kHz around the center frequency 136.36 kHz. The output voltage is the demodulated signal that varies with frequency within the operating range specified.

Frequency Synthesis A frequency synthesizer can be built around a PLL as shown in Fig. 13.27. A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o and the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. The input



Input
f_1
Phase comparator
Low-pass filter
Amp.
f_o
÷ N
VCO
Output
Nf_o

(a)



C_2
330 pF
+5 V
R_1
10 kΩ
5.1 kΩ
Input A
8
7
10
10 kΩ
2
4
565
Nf_o
3
5
9
1
V_i
f_1
C_1
220 pF
–5 V
f_o
14
5
1
12
$Q_A \div 2$
$Q_B \div 4$
9
7490
$Q_C \div 8$
8
$Q_D \div 16$
10
11
2
3
6
7
R_0 (1)
R_0 (2)
R_9 (1)
R_9 (2)

(b)

FIG. 13.27

Frequency synthesizer: (a) block diagram; (b) implementation using 565 PLL unit.

signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set up to lock at the fundamental frequency (when $f_o = f_1$). Figure 13.27b shows an example using a 565 PLL as frequency multiplier and a 7490 as divider. The input V_i at frequency f_1 is compared to the input (frequency f_o) at pin 5. An output at Nf_o ($4f_o$ in the present example) is connected through an inverter circuit to provide an input at pin 14 of the 7490, which varies between 0 V and +5V. Using the output at pin 9, which is one-fourth that at the input to the 7490, we find that the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock. Since the VCO can vary over only a limited range from its center frequency, it may be necessary to change the VCO frequency whenever the divider value is changed. As long as the PLL circuit is in lock, the VCO output frequency will be exactly N times the input frequency. It is only necessary to readjust f_o to be within the capture-and-lock range, the closed loop then resulting in the VCO output becoming exactly Nf_1 at lock.

FSK Decoders An FSK (frequency-shift keyed) signal decoder can be built as shown in Fig. 13.28. The decoder receives a signal at one of two distinct carrier frequencies, 1270 Hz or 1070 Hz, representing the RS-232C logic levels or mark (−5 V) or space (+14 V), respectively. As the signal appears at the input, the loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output.

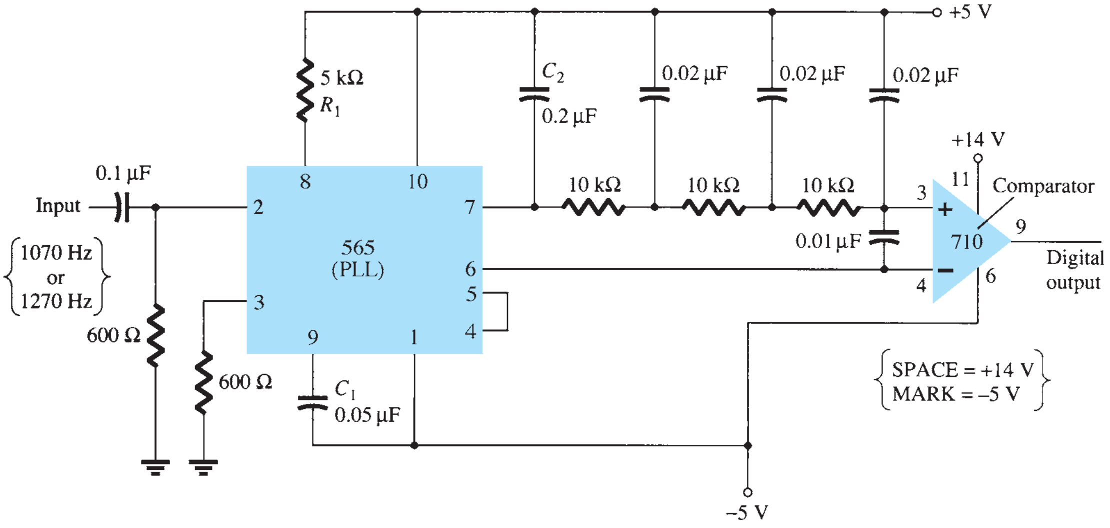


FIG. 13.28
Connection of 565 as FSK decoder.

The RC ladder filter (three sections of $C = 0.02\ \mu\text{F}$ and $R = 10\ \text{k}\Omega$) is used to remove the sum-frequency component. The free-running frequency is adjusted with R_1 so that the dc voltage level at the output (pin 7) is the same as that at pin 6. Then an input at frequency 1070 Hz will drive the decoder output voltage to a more positive voltage level, driving the digital output to the high level (space, or +14 V). An input at 1270 Hz will correspondingly drive the 565 dc output less positive with the digital output, which then drops to the low level (mark, or −5 V).

13.7 INTERFACING CIRCUITRY

Connecting different types of circuits, either in digital or analog circuits, may require some sort of interfacing circuit. An interface circuit may be used to drive a load or to obtain a signal as a receiver circuit. A driver circuit provides the output signal at a voltage or current level suitable to operate a number of loads, or to operate such devices as relays, displays, or power units. A receiver circuit essentially accepts an input signal, providing high input impedance to minimize loading of the input signal. Furthermore, the interface circuits may include strobing, which provides connecting the interface signals during specific time intervals established by the strobe.

Figure 13.29a shows a dual-line driver, each driver accepting input of TTL signals, providing output capable of driving TTL or MOS device circuits. This type of interface circuit comes in various forms, some as inverting and others as noninverting units. The circuit of Fig. 13.29b shows a dual-line receiver having both inverting and noninverting inputs so that either operating condition can be selected. As an example, connection of an input signal to the inverting input would result in an inverted output from the receiver unit. Connecting the input to the noninverting input would provide the same interfacing except that the output obtained would have the same polarity as the received signal. The driver–receiver unit of Fig. 13.29 provides an output when the strobe signal is present (high in this case).

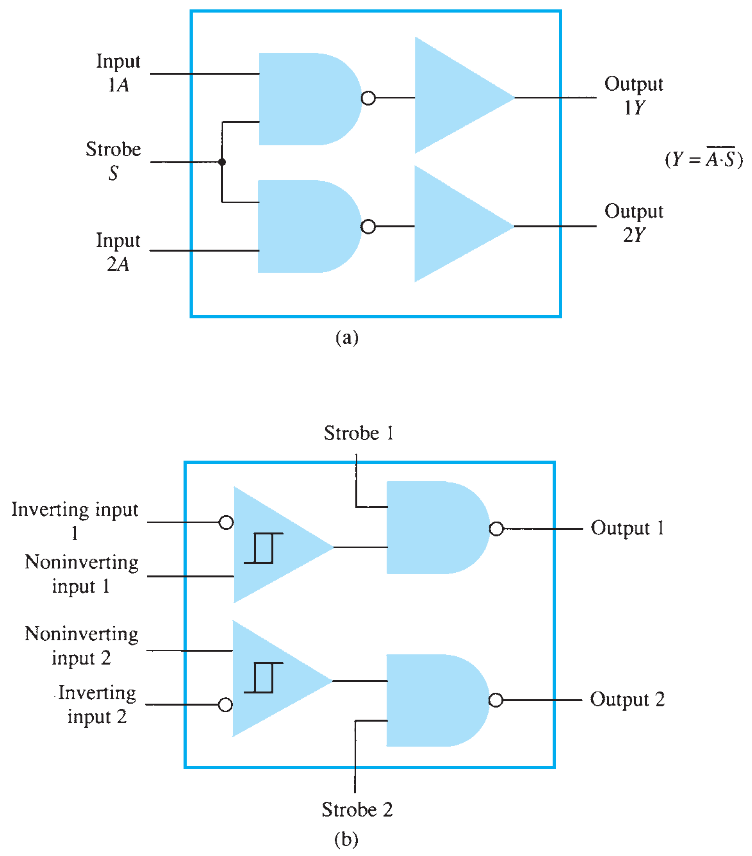
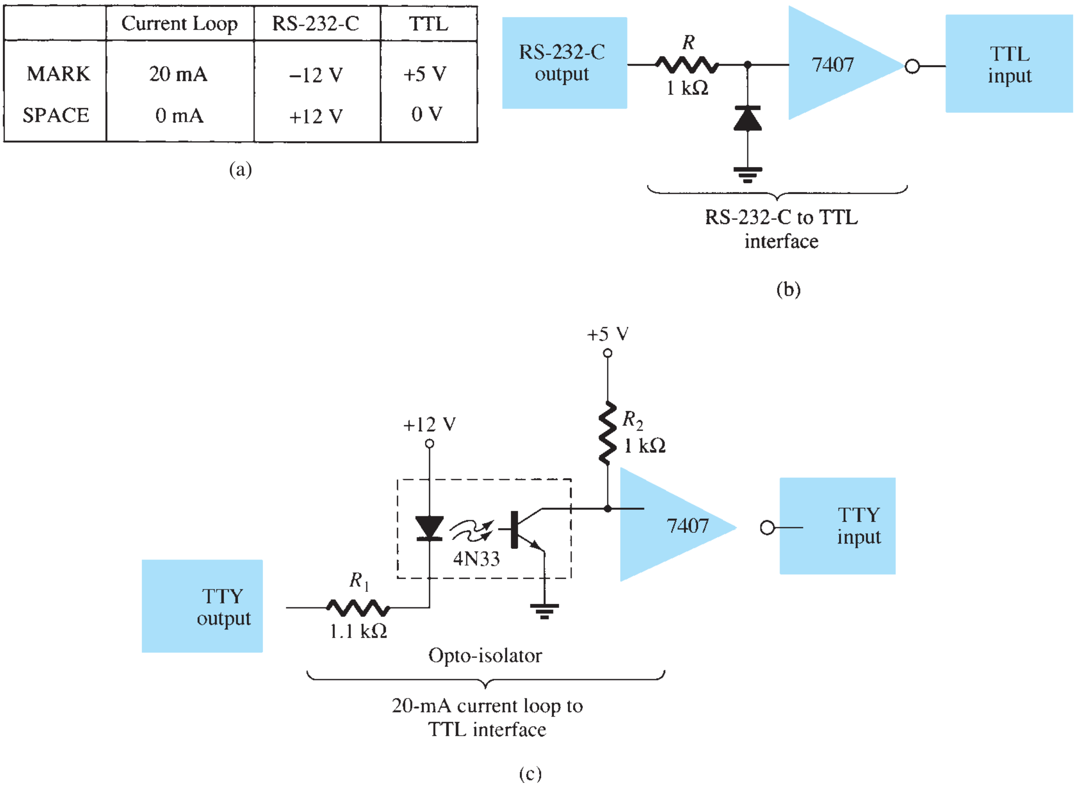


FIG. 13.29
Interface units: (a) dual-line drivers (SN75150); (b) dual-line receivers (SN75152).

Another type of interface circuit is that used to connect various digital input and output units, signals with devices such as keyboards, video terminals, and printers. One of the EIA electronic industry standards is referred to as RS-232C. This standard states that a digital signal represents a mark (logic-1) and a space (logic-0). The definitions of mark and space vary with the type of circuit used (although a full reading of the standard will spell out the acceptable limits of mark and space signals).

RS-232C-to-TTL Converter

For TTL circuits, +5 V is a mark and 0 V is a space. For RS-232C, a mark could be −12 V and a space +12 V. Figure 13.30a provides a tabulation of some mark and space definitions. For a unit having outputs defined by RS-232C that is to operate into another unit operating with a TTL signal level, an interface circuit as shown in Fig. 13.30b could be used. A mark output from the driver (at −12 V) would be clipped by the diode so that the input to the inverter circuit is near 0 V, resulting in an output of +5 V (TTL mark). A space output at +12 V would drive the inverter output low for a 0-V output (a space).



	Current Loop	RS-232-C	TTL
MARK	20 mA	−12 V	+5 V
SPACE	0 mA	+12 V	0 V

(a)

RS-232-C output
R
1 kΩ
7407
TTL input
RS-232-C to TTL interface

(b)

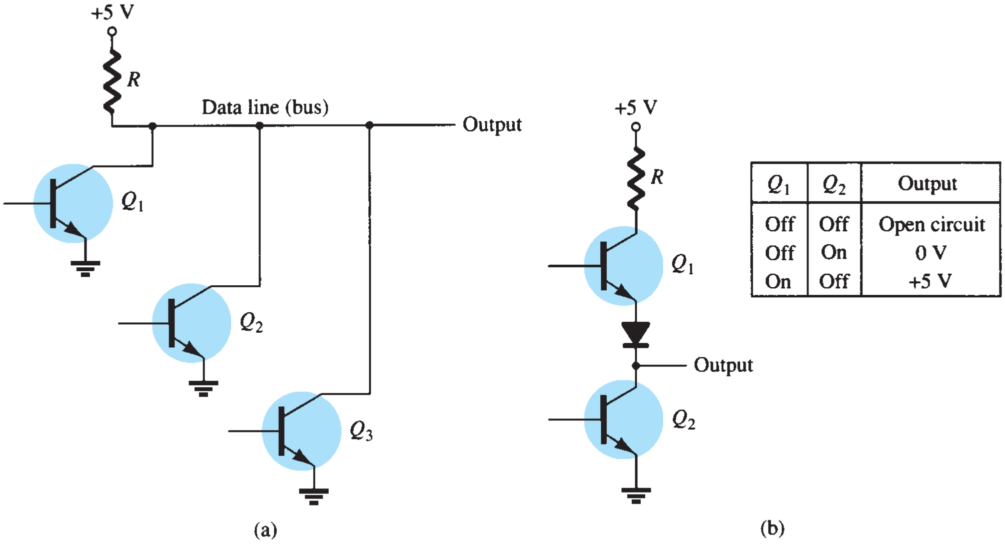
+5 V
R2
1 kΩ
+12 V
4N33
7407
TTY input
R1
TTY output
1.1 kΩ
Opto-isolator
20-mA current loop to TTL interface

(c)

FIG. 13.30
Interfacing signal standards and converter circuits.

Another example of an interface circuit converts the signals from a TTY current loop into TTL levels as shown in Fig. 13.30c. An input mark results when 20 mA of current is drawn from the source through the output line of the teletype (TTY). This current then goes through the diode element of an opto-isolator, driving the output transistor on. The input to the inverter going low results in a +5-V signal from the 7407 inverter output so that a mark from the teletype results in a mark to the TTL input. A space from the teletype current loop provides no current, with the opto-isolator transistor remaining off and the inverter output then 0 V, which is a TTL space signal.

Another means of interfacing digital signals is made using open-collector output or tri-state output. When a signal is output from a transistor collector (see Fig. 13.31) that is not



+5 V
R
Data line (bus)
Output
Q_1
Q_2
Q_3

(a)

+5 V
R
Q_1
Output
Q_2

Q_1	Q_2	Output
Off	Off	Open circuit
Off	On	0 V
On	Off	+5 V

(b)

FIG. 13.31
Connections to data lines: (a) open-collector output; (b) tri-state output.

connected to any other electronic component, the output is open-collector. This permits connecting a number of signals to the same wire or bus. Any transistor going on then provides a low output voltage, whereas all transistors remaining off provides a high output voltage.

13.8 SUMMARY

Important Conclusions and Concepts

1. A comparator provides an output of either maximum high or maximum low when one input goes above or below the other.
2. A DAC is a digital-to-analog converter.
3. An ADC is an analog-to-digital converter.
4. Timer IC:
   a. An astable circuit acts as a clock.
   b. A monostable circuit acts as a one-shot or timer.
5. A phase-locked loop (PLL) circuit contains a phase detector, a low-pass filter, and a voltage-controlled oscillator (VCO).
6. There are two standard types of interfacing circuits: **the RS-232-C and the TTL**.

13.9 COMPUTER ANALYSIS

PSpice Windows

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems can display the resulting dc bias, or one can use **PROBE** to display resulting waveforms.

Program 13.1—Comparator Circuit Used to Drive an LED Using PSpice, draw the circuit of a comparator circuit with output driving an LED indicator as shown in Fig. 13.32. To be able to view the magnitude of the dc output voltage, place a **VPRINT1** component at V_o with **DC** and **MAG** selected. To view the dc current through the LED, place an **IPRINT** component in series with the **LED** current meter as shown in Fig. 13.32. The **Analysis Setup** provides for a dc sweep as shown in Fig. 13.33. The **DC Sweep** is set, as shown, for V_i from 4 V to 8 V in 1-V steps. After running the simulation, some of the resulting analysis output obtained is as shown in Fig. 13.34.

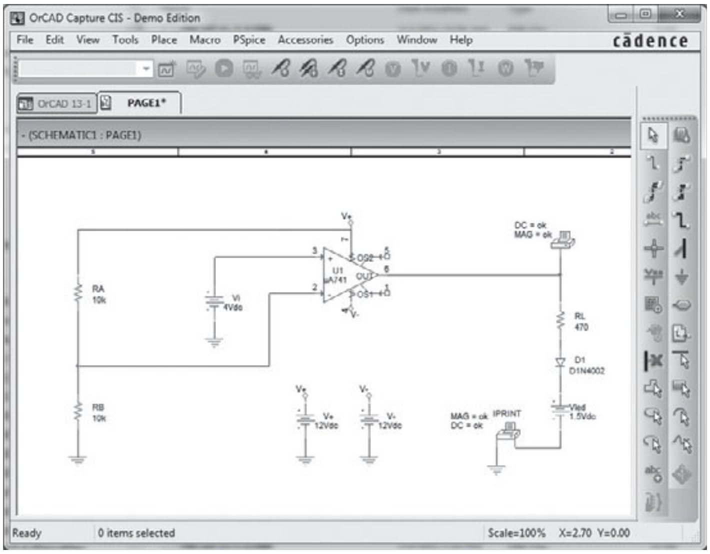
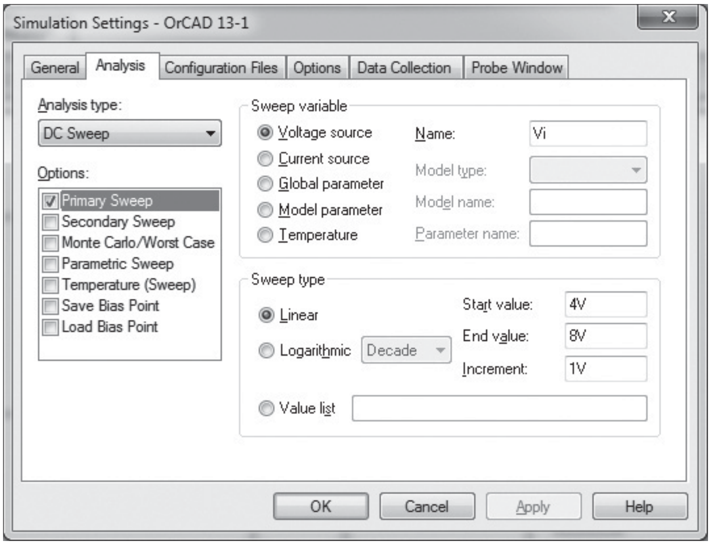

OrCAD Capture CIS - Demo Edition
File
Edit
View
Tools
Place
Macro
PSpice
Accessories
Options
Window
Help
cādence
OrCAD 13-1
PAGE1*
- (SCHEMATIC1 : PAGE1)
V+
DC = ok
MAG = ok
3
2
+
-
U1
uA741
OUT
OS2
OS1
5
6
1
V-
RA
10k
Vi
4Vdc
RL
470
D1
D1N4002
RB
10k
V+
V+
12Vdc
V-
V-
12Vdc
MAG = ok
DC = ok
IPRINT
Vled
1.5Vdc
Ready
0 items selected
Scale=100%
X=2.70 Y=0.00

FIG. 13.32

Comparator circuit used to drive an LED.



Analysis type: DC Sweep

Options:
☑ Primary Sweep
☐ Secondary Sweep
☐ Monte Carlo/Worst Case
☐ Parametric Sweep
☐ Temperature (Sweep)
☐ Save Bias Point
☐ Load Bias Point

Sweep variable
● Voltage source
○ Current source
○ Global parameter
○ Model parameter
○ Temperature

Name: Vi
Model type:
Model name:
Parameter name:

Sweep type
● Linear
○ Logarithmic Decade
○ Value list

Start value: 4V
End value: 8V
Increment: 1V

FIG. 13.33

Analysis Setup for a dc sweep of the circuit of Fig. 13.32.

```
****        DC TRANSFER CURVES
*******************************************
V_Vi            V(N00334)

4.000E+00      1.200E+01
5.000E+00      1.200E+01
6.000E+00      1.200E+01
7.000E+00      1.200E+01
8.000E+00      1.200E+01

****        DC TRANSFER CURVES
*******************************************
V_Vi           I(V_PRINT2)

4.000E+00     -2.079E-02
5.000E+00     -2.079E-02
6.000E+00     -2.079E-02
7.000E+00     -2.079E-02
8.000E+00     -2.079E-02
```

FIG. 13.34

Analysis output (edited) for circuit of Fig. 13.32.

The circuit of Fig. 13.32 shows a voltage divider that provides 6 V to the minus input, so that any input V_i below 6 V will result in the output at the minus saturation voltage (near −10 V). Any input above +6 V results in the output going to the positive saturation level (near +10 V). The LED will therefore be driven *on* by any input above the reference level of +6 V and left *off* by any input below +6 V. Figure 13.34 shows a table of the output voltage and a table of the LED current for inputs from 4 V to 8 V. The table shows that the LED current is nearly 0 for inputs up to +6 V, and that a current of about 20 mA lights the LED for inputs at +6 V or above.

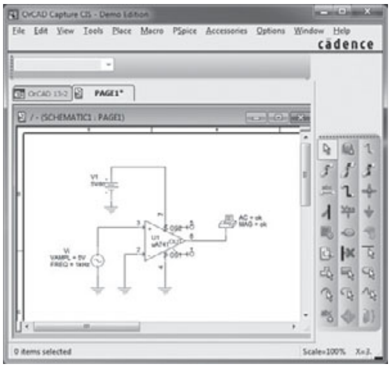


FIG. 13.35

Schematic for a comparator.

Program 13.2—Comparator Operation The operation of a comparator IC can be demonstrated using a 741 op-amp as shown in Fig. 13.35. The input is a 5 V, peak sinusoidal signal. The **Analysis Setup** provides for **Transient** analysis with **Print Step** of **20 ns** and **Run Time** of **3 ms**. Since the input signal is applied to the noninverting input, the output is in phase with the input. When the input goes above 0 V, the output goes to the positive saturation level, near +5 V. When the input goes below 0 V, the output goes to the negative saturation level—this being 0 V since the minus voltage input is set to that value. Figure 13.36 shows input and output voltages.

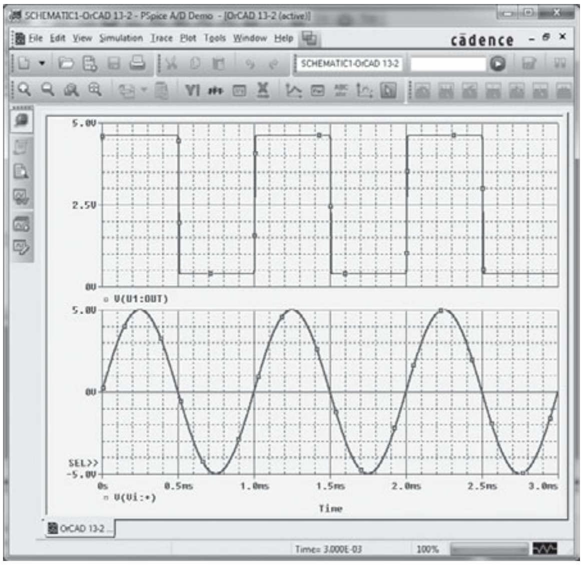


FIG. 13.36

Output for the comparator of Fig. 13.35.

Program 13.3—Operation of 555 Timer as Oscillator Figure 13.37 shows a 555 timer connected as an oscillator. Equations (13.3) and (13.4) can be used to calculate the charge and discharge times as follows:

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5\text{ k}\Omega + 7.15\text{ k}\Omega)(0.1\ \mu\text{F}) = 1.05\text{ ms}$$
$$T_{\text{low}} = 0.7R_BC = 0.7(7.5\text{ k}\Omega)(0.1\ \mu\text{F}) = 0.525\text{ ms}$$

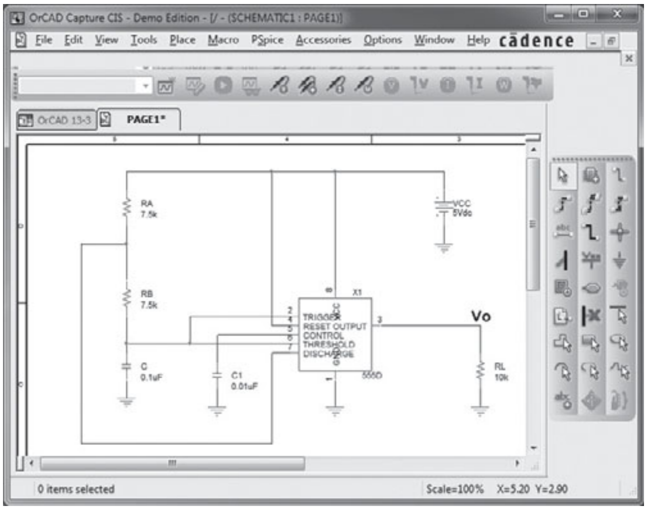

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
OrCAD 13-3
PAGE1*
RA
7.5k
RB
7.5k
C
0.1uF
C1
0.01uF
VCC
5Vdc
X1
TRIGGER
RESET OUTPUT
CONTROL
THRESHOLD
DISCHARGE
555D
Vo
RL
10k
0 items selected
Scale=100% X=5.20 Y=2.90

FIG. 13.37
Schematic of a 555 timer oscillator.

The resulting trigger and output waveforms are shown in Fig. 13.38. When the trigger charges to the upper trigger level, the output goes to the low output level of 0 V. The output stays low until the trigger input discharges to the low trigger level, at which time the output goes to the high level of +5 V.

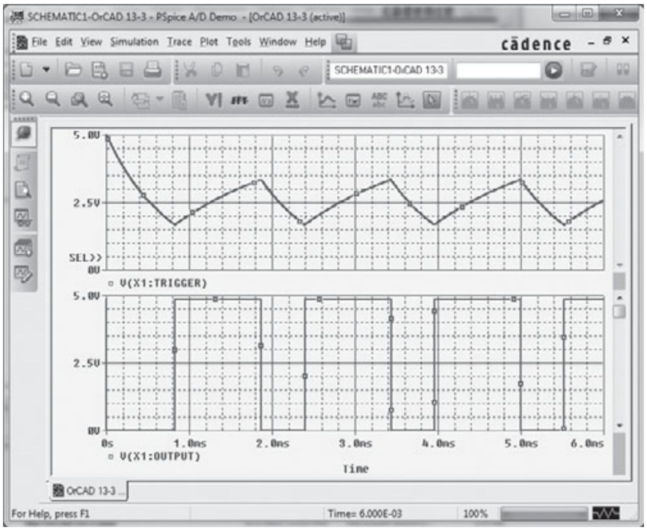
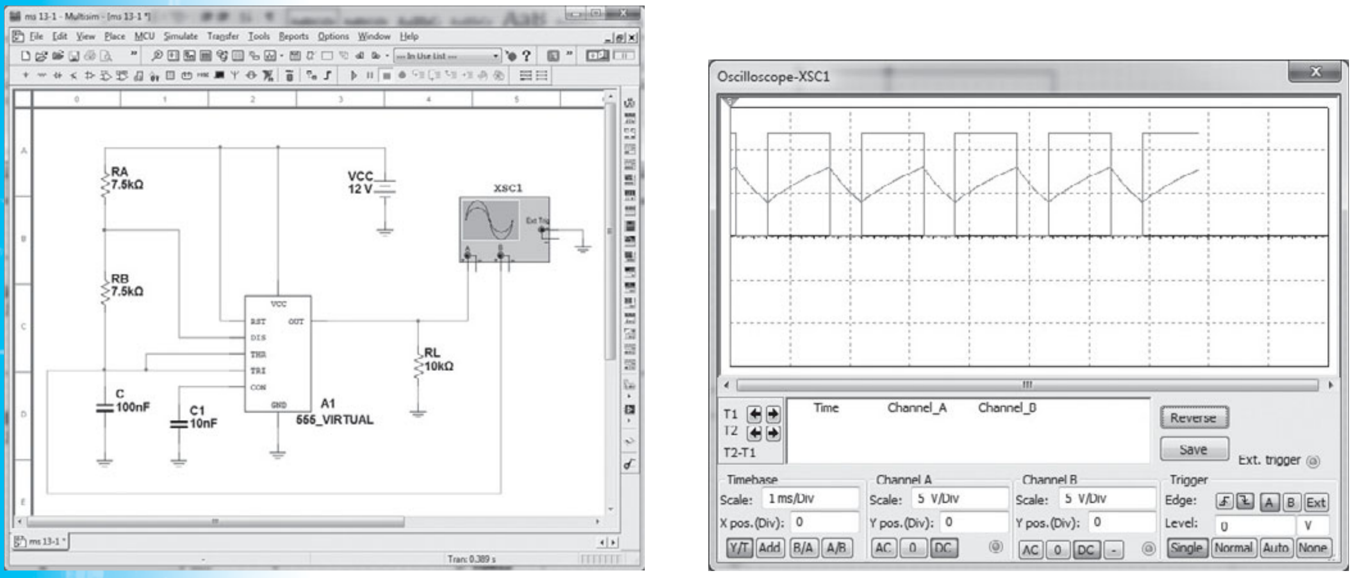

SCHEMATIC1-OrCAD 13-3 - PSpice A/D Demo - [OrCAD 13-3 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 13-3
5.0V
2.5V
SEL>>
0V
V(X1:TRIGGER)
5.0V
2.5V
0V
0s
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
6.0ms
V(X1:OUTPUT)
Time
OrCAD 13-3
For Help, press F1
Time= 6.000E-03
100%

FIG. 13.38
Probe output for the 555 oscillator of Fig. 13.37.

Multisim

Program 13.4—The 555 Timer as an Oscillator Figure 13.39(a) shows the same oscillator circuit as in Program 13.3, this time using Multisim to build the circuit and to show


ms 13-1 - Multisim - [ms 13-1 *]
RA
7.5kΩ
RB
7.5kΩ
C
100nF
C1
10nF
VCC
12 V
XSC1
Ext Trig
A
B
VCC
RST
OUT
DIS
THR
TRI
CON
GND
A1
555_VIRTUAL
RL
10kΩ
Tran: 0.389 s
Oscilloscope-XSC1
T1
T2
T2-T1
Time
Channel_A
Channel_B
Reverse
Save
Ext. trigger

Timebase
Scale: 1 ms/Div
X pos.(Div): 0
Y/T Add B/A A/B

Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC 0 DC

Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC 0 DC -

Trigger
Edge:
Level: 0 V
Single Normal Auto None

(a)

(b)

FIG. 13.39

(a) Timer oscillator using EWB; (b) scope display.

resulting waveforms on an oscilloscope. Using the oscilloscope instrument, we find the waveform across the capacitor and that from the output as shown in Fig. 13.39(b).

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

13.2 Comparator Unit Operation

1. Draw the diagram of a 741 op-amp operated from ±15-V supplies with $V_i(-) = 0$ V and $V_i(+) = +5$ V. Include terminal pin connections.
2. Sketch the output waveform for the circuit of Fig. 13.40.
3. Draw a circuit diagram of a 311 op-amp showing an input of 10 V rms applied to the inverting input and the plus input to ground. Identify all pin numbers.
4. Draw the resulting output waveform for the circuit of Fig. 13.41.

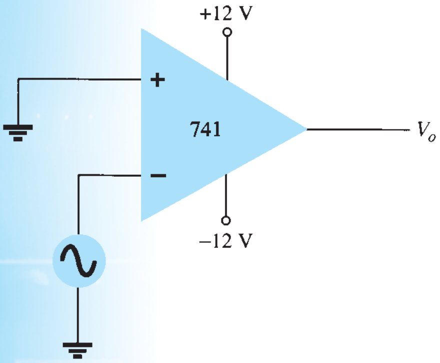

+12 V
+
741
−
−12 V
V_o

FIG. 13.40

Problem 2.

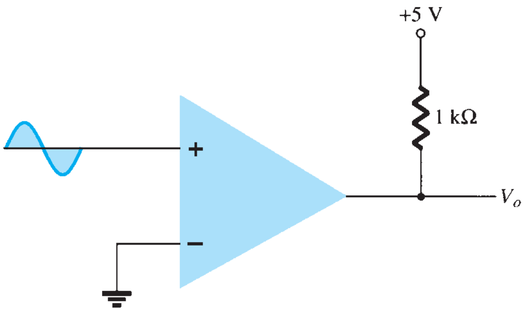


FIG. 13.41

Problem 4.

5. Draw the circuit diagram of a zero-crossing detector using a 339 comparator stage with ±12-V supplies.

6. Sketch the output waveform for the circuit of Fig. 13.42.

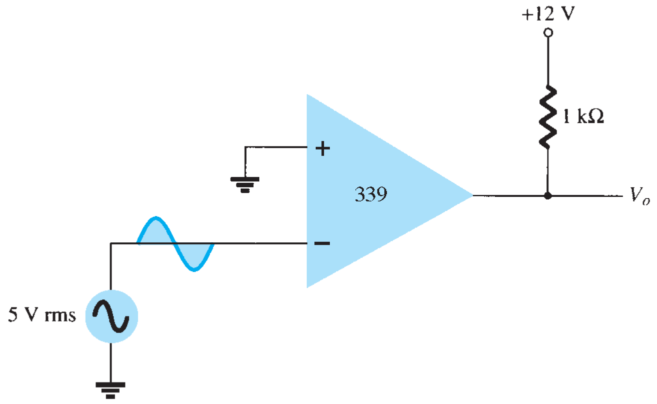

+12 V
1 kΩ
+
339
−
V_o
5 V rms

FIG. 13.42
Problem 6.

***7.** Describe the operation of the circuit in Fig. 13.43.

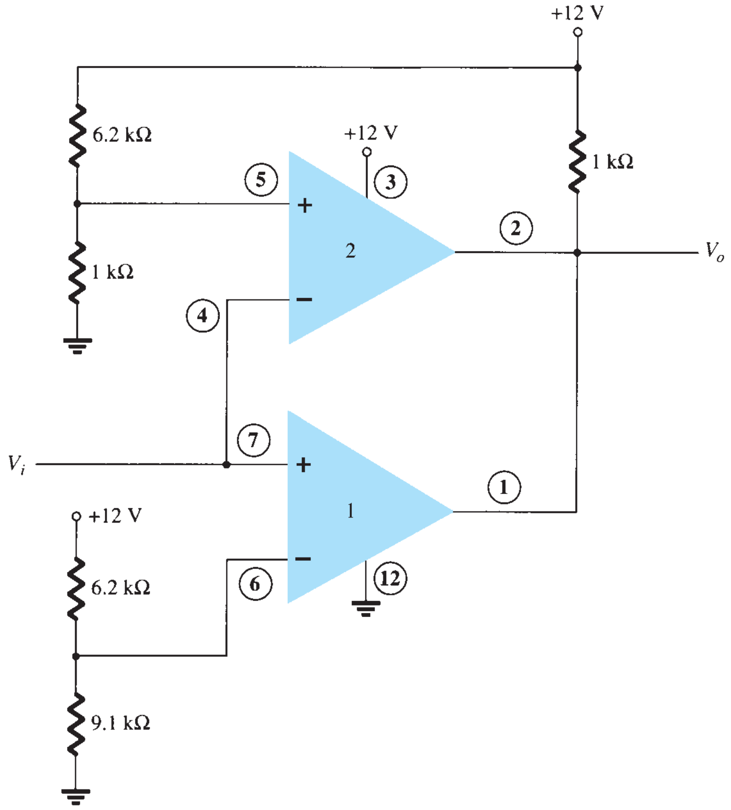

+12 V
6.2 kΩ
+12 V
⑤
③
+
1 kΩ
2
②
V_o
1 kΩ
④
−
⑦
V_i
+
1
①
+12 V
−
6.2 kΩ
⑥
⑫
9.1 kΩ

FIG. 13.43
Problem 7.

13.3 Digital–Analog Converters

8. Sketch a five-stage ladder network using 15-kΩ and 30-kΩ resistors.

9. For a reference voltage of 16 V, calculate the output voltage for an input of 11010 to the circuit of Problem 8.

10. What voltage resolution is possible using a 12-stage ladder network with a 10-V reference voltage?

11. For a dual-slope converter, describe what occurs during the fixed time interval and the count interval.

12. How many count steps occur using a 12-stage digital counter at the output of an ADC?

13. What is the maximum count interval using a 12-stage counter operated at a clock rate of 20 MHz?

13.4 Timer IC Unit Operation

14. Sketch the circuit of a 555 timer connected as an astable multivibrator for operation at 350 kHz. Determine the value of capacitor C needed using $R_A = R_B = 7.5\ \text{k}\Omega$.

15. Draw the circuit of a one-shot using a 555 timer to provide one time period of 20μs. If $R_A = 7.5\ \text{k}\Omega$, what value of C is needed?

16. Sketch the input and output waveforms for a one-shot using a 555 timer triggered by a 10-kHz clock for $R_A = 5.1\ \text{k}\Omega$ and $C = 5$ nF.

13.5 Voltage-Controlled Oscillator

17. Calculate the center frequency of a VCO using a 566 IC as in Fig. 13.22 for $R_1 = 4.7\ \text{k}\Omega$, $R_2 = 1.8\ \text{k}\Omega$, $R_3 = 11\ \text{k}\Omega$, and $C_1 = 0.001\ \mu\text{F}$.

*18. What frequency range results in the circuit of Fig. 13.23 for $C_1 = 0.001\ \mu\text{F}$?

19. Determine the capacitor needed in the circuit of Fig. 13.22 to obtain a 200-kHz output.

13.6 Phase-Locked Loop

20. Calculate the VCO free-running frequency for the circuit of Fig. 13.26b with $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$.

21. What value of capacitor C_1 is required in the circuit of Fig. 13.26b to obtain a center frequency of 100 kHz?

22. What is the lock range of the PLL circuit in Fig. 13.26b for $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$?

13.7 Interfacing Circuitry

23. Describe the signal conditions for current-loop and RS-232C interfaces.

24. What is a data bus?

25. What is the difference between open-collector and tri-state output?

13.9 Computer Analysis

*26. Use Design Center to draw a schematic circuit as in Fig. 13.32, using an LM111 with $V_i = 5$ V rms applied to minus $(-)$ input and $+5$ V rms applied to plus $(+)$ input. Use Probe to view the output waveform.

*27. Use Design Center to draw a schematic circuit as in Fig. 13.35. Examine the output listing for the results.

*28. Use Multisim to draw a 555 oscillator with resulting output with $t_{\text{low}} = 2$ ms and $t_{\text{high}} = 5$ ms.

Feedback and Oscillator Circuits

14

CHAPTER OBJECTIVES

- The concept of negative feedback
- About practical feedback circuits
- Various types of oscillator circuits

14.1 FEEDBACK CONCEPTS

Feedback has been mentioned previously, in particular, in op-amp circuits as described in Chapters 10 and 11. Depending on the relative polarity of the signal being fed back into a circuit, one may have negative or positive feedback. Negative feedback results in decreased voltage gain, for which a number of circuit features are improved, as summarized below. Positive feedback drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown in Fig. 14.1. The input signal V_s is applied to a mixer network, where it is combined with a feedback signal V_f. The difference of these signals V_i is then the input voltage to the amplifier. A portion of the amplifier output V_o is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal to the input mixer network.

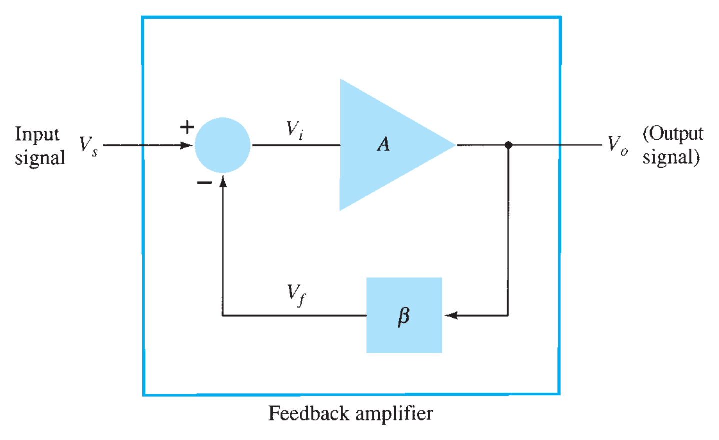


FIG. 14.1
Simple block diagram of feedback amplifier.

If the feedback signal is of opposite polarity to the input signal, as shown in Fig. 14.1, negative feedback results. Although negative feedback results in reduced overall voltage gain, a number of improvements are obtained, among them being:

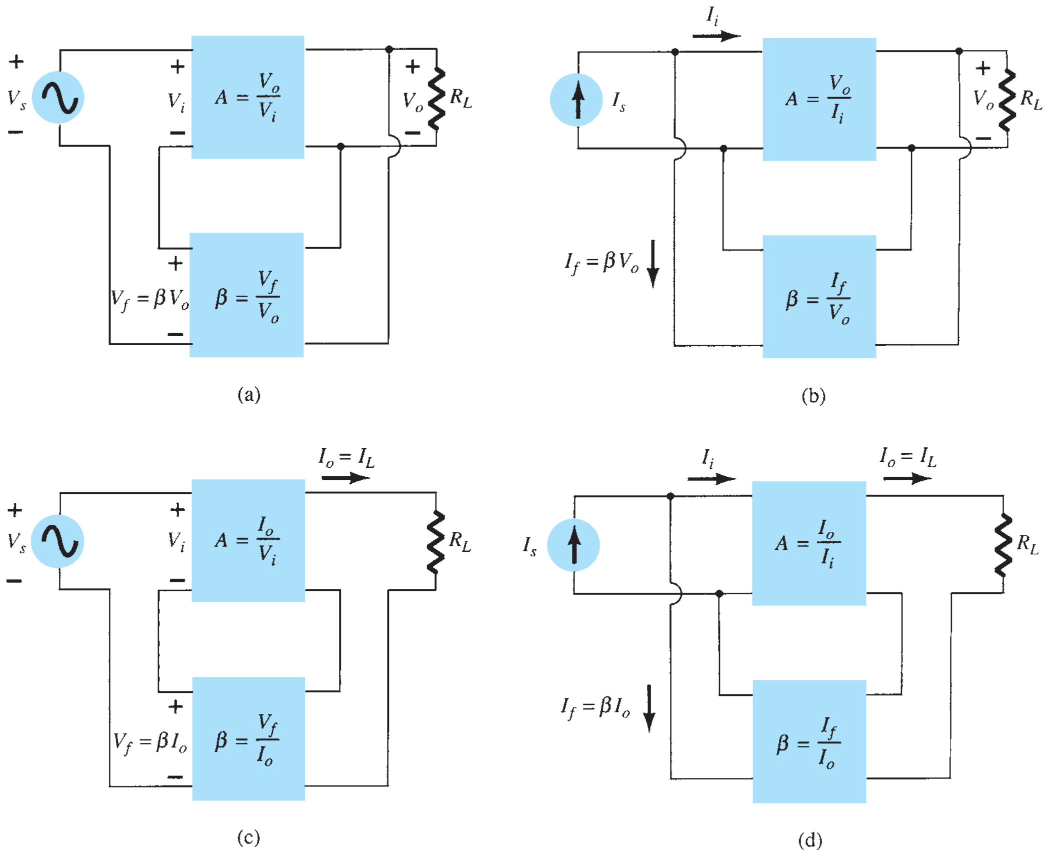
1. Higher input impedance.
2. Better stabilized voltage gain.
3. Improved frequency response.
4. Lower output impedance.
5. Reduced noise.
6. More linear operation.

14.2 FEEDBACK CONNECTION TYPES

There are four basic ways of connecting the feedback signal. Both *voltage* and *current* can be fed back to the input either in *series* or *parallel*. Specifically, there can be:

1. Voltage-series feedback (Fig. 14.2a).
2. Voltage-shunt feedback (Fig. 14.2b).
3. Current-series feedback (Fig. 14.2c).
4. Current-shunt feedback (Fig. 14.2d).

In the list above, *voltage* refers to connecting the output voltage as input to the feedback network; *current* refers to tapping off some output current through the feedback network. *Series* refers to connecting the feedback signal in series with the input signal voltage; *shunt* refers to connecting the feedback signal in shunt (parallel) with an input current source.



V_s
V_i
$A = \frac{V_o}{V_i}$
V_o
R_L
$V_f = \beta V_o$
$\beta = \frac{V_f}{V_o}$
(a)
I_i
I_s
$A = \frac{V_o}{I_i}$
V_o
R_L
$I_f = \beta V_o$
$\beta = \frac{I_f}{V_o}$
(b)
$I_o = I_L$
V_s
V_i
$A = \frac{I_o}{V_i}$
R_L
$V_f = \beta I_o$
$\beta = \frac{V_f}{I_o}$
(c)
I_i
$I_o = I_L$
I_s
$A = \frac{I_o}{I_i}$
R_L
$I_f = \beta I_o$
$\beta = \frac{I_f}{I_o}$
(d)

FIG. 14.2

Feedback amplifier types: (a) voltage-series feedback, $A_f = V_o/V_s$; (b) voltage-shunt feedback, $A_f = V_o/I_s$; (c) current-series feedback, $A_f = I_o/V_s$; (d) current-shunt feedback, $A_f = I_o/I_s$.

Series feedback connections tend to *increase* the input resistance, whereas shunt feedback connections tend to *decrease* the input resistance. Voltage feedback tends to *decrease* the output impedance, whereas current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection. We shall therefore concentrate first on this amplifier connection.

Gain with Feedback

In this section we examine the gain of each of the feedback circuit connections of Fig. 14.2. The gain without feedback, A, is that of the amplifier stage. With feedback β, the overall gain of the circuit is reduced by a factor $(1 + \beta A)$, as detailed below. A summary of the gain, feedback factor, and gain with feedback of Fig. 14.2 is provided for reference in Table 14.1.

TABLE 14.1

Summary of Gain, Feedback, and Gain with Feedback from Fig. 14.2

		Voltage-Series	**Voltage-Shunt**	**Current-Series**	**Current-Shunt**
Gain without feedback	A	$\dfrac{V_o}{V_i}$	$\dfrac{V_o}{I_i}$	$\dfrac{I_o}{V_i}$	$\dfrac{I_o}{I_i}$
Feedback	β	$\dfrac{V_f}{V_o}$	$\dfrac{I_f}{V_o}$	$\dfrac{V_f}{I_o}$	$\dfrac{I_f}{I_o}$
Gain with feedback	A_f	$\dfrac{V_o}{V_s}$	$\dfrac{V_o}{I_s}$	$\dfrac{I_o}{V_s}$	$\dfrac{I_o}{I_s}$

Voltage-Series Feedback Figure 14.2a shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \qquad \textbf{(14.1)}$$

If a feedback signal V_f is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

then $$(1 + \beta A)V_o = AV_s$$

so that the overall voltage gain *with* feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}} \qquad \textbf{(14.2)}$$

Equation (14.2) shows that the gain *with* feedback is the amplifier gain reduced by the factor $(1 + \beta A)$. This factor will be seen also to affect input and output impedance among other circuit features.

Voltage-Shunt Feedback The gain with feedback for the network of Fig. 14.2b is

$$A_f = \frac{V_o}{I_s} = \frac{A\,I_i}{I_i + I_f} = \frac{A\,I_i}{I_i + \beta V_o} = \frac{A\,I_i}{I_i + \beta A\,I_i}$$

$$\boxed{A_f = \frac{A}{1 + \beta A}} \qquad \textbf{(14.3)}$$

Input Impedance with Feedback

Voltage-Series Feedback A more detailed voltage-series feedback connection is shown in Fig. 14.3. The input impedance can be determined as follows:

$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$\boxed{Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i = Z_i(1 + \beta A)} \tag{14.4}$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1 + \beta A)$, and applies to both voltage-series (Fig. 14.2a) and current-series (Fig. 14.2c) configurations.

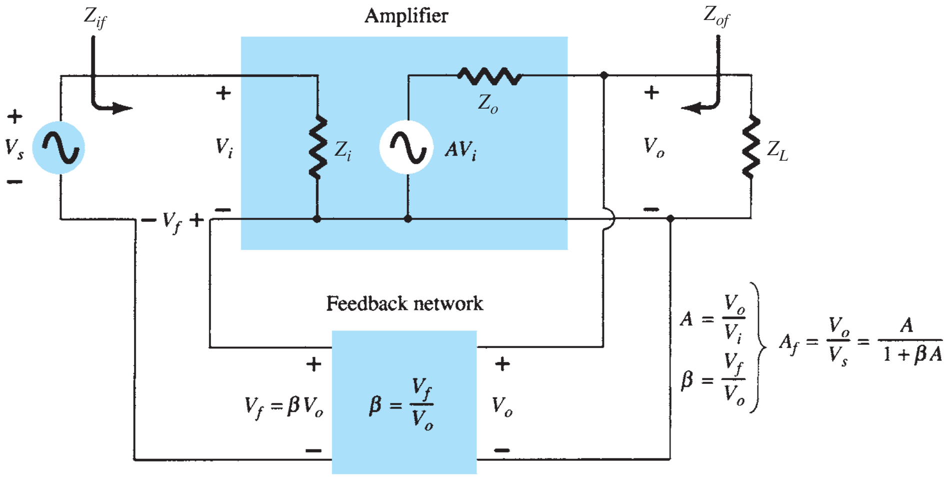

Z_{if}
Amplifier
Z_{of}
+
V_s
−
+
V_i
−
Z_i
AV_i
Z_o
+
V_o
−
Z_L
$- V_f +$
Feedback network
+
$V_f = \beta V_o$
−
$\beta = \frac{V_f}{V_o}$
+
V_o
−
$A = \frac{V_o}{V_i}$
$\beta = \frac{V_f}{V_o}$
$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$

FIG. 14.3

Voltage-series feedback connection.

Voltage-Shunt Feedback A more detailed voltage-shunt feedback connection is shown in Fig. 14.4. The input impedance can be determined to be

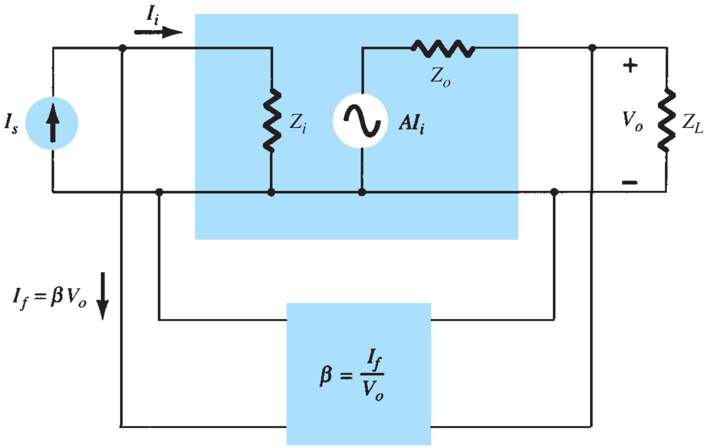

I_i
I_s
Z_i
AI_i
Z_o
+
V_o
−
Z_L
$I_f = \beta V_o$
$\beta = \frac{I_f}{V_o}$

FIG. 14.4

Voltage-shunt feedback connection.

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o}$$

$$= \frac{V_i/I_i}{I_i/I_i + \beta V_o/I_i}$$

$$\boxed{Z_{if} = \frac{Z_i}{1 + \beta A}} \qquad \textbf{(14.5)}$$

This reduced input impedance applies to the voltage-series connection of Fig. 14.2a and the voltage-shunt connection of Fig. 14.2b.

Output Impedance with Feedback

The output impedance for the connections of Fig. 14.2 is dependent on whether voltage or current feedback is used. For voltage feedback, the output impedance is decreased, whereas current feedback increases the output impedance.

Voltage-Series Feedback The voltage-series feedback circuit of Fig. 14.3 provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage V, resulting in a current I, with V_s shorted out ($V_s = 0$). The voltage V is then

$$V = IZ_o + AV_i$$

For $V_s = 0$,

$$V_i = -V_f$$

so that

$$V = IZ_o - AV_f = IZ_o - A(\beta V)$$

Rewriting the equation as

$$V + \beta AV = IZ_o$$

allows solving for the output impedance with feedback:

$$\boxed{Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A}} \qquad \textbf{(14.6)}$$

Equation (14.6) shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor $(1 + \beta A)$.

Current-Series Feedback The output impedance with current-series feedback can be determined by applying a signal V to the output with V_s shorted out, resulting in a current I, the ratio of V to I being the output impedance. Figure 14.5 shows a more detailed

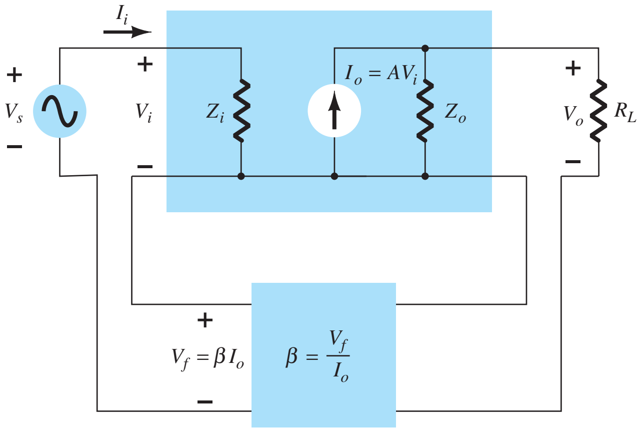


FIG. 14.5
Current-series feedback connection.

connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. 14.5, the resulting output impedance is determined as follows. With $V_s = 0$,

$$V_i = V_f$$

$$I = \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I$$

$$Z_o(1 + \beta A)I = V$$

$$\boxed{Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)} \tag{14.7}$$

A summary of the effect of feedback on input and output impedance is provided in Table 14.2.

TABLE 14.2

Effect of Feedback Connection on Input and Output Impedance

	Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
Z_{if}	$Z_i(1 + \beta A)$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\dfrac{Z_i}{1 + \beta A}$ (decreased)	$\dfrac{Z_i}{1 + \beta A}$ (decreased)
Z_{of}	$\dfrac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)	$\dfrac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

EXAMPLE 14.1 Determine the voltage gain, input, and output impedance with feedback for voltage-series feedback having $A = -100$, $R_i = 10\,\text{k}\Omega$, and $R_o = 20\,\text{k}\Omega$ for feedback of (a) $\beta = -0.1$ and (b) $\beta = -0.5$.

Solution: Using Eqs. (14.2), (14.4), and (14.6), we obtain

a. $$A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (-0.1)(-100)} = \frac{-100}{11} = \mathbf{-9.09}$$

$$Z_{if} = Z_i(1 + \beta A) = 10\,\text{k}\Omega\,(11) = \mathbf{110\,k\Omega}$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{11} = \mathbf{1.82\,k\Omega}$$

b. $$A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (-0.5)(-100)} = \frac{-100}{51} = \mathbf{-1.96}$$

$$Z_{if} = Z_i(1 + \beta A) = 10\,\text{k}\Omega\,(51) = \mathbf{510\,k\Omega}$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{51} = \mathbf{392.16\,\Omega}$$

Example 14.1 demonstrates the trade-off of gain for desired input and output resistance. Reducing the gain by a factor of 11 (from 100 to 9.09) is complemented by a reduced output resistance and increased input resistance by the same factor of 11. Reducing the gain by a factor of 51 provides a gain of only 2 but with input resistance increased by the factor of 51 (to over 500 kΩ) and output resistance reduced from 20 kΩ to under 400 Ω. Feedback offers the designer the choice of trading away some of the available amplifier gain for other desired circuit features.

Reduction in Frequency Distortion

For a negative-feedback amplifier having $\beta A \gg 1$, the gain with feedback is $A_f \cong 1/\beta$. It follows from this that if the feedback network is purely resistive, the gain with feedback is not dependent on frequency even though the basic amplifier gain is frequency dependent. Practically, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative-voltage feedback amplifier circuit.

Reduction in Noise and Nonlinear Distortion

Signal feedback tends to hold down the amount of noise signal (such as power-supply hum) and nonlinear distortion. The factor $(1 + \beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. However, there is a reduction in overall gain (the price required for the improvement in circuit performance). If additional stages are used to bring the overall gain up to the level without feedback, the extra stage(s) might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback-amplifier circuit to obtain higher gain while also providing reduced noise signal.

Effect of Negative Feedback on Gain and Bandwidth

In Eq. (14.2), the overall gain with negative feedback is shown to be

$$A_f = \frac{A}{1 + \beta A} \cong \frac{A}{\beta A} = \frac{1}{\beta} \qquad \text{for } \beta A \gg 1$$

As long as $\beta A \gg 1$, the overall gain is approximately $1/\beta$. For a practical amplifier (for single low- and high-frequency breakpoints) the open-loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain may also drop off at low frequencies for capacitively coupled amplifier stages. Once the open-loop gain A drops low enough and the factor βA is no longer much larger than 1, the conclusion of Eq. (14.2) that $A_f \cong 1/\beta$ no longer holds true.

Figure 14.6 shows that the amplifier with negative feedback has more bandwidth (B_f) than the amplifier without feedback (B). The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.

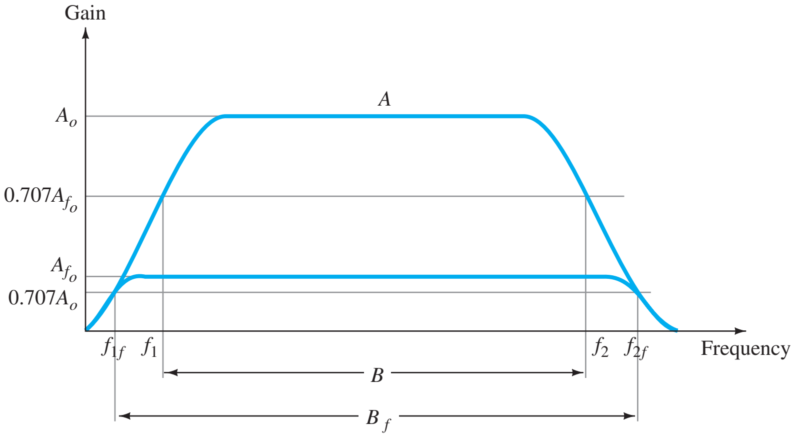


FIG. 14.6
Effect of negative feedback on gain and bandwidth.

It is interesting to note that the use of feedback, although resulting in a lowering of voltage gain, has provided an increase in B and in the upper 3-dB frequency particularly. In fact, the product of gain and frequency remains the same, so that the gain–bandwidth product of the basic amplifier is the same value for the feedback amplifier. However, since the feedback amplifier has lower gain, the net operation was to *trade* gain for bandwidth (we use bandwidth for the upper 3-dB frequency since typically $f_2 \gg f_1$).

Gain Stability with Feedback

In addition to the β factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback. Differentiating Eq. (14.2) leads to

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right| \tag{14.8}$$

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \qquad \text{for } \beta A \gg 1 \tag{14.9}$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

EXAMPLE 14.2 If an amplifier with gain of -1000 and feedback of $\beta = -0.1$ has a gain change of 20% due to temperature, calculate the change in gain of the feedback amplifier.

Solution: Using Eq. (14.9), we get

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| = \left|\frac{1}{-0.1(-1000)}(20\%)\right| = \mathbf{0.2\%}$$

The improvement is 100 times. Thus, whereas the amplifier gain changes from $|A| = 1000$ by 20%, the gain with feedback changes from $|A_f| = 100$ by only 0.2%.

14.3 PRACTICAL FEEDBACK CIRCUITS

Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

Voltage-Series Feedback

Figure 14.7 shows an FET amplifier stage with voltage-series feedback. A part of the output signal (V_o) is obtained using a feedback network of resistors R_1 and R_2. The feedback voltage V_f is connected in series with the source signal V_s, their difference being the input signal V_i.

Without feedback the amplifier gain is

$$A = \frac{V_o}{V_i} = -g_m R_L \tag{14.10}$$

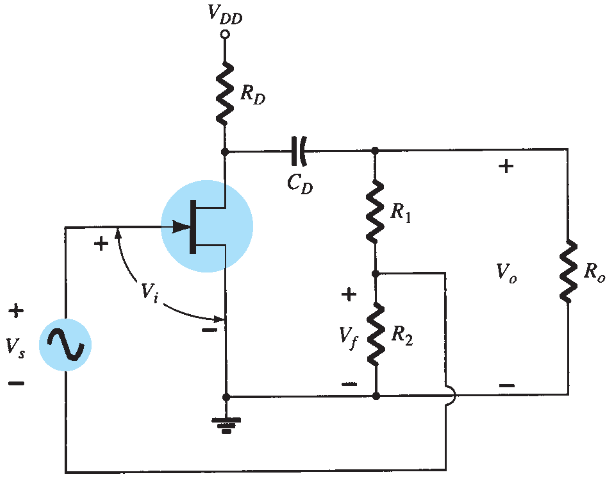


FIG. 14.7
FET amplifier stage with voltage-series feedback.

where R_L is the parallel combination of resistors:

$$R_L = R_D R_o (R_1 + R_2) \tag{14.11}$$

The feedback network provides a feedback factor of

$$\beta = \frac{V_f}{V_o} = \frac{-R_2}{R_1 + R_2} \tag{14.12}$$

Using the values of A and β above in Eq. (14.2), we find the gain with negative feedback to be

$$A_f = \frac{A}{1 + \beta A} = \frac{-g_m R_L}{1 + [R_2 R_L/(R_1 + R_2)]g_m} \tag{14.13}$$

If $\beta A \gg 1$, we have

$$\boxed{A_f \cong \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2}} \tag{14.14}$$

EXAMPLE 14.3 Calculate the gain without and with feedback for the FET amplifier circuit of Fig. 14.7 and the following circuit values: $R_1 = 80\ \text{k}\Omega$, $R_2 = 20\ \text{k}\Omega$, $R_o = 10\ \text{k}\Omega$, $R_D = 10\ \text{k}\Omega$, and $g_m = 4000\ \mu\text{S}$.

Solution:

$$R_L \cong \frac{R_o R_D}{R_o + R_D} = \frac{10\ \text{k}\Omega(10\ \text{k}\Omega)}{10\ \text{k}\Omega + 10\ \text{k}\Omega} = 5\ \text{k}\Omega$$

Neglecting the 100-kΩ resistance of R_1 and R_2 in series gives

$$A = -g_m R_L = -(4000 \times 10^{-6}\ \mu\text{S})(5\ \text{k}\Omega) = \mathbf{-20}$$

The feedback factor is

$$\beta = \frac{-R_2}{R_1 + R_2} = \frac{-20\ \text{k}\Omega}{80\ \text{k}\Omega + 20\ \text{k}\Omega} = -0.2$$

The gain with feedback is

$$A_f = \frac{A}{1 + \beta A} = \frac{-20}{1 + (-0.2)(-20)} = \frac{-20}{5} = \mathbf{-4}$$

Figure 14.8 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp, A, without feedback, is reduced by the feedback factor

$$\beta = \frac{R_2}{R_1 + R_2} \tag{14.15}$$

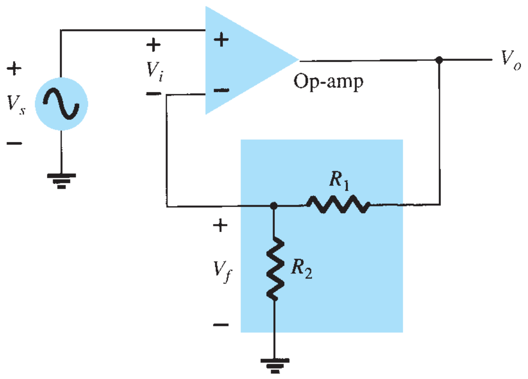


FIG. 14.8
Voltage-series feedback in an op-amp connection.

EXAMPLE 14.4 Calculate the amplifier gain of the circuit of Fig. 14.8 for op-amp gain $A = 100{,}000$ and resistances $R_1 = 1.8\text{ k}\Omega$ and $R_2 = 200\ \Omega$.

Solution:

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{200\ \Omega}{200\ \Omega + 1.8\text{ k}\Omega} = 0.1$$

$$A_f = \frac{A}{1 + \beta A} = \frac{100{,}000}{1 + (0.1)(100{,}000)} = \frac{100{,}000}{10{,}001} = 9.999$$

Note that since $\beta A \gg 1$,

$$A_f \cong \frac{1}{\beta} = \frac{1}{0.1} = \mathbf{10}$$

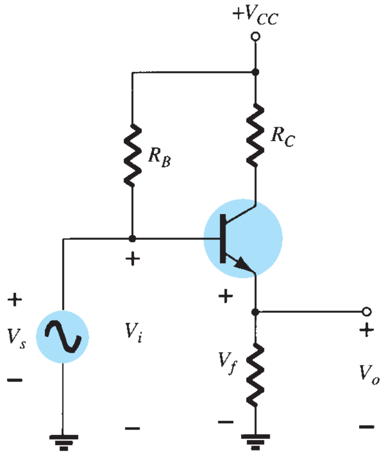


FIG. 14.9
Voltage-series feedback circuit (emitter-follower).

The emitter-follower circuit of Fig. 14.9 provides voltage-series feedback. The signal voltage V_s is the input voltage V_i. The output voltage V_o is also the feedback voltage in series with the input voltage. The amplifier, as shown in Fig. 14.9, provides the operation *with* feedback. The operation of the circuit without feedback provides $V_f = 0$, so that

$$A = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_E}{V_s} = \frac{h_{fe} R_E (V_s/h_{ie})}{V_s} = \frac{h_{fe} R_E}{h_{ie}}$$

and

$$\beta = \frac{V_f}{V_o} = 1$$

The operation with feedback then provides that

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} = \frac{h_{fe} R_E / h_{ie}}{1 + (1)(h_{fe} R_E / h_{ie})}$$

$$= \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E}$$

For $h_{fe} R_E \gg h_{ie}$,

$$A_f \cong 1$$

Current-Series Feedback

Another feedback technique is to sample the output current I_o and return a proportional voltage in series with the input. Although it stabilizes the amplifier gain, the current-series feedback connection increases input resistance.

Figure 14.10 shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current-series feedback. The current through resistor R_E results in a feedback voltage that opposes the source signal applied, so that the output voltage V_o is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).

Without Feedback Referring to the basic format of Fig. 14.2a and summarized in Table 14.1, we have

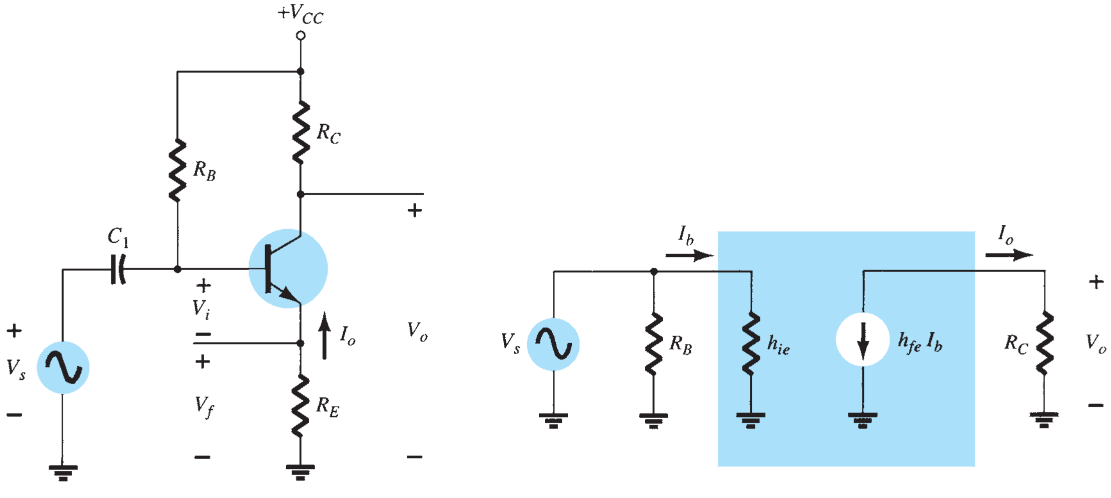
$$A = \frac{I_o}{V_i} = \frac{-I_b h_{fe}}{I_b h_{ie} + R_E} = \frac{-h_{fe}}{h_{ie} + R_E} \tag{14.16}$$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E \tag{14.17}$$

The input and output impedances are, respectively,

$$Z_i = R_B \| (h_{ie} + R_E) \cong h_{ie} + R_E \tag{14.18}$$

$$Z_o = R_C \tag{14.19}$$


+V_{CC}
R_C
R_B
C_1
+
V_i
−
+
V_f
−
I_o
V_o
R_E
+
V_s
−
−
I_b
I_o
V_s
R_B
h_{ie}
$h_{fe} I_b$
R_C
+
V_o
−

(a) (b)

FIG. 14.10

Transistor amplifier with unbypassed emitter resistor (R_E) for current-series feedback: (a) amplifier circuit; (b) ac equivalent circuit without feedback.

With Feedback

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-h_{fe}/h_{ie}}{1 + (-R_E)\left(\dfrac{-h_{fe}}{h_{ie} + R_E}\right)} \cong \frac{-h_{fe}}{h_{ie} + h_{fe}R_E} \qquad \textbf{(14.20)}$$

The input and output impedances are calculated as specified in Table 14.2:

$$Z_{if} = Z_i(1 + \beta A) \cong h_{ie}\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right) = h_{ie} + h_{fe}R_E \qquad \textbf{(14.21)}$$

$$Z_{of} = Z_o(1 + \beta A) = R_C\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right) \qquad \textbf{(14.22)}$$

The voltage gain A with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_oR_C}{V_s} = \left(\frac{I_o}{V_s}\right)R_C = A_fR_C \cong \frac{-h_{fe}R_C}{h_{ie} + h_{fe}R_E} \qquad \textbf{(14.23)}$$

EXAMPLE 14.5 Calculate the voltage gain of the circuit of Fig. 14.11.

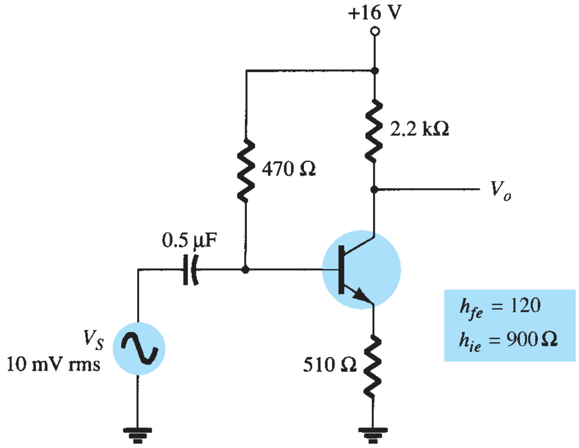

+16 V
2.2 kΩ
470 Ω
V_o
0.5 μF
V_S
10 mV rms
510 Ω
h_{fe} = 120
h_{ie} = 900 Ω

FIG. 14.11

BJT amplifier with current-series feedback for Example 14.5.

Solution: Without feedback,

$$A = \frac{I_o}{V_i} = \frac{-h_{fe}}{h_{ie} + R_E} = \frac{-120}{900 + 510} = -0.085$$

$$\beta = \frac{V_f}{I_o} = -R_E = -510$$

The factor $(1 + \beta A)$ is then

$$1 + \beta A = 1 + (-0.085)(-510) = 44.35$$

The gain with feedback is then

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-0.085}{44.35} = -1.92 \times 10^{-3}$$

and the voltage gain with feedback A_{vf} is

$$A_{vf} = \frac{V_o}{V_s} = A_f R_C = (-1.92 \times 10^{-3})(2.2 \times 10^3) = \mathbf{-4.2}$$

Without feedback ($R_E = 0$), the voltage gain is

$$A_v = \frac{-R_C}{r_e} = \frac{-2.2 \times 10^3}{7.5} = \mathbf{-293.3}$$

Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 14.12a provides voltage-shunt feedback. Referring to Fig. 14.2b and Table 14.1 and the op-amp ideal characteristics $I_i = 0$, $V_i = 0$, and voltage gain of infinity, we have

$$A = \frac{V_o}{I_i} = \infty \qquad \textbf{(14.24)}$$

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_o} \qquad \textbf{(14.25)}$$

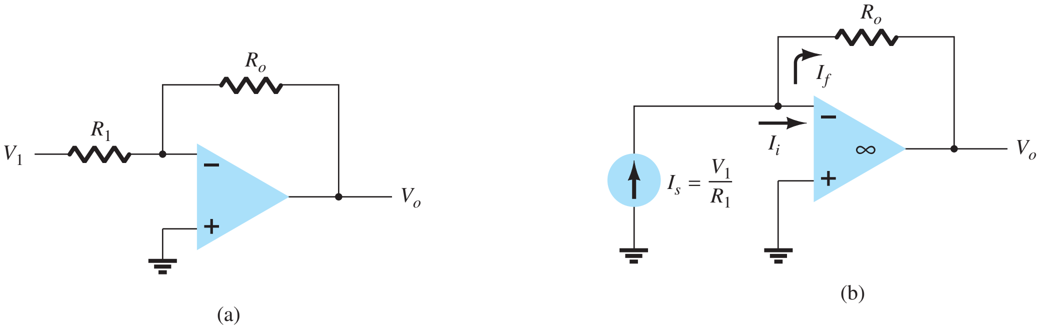


FIG. 14.12

Voltage-shunt negative feedback amplifier: (a) constant-gain circuit; (b) equivalent circuit.

The gain with feedback is then

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -R_o \qquad \textbf{(14.26)}$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_1} = (-R_o)\frac{1}{R_1} = \frac{-R_o}{R_1} \qquad \textbf{(14.27)}$$

The circuit of Fig. 14.13 is a voltage-shunt feedback amplifier using an FET with no feedback, $V_f = 0$.

$$A = \frac{V_o}{I_i} \cong -g_m R_D R_S \qquad \textbf{(14.28)}$$

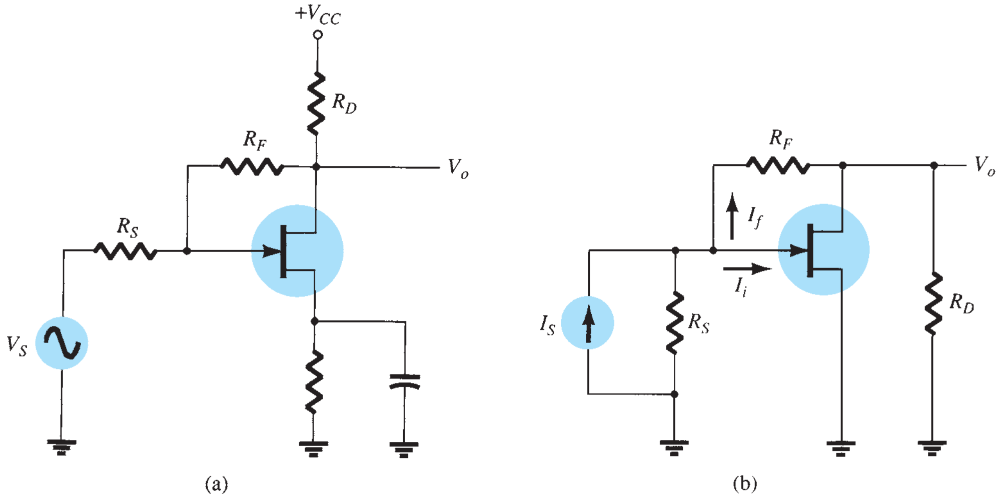


FIG. 14.13
Voltage-shunt feedback amplifier using an FET: (a) circuit; (b) equivalent circuit.

The feedback is

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_F} \tag{14.29}$$

With feedback, the gain of the circuit is

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + \beta A} = \frac{-g_m R_D R_S}{1 + (-1/R_F)(-g_m R_D R_S)}$$

$$= \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \tag{14.30}$$

The voltage gain of the circuit with feedback is then

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_s} = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}\left(\frac{1}{R_S}\right)$$

$$= \frac{-g_m R_D R_F}{R_F + g_m R_D R_S} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S} \tag{14.31}$$

EXAMPLE 14.6 Calculate the voltage gain with and without feedback for the circuit of Fig. 14.13a with values of $g_m = 5\text{ mS}$, $R_D = 5.1\text{ k}\Omega$, $R_S = 1\text{ k}\Omega$, and $R_F = 20\text{ k}\Omega$.

Solution: Without feedback, the voltage gain is

$$A_v = -g_m R_D = -(5 \times 10^{-3})(5.1 \times 10^3) = \mathbf{-25.5}$$

With feedback the gain is reduced to

$$A_{vf} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S}$$

$$= (-25.5)\frac{20 \times 10^3}{(20 \times 10^3) + (5 \times 10^{-3})(5.1 \times 10^3)(1 \times 10^3)}$$

$$= -25.5(0.44) = \mathbf{-11.2}$$

14.4 FEEDBACK AMPLIFIER—PHASE AND FREQUENCY CONSIDERATIONS

So far we have considered the operation of a feedback amplifier in which the feedback signal was *opposite* to the input signal—negative feedback. In any practical circuit this condition occurs only for some mid-frequency range of operation. We know that an amplifier gain will change with frequency, dropping off at high frequencies from the mid-frequency value. In addition, the phase shift of an amplifier will also change with frequency.

If, as the frequency increases, the phase shift changes, then some of the feedback signal will *add* to the input signal. It is then possible for the amplifier to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit be stable at *all* frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating.

Harry Nyquist was born in Sweden in 1889. He immigrated to the United States in 1907, and died in Texas in 1976. He received a Ph.D. in physics from Yale University in 1917. He worked at AT&T's Department of Development and Research and at Bell Telephone Laboratories from 1917 until his retirement in 1954. As an engineer at Bell Laboratories, Nyquist did important work on thermal noise, the stability of feedback amplifiers, telegraphy, facsimile, television, and other important communications problems. In 1932, he published a classic paper on stability of feedback amplifiers: The Nyquist stability criterion can now be found in all textbooks on feedback control theory.

(Courtesy of AT&T Archives and History Center)

Nyquist Criterion

In judging the stability of a feedback amplifier as a function of frequency, the βA product and the phase shift between input and output are the determining factors. One of the most popular techniques used to investigate stability is the Nyquist method. A Nyquist diagram is used to plot gain and phase shift as a function of frequency on a complex plane. The Nyquist plot, in effect, combines the two Bode plots of gain versus frequency and phase shift versus frequency on a single plot. A Nyquist plot is used to quickly show whether an amplifier is stable for all frequencies and how stable the amplifier is relative to some gain or phase-shift criteria.

As a start, consider the *complex plane* shown in Fig. 14.14. A few points of various gain (βA) values are shown at a few different phase-shift angles. By using the positive real axis as reference (0°), we see a magnitude of $\beta A = 2$ at a phase shift of 0° at point 1. Additionally, a magnitude of $\beta A = 3$ at a phase shift of $-135°$ is shown at point 2 and a magnitude/phase of $\beta A = 1$ at 180° is shown at point 3. Thus points on this plot can represent *both* gain magnitude of βA and phase shift. If the points representing gain and phase shift for an amplifier circuit are plotted at increasing frequency, then a Nyquist plot is obtained as shown by the plot in Fig. 14.15. At the origin, the gain is 0 at a frequency of 0 (for *RC*-type coupling). At increasing frequency, points f_1, f_2, and f_3 and the phase shift increase, as does the magnitude of βA. At a representative frequency f_4, the value of A is the vector length from the origin to point f_4 and the phase shift is the angle ϕ. At a frequency f_5, the phase shift is 180°. At higher frequencies, the gain is shown to decrease back to 0.

The Nyquist criterion for stability can be stated as follows:

The amplifier is unstable if the Nyquist curve encloses (encircles) the –1 point, and it is stable otherwise.

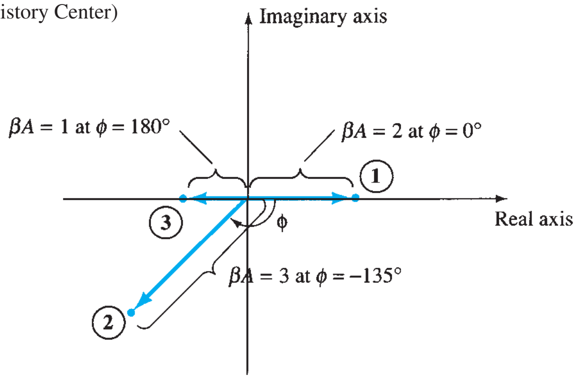

Imaginary axis
$\beta A = 1$ at $\phi = 180°$
$\beta A = 2$ at $\phi = 0°$
①
③
ϕ
Real axis
$\beta A = 3$ at $\phi = -135°$
②

FIG. 14.14
Complex plane showing typical gain-phase points.

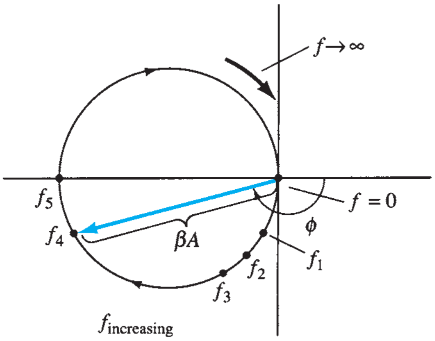


FIG. 14.15
Nyquist plot.

An example of the Nyquist criterion is demonstrated by the curves in Fig. 14.16. The Nyquist plot in Fig. 14.16a is stable since it does not encircle the -1 point, whereas that shown in Fig. 14.16b is unstable since the curve does encircle the -1 point. Keep in mind that encircling the -1 point means that at a phase shift of 180° the loop gain (βA) is greater than 1; therefore, the feedback signal is in phase with the input and large enough to result in a larger input signal than that applied, with the result that oscillation occurs.

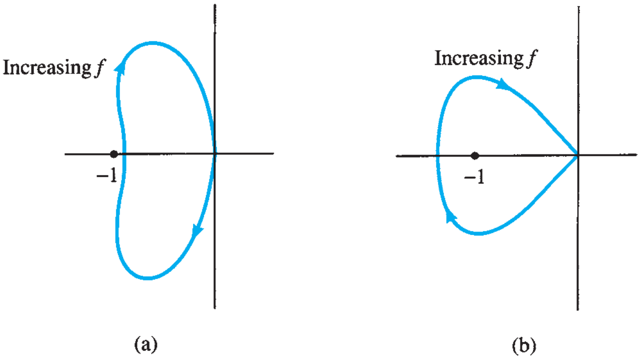


FIG. 14.16
Nyquist plots showing stability conditions: (a) stable; (b) unstable.

Gain and Phase Margins

From the Nyquist criterion, we know that a feedback amplifier is stable if the loop gain (βA) is less than unity (0 dB) when its phase angle is 180°. We can additionally determine some margins of stability to indicate how close to instability the amplifier is. That is, if the gain (βA) is less than unity but, say, 0.95 in value, this would not be as relatively stable as another amplifier having, say, $\beta A = 0.7$ (both measured at 180°). Of course, amplifiers with loop gains 0.95 and 0.7 are both stable, but one is closer to instability, if the loop gain increases, than the other. We can define the following terms:

Gain margin (GM) is defined as the negative of the value of $|\beta A|$ in decibels at the frequency at which the phase angle is 180°. Thus, 0 dB, equal to a value of $\beta A = 1$, is on the border of stability and any negative decibel value is stable. The GM may be evaluated in decibels from the curve of Fig. 14.17.

Phase margin (PM) is defined as the angle of 180° minus the magnitude of the angle at which the value $|\beta A|$ is unity (0 dB). The PM may also be evaluated directly from the curve of Fig. 14.17.

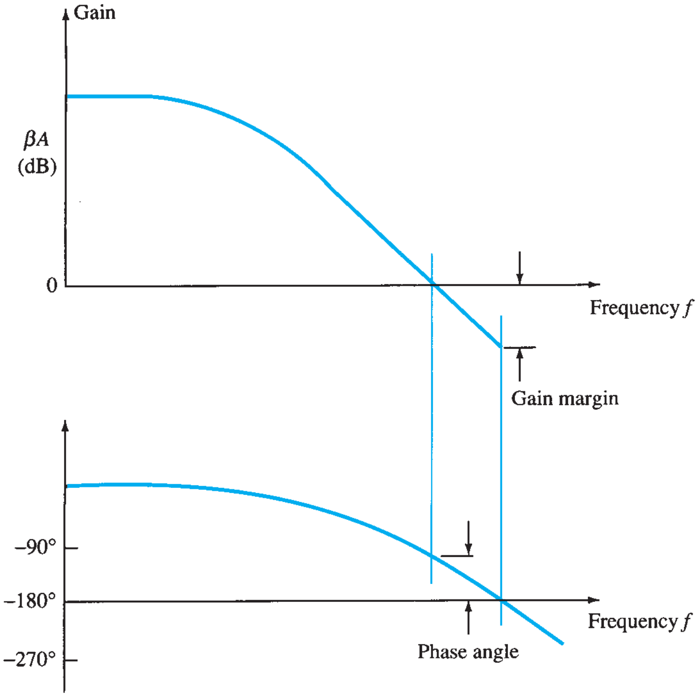


FIG. 14.17
Bode plots showing gain and phase margins.

14.5 OSCILLATOR OPERATION

The use of positive feedback that results in a feedback amplifier having closed-loop gain $|A_f|$ greater than 1 and satisfies the phase conditions will result in operation as an oscillator circuit. An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a *sinusoidal oscillator.* If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as a *pulse* or *square-wave oscillator.*

To understand how a feedback circuit performs as an oscillator, consider the feedback circuit of Fig. 14.18. When the switch at the amplifier input is open, no oscillation occurs. Consider that we have a *fictitious* voltage at the amplifier input V_i. This results in an output voltage $V_o = AV_i$ after the amplifier stage and in a voltage $V_f = \beta(AV_i)$ after the feedback stage. Thus, we have a feedback voltage $V_f = \beta AV_i$, where βA is referred to as the *loop gain.* If the circuits of the base amplifier and feedback network provide βA of a correct magnitude and phase, V_f can be made equal to V_i. Then, when the switch is closed and the fictitious voltage V_i is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits, resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition

$$\beta A = 1 \tag{14.32}$$

is met. This is known as the *Barkhausen criterion* for oscillation.

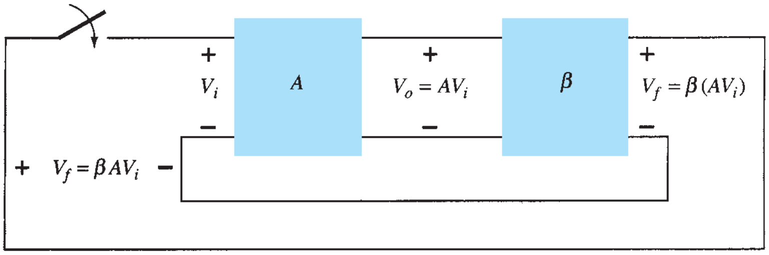


FIG. 14.18
Feedback circuit used as an oscillator.

In reality, no input signal is needed to start the oscillator going. Only the condition $\beta A = 1$ must be satisfied for self-sustained oscillations to result. In practice, βA is made greater than 1 and the system is started oscillating by amplifying noise voltage, which is always present. Saturation factors in the practical circuit provide an "average" value of βA of 1. The resulting waveforms are never exactly sinusoidal. However, the closer the value βA is to exactly 1, the more nearly sinusoidal is the waveform. Figure 14.19 shows how the noise signal results in a buildup of a steady-state oscillation condition.

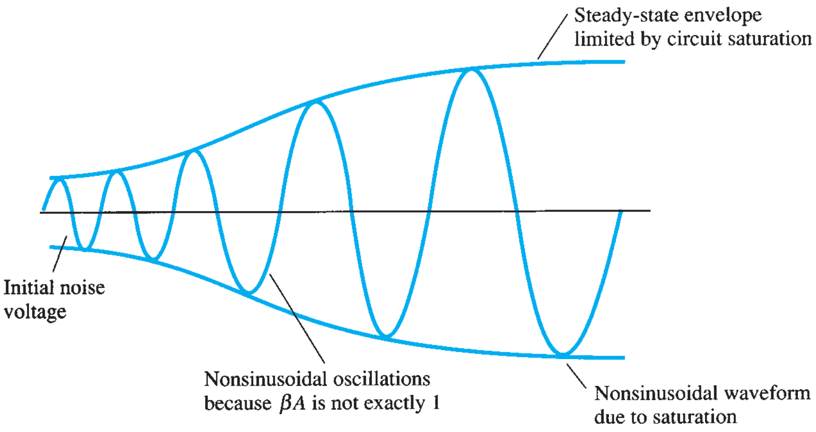

Steady-state envelope limited by circuit saturation
Initial noise voltage
Nonsinusoidal oscillations because βA is not exactly 1
Nonsinusoidal waveform due to saturation

FIG. 14.19
Buildup of steady-state oscillations.

Another way of seeing how the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic feedback equation (14.2), $A_f = A/(1 + \beta A)$. When $\beta A = -1$ or magnitude 1 at a phase angle of 180°, the denominator becomes 0 and the gain with feedback A_f becomes infinite. Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

The remainder of this chapter is devoted to various oscillator circuits that use a variety of components. Practical examples are included so that workable circuits in each of the various cases are discussed.

14.6 PHASE-SHIFT OSCILLATOR

An example of an oscillator circuit that follows the basic development of a feedback circuit is the *phase-shift oscillator*. An idealized version of this circuit is shown in Fig. 14.20. Recall that the requirements for oscillation are that the loop gain βA is greater than unity *and* that the phase shift around the feedback network is 180° (providing positive feedback). In the present idealization, we are considering the feedback network to be driven by a perfect source (zero source impedance) and the output of the feedback network to be connected into a perfect load (infinite load impedance). The idealized case will allow development of the theory behind the operation of the phase-shift oscillator. Practical circuit versions will then be considered.

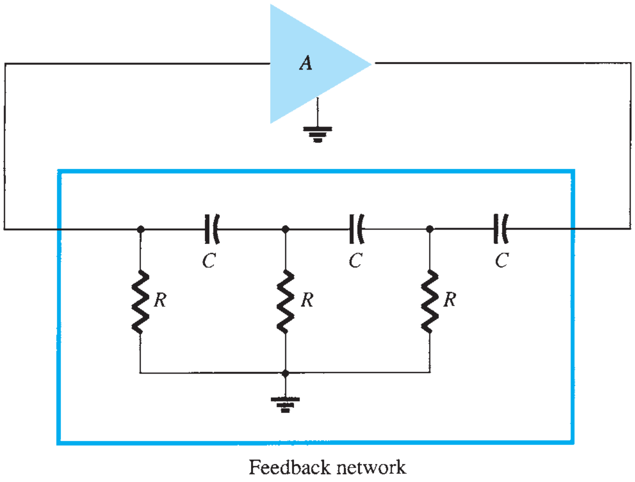


FIG. 14.20
Idealized phase-shift oscillator.

Concentrating our attention on the phase-shift network, we are interested in the attenuation of the network at the frequency at which the phase shift is exactly 180°. Using classical network analysis, we find that

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}} \tag{14.33}$$

$$\beta = \frac{1}{29} \tag{14.34}$$

and the phase shift is 180°.

For the loop gain βA to be greater than unity, the gain of the amplifier stage must be greater than $1/\beta$ or 29:

$$A > 29 \tag{14.35}$$

When considering the operation of the feedback network, one might naively select the values of R and C to provide (at a specific frequency) 60°-phase shift per section for three sections, resulting in a 180° phase shift, as desired. This, however, is not the case, since each section of the RC in the feedback network loads down the previous one. The net result that the *total* phase shift be 180° is all that is important. The frequency given by Eq. (14.33) is that at which the *total* phase shift is 180°. If one measured the phase shift per RC section, each section would not provide the same phase shift (although the overall phase shift is 180°). If it were desired to obtain exactly a 60° phase shift for each of three stages, then emitter-follower stages would be needed for each RC section to prevent each from being loaded from the following circuit.

FET Phase-Shift Oscillator

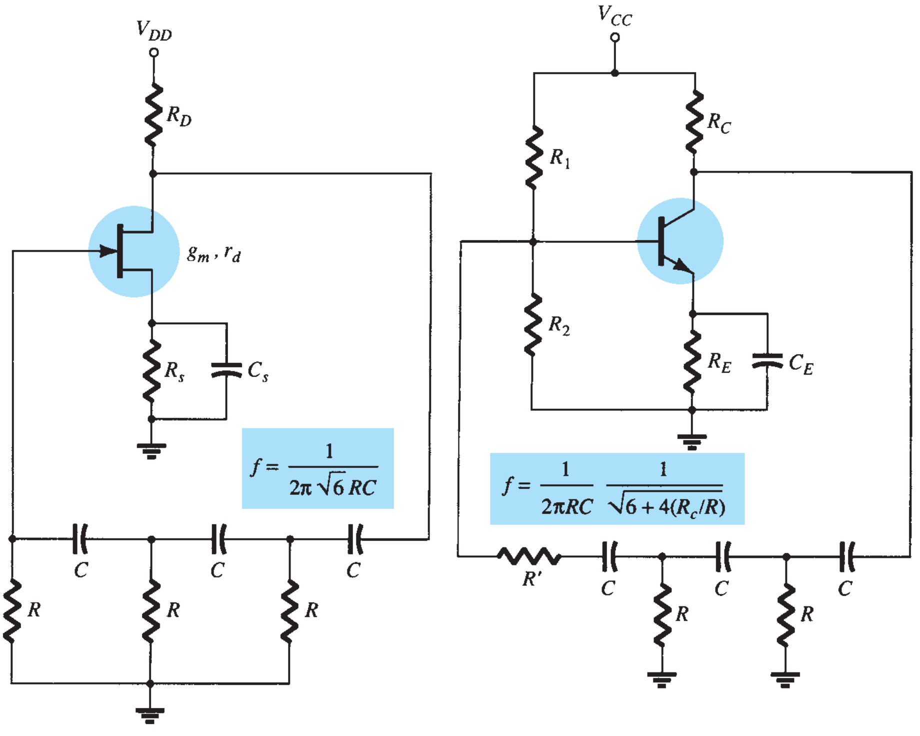
A practical version of a phase-shift oscillator circuit is shown in Fig. 14.21a. The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-biased with a capacitor bypassed source resistor R_S and a drain bias resistor R_D. The FET device parameters of interest are g_m and r_d. From FET amplifier theory, the amplifier gain magnitude is calculated from

$$|A| = g_m R_L \tag{14.36}$$

where R_L in this case is the parallel resistance of R_D and r_d,

$$R_L = \frac{R_D r_d}{R_D + r_d} \tag{14.37}$$

We shall assume as a very good approximation that the input impedance of the FET amplifier stage is infinite. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected. The output impedance of the amplifier stage given by R_L should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs. In practice, these considerations are not always negligible, and the amplifier stage gain is then selected somewhat larger than the needed factor of 29 to assure oscillator action.


V_{DD}
R_D
g_m, r_d
R_s
C_s
$f = \frac{1}{2\pi\sqrt{6}RC}$
C
C
C
R
R
R
V_{CC}
R_C
R_1
R_2
R_E
C_E
$f = \frac{1}{2\pi RC} \frac{1}{\sqrt{6 + 4(R_c/R)}}$
R'
C
C
C
R
R

(a) (b)

FIG. 14.21

Practical phase-shift oscillator circuits: (a) FET version; (b) BJT version.

EXAMPLE 14.7 It is desired to design a phase-shift oscillator (as in Fig. 14.21a) using an FET having $g_m = 5000\ \mu S$, $r_d = 40\ k\Omega$, and a feedback circuit value of $R = 10\ k\Omega$. Select the value of C for oscillator operation at 1 kHz and R_D for $A > 29$ to ensure oscillator action.

Solution: Equation (14.33) is used to solve for the capacitor value. Since $f = 1/2\pi RC\sqrt{6}$, we can solve for C:

$$C = \frac{1}{2\pi Rf\sqrt{6}} = \frac{1}{(6.28)(10 \times 10^3)(1 \times 10^3)(2.45)} = \mathbf{6.5\ nF}$$

Using Eq. (14.36), we solve for R_L to provide a gain of, say, $A = 40$ (this allows for some loading between R_L and the feedback network input impedance):

$$|A| = g_m R_L$$

$$R_L = \frac{|A|}{g_m} = \frac{40}{5000 \times 10^{-6}} = 8\ \text{k}\Omega$$

Using Eq. (14.37), we solve for $R_D = \mathbf{10\ k\Omega}$.

Transistor Phase-Shift Oscillator

If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance (h_{ie}) of the transistor. Of course, an emitter-follower input stage followed by a common-emitter amplifier stage could be used. If a single transistor stage is desired, however, the use of voltage-shunt feedback (as shown in Fig. 14.21b) is more suitable. In this connection, the feedback signal is coupled through the feedback resistor R' in *series* with the amplifier stage input resistance (R_i).

Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:

$$\boxed{f = \frac{1}{2\pi RC} \frac{1}{\sqrt{6 + 4(R_C/R)}}} \qquad \textbf{(14.38)}$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R} \qquad \textbf{(14.39)}$$

IC Phase-Shift Oscillator

As IC circuits have become more popular, they have been adapted to operate in oscillator circuits. One need buy only an op-amp to obtain an amplifier circuit of stabilized gain setting and incorporate some means of signal feedback to produce an oscillator circuit. For example, a phase-shift oscillator is shown in Fig. 14.22. The output of the op-amp is fed to a three-stage *RC* network, which provides the needed 180° of phase shift (at an attenuation factor of 1/29). If the op-amp provides gain (set by resistors R_i and R_f) of greater than 29,

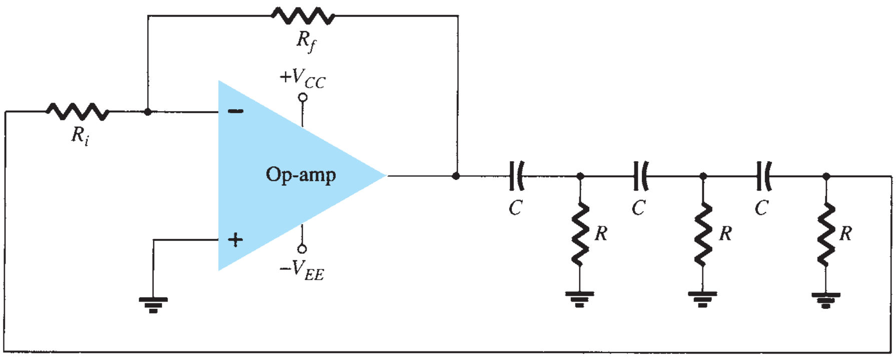


FIG. 14.22
Phase-shift oscillator using an op-amp.

a loop gain greater than unity results and the circuit acts as an oscillator [oscillator frequency is given by Eq. (14.33)].

14.7 WIEN BRIDGE OSCILLATOR

A practical oscillator circuit uses an op-amp and *RC* bridge circuit, with the oscillator frequency set by the *R* and *C* components. Figure 14.23 shows a basic version of a Wien bridge oscillator circuit. Note the basic bridge connection. Resistors R_1 and R_2 and capacitors C_1 and C_2 form the frequency-adjustment elements, and resistors R_3 and R_4 form part of the feedback path. The op-amp output is connected as the bridge input at points *a* and *c*. The bridge circuit output at points *b* and *d* is the input to the op-amp.

Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \tag{14.40}$$

and

$$\boxed{f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}} \tag{14.41}$$

If, in particular, the values are $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the resulting oscillator frequency is

$$\boxed{f_o = \frac{1}{2\pi RC}} \tag{14.42}$$

and

$$\boxed{\frac{R_3}{R_4} = 2} \tag{14.43}$$

Thus a ratio of R_3 to R_4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency calculated using Eq. (14.42).

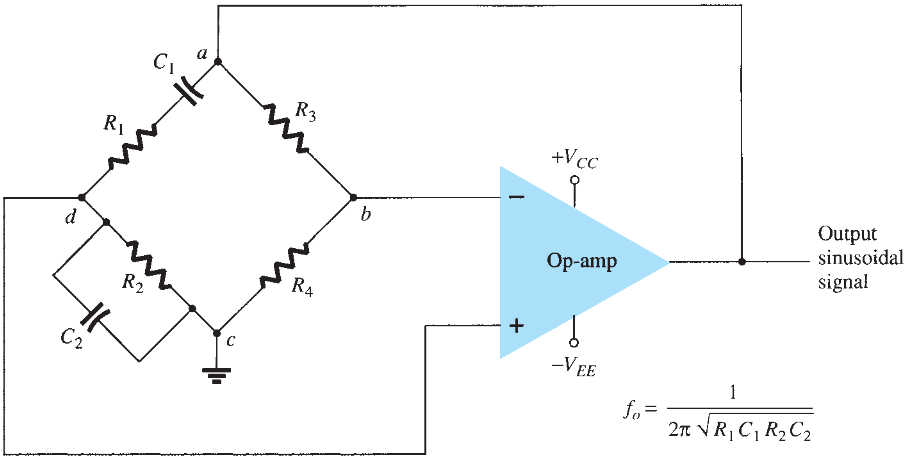


FIG. 14.23
Wien bridge oscillator circuit using an op-amp amplifier.

EXAMPLE 14.8 Calculate the resonant frequency of the Wien bridge oscillator of Fig. 14.24.

Solution: Using Eq. (14.42) yields

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi(51 \times 10^3)(0.001 \times 10^{-6})} = \mathbf{3120.7\ Hz}$$

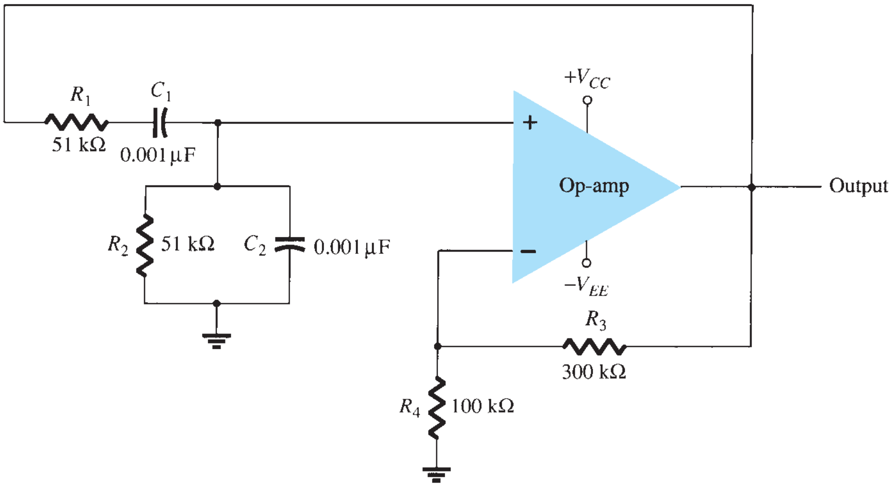


FIG. 14.24
Wien bridge oscillator circuit for Example 14.8.

EXAMPLE 14.9 Design the *RC* elements of a Wien bridge oscillator as in Fig. 14.24 for operation at $f_o = 10\text{ kHz}$.

Solution: Using equal values of *R* and *C*, we can select $R = 100\text{ k}\Omega$ and calculate the required value of *C* using Eq. (14.42):

$$C = \frac{1}{2\pi f_o R} = \frac{1}{6.28(10 \times 10^3)(100 \times 10^3)} = \frac{10^{-9}}{6.28} = \mathbf{159\ pF}$$

We can use $R_3 = 300\text{ k}\Omega$ and $R_4 = 100\text{ k}\Omega$ to provide a ratio R_3/R_4 greater than 2 for oscillation to take place.

14.8 TUNED OSCILLATOR CIRCUIT

Tuned-Input, Tuned-Output Oscillator Circuits

A variety of circuits can be built using that shown in Fig. 14.25 by providing tuning in both the input and output sections of the circuit. Analysis of the circuit of Fig. 14.25 reveals that the following types of oscillators are obtained when the reactance elements are as designated:

	Reactance Element		
Oscillator Type	X_1	X_2	X_3
Colpitts oscillator	*C*	*C*	*L*
Hartley oscillator	*L*	*L*	*C*
Tuned input, tuned output	*LC*	*LC*	—

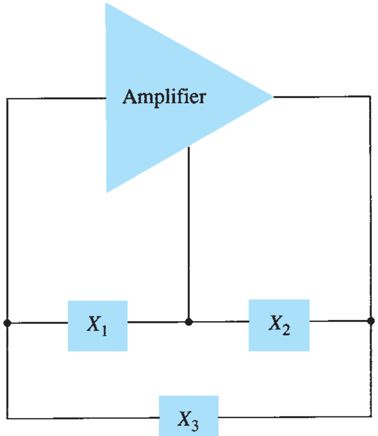


FIG. 14.25
Basic configuration of resonant circuit oscillator.

Colpitts Oscillator

FET Colpitts Oscillator A practical version of an FET Colpitts oscillator is shown in Fig. 14.26. The circuit is basically the same form as shown in Fig. 14.25 with the addition of the components needed for dc bias of the FET amplifier. The oscillator frequency can be found to be

$$\boxed{f_o = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}}} \qquad \mathbf{(14.44)}$$

where

$$C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} \qquad \mathbf{(14.45)}$$

Edwin Henry Colpitts (1872–1949) was a communications pioneer best known for his invention of the Colpitts oscillator. In 1915, his Western Electric team successfully demonstrated the first transatlantic radio telephone. In 1895 he entered Harvard University where he studied physics and mathematics. He received a B.A. in 1896 and a master's degree in 1897 from that institution. In 1899, Colpitts accepted a position with American Bell Telephone Company. He moved to Western Electric in 1907. His colleague Ralph Hartley invented an inductive coupling oscillator, which Colpitts improved in 1915. Colpitts served in the U.S. Army Signal Corps during World War I and spent some time in France as a staff officer involved with military communication. Colpitts died at home in 1949 in Orange, New Jersey.

(Courtesy of AT&T Archives and History Center)

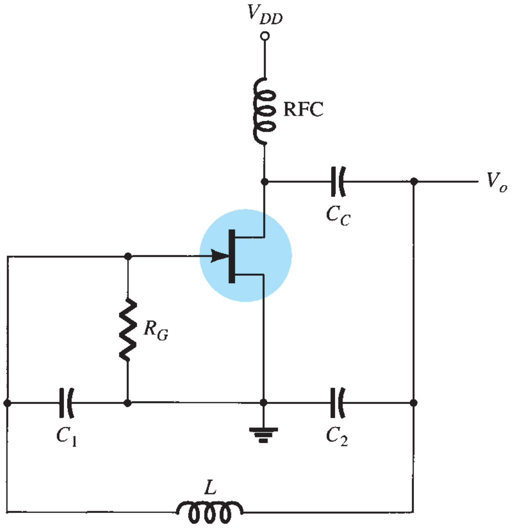


FIG. 14.26
FET Colpitts oscillator.

Transistor Colpitts Oscillator A transistor Colpitts oscillator circuit can be made as shown in Fig. 14.27. The circuit frequency of oscillation is given by Eq. (14.44).

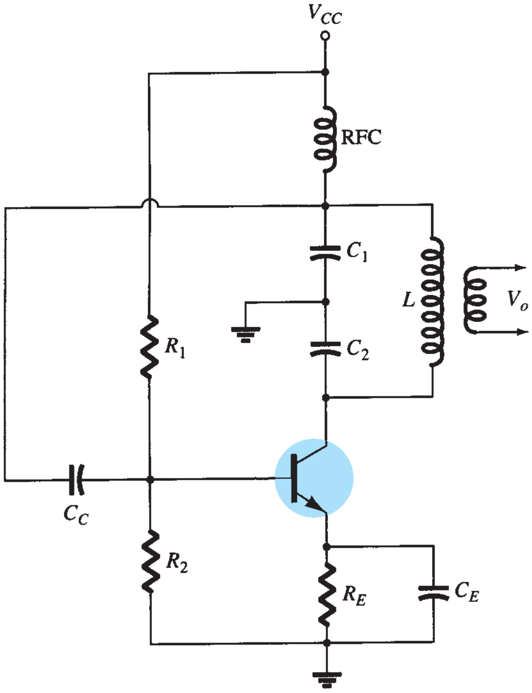


FIG. 14.27
Transistor Colpitts oscillator.

IC Colpitts Oscillator An op-amp Colpitts oscillator circuit is shown in Fig. 14.28. Again, the op-amp provides the basic amplification needed, and the oscillator frequency is set by an *LC* feedback network of a Colpitts configuration. The oscillator frequency is given by Eq. (14.44).

Hartley Oscillator

If the elements in the basic resonant circuit of Fig. 14.25 are X_1 and X_2 (inductors) and X_3 (capacitor), the circuit is a Hartley oscillator.

FET Hartley Oscillator An FET Hartley oscillator circuit is shown in Fig. 14.29. The circuit is drawn so that the feedback network conforms to the form shown in the basic resonant circuit (Fig. 14.25). Note, however, that inductors L_1 and L_2 have a mutual coupling M,

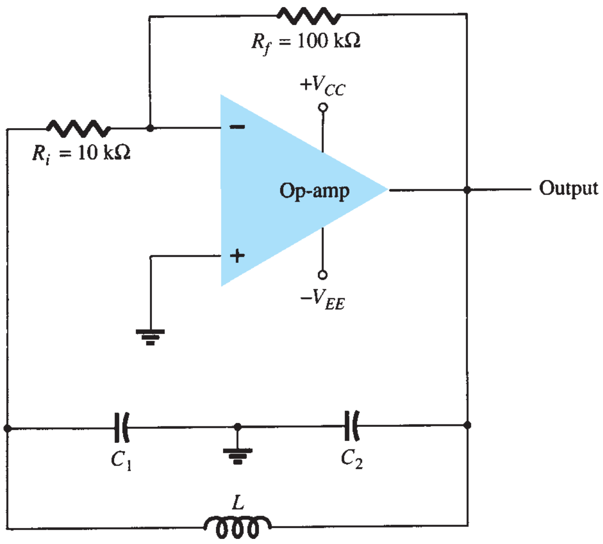


FIG. 14.28
Op-amp Colpitts oscillator.

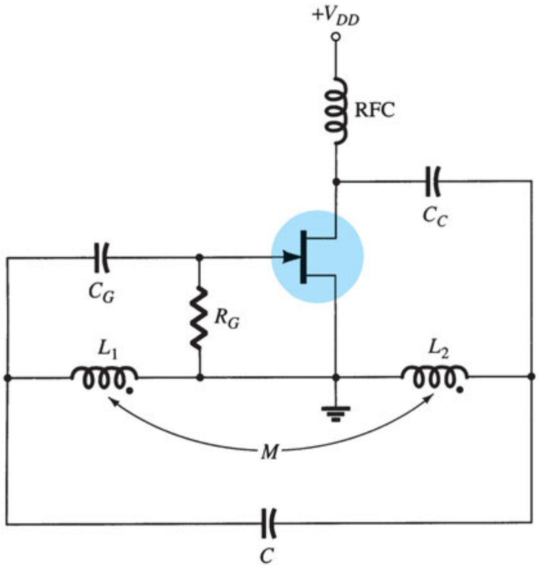


FIG. 14.29
FET Hartley oscillator.

which must be taken into account in determining the equivalent inductance for the resonant tank circuit. The circuit frequency of oscillation is then given approximately by

$$f_o = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} \tag{14.46}$$

with

$$\boxed{L_{\text{eq}} = L_1 + L_2 + 2M} \tag{14.47}$$

Transistor Hartley Oscillator Figure 14.30 shows a transistor Hartley oscillator circuit. The circuit operates at a frequency given by Eq. (14.46).

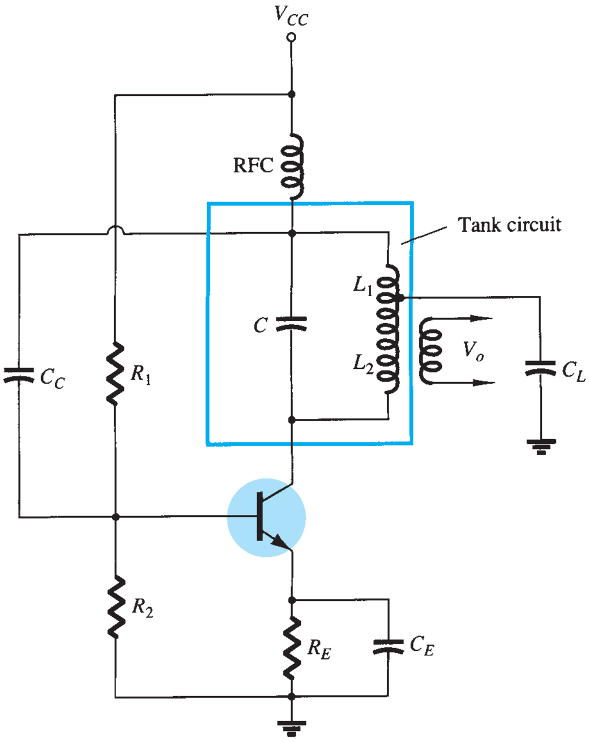


FIG. 14.30
Transistor Hartley oscillator circuit.

Ralph Hartley was born in Nevada in 1888 and attended the University of Utah, receiving an A.B. degree in 1909. He became a Rhodes Scholar at Oxford University in 1910 and received a B.A. degree in 1912 and a B.Sc. degree in 1913.

He returned to the United States and was employed at the Research Laboratory of the Western Electric Company. In 1915 he was in charge of radio receiver development for Bell Systems. He developed the Hartley oscillator and also a neutralizing circuit to eliminate triode singing resulting from internal coupling. During World War I he established the principles that led to sound-type directional finders. He retired from Bell Labs in 1950 and died on May 1, 1970.

(Courtesy of AT&T Archives and History Center)

14.9 CRYSTAL OSCILLATOR

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

Characteristics of a Quartz Crystal

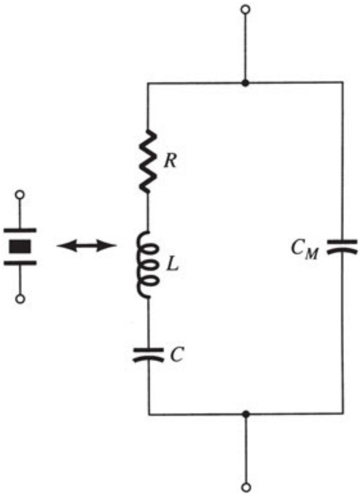


FIG. 14.31
Electrical equivalent circuit of a crystal.

A quartz crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across one set of its faces, a difference of potential develops across the opposite faces. This property of a crystal is called the *piezoelectric effect.* Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape.

When alternating voltage is applied to a crystal, mechanical vibrations are set up—these vibrations having a natural resonant frequency dependent on the crystal. Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical resonant circuit as shown in Fig. 14.31. The inductor L and capacitor C represent electrical equivalents of crystal mass and compliance, respectively, whereas resistance R is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance C_M represents the capacitance due to mechanical mounting of the crystal. Because the crystal losses, represented by R, are small, the equivalent crystal Q (quality factor) is high—typically 20,000. Values of Q up to almost 10^6 can be achieved by using crystals.

The crystal as represented by the equivalent electrical circuit of Fig. 14.31 can have two resonant frequencies. One resonant condition occurs when the reactances of the series RLC leg are equal (and opposite). For this condition, the *series-resonant* impedance is very low (equal to R). The other resonant condition occurs at a higher frequency when the reactance of the series-resonant leg equals the reactance of capacitor C_M. This is a parallel resonance or antiresonance condition of the crystal. At this frequency, the crystal offers a very high impedance to the external circuit. The impedance versus frequency of the crystal is shown in Fig. 14.32. To use the crystal properly, it must be connected in a circuit so that its low impedance in the series-resonant operating mode or high impedance in the antiresonant operating mode is selected.

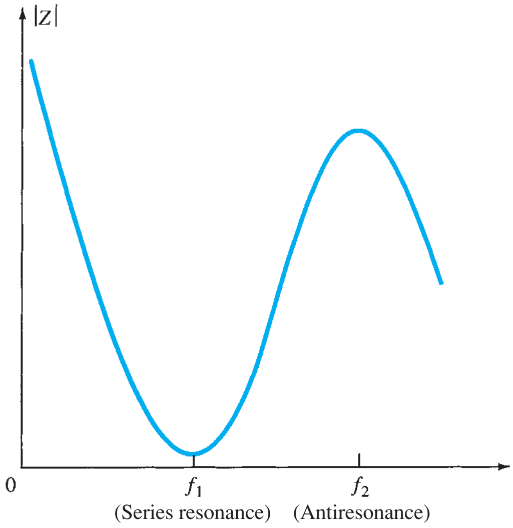


FIG. 14.32
Crystal impedance versus frequency.

Series-Resonant Circuits

To excite a crystal for operation in the series-resonant mode, it may be connected as a series element in a feedback path. At the series-resonant frequency of the crystal, its impedance is smallest and the amount of (positive) feedback is largest. A typical transistor circuit is

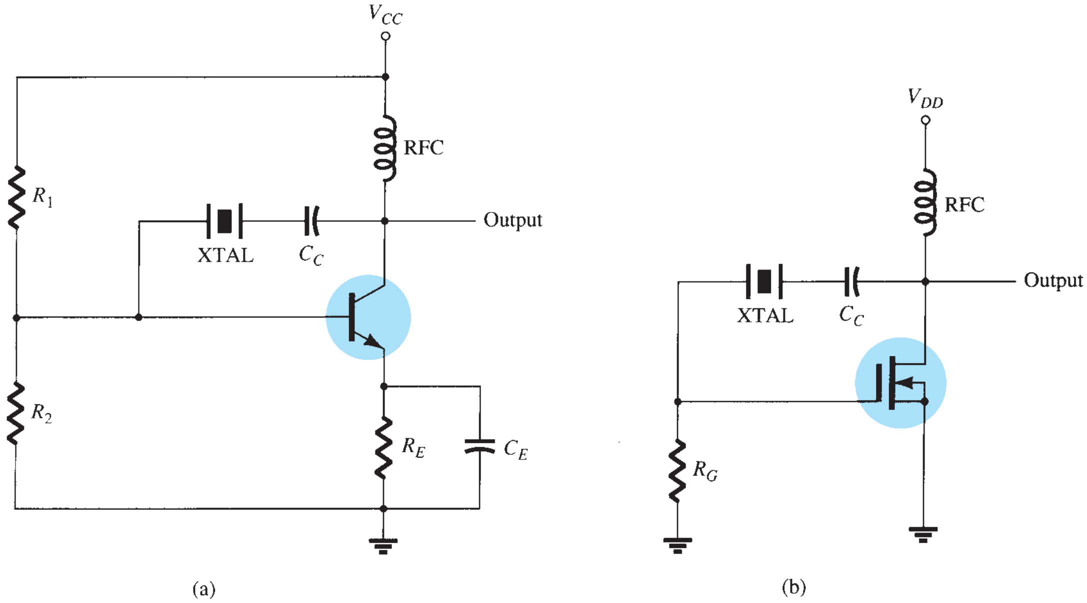


FIG. 14.33

Crystal-controlled oscillator using a crystal (XTAL) in a series-feedback path: (a) BJT circuit; (b) FET circuit.

shown in Fig. 14.33. Resistors R_1, R_2, and R_E provide a voltage-divider stabilized dc bias circuit. Capacitor C_E provides ac bypass of the emitter resistor, and the RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series-resonant mode). The coupling capacitor C_C has negligible impedance at the circuit operating frequency but blocks any dc between collector and base.

The resulting circuit frequency of oscillation is set, then, by the series-resonant frequency of the crystal. Changes in supply voltage, transistor device parameters, and so on, have no effect on the circuit operating frequency, which is held stabilized by the crystal. The circuit frequency stability is set by the crystal frequency stability, which is good.

Parallel-Resonant Circuits

Since the parallel-resonant impedance of a crystal is a maximum value, it is connected in shunt. At the parallel-resonant operating frequency, a crystal appears as an inductive reactance of largest value. Figure 14.34 shows a crystal connected as the inductor element in a

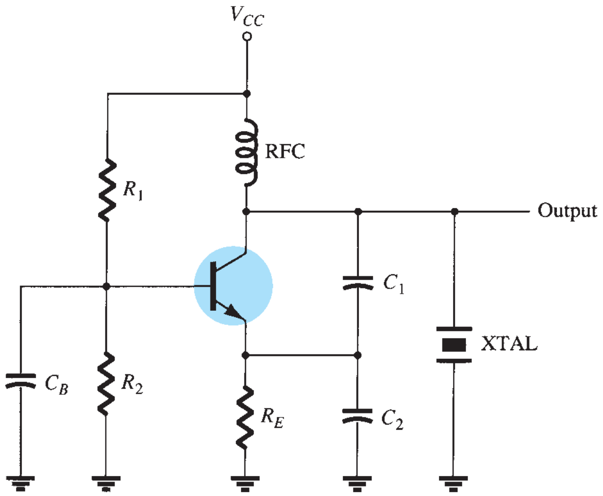


FIG. 14.34

Crystal-controlled oscillator operating in parallel-resonant mode.

modified Colpitts circuit. The basic dc bias circuit should be evident. Maximum voltage is developed across the crystal at its parallel-resonant frequency. The voltage is coupled to the emitter by a capacitor voltage divider—capacitors C_1 and C_2.

A *Miller crystal-controlled oscillator* circuit is shown in Fig. 14.35. A tuned *LC* circuit in the drain section is adjusted near the crystal parallel-resonant frequency. The maximum gate–source signal occurs at the crystal antiresonant frequency, controlling the circuit operating frequency.

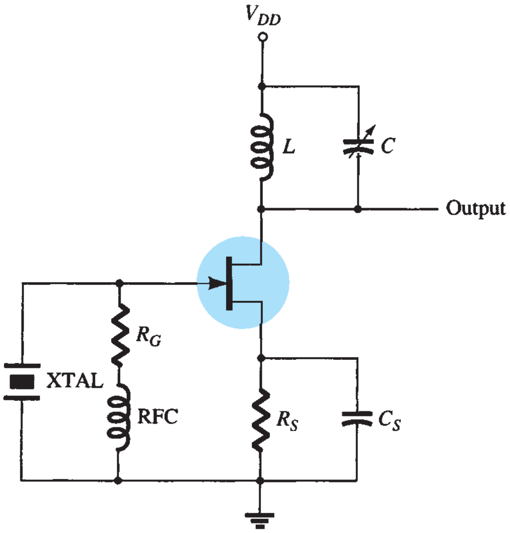


FIG. 14.35
Miller crystal-controlled oscillator.

Crystal Oscillator

An op-amp can be used in a crystal oscillator as shown in Fig. 14.36. The crystal is connected in the series-resonant path and operates at the crystal series-resonant frequency. The present circuit has a high gain, so that an output square-wave signal results as shown in the figure. A pair of Zener diodes is shown at the output to provide output amplitude at exactly the Zener voltage (V_Z).

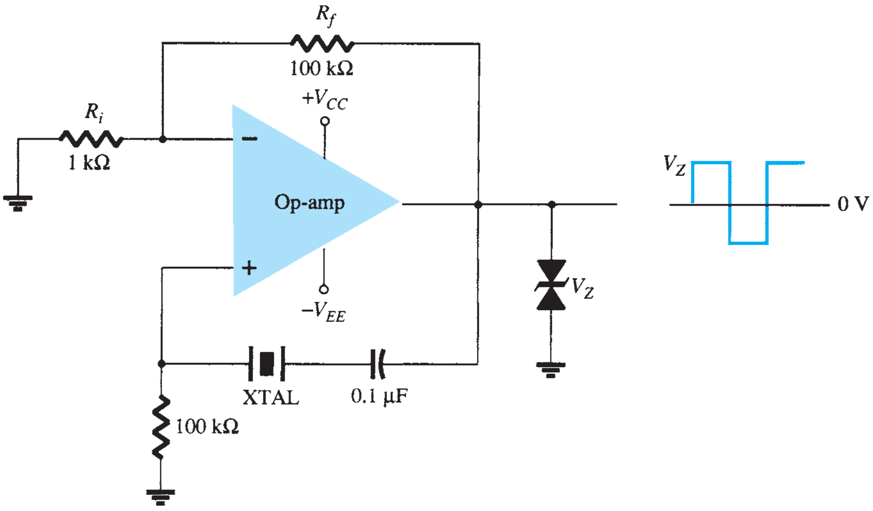


FIG. 14.36
Crystal oscillator using an op-amp.

14.10 UNIJUNCTION OSCILLATOR

A particular device, the unijunction transistor, can be used in a single-stage oscillator circuit to provide a pulse signal suitable for digital-circuit applications. The unijunction transistor can be used in what is called a *relaxation oscillator* as shown by the basic circuit of Fig. 14.37. Resistor R_T and capacitor C_T are the timing components that set the circuit oscillating rate. The oscillating frequency may be calculated using Eq. (14.48), which includes the unijunction transistor *intrinsic stand-off ratio* η as a factor (in addition to R_T and C_T) in the oscillator operating frequency:

$$\boxed{f_o \cong \frac{1}{R_T C_T \ln[1/(1-\eta)]}} \tag{14.48}$$

Typically, a unijunction transistor has a stand-off ratio from 0.4 to 0.6. Using a value of $\eta = 0.5$, we get

$$\begin{aligned} f_o &\cong \frac{1}{R_T C_T \ln[1/(1-0.5)]} = \frac{1.44}{R_T C_T \ln 2} = \frac{1.44}{R_T C_T} \\ &\cong \frac{1.5}{R_T C_T} \end{aligned} \tag{14.49}$$

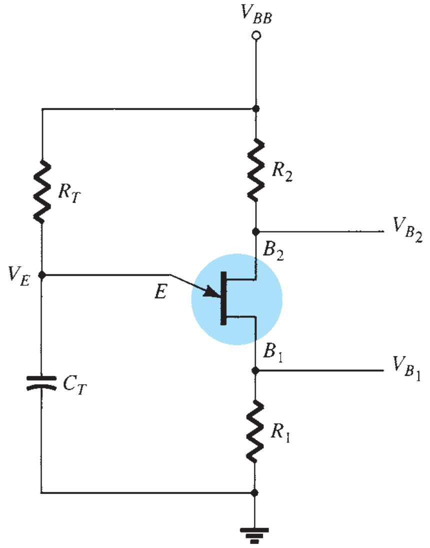


FIG. 14.37
Basic unijunction oscillator circuit.

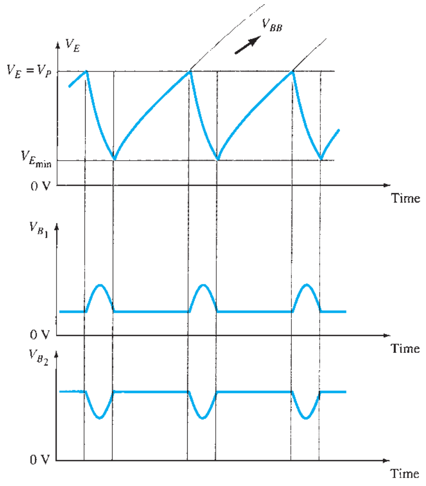
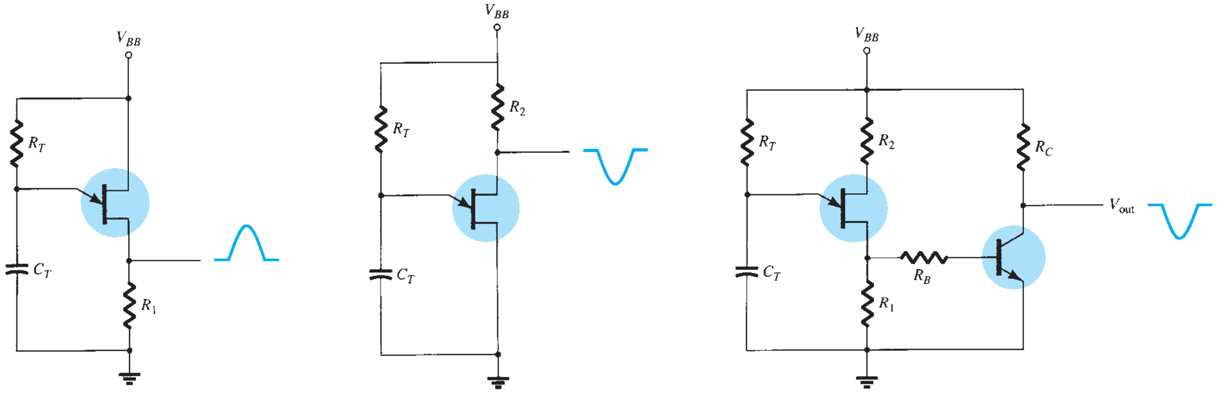


FIG. 14.38
Unijunction oscillator waveforms.

Capacitor C_T is charged through resistor R_T toward supply voltage V_{BB}. As long as the capacitor voltage V_E is below a stand-off voltage (V_P) set by the voltage across $B_1 - B_2$ and the transistor stand-off ratio η,

$$V_P = \eta V_{B_1} V_{B_2} - V_D \tag{14.50}$$

the unijunction emitter lead appears as an open circuit. When the emitter voltage across capacitor C_T exceeds this value (V_P), the unijunction circuit fires, discharging the capacitor, after which a new charge cycle begins. When the unijunction fires, a voltage rise is developed across R_1 and a voltage drop is developed across R_2 as shown in Fig. 14.38. The signal at the emitter is a sawtooth voltage waveform that at base 1 is a positive-going pulse and at base 2 is a negative-going pulse. A few circuit variations of the unijunction oscillator are provided in Fig. 14.39.



(a) (b) (c)

FIG. 14.39

Some unijunction oscillator circuit configurations.

14.11 SUMMARY

Equations

Voltage-series feedback:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}, \qquad Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A)Z_i = Z_i(1 + \beta A),$$

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{(1 + \beta A)}$$

Voltage-shunt feedback:

$$A_f = \frac{A}{1 + \beta A}, \qquad Z_{if} = \frac{Z_i}{(1 + \beta A)}$$

Current-series feedback:

$$Z_{if} = \frac{V}{I} = Z_i(1 + \beta A), \qquad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

Current shunt feedback:

$$Z_{if} = \frac{Z_i}{(1 + \beta A)}, \qquad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

Phase-shift oscillator:

$$f = \frac{1}{2\pi RC\sqrt{6}}, \qquad \beta = \frac{1}{29}$$

Wien bridge oscillator:

$$f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

Colpitts oscillator:

$$f_o = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} \qquad \text{where} \qquad C_{\text{eq}} = \frac{C_1C_2}{C_1 + C_2}$$

Hartley oscillator:

$$f_o = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} \qquad \text{where} \qquad L_{\text{eq}} = L_1 + L_2 + 2M$$

Unijunction oscillator:

$$f_o \cong \frac{1}{R_T C_T \ln[1/(1 - \eta)]}$$

14.12 COMPUTER ANALYSIS

Multisim

Example 14.10—IC Phase-Shift Oscillator Using Multisim, we draw a phase-shift oscillator as shown in Fig. 14.40. The diode network helps the circuit go into self-oscillation, with the output frequency calculated using

$$\begin{aligned} f_o &= 1/(2\pi\sqrt{6}RC) \\ &= 1/[2\pi\sqrt{6}(20 \times 10^3)(0.001 \times 10^{-6})] = 3{,}248.7\text{ Hz} \end{aligned}$$

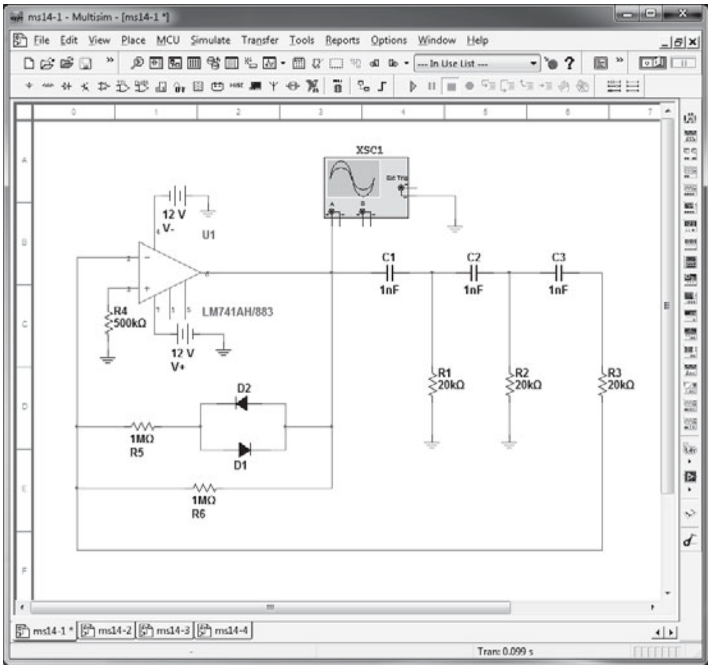
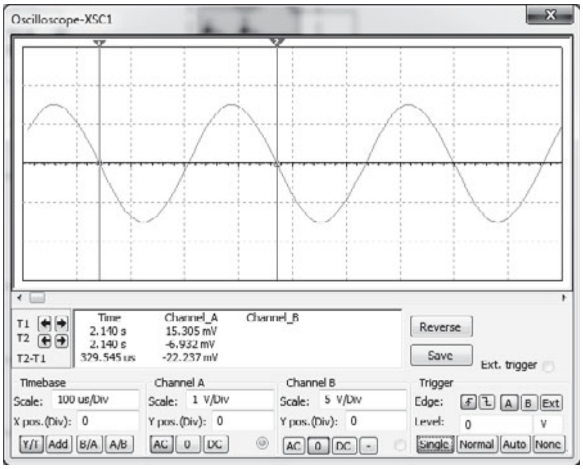

ms14-1 - Multisim - [ms14-1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
XSC1
Ext Trig
A
B
12 V
V-
U1
LM741AH/883
R4
500kΩ
12 V
V+
C1
1nF
C2
1nF
C3
1nF
R1
20kΩ
R2
20kΩ
R3
20kΩ
D2
D1
1MΩ
R5
1MΩ
R6
ms14-1 * ms14-2 ms14-3 ms14-4
Tran: 0.099 s

FIG. 14.40

Phase-shift oscillator using Multisim.

The oscilloscope waveform in Fig. 14.41 shows a cycle in about three divisions. The measured frequency for the scope set at 0.1 ms/div is

$$f_{\text{measured}} = 1/(3\text{ div} \times 0.1\text{ ms/div}) = 3{,}333\text{ Hz}$$


Oscilloscope-XSC1
Reverse
Save
Ext. trigger
Edge:
A
B
Ext
Y/T
Add
B/A
A/B
AC
0
DC
AC
0
DC
-
Single
Normal
Auto
None

	Time	Channel_A	Channel_B
T1	2.140 s	15.305 mV	
T2	2.140 s	-6.932 mV	
T2-T1	329.545 us	-22.237 mV	

Timebase
Scale: 100 us/Div
X pos.(Div): 0

Channel A
Scale: 1 V/Div
Y pos.(Div): 0

Channel B
Scale: 5 V/Div
Y pos.(Div): 0

Trigger
Level: 0 V

FIG. 14.41

Oscilloscope waveform.

Example 14.11—IC Wien Bridge Oscillator Using Multisim, we construct an IC Wien bridge oscillator as shown in Fig. 14.42a. The oscillator frequency is calculated using

$$f_o = 1/(2\pi\sqrt{R_1C_1R_2C_2})$$

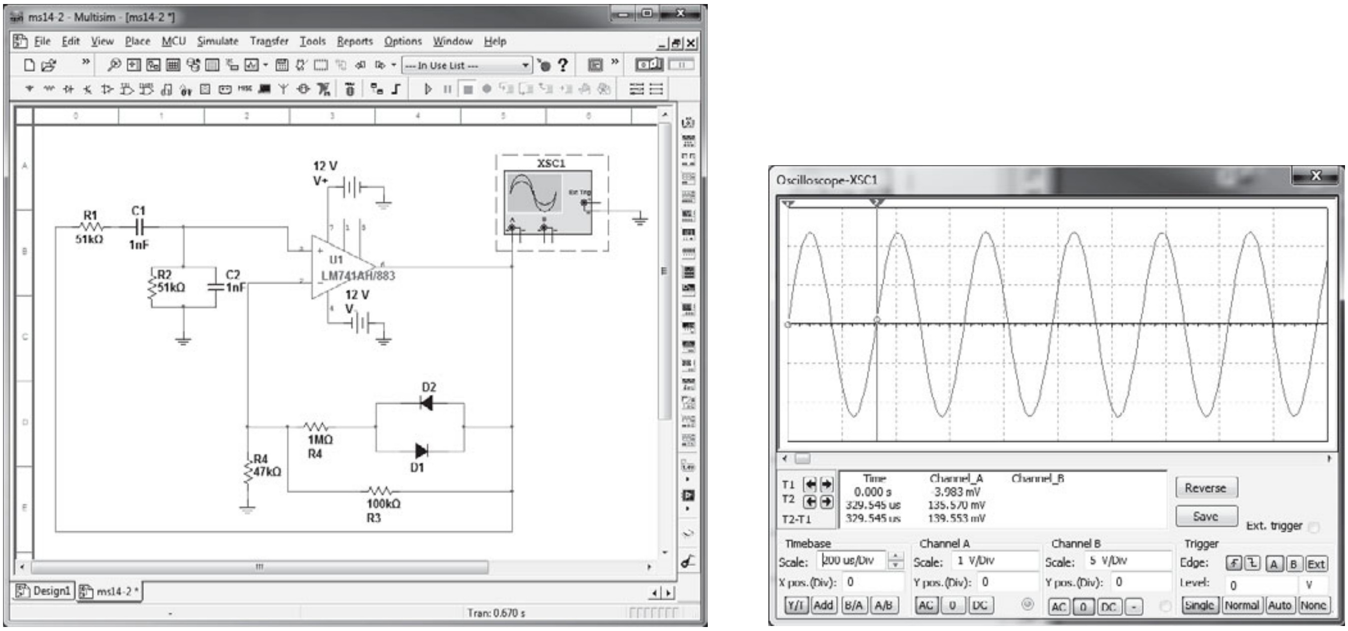
which, for $R_1 = R_2 = R$ and $C_1 = C_2 = C$, is

$$f_o = 1/(2\pi RC) = \frac{1}{2\pi(51\text{ k})(1nf)}$$

$$= 312\text{ Hz}$$

The oscilloscope waveform in Fig. 14.42b shows the resonating waveform with cursors $T2 - T1 = 329.545\ \mu\text{S}$, the scope frequency is

$$f = \frac{1}{T} = \frac{1}{329.545\ \mu\text{S}} \cong 3{,}034.5\text{ Hz}$$


ms14-2 - Multisim - [ms14-2 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In Use List ---
12 V
V+
XSC1
R1
51kΩ
C1
1nF
R2
51kΩ
C2
1nF
U1
LM741AH/883
12 V
V-
D2
1MΩ
R4
D1
R4
47kΩ
100kΩ
R3
Design1
ms14-2 *
Tran: 0.670 s
Oscilloscope-XSC1
Reverse
Save
Ext. trigger
Y/T Add B/A A/B
AC 0 DC
AC 0 DC -
Single Normal Auto None

	Time	Channel_A	Channel_B
T1	0.000 s	3.983 mV	
T2	329.545 us	135.570 mV	
T2-T1	329.545 us	139.553 mV	

Timebase
Scale: 200 us/Div
X pos.(Div): 0

Channel A
Scale: 1 V/Div
Y pos.(Div): 0

Channel B
Scale: 5 V/Div
Y pos.(Div): 0

Trigger
Edge: A
Level: 0 V

(a) (b)

FIG. 14.42

(a) Wien bridge oscillator using Multisim; (b) scope waveform.

Example 14.12—IC Colpitts Oscillator Using Multisim, we construct a Colpitts oscillator as shown in Fig. 14.43a.

Using Eq. 14.45

$$Ce_1 = \frac{C_1C_2}{C_1 + C_2} = \frac{(150\text{ pF})(150\text{ pF})}{(150\text{ pF} + 150\text{ pF})} = 75\text{ pF}$$

The oscillator frequency for this circuit is then (Eq. 14.44)

$$f_o = \frac{1}{(2\pi\sqrt{LC_{\text{eq}}})}$$

$$= \frac{1}{2\pi\sqrt{(100\ \mu\text{H})(75\text{ pF})}}$$

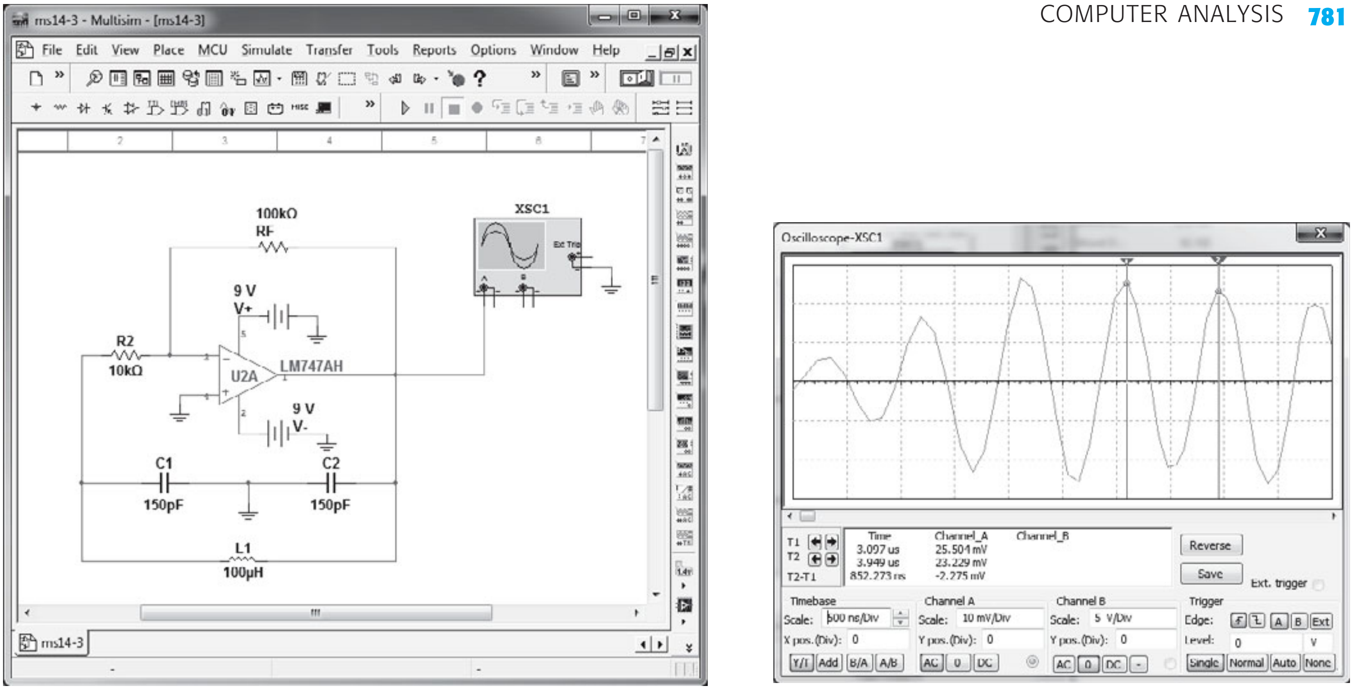
$$= 1{,}837{,}762.985\text{ Hz}$$

$$\cong 1.8\text{ MHz}$$

Fig. 14.43b shows the oscilloscope waveform with

$$f = \frac{1}{T} = \frac{1}{(852.273\ \mu\text{S})}$$

$$\cong 1.2\text{ MHz}$$


ms14-3 - Multisim - [ms14-3]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
100kΩ
RF
XSC1
Ext Trig
A
B
9 V
V+
R2
10kΩ
U2A
LM747AH
9 V
V-
C1
150pF
C2
150pF
L1
100μH
ms14-3
Oscilloscope-XSC1

```
      Time        Channel_A    Channel_B
T1    3.097 us    25.504 mV
T2    3.949 us    23.229 mV
T2-T1 852.273 ns  -2.275 mV

Timebase                 Channel A              Channel B              Trigger
Scale: 500 ns/Div        Scale: 10 mV/Div       Scale: 5 V/Div         Edge:
X pos.(Div): 0           Y pos.(Div): 0         Y pos.(Div): 0         Level: 0 V
```

Reverse
Save
Ext. trigger
Y/T Add B/A A/B
AC 0 DC
AC 0 DC -
A B Ext
Single Normal Auto None

(a)

(b)

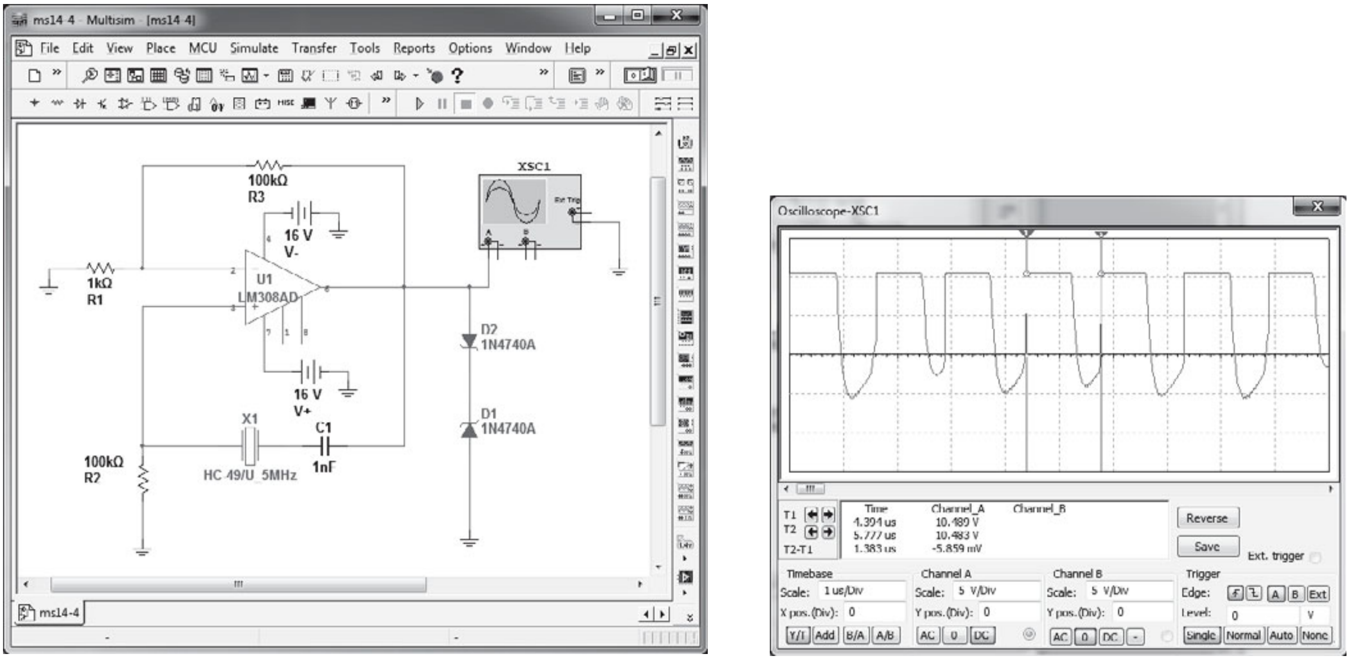
FIG. 14.43

(a) IC Colpitts oscillator using Multisim; (b) scope waveform.

Example 14.13–Crystal Oscillator Using Multisim, we draw a crystal oscillator circuit as shown in Fig. 14.44a. The oscillator frequency is kept from changing by the crystal. The waveform in Fig. 14.44b shows the period to be about 2.383 μS.

The frequency is then

$$f = 1/T = 1/2.383\ \mu\text{s} = 0.42\ \text{MHz}$$


ms14 4 Multisim [ms14 4]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
100kΩ
R3
XSC1
Ext Trig
A
B
16 V
V-
1kΩ
R1
U1
LM308AD
D2
1N4740A
16 V
V+
X1
C1
1nF
D1
1N4740A
100kΩ
R2
HC 49/U_5MHz
ms14-4
Oscilloscope-XSC1

```
      Time        Channel_A    Channel_B
T1    4.394 us    10.489 V
T2    5.777 us    10.483 V
T2-T1 1.383 us    -5.859 mV

Timebase                 Channel A              Channel B              Trigger
Scale: 1 us/Div          Scale: 5 V/Div         Scale: 5 V/Div         Edge:
X pos.(Div): 0           Y pos.(Div): 0         Y pos.(Div): 0         Level: 0 V
```

Reverse
Save
Ext. trigger
Y/T Add B/A A/B
AC 0 DC
AC 0 DC -
A B Ext
Single Normal Auto None

(a)

(b)

FIG. 14.44

(a) Crystal oscillator using Multisim; (b) oscilloscope output using Multisim.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

14.2 Feedback Connection Types

1. Calculate the gain of a negative-feedback amplifier having $A = -2000$ and $\beta = -1/10$.

2. If the gain of an amplifier changes from a value of -1000 by 10%, calculate the gain change if the amplifier is used in a feedback circuit having $\beta = -1/20$.

3. Calculate the gain, input, and output impedances of a voltage-series feedback amplifier having $A = -300$, $R_i = 1.5\ \text{k}\Omega$, $R_o = 50\ \text{k}\Omega$, and $\beta = -1/15$.

14.3 Practical Feedback Circuits

***4.** Calculate the gain with and without feedback for an FET amplifier as in Fig. 14.7 for circuit values $R_1 = 800\ \text{k}\Omega$, $R_2 = 200\ \Omega$, $R_o = 40\ \text{k}\Omega$, $R_D = 8\ \text{k}\Omega$, and $g_m = 5000\ \mu\text{S}$.

5. For a circuit as in Fig. 14.11 and the following circuit values, calculate the circuit gain and the input and output impedances with and without feedback: $R_B = 600\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $R_C = 4.7\ \text{k}\Omega$, and $\beta = 75$. Use $V_{CC} = 16\ \text{V}$.

14.6 Phase-Shift Oscillator

6. An FET phase-shift oscillator having $g_m = 6000\ \mu\text{S}$, $r_d = 36\ \text{k}\Omega$, and feedback resistor $R = 12\ \text{k}\Omega$ is to operate at 2.5 kHz. Select C for specified oscillator operation.

7. Calculate the operating frequency of a BJT phase-shift oscillator as in Fig. 14.21b for $R = 6\ \text{k}\Omega$, $C = 1500\ \text{pF}$, and $R_C = 18\ \text{k}\Omega$.

14.7 Wien Bridge Oscillator

8. Calculate the frequency of a Wien bridge oscillator circuit (as in Fig. 14.23) when $R = 10\ \text{k}\Omega$ and $C = 2400\ \text{pF}$.

14.8 Tuned Oscillator Circuit

9. For an FET Colpitts oscillator as in Fig. 14.26 and the following circuit values determine the circuit oscillation frequency: $C_1 = 750\ \text{pF}$, $C_2 = 2500\ \text{pF}$, and $L = 40\ \mu\text{H}$.

10. For the transistor Colpitts oscillator of Fig. 14.27 and the following circuit values, calculate the oscillation frequency: $L = 100\ \mu\text{H}$, $L_{RFC} = 0.5\ \text{mH}$, $C_1 = 0.005\ \mu\text{F}$, $C_2 = 0.01\ \mu\text{F}$, and $C_C = 10\ \mu\text{F}$.

11. Calculate the oscillator frequency for an FET Hartley oscillator as in Fig. 14.29 for the following circuit values: $C = 250\ \text{pF}$, $L_1 = 1.5\ \text{mH}$, $L_2 = 1.5\ \text{mH}$, and $M = 0.5\ \text{mH}$.

12. Calculate the oscillation frequency for the transistor Hartley circuit of Fig. 14.30 and the following circuit values: $L_{RFC} = 0.5\ \text{mH}$, $L_1 = 750\ \mu\text{H}$, $L_2 = 750\ \mu\text{H}$, $M = 150\ \mu\text{H}$, and $C = 150\ \text{pF}$.

14.9 Crystal Oscillator

13. Draw circuit diagrams of (a) a series-operated crystal oscillator and (b) a shunt-excited crystal oscillator.

14.10 Unijunction Oscillator

14. Design a unijunction oscillator circuit for operation at (a) 1 kHz and (b) 150 kHz.

15

Power Supplies (Voltage Regulators)

CHAPTER OBJECTIVES

- How power supply circuits operate
- Operation of RC filters
- Discrete voltage regulator operation
- About practical IC voltage regulators

15.1 INTRODUCTION

Chapter 15 introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. (Refer to Chapter 2 for the initial description of diode rectifier circuits.) Starting with an ac voltage, we obtain a steady dc voltage by rectifying the ac voltage, then filtering to a dc level, and, finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in Fig. 15.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage, which is initially filtered by a basic capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage, but also remains at the same dc value even if the input dc voltage varies somewhat or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

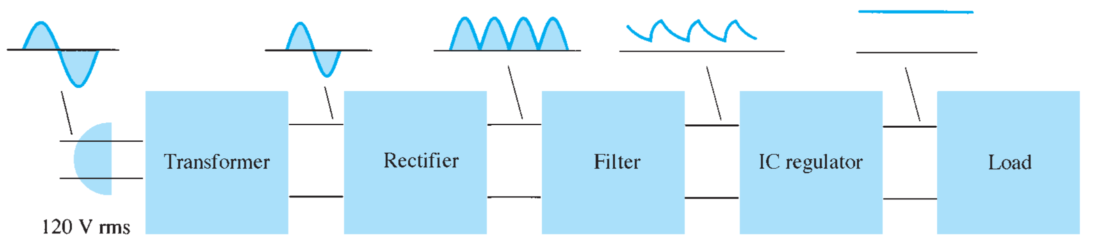


FIG. 15.1
Block diagram showing parts of a power supply.

15.2 GENERAL FILTER CONSIDERATIONS

A rectifier circuit is necessary to convert a signal having zero average value into one that has a nonzero average. The output resulting from a rectifier is a pulsating dc voltage and not yet suitable as a battery replacement. Such a voltage could be used in, say, a battery charger, where the average dc voltage is large enough to provide a charging current for the battery. For dc supply voltages, such as those used in a radio, stereo system, computer, and so on, the pulsating dc voltage from a rectifier is not good enough. A filter circuit is necessary to provide a steadier dc voltage.

Filter Voltage Regulation and Ripple Voltage

Before going into the details of a filter circuit, it would be appropriate to consider the usual methods of rating filter circuits so that we can compare a circuit's effectiveness as a filter. Figure 15.2 shows a typical filter output voltage, which will be used to define some of the signal factors. The filtered output of Fig. 15.2 has a dc value and some ac variation (ripple). Although a battery has essentially a constant or dc output voltage, the dc voltage derived from an ac source signal by rectifying and filtering will have some ac variation (ripple). The smaller the ac variation with respect to the dc level, the better is the filter circuit's operation.

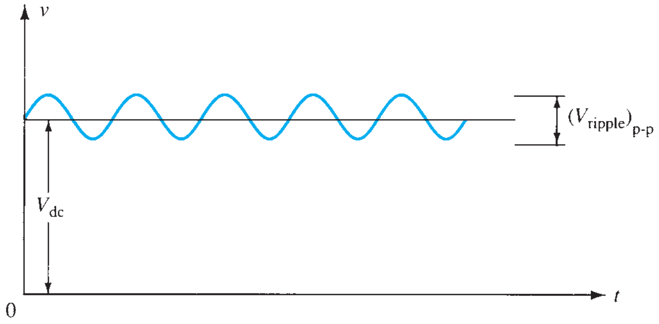


FIG. 15.2
Filter voltage waveform showing dc and ripple voltages.

Consider measuring the output voltage of a filter circuit using a dc voltmeter and an ac (rms) voltmeter. The dc voltmeter will read only the average or dc level of the output voltage. The ac (rms) meter will read only the rms value of the ac component of the output voltage (assuming the ac signal is coupled through a capacitor to block out the dc level).

Definition: Ripple is defined as

$$\boxed{r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\%} \qquad \textbf{(15.1)}$$

EXAMPLE 15.1 Using a dc and ac voltmeter to measure the output signal from a filter circuit, we obtain readings of 25 V dc and 1.5 V rms. Calculate the ripple of the filter output voltage.

Solution:

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{1.5\text{ V}}{25\text{ V}} \times 100\% = \mathbf{6\%}$$

Voltage Regulation Another factor of importance in a power supply is the amount the dc output voltage changes over a range of circuit operation. The voltage provided at the output under no-load condition (no current drawn from the supply) is reduced when load current is drawn from the supply (under load). The amount the dc voltage changes between the no-load and load conditions is described by a factor called voltage regulation.

Definition: Voltage regulation is given by

$$\text{Voltage regulation} = \frac{\text{no-load voltage} - \text{full-load voltage}}{\text{full-load voltage}}$$

$$\boxed{\%\text{V.R.} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100\%} \qquad \textbf{(15.2)}$$

EXAMPLE 15.2 A dc voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation.

Solution:

$$\text{Eq. (15.2):} \quad \%\text{V.R.} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100\% = \frac{60\text{ V} - 56\text{ V}}{56\text{ V}} \times 100\% = \mathbf{7.1\%}$$

If the value of full-load voltage is the same as the no-load voltage, the voltage regulation calculated is 0%, which is the best expected. This means that the supply is a perfect voltage source for which the output voltage is independent of the current drawn from the supply. The smaller the voltage regulation, the better is the operation of the voltage supply circuit.

Ripple Factor of Rectified Signal Although the rectified voltage is not a filtered voltage, it nevertheless contains a dc component and a ripple component. We will see that the full-wave rectified signal has a larger dc component and less ripple than the half-wave rectified voltage.

Half-wave: For a half-wave rectified signal, the output dc voltage is

$$V_{\text{dc}} = 0.318V_m \qquad \textbf{(15.3)}$$

The rms value of the ac component of the output signal can be calculated (see Appendix C) to be

$$V_r(\text{rms}) = 0.385V_m \qquad \textbf{(15.4)}$$

The percentage ripple of a half-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{0.385V_m}{0.318V_m} \times 100\% = 121\% \qquad \textbf{(15.5)}$$

Full-wave: For a full-wave rectified voltage the dc value is

$$V_{\text{dc}} = 0.636V_m \qquad \textbf{(15.6)}$$

The rms value of the ac component of the output signal can be calculated (see Appendix C) to be

$$V_r(\text{rms}) = 0.308V_m \qquad \textbf{(15.7)}$$

The percentage ripple of a full-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{0.308V_m}{0.636V_m} \times 100\% = 48\% \qquad \textbf{(15.8)}$$

In summary, a full-wave rectified signal has less ripple than a half-wave rectified signal and is thus better to apply to a filter.

15.3 CAPACITOR FILTER

A very popular filter circuit is the capacitor-filter circuit shown in Fig. 15.3. A capacitor is connected at the rectifier output, and a dc voltage is obtained across the capacitor. Figure 15.4a shows the output voltage of a full-wave rectifier before the signal is filtered, whereas Fig. 15.4b shows the resulting waveform after the filter capacitor is connected at the rectifier output. Notice that the filtered waveform is essentially a dc voltage with some ripple (or ac variation).

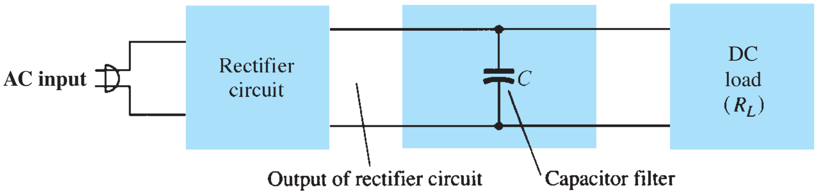

AC input
Rectifier circuit
C
DC load (R_L)
Output of rectifier circuit
Capacitor filter

FIG. 15.3
Basic capacitor filter.

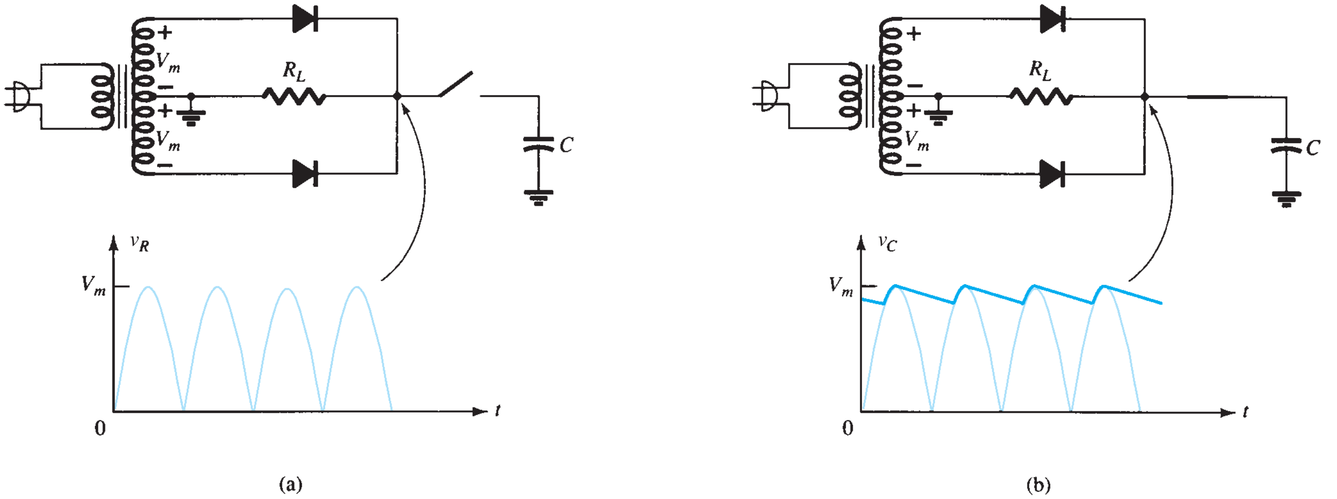

+
V_m
−
+
V_m
−
R_L
C
v_R
V_m
0
t
v_C
V_m
0
t
(a)
(b)

FIG. 15.4
Capacitor filter operation: (a) full-wave rectifier voltage; (b) filtered output voltage.

Figure 15.5a shows a full-wave bridge rectifier and the output waveform obtained from the circuit when connected to a load (R_L). If no load were connected across the capacitor, the output waveform would ideally be a constant dc level equal in value to the peak voltage (V_m) from the rectifier circuit. However, the purpose of obtaining a dc voltage is to provide

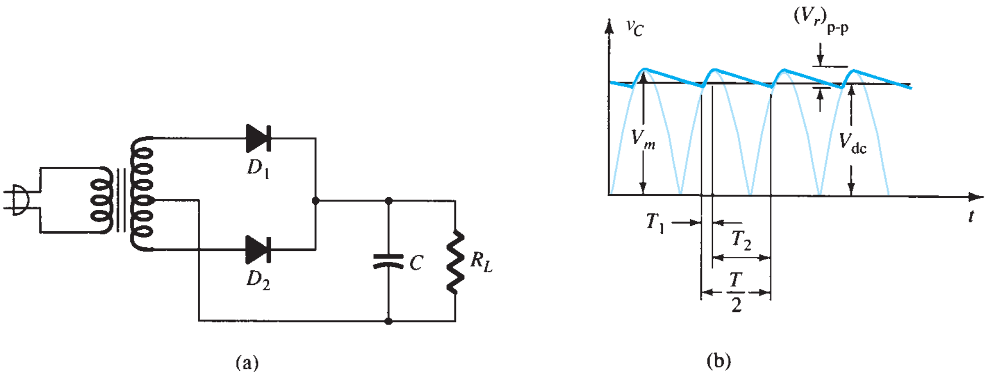

D_1
D_2
C
R_L
v_C
$(V_r)_{\text{p-p}}$
V_m
V_{dc}
t
T_1
T_2
$\frac{T}{2}$
(a)
(b)

FIG. 15.5
Capacitor filter: (a) capacitor filter circuit; (b) output voltage waveform.

this voltage for use by various electronic circuits, which then constitute a load on the voltage supply. Since there will always be a load on the filter output, we must consider this practical case in our discussion.

Output Waveform

Figure 15.5b shows the waveform across a capacitor filter. Time T_1 is the time during which diodes of the full-wave rectifier conduct, charging the capacitor up to the peak rectifier voltage V_m. Time T_2 is the time interval during which the rectifier voltage drops below the peak voltage, and the capacitor discharges through the load. Since the charge–discharge cycle occurs for each half-cycle for a full-wave rectifier, the period of the rectified waveform is $T/2$. The filtered voltage, as shown in Fig. 15.6, shows the output waveform to have a dc level V_{dc} and a ripple voltage V_r (rms) as the capacitor charges and discharges. Some details of these waveforms and the circuit elements are considered next.

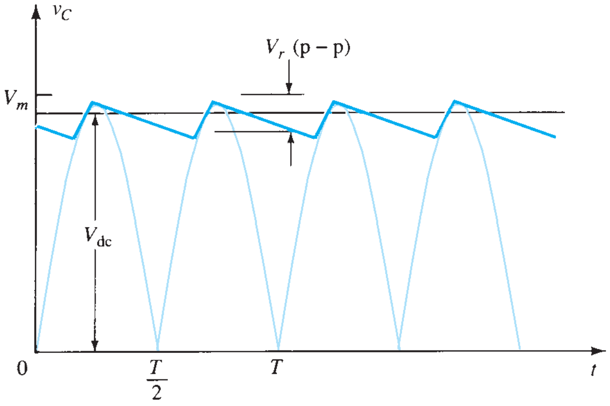


FIG. 15.6

Approximate output voltage of capacitor filter circuit.

Ripple Voltage V_r (RMS) Appendix C provides the details for determining the value of the ripple voltage in terms of the other circuit parameters. The ripple voltage can be calculated from

$$\boxed{V_r(\text{rms}) = \frac{I_{\text{dc}}}{4\sqrt{3}fC} = \frac{2.4I_{\text{dc}}}{C} = \frac{2.4V_{\text{dc}}}{R_LC}} \qquad \textbf{(15.9)}$$

where I_{dc} is in milliamperes, C is in microfarads, and R_L is in kilohms.

EXAMPLE 15.3 Calculate the ripple voltage of a full-wave rectifier with a 100-μF filter capacitor connected to a load drawing 50 mA.

Solution:

$$\text{Eq. (15.9):} \quad V_r(\text{rms}) = \frac{2.4(50)}{100} = \mathbf{1.2\ V}$$

DC Voltage V_{dc} From Appendix C, we can express the dc value of the waveform across the filter capacitor as

$$\boxed{V_{\text{dc}} = V_m - \frac{I_{\text{dc}}}{4fC} = V_m - \frac{4.17I_{\text{dc}}}{C}} \qquad \textbf{(15.10)}$$

where V_m is the peak rectifier voltage, I_{dc} is the load current in milliamperes, and C is the filter capacitor in microfarads.

EXAMPLE 15.4 If the peak rectified voltage for the filter circuit of Example 15.3 is 30 V, calculate the filter dc voltage.

Solution:

$$\text{Eq. (15.10):}\quad V_{dc} = V_m - \frac{4.17 I_{dc}}{C} = 30 - \frac{4.17(50)}{100} = \mathbf{27.9\ V}$$

Filter Capacitor Ripple

Using the definition of ripple [Eq. (15.1)], Eq. (15.9), and Eq. (15.10), with $V_{dc} \approx V_m$, we can obtain the expression for the output waveform ripple of a full-wave rectifier and filter-capacitor circuit:

$$\boxed{r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{2.4 I_{dc}}{C V_{dc}} \times 100\% = \frac{2.4}{R_L C} \times 100\%} \qquad \textbf{(15.11)}$$

where I_{dc} is in milliamperes, C is in microfarads, V_{dc} is in volts, and R_L is in kilohms.

EXAMPLE 15.5 Calculate the ripple of a capacitor filter for a peak rectified voltage of 30 V, capacitor $C = 50\ \mu\text{F}$, and a load current of 50 mA.

Solution:

$$\text{Eq. (15.11):}\quad r = \frac{2.4 I_{dc}}{C V_{dc}} \times 100\% = \frac{2.4(50)}{100(27.9)} \times 100\% = \mathbf{4.3\%}$$

We could also calculate the ripple using the basic definition:

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{1.2\ \text{V}}{27.9\ \text{V}} \times 100\% = \mathbf{4.3\%}$$

Diode Conduction Period and Peak Diode Current

From the previous discussion, it should be clear that larger values of capacitance provide less ripple and higher average voltage, thereby providing better filter action. From this one might conclude that to improve the performance of a capacitor filter it is only necessary to increase the size of the filter capacitor. The capacitor, however, also affects the peak current drawn through the rectifying diodes, and, as will be shown next, the larger the value of the capacitor, the larger is the peak current drawn through the rectifying diodes.

Recall that the diodes conduct during period T_1 (see Fig. 15.5), during which time the diode must provide the necessary average current to charge the capacitor. The shorter this time interval, the larger is the amount of the charging current. Figure 15.7 shows this relation for a half-wave rectified signal (it would be the same basic operation for the full-wave case). Notice that for smaller values of capacitor, with T_1 larger, the peak diode current is less than for larger values of filter capacitor.

Since the average current drawn from the supply must equal the average diode current during the charging period, the following relation can be used (assuming constant diode current during charge time):

$$I_{dc} = \frac{T_1}{T} I_{peak}$$

from which we obtain

$$\boxed{I_{peak} = \frac{T}{T_1} I_{dc}} \qquad \textbf{(15.12)}$$

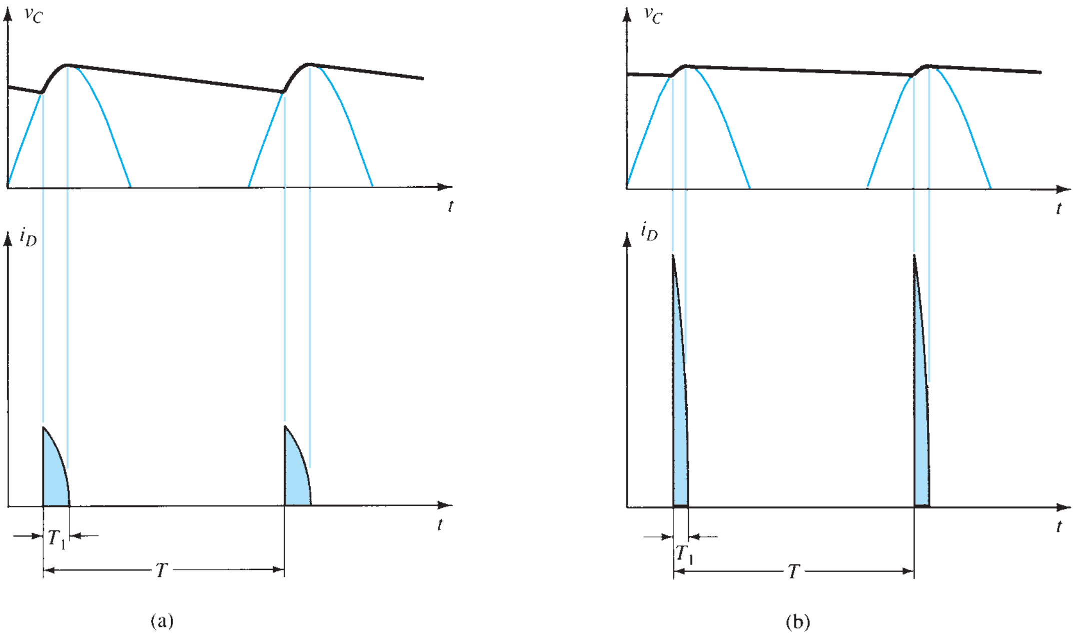


FIG. 15.7

Output voltage and diode current waveforms: (a) small C; (b) large C.

where T_1 = diode conduction time
$T = 1/f$ ($f = 2 \times 60$ for the full-wave case)
I_{dc} = average current drawn from the filter
I_{peak} = peak current through the conducting diodes

15.4 *RC* FILTER

It is possible to further reduce the amount of ripple across a filter capacitor by using an additional *RC* filter section as shown in Fig. 15.8. The purpose of the added *RC* section is to pass most of the dc component while attenuating (reducing) as much of the ac component as possible. Figure 15.9 shows a full-wave rectifier with capacitor filter followed by an *RC* filter section. The operation of the filter circuit can be analyzed using superposition for the dc and ac components of the signal.

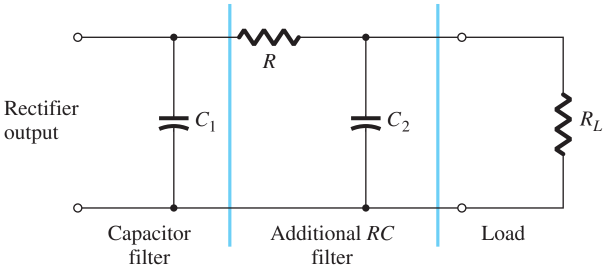


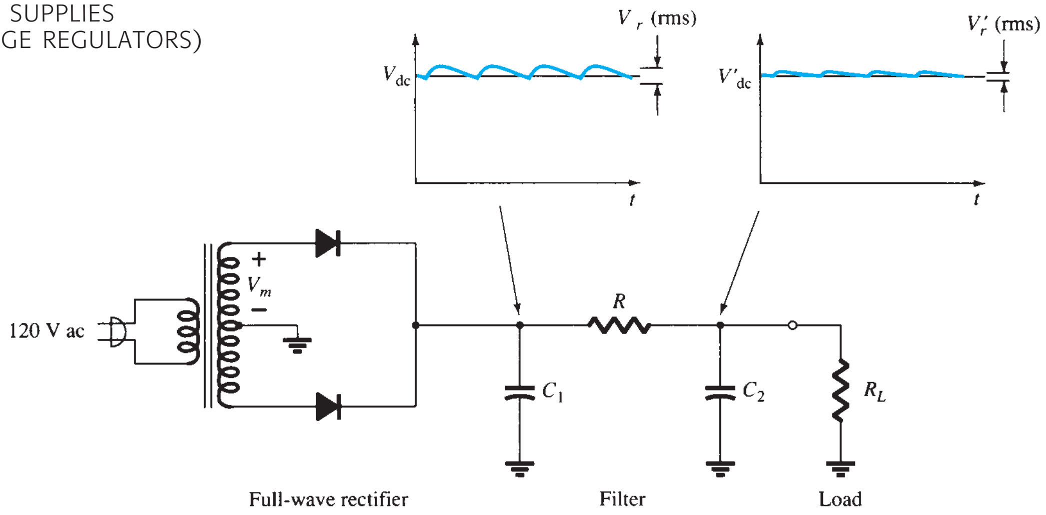
FIG. 15.8

RC filter stage.

DC Operation of *RC* Filter Section

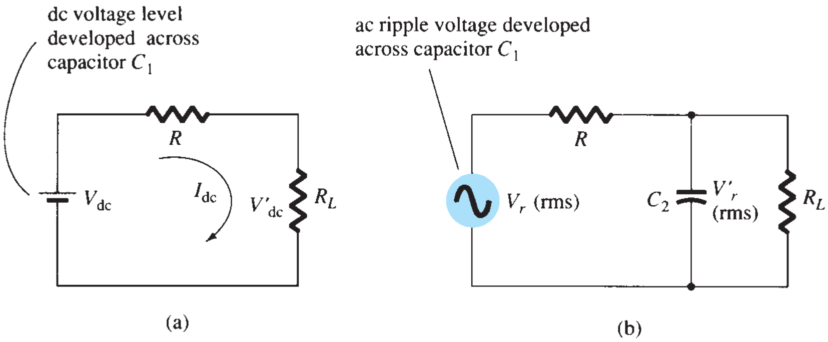
Figure 15.10a shows the dc equivalent circuit to use in analyzing the *RC* filter circuit of Fig. 15.9. Since both capacitors are open-circuit for dc operation, the resulting output dc voltage is

$$\boxed{V'_{\text{dc}} = \frac{R_L}{R + R_L} V_{\text{dc}}} \tag{15.13}$$



V r (rms)
V′r (rms)
Vdc
V′dc
t
t
120 V ac
+
Vm
−
R
C1
C2
RL
Full-wave rectifier
Filter
Load

FIG. 15.9
Full-wave rectifier and RC filter circuit.



dc voltage level developed across capacitor C1
ac ripple voltage developed across capacitor C1
R
Vdc
Idc
V′dc
RL
R
Vr (rms)
C2
V′r (rms)
RL
(a)
(b)

FIG. 15.10
(a) DC and (b) ac equivalent circuits of RC filter.

EXAMPLE 15.6 Calculate the dc voltage across a 1-kΩ load for an *RC* filter section ($R = 120\ \Omega$, $C = 10\ \mu$F). The dc voltage across the initial filter capacitor is $V_{dc} = 60$ V.

Solution:

$$\text{Eq. (15.13):}\quad V'_{dc} = \frac{R_L}{R + R_L} V_{dc} = \frac{1000}{120 + 1000}(60\text{ V}) = \mathbf{53.6\ V}$$

AC Operation of *RC* Filter Section

Figure 15.10b shows the ac equivalent circuit of the *RC* filter section. Due to the voltage-divider action of the capacitor ac impedance and the load resistor, the ac component of voltage resulting across the load is

$$\boxed{V'_r(\text{rms}) \approx \frac{X_C}{R} V_r(\text{rms})} \qquad \textbf{(15.14)}$$

For a full-wave rectifier with ac ripple at 120 Hz, the impedance of a capacitor can be calculated using

$$\boxed{X_C = \frac{1.3}{C}} \qquad \textbf{(15.15)}$$

where C is in microfarads and X_C is in kilohms.

EXAMPLE 15.7 Calculate the dc and ac components of the output signal across load R_L in the circuit of Fig. 15.11. Calculate the ripple of the output waveform.

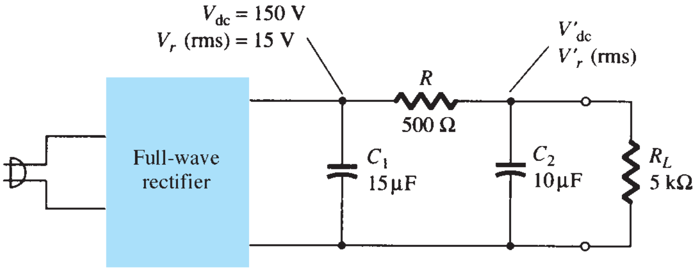

V_{dc} = 150 V
V_r (rms) = 15 V
V'_{dc}
V'_r (rms)
R
500 Ω
Full-wave rectifier
C_1
15 μF
C_2
10 μF
R_L
5 kΩ

FIG. 15.11

RC filter circuit for Example 15.7.

Solution:

DC Calculation We obtain

$$\text{Eq. (15.13):} \quad V'_{dc} = \frac{R_L}{R + R_L} V_{dc} = \frac{5\text{ k}\Omega}{500 + 5\text{ k}\Omega}(150\text{ V}) = \mathbf{136.4\text{ V}}$$

AC Calculation The *RC*-section capacitive impedance is

$$\text{Eq. (15.15):} \quad X_C = \frac{1.3}{C} = \frac{1.3}{10} = 0.13\text{ k}\Omega = 130\ \Omega$$

The ac component of the output voltage, calculated using Eq. (15.14), is

$$V'_r(\text{rms}) = \frac{X_C}{R} V_r(\text{rms}) = \frac{130}{500}(15\text{ V}) = \mathbf{3.9\text{ V}}$$

The ripple of the output waveform is then

$$r = \frac{V'_r(\text{rms})}{V'_{dc}} \times 100\% = \frac{3.9\text{ V}}{136.4\text{ V}} \times 100\% = \mathbf{2.86\%}$$

15.5 DISCRETE TRANSISTOR VOLTAGE REGULATION

Two types of transistor voltage regulators are the series voltage regulator and the shunt voltage regulator. Each type of circuit can provide an output dc voltage that is regulated or maintained at a set value even if the input voltage varies or if the load connected to the output changes.

Series Voltage Regulation

The basic connection of a series regulator circuit is shown in the block diagram of Fig. 15.12. The series element controls the amount of the input voltage that gets to the output.

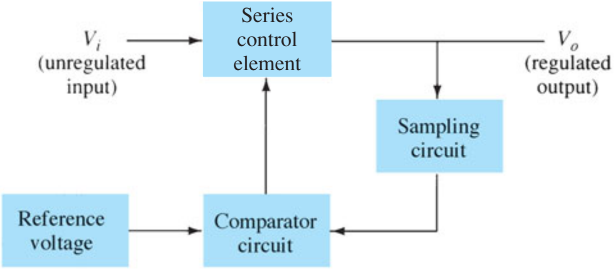

V_i (unregulated input)
Series control element
V_o (regulated output)
Sampling circuit
Reference voltage
Comparator circuit

FIG. 15.12

Series regulator block diagram.

The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage.

1. If the output voltage increases, the comparator circuit provides a control signal to cause the series control element to decrease the amount of the output voltage—thereby maintaining the output voltage.
2. If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element to increase the amount of the output voltage.

Series Regulator Circuit A simple series regulator circuit is shown in Fig. 15.13. Transistor Q_1 is the series control element, and Zener diode D_Z provides the reference voltage. The regulating operation can be described as follows:

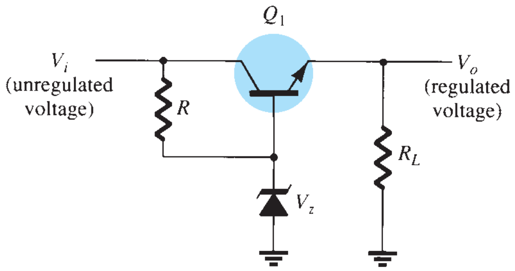


FIG. 15.13

Series regulator circuit.

1. If the output voltage decreases, the increased base-emitter voltage causes transistor Q_1 to conduct more, thereby raising the output voltage—maintaining the output constant.
2. If the output voltage increases, the decreased base-emitter voltage causes transistor Q_1 to conduct less, thereby reducing the output voltage—maintaining the output constant.

EXAMPLE 15.8 Calculate the output voltage and the Zener current in the regulator circuit of Fig. 15.14 for $R_L = 1\text{ k}\Omega$.

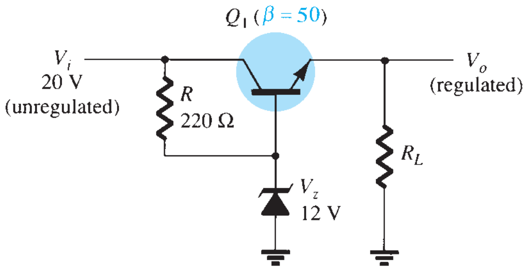


FIG. 15.14

Circuit for Example 15.8.

Solution:

$$V_o = V_Z - V_{BE} = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\text{ V}}$$

$$V_{CE} = V_i - V_o = 20\text{ V} - 11.3\text{ V} = 8.7\text{ V}$$

$$I_R = \frac{20\text{ V} - 12\text{ V}}{220\ \Omega} = \frac{8\text{ V}}{220\ \Omega} = 36.4\text{ mA}$$

For $R_L = 1\text{ k}\Omega$,

$$I_L = \frac{V_o}{R_L} = \frac{11.3\text{ V}}{1\text{ k}\Omega} = 11.3\text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{11.3\text{ mA}}{50} = 226\ \mu\text{A}$$

$$I_Z = I_R - I_B = 36.4\text{ mA} - 226\ \mu\text{A} \approx \mathbf{36\text{ mA}}$$

Improved Series Regulator An improved series regulator circuit is shown in Fig. 15.15. Resistors R_1 and R_2 act as a sampling circuit, with Zener diode D_Z providing a reference voltage, and transistor Q_2 then controls the base current to transistor Q_1 to vary the current passed by transistor Q_1 to maintain the output voltage constant.

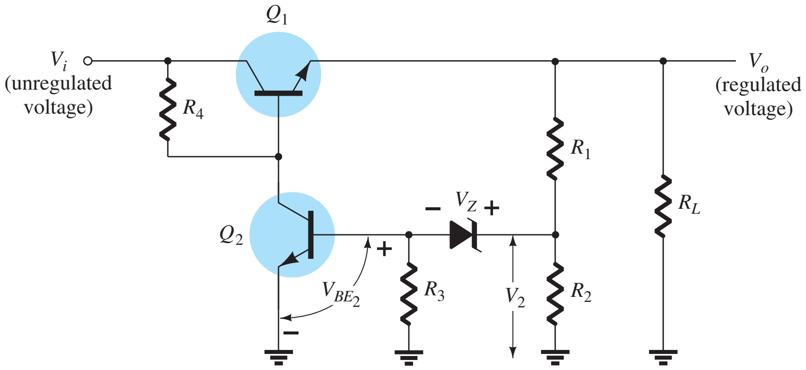


FIG. 15.15

Improved series regulator circuit.

If the output voltage tries to increase, the increased voltage, V_2, sampled by R_1 and R_2, causes the base-emitter voltage of transistor Q_2 to go up (since V_Z remains fixed). If Q_2 conducts more current, less goes to the base of transistor Q_1, which then passes less current to the load, reducing the output voltage—thereby maintaining the output voltage constant. The opposite takes place if the output voltage tries to decrease, causing less current to be supplied to the load, to keep the voltage from decreasing.

The voltage V_2 provided by sensing resistors R_1 and R_2 must equal the sum of the base-emitter voltage of Q_2 and the Zener diode, that is,

$$V_{BE_2} + V_Z = V_2 = \frac{R_2}{R_1 + R_2} V_o \tag{15.16}$$

Solving Eq. (15.16) for the regulated output voltage V_o gives

$$\boxed{V_o = \frac{R_1 + R_2}{R_2}(V_Z + V_{BE_2})} \tag{15.17}$$

EXAMPLE 15.9 What regulated output voltage is provided by the circuit of Fig. 15.15 for the circuit elements $R_1 = 20\text{ k}\Omega$, $R_2 = 30\text{ k}\Omega$, and $V_Z = 8.3$ V?

Solution: From Eq. (15.17), the regulated output voltage is

$$V_o = \frac{20\text{ k}\Omega + 30\text{ k}\Omega}{30\text{ k}\Omega}(8.3\text{ V} + 0.7\text{ V}) = \mathbf{15\text{ V}}$$

Op-Amp Series Regulator Another type of series regulator is shown in Fig. 15.16. The op-amp compares the Zener diode reference voltage with the feedback voltage from sensing resistors R_1 and R_2. If the output voltage varies, the conduction of transistor Q_1 is controlled to maintain the output voltage constant. The output voltage will be maintained at a value of

$$\boxed{V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z} \tag{15.18}$$

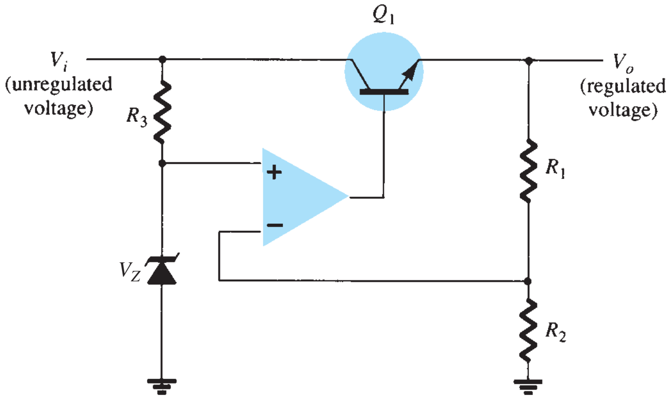


FIG. 15.16
Op-amp series regulator circuit.

EXAMPLE 15.10 Calculate the regulated output voltage in the circuit of Fig. 15.17.

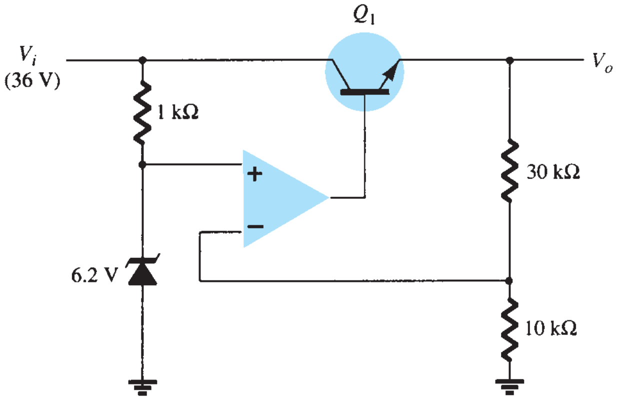


FIG. 15.17
Circuit for Example 15.10.

Solution:

$$\text{Eq. (15.18):} \quad V_o = \left(1 + \frac{30\text{ k}\Omega}{10\text{ k}\Omega}\right)6.2\text{ V} = \mathbf{24.8\text{ V}}$$

Current-Limiting Circuit One form of short-circuit or overload protection is current limiting, as shown in Fig. 15.18. As load current I_L increases, the voltage drop across the short-circuit sensing resistor R_{SC} increases. When the voltage drop across R_{SC} becomes large enough, it will drive Q_2 on, diverting current from the base of transistor Q_1, thereby reducing the load current through transistor Q_1, preventing any additional current to load R_L. The action of components R_{SC} and Q_2 limits the maximum load current.

Foldback Limiting Current limiting reduces the load voltage when the current becomes larger than the limiting value. The circuit of Fig. 15.19 provides foldback limiting, which reduces both the output voltage and the output current, protecting the load from overcurrent as well as protecting the regulator.

Foldback limiting is provided by the additional voltage-divider network of R_4 and R_5 in the circuit of Fig. 15.19 (over that of Fig. 15.17). The divider circuit senses the voltage at the output (emitter) of Q_1. When I_L increases to its maximum value, the voltage across R_{SC} becomes large enough to drive Q_2 on, thereby providing current limiting. If the load resistance is made smaller, the voltage driving Q_2 on becomes less, so that I_L drops when V_L also

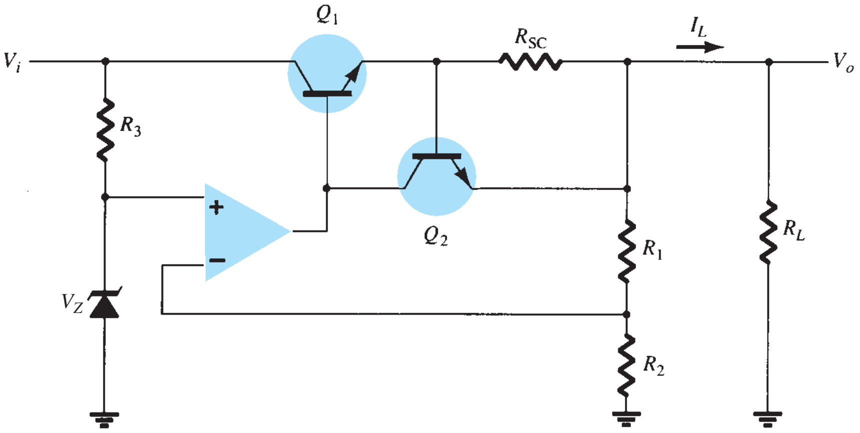

Q_1
R_{SC}
I_L
V_i
V_o
R_3
+
−
Q_2
R_1
R_L
V_Z
R_2

FIG. 15.18

Current-limiting voltage regulator.

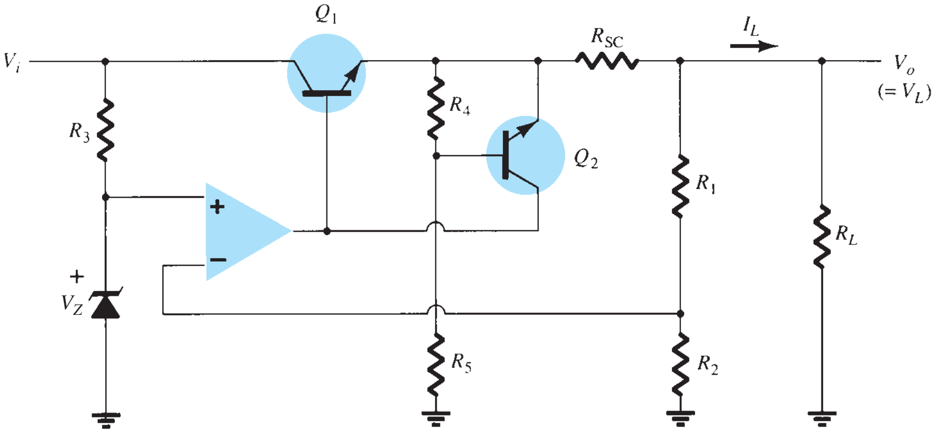

Q_1
R_{SC}
I_L
V_i
V_o
$(= V_L)$
R_4
R_3
Q_2
+
−
R_1
R_L
+
V_Z
R_5
R_2

FIG. 15.19

Foldback-limiting series regulator circuit.

drops in value—this action being foldback limiting. When the load resistance is returned to its rated value, the circuit resumes its voltage regulation action.

Shunt Voltage Regulation

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Figure 15.20 shows the block diagram of such a voltage regulator. The input unregulated voltage provides current to the load. Some of the current is pulled away by the control element to maintain the regulated output voltage across the load. If the load voltage tries to change due to a change in the load, the sampling circuit provides

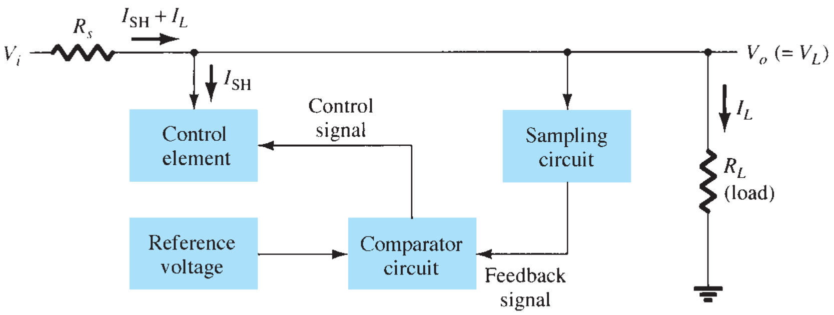

R_s
$I_{SH} + I_L$
V_i
$V_o\ (= V_L)$
I_{SH}
Control element
Control signal
Sampling circuit
I_L
R_L
(load)
Reference voltage
Comparator circuit
Feedback signal

FIG. 15.20

Block diagram of shunt voltage regulator.

a feedback signal to a comparator, which then provides a control signal to vary the amount of the current shunted away from the load. As the output voltage tries to get larger, for example, the sampling circuit provides a feedback signal to the comparator circuit, which then provides a control signal to draw increased shunt current, providing less load current, thereby keeping the regulated voltage from rising.

Basic Transistor Shunt Regulator A basic shunt regulator circuit is shown in Fig. 15.21. Resistor R_S drops the unregulated voltage by an amount that depends on the current supplied to the load R_L. The voltage across the load is set by the Zener diode and transistor base-emitter voltage. If the load resistance decreases, a reduced drive current to the base of Q_1 results, shunting less collector current. The load current is thus larger, thereby maintaining the regulated voltage across the load. The output voltage to the load is

$$V_L = V_Z + V_{BE} \tag{15.19}$$

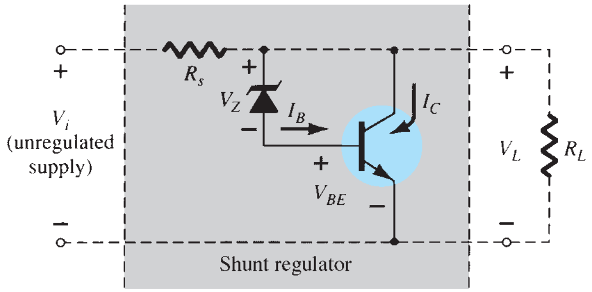


FIG. 15.21
Transistor shunt voltage regulator.

EXAMPLE 15.11 Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 15.22.

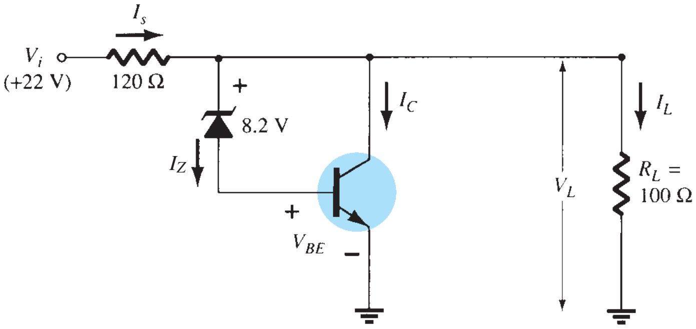


FIG. 15.22
Circuit for Example 15.11.

Solution: The load voltage is

$$\text{Eq. (15.19):} \quad V_L = 8.2\text{ V} + 0.7\text{ V} = \mathbf{8.9\text{ V}}$$

For the given load,

$$I_L = \frac{V_L}{R_L} = \frac{8.9\text{ V}}{100\ \Omega} = \mathbf{89\text{ mA}}$$

With the unregulated input voltage at 22 V, the current through R_S is

$$I_S = \frac{V_i - V_L}{R_S} = \frac{22\text{ V} - 8.9\text{ V}}{120} = \mathbf{109\text{ mA}}$$

so that the collector current is

$$I_C = I_S - I_L = 109\text{ mA} - 89\text{ mA} = \mathbf{20\text{ mA}}$$

(The current through the Zener and transistor base-emitter is smaller than I_C by the transistor beta.)

Improved Shunt Regulator The circuit of Fig. 15.23 shows an improved shunt voltage regulator circuit. The Zener diode provides a reference voltage so that the voltage across R_1 senses the output voltage. As the output voltage tries to change, the current shunted by transistor Q_1 is varied to maintain the output voltage constant. Transistor Q_2 provides a larger base current to transistor Q_1 than the circuit of Fig. 15.21, so that the regulator handles a larger load current. The output voltage is set by the Zener voltage and that across the two transistor base-emitters,

$$V_o = V_L = V_Z + V_{BE_2} + V_{BE_1} \tag{15.20}$$

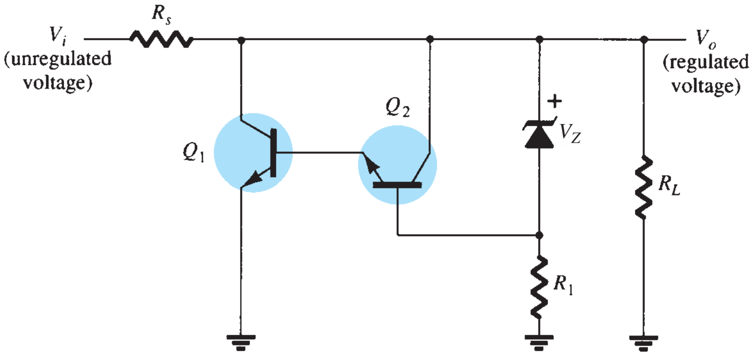


FIG. 15.23
Improved shunt voltage regulator circuit.

Shunt Voltage Regulator Using Op-Amp Figure 15.24 shows another version of a shunt voltage regulator using an op-amp as voltage comparator. The Zener voltage is compared to the feedback voltage obtained from voltage divider R_1 and R_2 to provide the control drive current to shunt element Q_1. The current through resistor R_S is thus controlled to drop a voltage across R_S so that the output voltage is maintained.

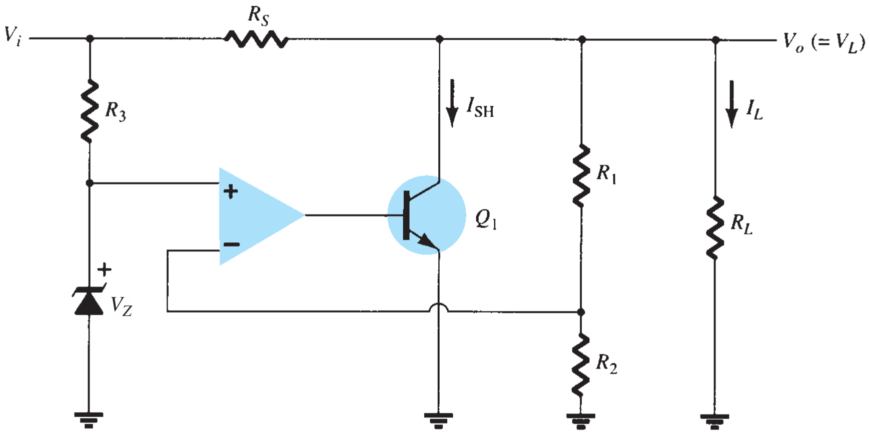


FIG. 15.24
Shunt voltage regulator using an op-amp.

Switching Regulation

A type of regulator circuit that is quite popular for its efficient transfer of power to the load is the switching regulator. Basically, a switching regulator passes voltage to the load in pulses, which are then filtered to provide a smooth dc voltage. Figure 15.25 shows the basic components of such a voltage regulator. The added circuit complexity is well worth the improved operating efficiency obtained.

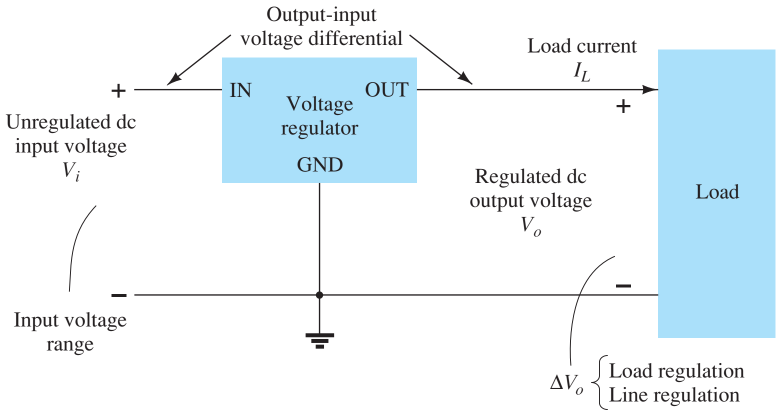


FIG. 15.25

Block representation of three-terminal voltage regulator.

15.6 IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and *RC* filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

Three-Terminal Voltage Regulators

Figure 15.25 shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage V_i applied to one input terminal, a regulated output dc voltage V_o from a second terminal, and the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

Fixed-Positive-Voltage Regulators

The series 78 regulators provide fixed regulated voltages from 5 V to 24 V. Figure 15.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12 V dc. An unregulated input voltage V_i is filtered by capacitor C_1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12 V, which is filtered by capacitor C_2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). Whereas the input voltage may vary over some permissible

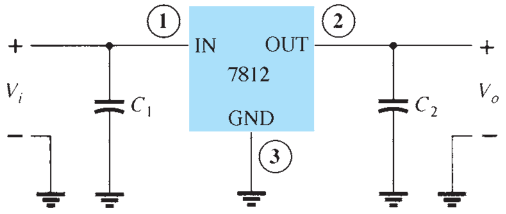


FIG. 15.26

Connection of a 7812 voltage regulator.

voltage range and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive-voltage regulator ICs is provided in Table 15.1.

TABLE 15.1

Positive-Voltage Regulators in the 7800 Series

IC Part	Output Voltage (V)	Minimum V_i (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

The connection of a 7812 in a complete voltage supply is shown in the connection of Fig. 15.27. The ac line voltage (120 V rms) is stepped down to 18 V rms across each half of the center-tapped transformer. A full-wave rectifier and capacitor filter then provides an unregulated dc voltage, shown as a dc voltage of about 22 V, with ac ripple of a few volts as input to the voltage regulator. The 7812 IC then provides an output that is a regulated +12 V dc.

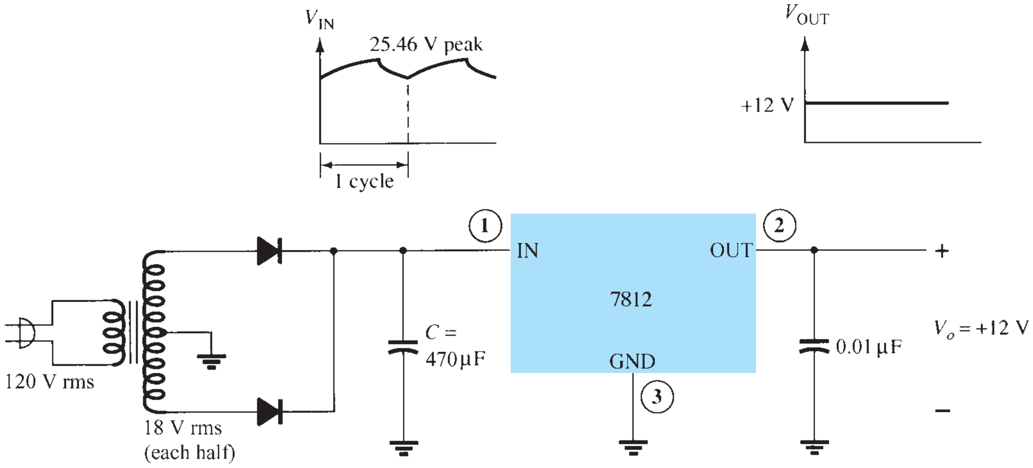


FIG. 15.27

A +12 V power supply.

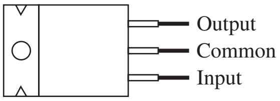
Positive-Voltage-Regulator Specifications The specifications sheet of voltage regulators is typified by that shown in Fig. 15.28 for the group of series 7800 positive-voltage regulators. Some consideration of a few of the more important parameters should be made.

Output voltage: The specification for the 7812 shows that the output voltage is typically +12 V but could be as low as 11.5 V or as high as 12.5 V.

Output regulation: The output voltage regulation is seen to be typically 4 mV, to a maximum of 100 mV (at output currents from 0.25 A to 0.75 A). This information specifies that the output voltage can typically vary only 4 mV from the rated 12 V dc.

Short-circuit output current: The amount of current is limited to typically 0.35 A if the output were to be short-circuited (presumably by accident or by another faulty component).

Peak output current: Although the rated maximum current is 1.5 A for this series of IC, the typical peak output current that might be drawn by a load is 2.2 A. This shows



Nominal output voltage	Regulator
5 V	7805
6 V	7806
8 V	7808
10 V	7810
12 V	7812
15 V	7815
18 V	7818
24 V	7824

Absolute maximum ratings:

Input voltage	40 V
Continuous total dissipation	2 W
Operating free-air temperature range	−65 to 150°C

μA 7812C electrical characteristics:

Parameter	Min.	Typ.	Max.	Units
Output voltage	11.5	12	12.5	V
Input regulation		3	120	mV
Ripple rejection	55	71		dB
Output regulation		4	100	mV
Output resistance		0.018		Ω
Dropout voltage		2.0		V
Short-circuit output current		350		mA
Peak output current		2.2		A

FIG. 15.28
Specification sheet data for voltage regulator ICs.

that although the manufacturer rates the IC as capable of providing 1.5 A, one could draw somewhat more current (possibly for a short period of time).

Dropout voltage: The dropout voltage, typically 2 V, is the minimum amount of voltage across the input–output terminals that must be maintained if the IC is to operate as a regulator. If the input voltage drops too low or the output rises so that at least 2 V is not maintained across the IC input–output, the IC will no longer provide voltage regulation. One therefore maintains an input voltage large enough to assure that the dropout voltage is provided.

Fixed-Negative-Voltage Regulators

The series 7900 ICs provide negative-voltage regulators, similar to those providing positive voltages. A list of negative-voltage regulator ICs is provided in Table 15.2. As shown, IC regulators are available for a range of fixed negative voltages, the selected IC providing the rated output voltage as long as the input voltage is maintained greater than the minimum input value. For example, the 7912 provides an output of −12 V as long as the input to the regulator IC is more negative than −14.6 V.

TABLE 15.2
Negative-Voltage Regulators in 7900 Series

IC Part	Output Voltage (V)	Minimum V_i (V)
7905	−5	−7.3
7906	−6	−8.4
7908	−8	−10.5
7909	−9	−11.5
7912	−12	−14.6
7915	−15	−17.7
7918	−18	−20.8
7924	−24	−27.1

EXAMPLE 15.12 Draw a voltage supply using a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +5 V.

Solution: The resulting circuit is shown in Fig. 15.29.

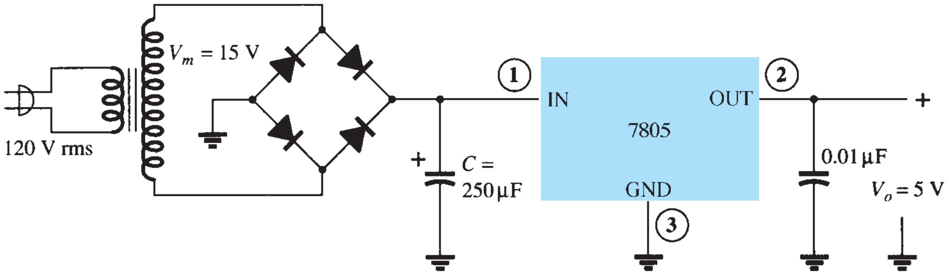


FIG. 15.29
A +5-V power supply.

EXAMPLE 15.13 For a transformer output of 15 V and a filter capacitor of 250 μF, calculate the minimum input voltage when connected to a load drawing 400 mA.

Solution: The voltages across the filter capacitor are

$$V_r(\text{peak}) = \sqrt{3}\,V_r(\text{rms}) = \sqrt{3}\,\frac{2.4 I_{\text{dc}}}{C} = \sqrt{3}\,\frac{2.4(400)}{250} = 6.65\text{ V}$$

$$V_{\text{dc}} = V_m - V_r(\text{peak}) = 15\text{ V} - 6.65\text{ V} = 8.35\text{ V}$$

Since the input swings around this dc level, the minimum input voltage can drop to as low as

$$V_i(\text{low}) = V_{\text{dc}} - V_r(\text{peak}) = 15\text{ V} - 6.65\text{ V} = \mathbf{8.35\text{ V}}$$

Since this voltage is greater than the minimum required for the IC regulator (from Table 15.1, V_i = 7.3 V), the IC can provide a regulated voltage to the given load.

EXAMPLE 15.14 Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 15.29.

Solution: To maintain $V_i(\text{min}) \geq 7.3$ V,

$$V_r(\text{peak}) \leq V_m - V_i(\text{min}) = 15\text{ V} - 7.3\text{ V} = 7.7\text{ V}$$

so that

$$V_r(\text{rms}) = \frac{V_r(\text{peak})}{\sqrt{3}} = \frac{7.7\text{ V}}{1.73} = 4.4\text{ V}$$

The value of load current is then

$$I_{\text{dc}} = \frac{V_r(\text{rms})C}{2.4} = \frac{(4.4\text{ V})(250)}{2.4} = \mathbf{458\text{ mA}}$$

Any current above this value is too large for the circuit to maintain the regulator output at +5 V.

Adjustable-Voltage Regulators

Voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317, for example, can be operated with the output voltage regulated at any setting over the range of voltage from 1.2 V to 37 V. Figure 15.30 shows how the regulated output voltage of an LM317 can be set.

Resistors R_1 and R_2 set the output to any desired voltage over the adjustment range (1.2 V to 37 V). The output voltage desired can be calculated using

$$V_o = V_{\text{ref}}\left(1 + \frac{R_2}{R_1}\right) + I_{\text{adj}}R_2 \qquad \textbf{(15.21)}$$

with typical IC values of

$$V_{\text{ref}} = 1.25\text{ V} \qquad \text{and} \qquad I_{\text{adj}} = 100\ \mu\text{A}$$

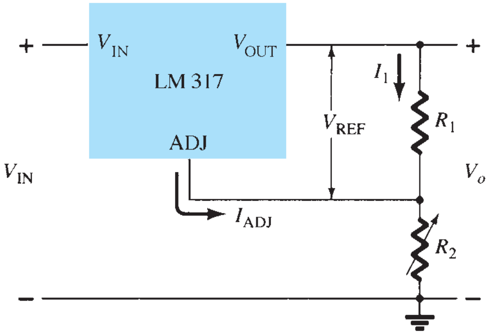


FIG. 15.30
Connection of LM317 adjustable-voltage regulator.

EXAMPLE 15.15 Determine the regulated voltage in the circuit of Fig. 15.30 with $R_1 = 240\ \Omega$ and $R_2 = 2.4\text{ k}\Omega$.

Solution:

$$\text{Eq. (15.21):}\quad V_o = 1.25\text{ V}\left(1 + \frac{2.4\text{ k}\Omega}{240\ \Omega}\right) + (100\ \mu\text{A})(2.4\text{ k}\Omega)$$

$$= 13.75\text{ V} + 0.24\text{ V} = \mathbf{13.99\text{ V}}$$

EXAMPLE 15.16 Determine the regulated output voltage of the circuit in Fig. 15.31.

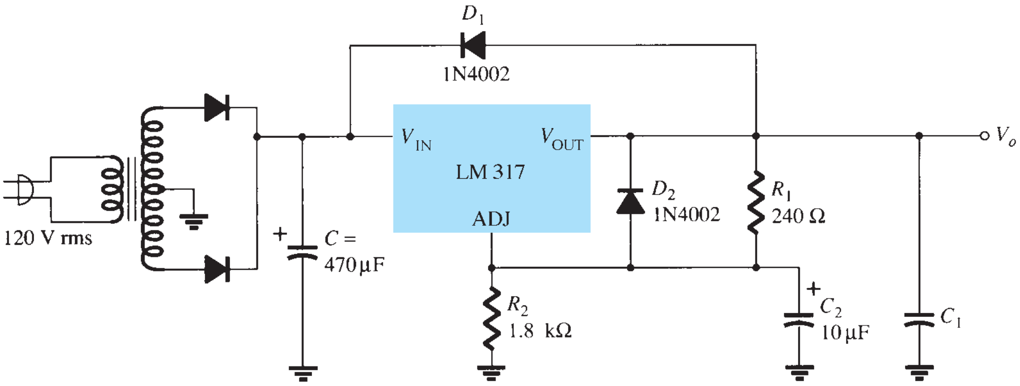


FIG. 15.31
Positive adjustable-voltage regulator for Example 15.16.

Solution: The output voltage calculated using Eq. (15.21) is

$$V_o = 1.25\text{ V}\left(1 + \frac{1.8\text{ k}\Omega}{240\ \Omega}\right) + (100\ \mu\text{A})(1.8\text{ k}\Omega) \approx \mathbf{10.8\text{ V}}$$

A check of the filter capacitor voltage shows that an input–output difference of 2 V can be maintained up to at least 200 mA load current.

15.7 PRACTICAL APPLICATIONS

Power Supplies

Power supplies are a part of every electronic device, so a wide variety of circuits are used to accommodate such factors as power rating, size of circuit, cost, desired regulation, and so on. This section will outline a number of practical supplies and chargers.

Simple DC Supply A simple way to drop the ac voltage, without a bulky and expensive transformer, is to use a capacitor in series with the line voltage. This type of supply, shown in Fig. 15.32, uses few parts and is thus very simple. A half-wave rectifier (or bridge rectifier) with a filter circuit is used to get a voltage with a dc component. This circuit has a number of drawbacks: There is no isolation from the ac line, a minimal current must always be drawn, and the load current cannot be excessive. Thus, the simple dc supply can be used to provide a poorly regulated dc voltage when light current draw is desired in an inexpensive device.

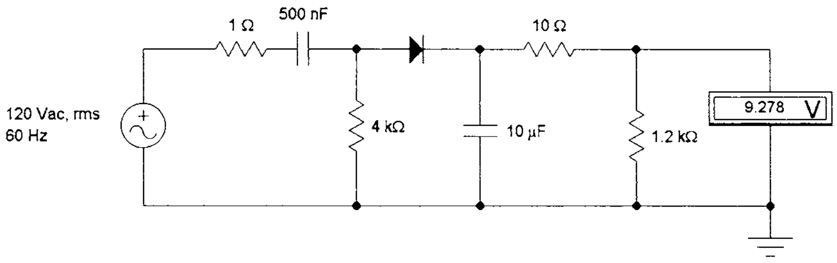


FIG. 15.32
Simple dc supply.

DC Supply with Transformer Input The next type of power supply uses a transformer to step down the ac line voltage. The transformer can be either a wall mount (external) or a chassis mount (internal). A rectifier is used after the transformer, followed by a capacitor filter and possibly a regulator. The regulator becomes a problem as the power requirements increase. Heat sink size, cooling, and power requirements become a major obstacle to these types of supplies.

Figure 15.33 shows a simple half-wave rectified supply with an isolating step-down transformer. This relatively simple circuit provides no regulation.

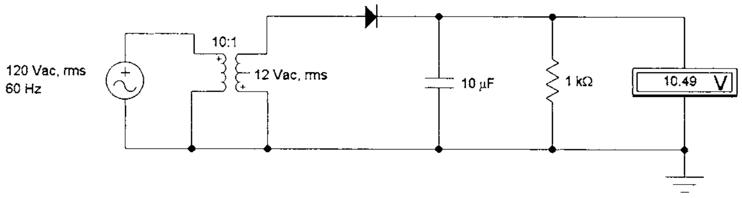


FIG. 15.33
DC supply with transformer input.

Figure 15.34 shows probably the best standard power supply—with transformer isolation and voltage step-down; a bridge rectifier; a dual filter with choke; and a regulator circuit made of a Zener reference, a parallel regulation transistor, and an op-amp with feedback to aid the regulation. This circuit obviously provides excellent voltage regulation.

Chopper Supply Today's power supplies convert ac to dc using a chopper circuit such as that shown in Fig. 15.35. The ac input is connected to the circuit through various line conditioners and filters. This removes any electrical noise. The input is then rectified and lightly filtered. The high dc voltage is chopped at a rate of approximately 100 kHz. The rate and the duration of the chopping are controlled by a special-function integrated circuit. An isolation transformer couples the chopped dc to a filtering and rectifying circuit. The output of the power supply is fed back to the control integrated circuit. By monitoring the output, the IC can regulate the output voltage. Although this type of power supply is more complicated, it

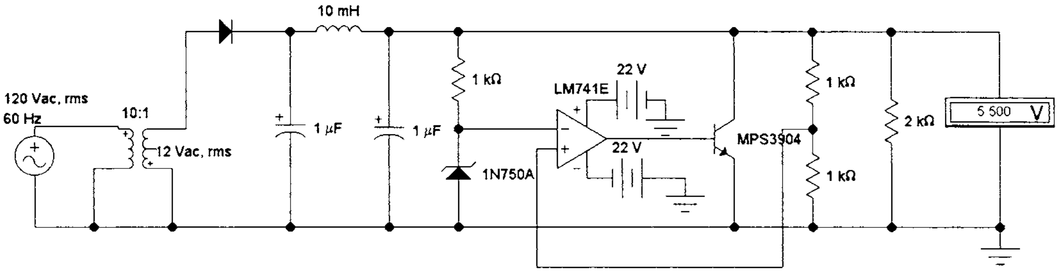

10 mH
120 Vac, rms
60 Hz
10:1
12 Vac, rms
1 μF
1 μF
1 kΩ
1N750A
LM741E
22 V
22 V
MPS3904
1 kΩ
1 kΩ
2 kΩ
5 500 V

FIG. 15.34

Series-regulated supply with transformer input and IC regulation.

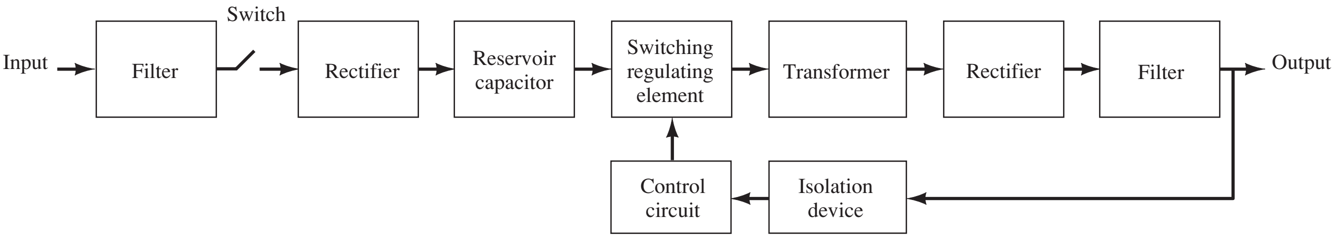

Input
Filter
Switch
Rectifier
Reservoir capacitor
Switching regulating element
Transformer
Rectifier
Filter
Output
Control circuit
Isolation device

FIG. 15.35

Block diagram of chopper power supply.

has many advantages over traditional supplies. For example, it operates over a very large range of input ac voltages, it operates independently of the input frequency, it can be made very small, and it operates over a large range of current demands and low heat dissipation.

Special TV Horizontal High-Voltage Supply Television sets require a very high dc voltage to operate the picture tube (cathode ray tube, CRT). In early TV sets this voltage was supplied by a high-voltage transformer with very high voltage rated capacitors. The circuit was very bulky, heavy, and dangerous. TV sets utilize two basic frequencies to scan the screen: 60 Hz (vertical oscillator) and 15 kHz (horizontal oscillator). Using the horizontal oscillator, one can build a high-voltage dc supply. The circuit is known as a *flyback power supply* (see Fig. 15.36). The low dc voltage is pulsed into a small flyback transformer. The flyback transformer is a step-up autotransformer. The output is rectified and filtered with a small-value capacitor. The flyback transformer can be small, and the filter capacitor can be a small, low-value unit, because the frequency is very high. This type of circuit is lightweight and very reliable.

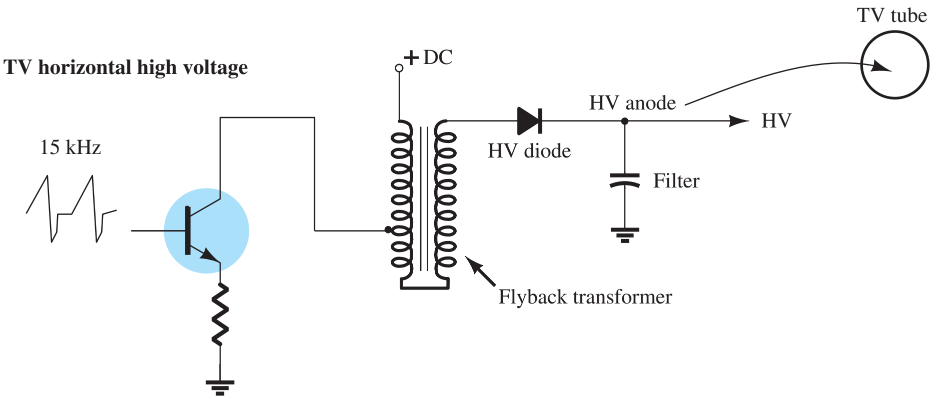

TV horizontal high voltage
15 kHz
+DC
HV diode
HV anode
HV
TV tube
Filter
Flyback transformer

FIG. 15.36

TV horizontal high-voltage supply.

Battery Charger Circuits Battery charger circuits employ variations of the power supply circuits mentioned above. Figure 15.37a shows the basics of a simple charging circuit using a transformer setting with a selector switch to determine the charge rate current provided. For NiCad batteries the voltage that supplies the battery must be greater than the

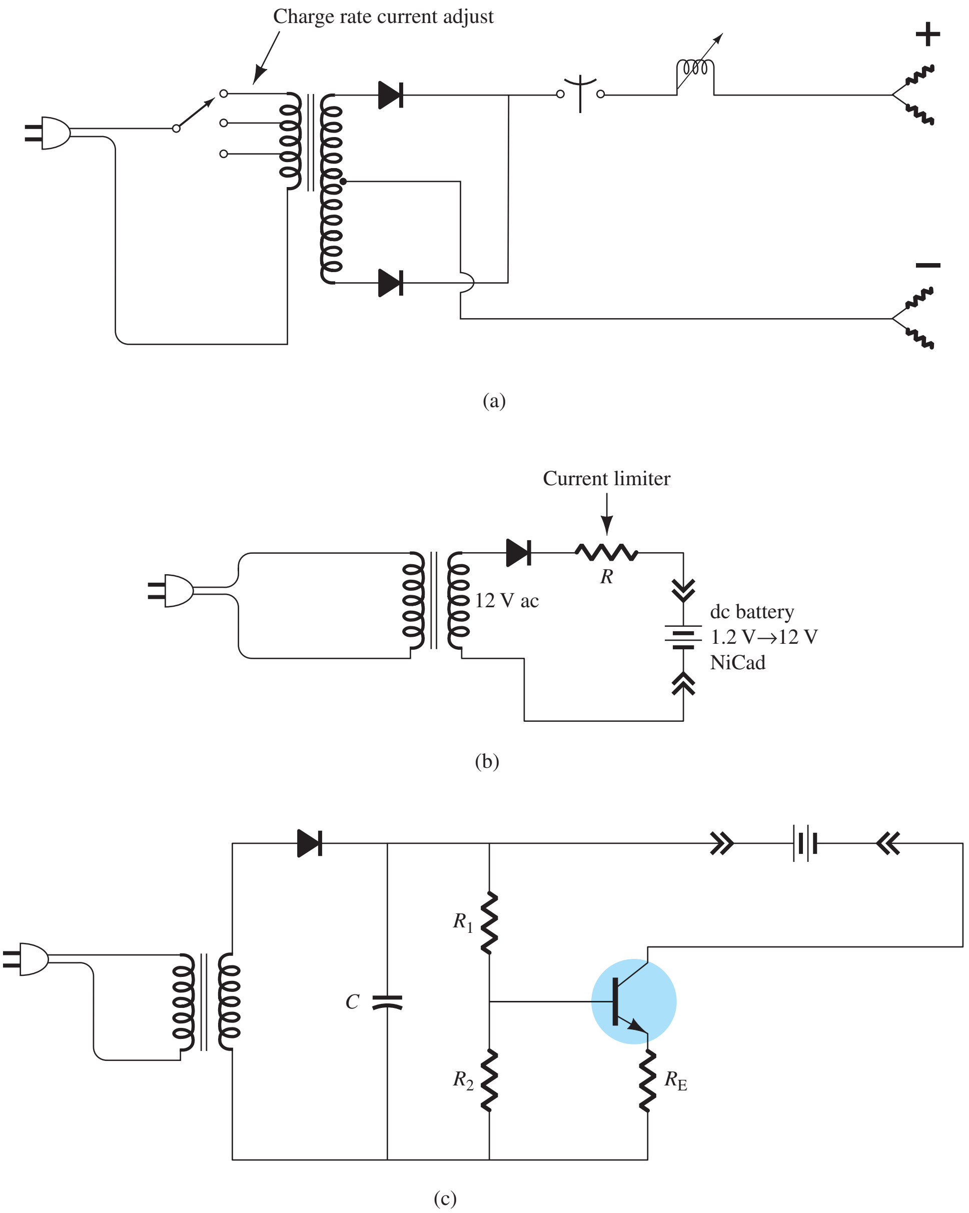


FIG. 15.37

Battery charger circuits: (a) Single charging circuit; (b) typical NiCad charging circuit; (c) lead–acid charging circuit.

battery being charged. The current must also be controlled and limited. Figure 15.37b shows a typical NiCad charging circuit. For a lead–acid battery, the voltage must be controlled so as not to exceed the battery's rated voltage. The charge current is determined by the power supply's capability, the power rating of the battery, and the amount of charge required. Figure 15.37c shows a simple lead–acid charging circuit.

Batteries can be charged using traditional dc supplies or from more elaborate chopper supplies. The major problem with charging batteries is determining when the battery is completely charged. Many exotic circuits exist to check the battery status.

15.8 SUMMARY

Equations

Ripple:

$$r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\%$$

Voltage regulation:

$$\%\text{V.R.} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100\%$$

Half-wave rectifier:

$$V_{\text{dc}} = 0.318V_m, \qquad V_r(\text{rms}) = 0.385V_m$$

$$r = \frac{0.385V_m}{0.318V_m} \times 100\% = 121\%$$

Full-wave rectifier:

$$V_{\text{dc}} = 0.636V_m, \qquad V_r(\text{rms}) = 0.308V_m$$

$$r = \frac{0.308V_m}{0.636V_m} \times 100\% = 48\%$$

Simple capacitor filter:

$$V_r(\text{rms}) = \frac{I_{\text{dc}}}{4\sqrt{3}fC} = \frac{2.4I_{\text{dc}}}{C} = \frac{2.4V_{\text{dc}}}{R_LC}, \qquad V_{\text{dc}} = V_m - \frac{I_{\text{dc}}}{4fC} = \frac{4.17I_{dc}}{C}$$

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} \times 100\% = \frac{2.4I_{\text{dc}}}{CV_{\text{dc}}} \times 100\% = \frac{2.4}{R_LC} \times 100\%$$

RC filter:

$$V'_{\text{dc}} = \frac{R_L}{R + R_L}V_{\text{dc}}, \qquad X_C = \frac{1.3}{C}, \qquad V'_r(\text{rms}) = \frac{X_C}{R}V_r(\text{rms})$$

Op-amp series regulator:

$$V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z$$

15.9 COMPUTER ANALYSIS

Program 15.1—Op-Amp Series Regulator

The op-amp series regulator circuit of Fig. 15.16 can be analyzed using PSpice, with the resulting schematic drawn as shown in Fig. 15.38. The **Analysis Setup** was used to provide

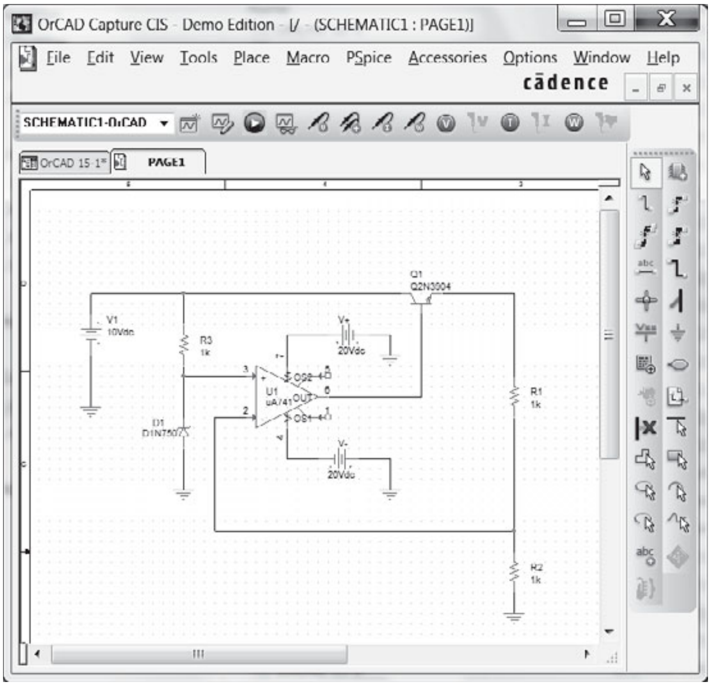

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File
Edit
View
Tools
Place
Macro
PSpice
Accessories
Options
Window
Help
cādence
SCHEMATIC1-OrCAD
OrCAD 15-1*
PAGE1
Q1
Q2N3004
V1
10Vdc
R3
1k
V+
20Vdc
U1
uA741
OS2
OUT
OS1
3
2
5
6
1
D1
D1N750
V-
20Vdc
R1
1k
R2
1k

FIG. 15.38

Op-amp series regulator using PSpice.

a dc voltage sweep from 8 V to 15 V in 0.5-V increments. Diode D_1 provides a Zener voltage of 4.7 V ($V_Z = 4.7$), and transistor Q_1 is set to beta = 100. Using Eq. (15.18), we obtain

$$V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z = \left(1 + \frac{1\text{ k}\Omega}{1\text{ k}\Omega}\right)4.7\text{ V} = 9.4\text{ V}$$

Notice in Fig. 15.38 that the regulated output voltage is 9.25 V when the input is 10 V. Figure 15.39 shows the **PROBE** output for the dc voltage sweep. Notice also that after the input goes above about 9 V, the output is held regulated at about 9.3 V.

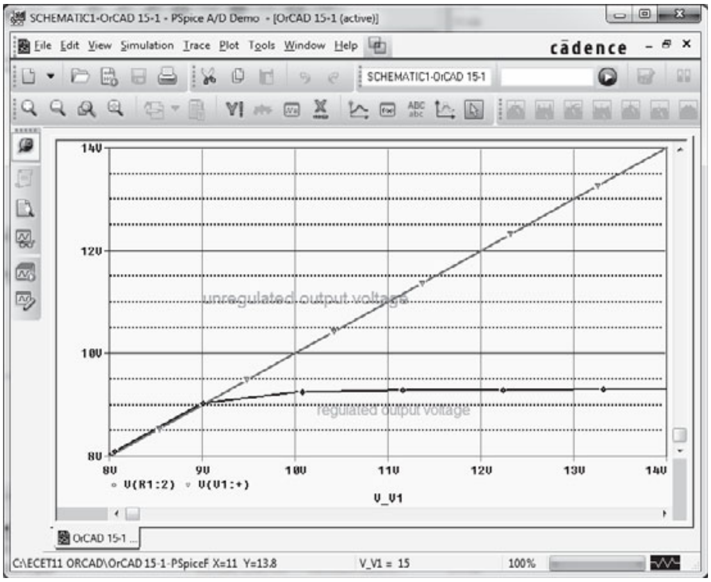

SCHEMATIC1-OrCAD 15-1 - PSpice A/D Demo - [OrCAD 15-1 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 15-1
14V
12V
10V
8V
8V
9V
10V
11V
12V
13V
14V
unregulated output voltage
regulated output voltage
V(R1:2) V(V1:+)
V_V1
OrCAD 15-1 ...
C:\ECET11 ORCAD\OrCAD 15-1-PSpiceF X=11 Y=13.8
V_V1 = 15
100%

FIG. 15.39

Probe output showing the voltage regulation of Fig. 15.38.

Program 15.2—Shunt Voltage Regulator Using Op-Amp

The shunt voltage regulator circuit of Fig. 15.40 was drawn using PSpice. With the Zener voltage set at 4.7 V and transistor beta set at 100, the output is 9.255 V when the input is 10 V. A dc sweep from 8 V to 15 V is shown in the **PROBE** output in Fig. 15.41. The circuit provides good voltage regulation for inputs from about 9.5 V to over 14 V, the output being held at the regulated value of about 9.3 V.

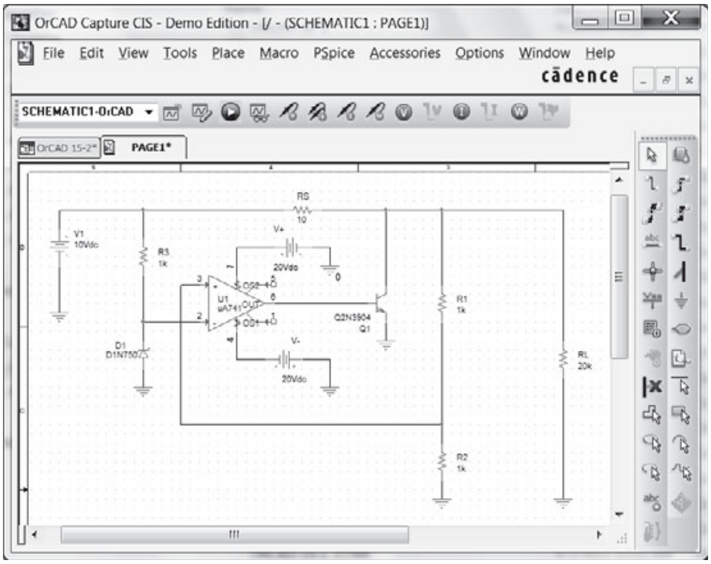

OrCAD Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Tools Place Macro PSpice Accessories Options Window Help
cādence
SCHEMATIC1-OrCAD
OrCAD 15-2*
PAGE1*
RS
10
V1
10Vdc
R3
1k
V+
20Vdc
0
U1
uA741
OUT
OS2
OS1
3
2
6
Q2N3904
Q1
R1
1k
D1
D1N750
V-
20Vdc
RL
20k
R2
1k

FIG. 15.40

Shunt voltage regulator using an op-amp.

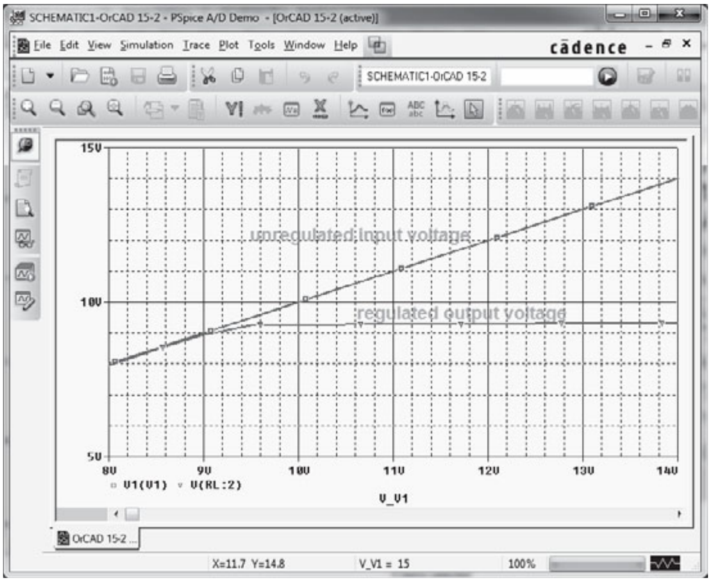

SCHEMATIC1-OrCAD 15-2 - PSpice A/D Demo - [OrCAD 15-2 (active)]
File Edit View Simulation Trace Plot Tools Window Help
cādence
SCHEMATIC1-OrCAD 15-2
15V
10V
5V
8V
9V
10V
11V
12V
13V
14V
unregulated input voltage
regulated output voltage
V1(V1)
V(RL:2)
V_V1
OrCAD 15-2
X=11.7 Y=14.8
V_V1 = 15
100%

FIG. 15.41

Probe output for the dc voltage sweep of Fig. 15.40.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

15.2 General Filter Considerations

1. What is the ripple factor of a sinusoidal signal having peak ripple of 2 V on an average of 50 V?
2. A filter circuit provides an output of 28 V unloaded and 25 V under full-load operation. Calculate the percentage voltage regulation.
3. A half-wave rectifier develops 20 V dc. What is the value of the ripple voltage?
4. What is the rms ripple voltage of a full-wave rectifier with output voltage 8 V dc?

15.3 Capacitor Filter

5. A simple capacitor filter fed by a full-wave rectifier develops 14.5 V dc at 8.5% ripple factor. What is the output ripple voltage (rms)?
6. A full-wave rectified signal of 18 V peak is fed into a capacitor filter. What is the voltage regulation of the filter if the output is 17 V dc at full load?
7. A full-wave rectified voltage of 18 V peak is connected to a 400-μF filter capacitor. What are the ripple and dc voltages across the capacitor at a load of 100 mA?
8. A full-wave rectifier operating from the 60-Hz ac supply produces a 20-V peak rectified voltage. If a 200-μF capacitor is used, calculate the ripple at a load of 120 mA.
9. A full-wave rectifier (operating from a 60-Hz supply) drives a capacitor-filter circuit ($C = 100\ \mu$F), which develops 12 V dc when connected to a 2.5-kΩ load. Calculate the output voltage ripple.
10. Calculate the size of the filter capacitor needed to obtain a filtered voltage having 15% ripple at a load of 150 mA. The full-wave rectified voltage is 24 V dc, and the supply is 60 Hz.

*11. A 500-μF capacitor provides a load current of 200 mA at 8% ripple. Calculate the peak rectified voltage obtained from the 60-Hz supply and the dc voltage across the filter capacitor.

12. Calculate the size of the filter capacitor needed to obtain a filtered voltage with 7% ripple at a load of 200 mA. The full-wave rectified voltage is 30 V dc and the supply is 60 Hz.
13. Calculate the percentage ripple for the voltage developed across a 120-μF filter capacitor when providing a load current of 80 mA. The full-wave rectifier operating from the 60-Hz supply develops a peak rectified voltage of 25 V.

15.4 *RC* Filter

14. An *RC* filter stage is added after a capacitor filter to reduce the percentage of ripple to 2%. Calculate the ripple voltage at the output of the *RC* filter stage providing 80 V dc.

***15.** An *RC* filter stage ($R = 33\ \Omega$, $C = 120\ \mu\text{F}$) is used to filter a signal of 24 V dc with 2 V rms operating from a full-wave rectifier. Calculate the percentage ripple at the output of the *RC* section for a 100-mA load. Also calculate the ripple of the filtered signal applied to the *RC* stage.

***16.** A simple capacitor filter has an input of 40 V dc. If this voltage is fed through an *RC* filter section ($R = 50\ \Omega$, $C = 40\ \mu\text{F}$), what is the load current for a load resistance of 500 Ω?

17. Calculate the rms ripple voltage at the output of an *RC* filter section that feeds a 1-kΩ load when the filter input is 50 V dc with 2.5-V rms ripple from a full-wave rectifier and capacitor filter. The *RC* filter section components are $R = 100\ \Omega$ and $C = 100\ \mu\text{F}$.

18. If the no-load output voltage for Problem 17 is 50 V, calculate the percentage voltage regulation with a 1-kΩ load.

15.5 Discrete Transistor Voltage Regulation

***19.** Calculate the output voltage and Zener diode current in the regulator circuit of Fig. 15.42.

20. What regulated output voltage results in the circuit of Fig. 15.43?

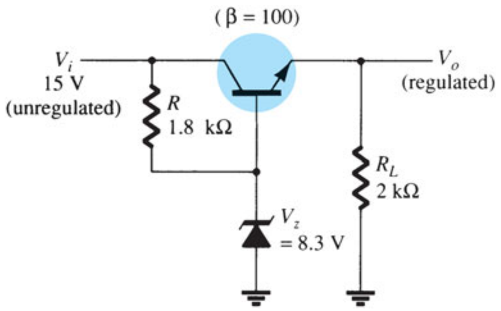


FIG. 15.42
Problem 19.

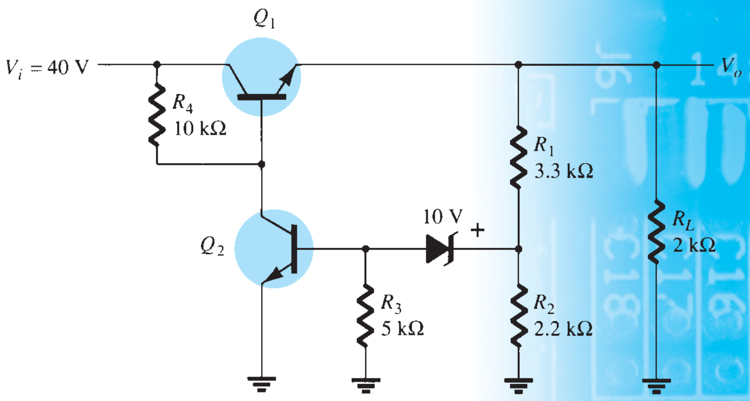


FIG. 15.43
Problem 20.

21. Calculate the regulated output voltage in the circuit of Fig. 15.44.

22. Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 15.45.

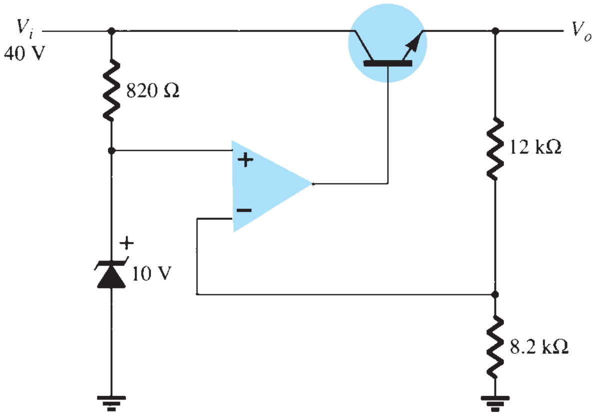


FIG. 15.44
Problem 21.

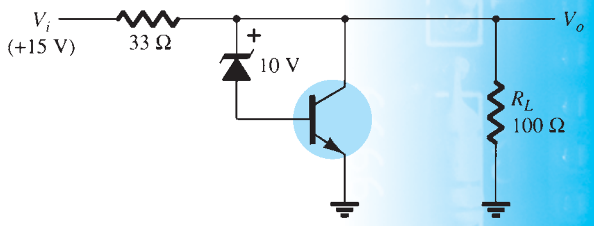


FIG. 15.45
Problem 22.

15.6 IC Voltage Regulators

23. Draw the circuit of a voltage supply comprised of a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +12 V.

***24.** Calculate the minimum input voltage of the full-wave rectifier and filter capacitor network in Fig. 15.46 when connected to a load drawing 250 mA.

***25.** Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 15.47.

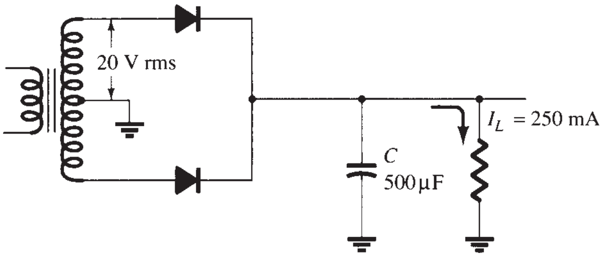

20 V rms
I_L = 250 mA
C
500 μF

FIG. 15.46
Problem 24.

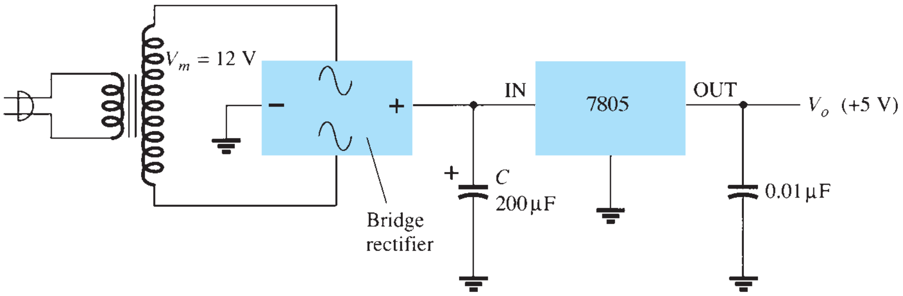

V_m = 12 V
−
+
IN
7805
OUT
V_o (+5 V)
+
C
200 μF
0.01 μF
Bridge
rectifier

FIG. 15.47
Problem 25.

26. Determine the regulated voltage in the circuit of Fig. 15.30 with $R_1 = 240\ \Omega$ and $R_2 = 1.8\ \text{k}\Omega$.

27. Determine the regulated output voltage from the circuit of Fig. 15.48.

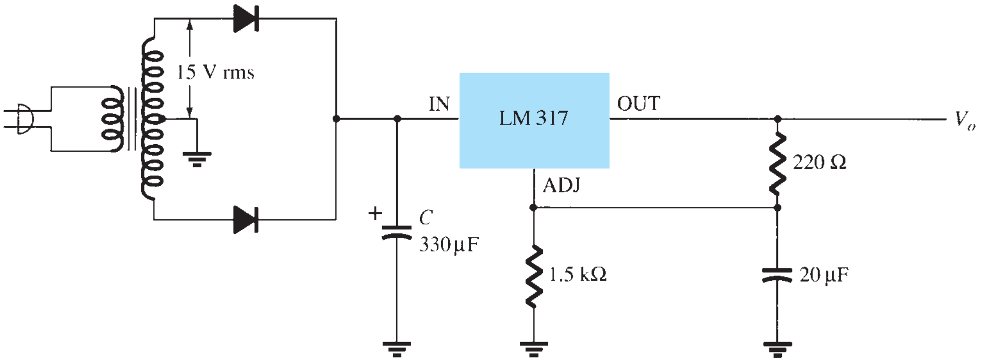

15 V rms
IN
LM 317
OUT
V_o
220 Ω
ADJ
+
C
330 μF
1.5 kΩ
20 μF

FIG. 15.48
Problem 27.

15.9 Computer Analysis

***28.** Modify the circuit of Fig. 15.38 to include a load resistor R_L. Keeping the input voltage fixed at 10 V, do a sweep of the load resistor from 100 Ω to 20 kΩ, showing the output voltage using Probe.

***29.** For the circuit of Fig. 15.40, do a sweep showing the output voltage for R_L varied from 5 kΩ to 20 kΩ.

***30.** Run a PSpice analysis of the circuit of Fig. 15.19 for $V_Z = 4.7$ V and beta (Q_1) = beta (Q_2) = 100, and vary V_i from 5 V to 20 V.

16

Other Two-Terminal Devices

CHAPTER OBJECTIVES

To become familiar with the characteristics and areas of application of

- Schottky barrier and varactor diodes
- Solar cells, photodiodes, photoconductive cells, and IR emitters
- LCDs
- Thermistors
- Tunnel diodes

16.1 INTRODUCTION

There are a number of two-terminal devices having a single *p–n* junction like the semiconductor or Zener diode but with different modes of operation, terminal characteristics, and areas of application. A number, including the Schottky barrier, varactor, solar cell, photodiode, IR emitter and tunnel diodes, will be introduced in this chapter. In addition, two-terminal devices of a different construction, such as the photoconductive cell, LCD (liquid-crystal display), and thermistor, will be examined.

16.2 SCHOTTKY BARRIER (HOT-CARRIER) DIODES

There has been increasing interest in a two-terminal device referred to as a *Schottky-barrier, surface-barrier,* or *hot-carrier* diode. Its areas of application were first limited to the very high frequency range due to its quick response time (especially important at high frequencies) and lower noise figure (a quantity of real importance in high-frequency applications). In recent years, however, it is appearing more and more in low-voltage/high-current power supplies and ac-to-dc converters. Other areas of application of the device include radar systems, Schottky TTL logic for computers, mixers and detectors in communication equipment, instrumentation, and analog-to-digital converters.

Its construction is quite different from the conventional *p–n* junction in that a metal–semiconductor junction is created such as shown in Fig. 16.1. The semiconductor is normally *n*-type silicon (although *p*-type silicon is sometimes used), whereas a host of different metals, such as molybdenum, platinum, chrome, or tungsten, are used. Different construction techniques result in a different set of characteristics for the device, such as increased frequency range, lower forward bias, and so on. In general, however, Schottky diode construction results in a more uniform junction region and a high level of ruggedness.

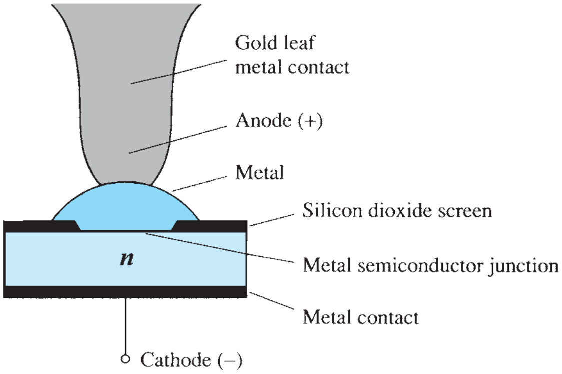


FIG. 16.1
Schottky diode.

In both materials, the electron is the majority carrier. In the metal, the level of minority carriers (holes) is insignificant. When the materials are joined, the electrons in the *n*-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very high kinetic energy level compared to the electrons of the metal, they are commonly called "hot carriers." In the conventional *p–n* junction, there was the injection of minority carriers into the adjoining region. Here the electrons are injected into a region of the same electron plurality. Schottky diodes are therefore unique in that conduction is entirely by majority carriers. The heavy flow of electrons into the metal creates a region near the junction surface depleted of carriers in the silicon material—much like the depletion region in the *p–n* junction diode. The additional carriers in the metal establish a "negative wall" in the metal at the boundary between the two materials. The net result is a "surface barrier" between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a "negative wall" at the surface of the metal.

The application of a forward bias as shown in the first quadrant of Fig. 16.2 will reduce the strength of the negative barrier through the attraction of the applied positive potential for electrons from this region. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential. The barrier at the junction for a Schottky diode is less than that of the *p–n* junction device in both the forward- and reverse-bias regions. The result is therefore a higher current at the

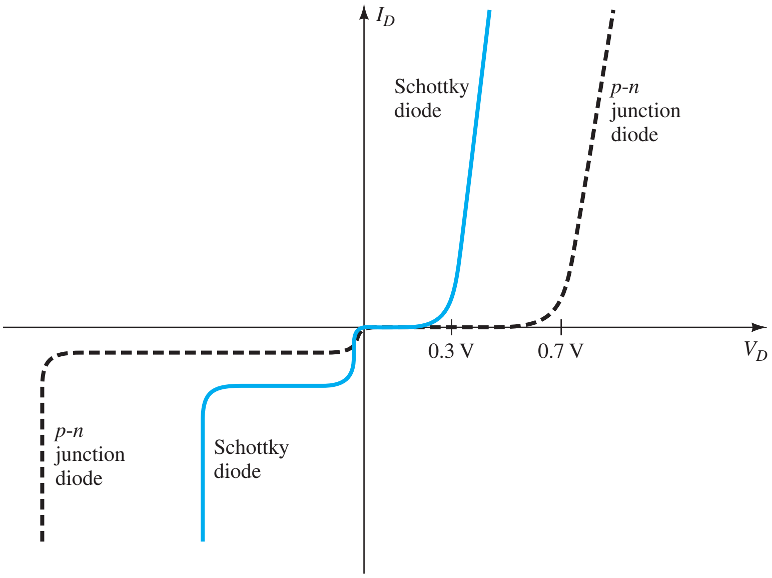


FIG. 16.2
Comparison of characteristics of hot-carrier and p–n junction diodes.

same applied bias in the forward- and reverse-bias regions. This is a desirable effect in the forward-bias region but highly undesirable in the reverse-bias region.

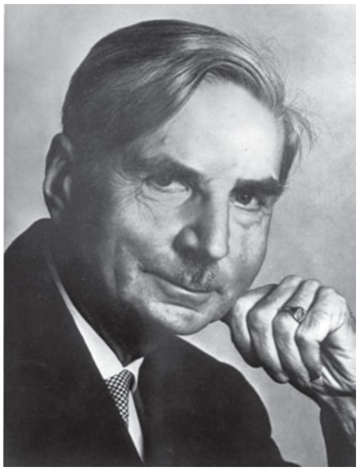
The exponential rise in current with forward bias is described by Eq. (1.2) but with n dependent on the construction technique (1.05 for the metal-whisker type of construction, which is somewhat similar to the germanium diode). In the reverse-bias region, the current I_s is due primarily to those electrons in the metal passing into the semiconductor material. One of the areas of continuing research on the Schottky diode centers on reducing the high leakage currents that result with temperatures over 100°C. Through design, improved units are available that have a temperature range from $-65°C$ to $+150°C$. At room temperature, I_s is typically in the microampere range for low-power units and the milliampere range for high-power devices, although it is typically larger than that encountered using conventional *p–n* junction devices with the same current limits. In addition, the PIV of Schottky diodes is usually significantly less than that of a comparable *p–n* junction unit. Typically, for a 50-A unit, the PIV of the Schottky diode is typically 50 V or less as compared to 150 V for the *p–n* junction variety. Recent advances, however, have resulted in Schottky diodes with PIVs greater than 100 V at this current level. It is obvious from the characteristics of Fig. 16.2 that the Schottky diode is closer to the ideal set of characteristics than the point contact and has levels of V_T less than those of the typical silicon semiconductor *p–n* junction. The level of V_T for the "hot-carrier" diode is controlled to a large measure by the metal employed. There is a trade-off between temperature range and level of V_T. An increase in one appears to correspond to a resulting increase in the other. In addition, the lower the range of allowable current levels, the lower is the value of V_T. For some low-level units, the value of V_T can be assumed to be essentially zero on an approximate basis. For the middle and high ranges, however, a value of 0.2 V appears to be a good representative value.

The maximum current rating of Schottky diodes is limited at present to about 100 A. One of the primary areas of application of this diode is in *switching power supplies* that operate in the frequency range of 20 kHz or more. A typical unit at 25°C may be rated at 50 A at a forward voltage of 0.6 V with a recovery time of 10 ns for use in one of these supplies. A *p–n* junction device with the same current limit of 50 A may have a forward voltage drop of 1.1 V and a recovery time of 30 ns to 50 ns. The difference in forward voltage may not appear significant, but consider the power dissipation difference: $P_{\text{hot carrier}} = (0.6\text{ V})(50\text{ A}) = 30\text{ W}$ compared to $P_{p\text{–}n} = (1.1\text{ V})(50\text{ A}) = 55\text{ W}$, which is a measurable difference when efficiency criteria must be met. There will, of course, be a higher dissipation in the reverse-bias region for the Schottky diode due to the higher leakage current, but the total power loss in the forward- and reverse-bias regions is still significantly improved as compared to the *p–n* junction device.

Recall from our discussion of reverse recovery time in Chapter 1 that the injected minority carriers accounted for the high level of t_{rr}. The absence of minority carriers at any appreciable level in the Schottky diode results in a reverse recovery time of significantly lower levels, as indicated above. This is the primary reason Schottky diodes are so effective at frequencies approaching 20 GHz, where the device must switch states at a very high rate. For higher frequencies the point-contact diode, with its very small junction area, is still employed.

The equivalent circuit for the device (with typical values) and a commonly used symbol appear in Fig. 16.3. A number of manufacturers prefer to use the standard diode symbol for the device since its function is essentially the same. The inductance L_P and capacitance C_P are package values, and r_B is the series resistance, which includes the contact and the bulk resistance. The resistance r_d and the capacitance C_J are defined by equations introduced in earlier chapters. For many applications, an excellent approximate equivalent circuit simply includes an ideal diode in parallel with the junction capacitance as shown in Fig. 16.4.

A general-purpose Schottky diode manufactured by the Vishay Corporation appears in Fig. 16.5 with the maximum ratings and electrical characteristics. Note in the maximum ratings that the peak V_R is limited to 30 V and the maximum forward current is limited to 200 mA = 0.2 A. However, it can handle a surge current of 5 A if necessary. The electrical characteristics reveal that at low currents neighboring 1 mA (just above the turn-on level) the forward voltage is a maximum of 0.32 V, which is significantly less than the 0.7 V of a typical silicon diode. The current must reach a level approaching 80 mA before the forward



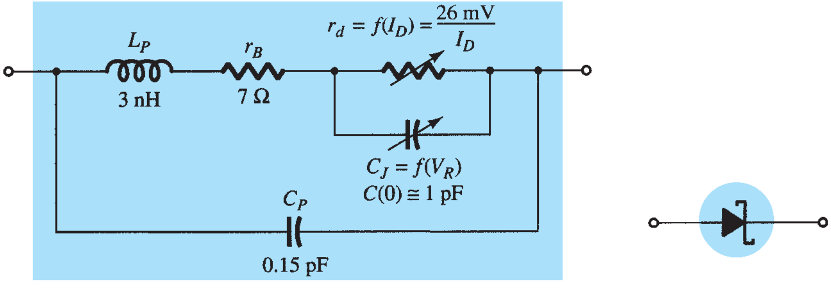
German (Marburg and Berlin, Germany)
(1886–1976)
Professor of Theoretical Physics—University of Rostock
Research Physicist—Siemens Industrial Research Laboratories

Dr. Walter Hermann Schottky was born in Zurich, Switzerland, on July 23, 1886. After obtaining his bachelor of science degree in physics from the University of Berlin in 1908 he obtained his PhD in physics at the university in 1912.

Best known for the Schottky effect, which defines the interaction between a point charge and a flat metal surface. An effect resulting in the popular Schottky diode that has a number of important improvements over the typical semiconductor diode. He is also recognized for the invention of the superhet, the tetrode thermonic valve (multigrid vacuum tube) and co-invention (with Erwin Gerlach) of the ribbon microphone.

Awards include the Royal Society Hughes award in 1936 and the Werner-von-Siemens-Ring in 1964. In addition the Walter Schottky Institute in Germany is named after him.

Dr. Walter Herman Schottky
(Photo courtesy of the Siemens Corporate Archives, Munich.)



(a) (b)

FIG. 16.3
Schottky (hot-carrier) diode: (a) equivalent circuit; (b) symbol.

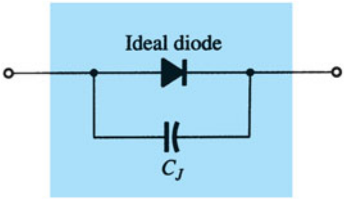
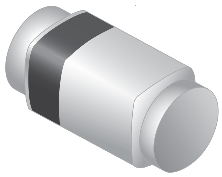


FIG. 16.4
Approximate equivalent circuit for the Schottky diode.

Small-Signal Schottky Diode



Applications
- Applications where a very low forward voltage is required

ABSOLUTE MAXIMUM RATINGS T_{amb} = 25°C, unless otherwise specified

Parameter	Test Condition	Symbol	Value	Unit
Reverse voltage		V_R	30	V
Peak forward surge current	$t_p = 10$ ms	I_{FSM}	5	A
Repetitive peak forward current	$t_p \leq 1$ s	I_{FRM}	300	mA
Forward current		I_F	200	mA
Average forward current		I_{FAV}	200	mA

THERMAL CHARACTERISTICS T_{amb} = 25°C, unless otherwise specified

Parameter	Test Condition	Symbol	Value	Unit
Junction to ambient air	on PC board 50 mm × 50 mm × 1.6 mm	R_{thJA}	320	K/W
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	–65 to + 150	°C

ELECTRICAL CHARACTERISTICS T_{amb} = 25°C, unless otherwise specified

Parameter	Test Condition	Symbol	Min	Typ.	Max	Unit
Forward voltage	$I_F = 0.1$ mA	V_F			240	mV
	$I_F = 1$ mA	V_F			320	mV
	$I_F = 10$ mA	V_F			400	mV
	$I_F = 30$ mA	V_F			500	mV
	$I_F = 100$ mA	V_F			800	mV
Reverse current	$V_R = 25$ V, $t_p = 300$ µs	I_R			2.3	µA
Diode capacitance	$V_R = 1$ V, $f = 1$ MHz	C_D			10	pF

FIG. 16.5
Maximum ratings, thermal characteristics, and electrical characteristics for a Vishay BAS285 Schottky diode.

voltage reaches a level that approaches 0.7 V. For switching applications the capacitance level is important, but the level of 10 pF is generally acceptable for most applications. Finally, note that the reverse current is only 2.3 μA.

The typical characteristics of the device appear in Fig. 16.6. In Fig. 16.6a we find that the forward voltage is about 0.5 V at 20 mA but drops to about 0.45 V at 10 mA. At 0.1 mA

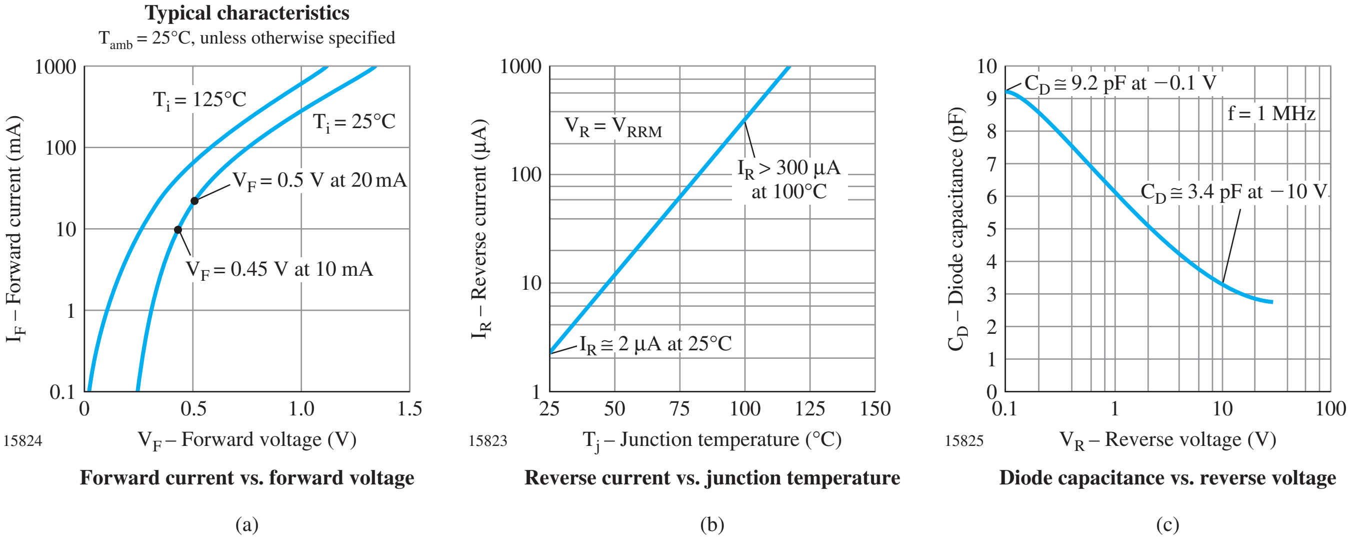


FIG. 16.6

Typical characteristics for a Vishay BAS285 Shottky diode.

the forward voltage drops to only 0.25 V. In Fig. 16.6b we find that the reverse current increases rapidly with temperature. At 100°C it is exceeding 300 μA $=$ 0.3 mA, which is quite excessive. Fortunately at lower temperatures such as 25°C it is only 2 μA. Fig. 16.6c reveals why the capacitive element is an integral part of the equivalent circuit. At $V_R = -0.1$ V it is close to 9.2 pF, whereas at $V_R = -10$ V it has dropped to 3.4 pF.

16.3 VARACTOR (VARICAP) DIODES

Varactor (also called varicap, VVC [voltage-variable capacitance], or tuning) diodes are semiconductor, voltage-dependent, variable capacitors. Their mode of operation depends on the capacitance that exists at the *p–n* junction when the element is reverse-biased. Under reverse-bias conditions, there is a region of uncovered charge on either side of the junction that together make up the depletion region and define the depletion width W_d. The transition capacitance C_T established by the isolated uncovered charges is determined by

$$\boxed{C_T = \epsilon \frac{A}{W_d}} \tag{16.1}$$

where ϵ is the permittivity of the semiconductor materials, A is the *p–n* junction area, and W_d is the depletion width.

As the reverse-bias potential increases, the width of the depletion region increases, which in turn reduces the transition capacitance. The characteristics of a typical commercially available varicap diode appear in Fig. 16.7. Note the initial sharp decline in C_T with increase in reverse bias. The normal range of V_R for VVC diodes is limited to about 20 V. In terms of the applied reverse bias, the transition capacitance is given approximately by

$$\boxed{C_T = \frac{K}{(V_T + V_R)^n}} \tag{16.2}$$

where K = constant determined by the semiconductor material and construction technique
V_T = knee potential as defined in Section 1.6
V_R = magnitude of the applied reverse-bias potential
$n = \frac{1}{2}$ for alloy junctions and $\frac{1}{3}$ for diffused junctions

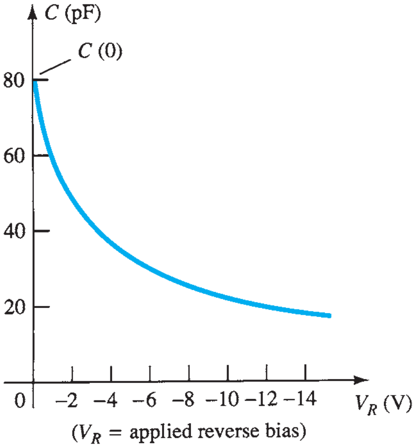


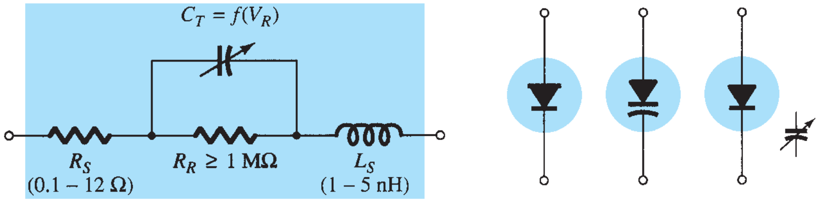
FIG. 16.7

Varicap characteristics: C (pF) versus V_R.

In terms of the capacitance at the zero-bias condition $C(0)$, the capacitance as a function of V_R is given by

$$\boxed{C_T(V_R) = \frac{C(0)}{(1 + |V_R/V_T|)^n}} \tag{16.3}$$

The symbols most commonly used for the varicap diode and a first approximation for its equivalent circuit in the reverse-bias region are shown in Fig. 16.8. Since we are in the reverse-bias region, the resistance in the equivalent circuit is very large in magnitude—typically 1 MΩ or larger—whereas R_S, the geometric resistance of the diode, is, as indicated in Fig. 16.8, very small. The magnitude of C_T will vary from about 2 pF to 100 pF depending on the varicap considered. To ensure that R_R is as large (for minimum leakage current) as possible, silicon is normally used in varicap diodes. The fact that the device will be employed at very high frequencies requires that we include the inductance L_S even though it is measured in nanohenries. Recall that $X_L = 2\pi fL$, and a frequency of 10 GHz with $L_S = 1$ nH results in $X_{L_S} = 2\pi fL = (6.28)(10^{10}\text{ Hz})(10^{-9}\text{ F}) = 62.8\ \Omega$. There is obviously, therefore, a frequency limit associated with the use of each varicap diode. Assuming the proper frequency range and a low value of R_S and X_{L_S} compared to the other series elements, then we can replace the equivalent circuit for the varicap of Fig. 16.8a by the variable capacitor alone.



(a)

(b)

FIG. 16.8

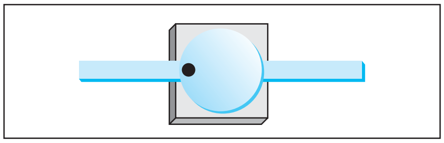
Varicap diode: (a) equivalent circuit in the reverse-bias region; (b) symbols.

The *capacitance temperature coefficient* is defined by

$$\boxed{TC_C = \frac{\Delta C}{C_0(T_1 - T_0)} \times 100\%} \quad \%/^\circ\text{C} \tag{16.4}$$

where ΔC is the change in capacitance due to the temperature change $T_1 - T_0$ and C_0 is the capacitance at T_0 for a particular reverse-bias potential. For example, at $V_R = -3$ V and $C_0 = 29$ pF with $V_R = 3$ V and $T_0 = 25°\text{C}$. A change in capacitance ΔC could then be determined using Eq. (16.4) simply by substituting the new temperature T_1 and the associated TC_C. At a new V_R, the value of TC_C would change accordingly.

The packaging and maximum ratings for a Micrometrics hyperabrupt tuning varactor are provided in Fig. 16.9(a). The hyperabrupt junction is created using a special ion-implantation technique that results in a more abrupt junction than the more common abrupt junction varactor. The hyperabrupt junction varactor is chosen when a more linear relationship between the generated frequency of a VCO (voltage-controlled oscillator) and the controlling voltage is desired. This series of diodes is ideal for LC resonant frequencies up to 100 MHz with an almost straight-line relationship for the 1.5 V to 4 V tuning range. As indicated by the maximum ratings, the peak forward current is about 100 mA and the power dissipation 250 mW. The reverse voltage rating is defined by the V_{br} level in the performance characteristics of Fig. 16.10.



(a)

Maximum Ratings

Parameter	Symbol	Value	Units
Reverse voltage	V_r	Same as V_{br}	Volts
Forward current	I_f	100	mA
Power dissipation	Pd (25°C)	250	mW
Operating temperature	T_{op}	–55 to +150	°C
Storage temperature	T_{stg}	–65 to +200	°C

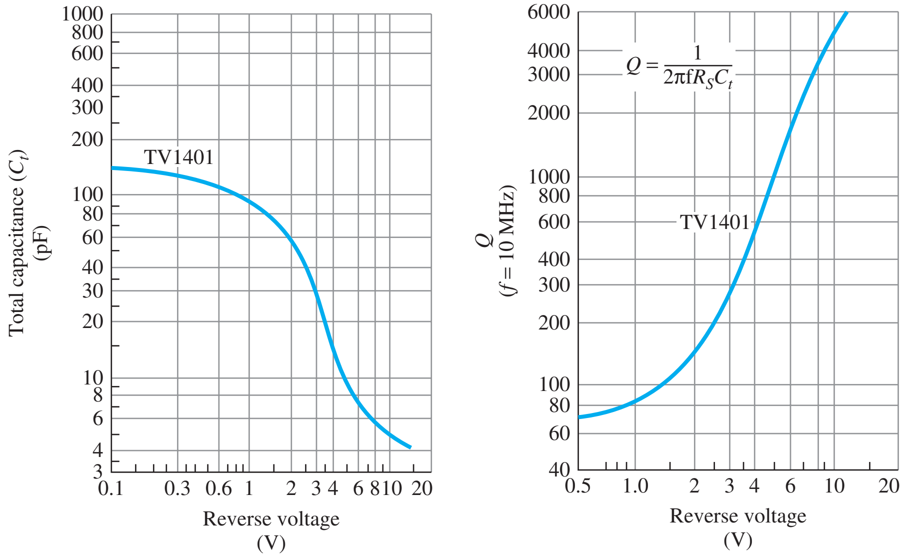
(b)

FIG. 16.9

Micrometrics hyperabrupt tuning varactor: (a) packaging; (b) maximum ratings.

The electrical characteristics and typical performance characteristics are provided in Fig. 16.10. Note for the TV 1401 that the capacitance can run from about 58 pF at a reverse voltage of 2 V down to 6.1 pF at a reverse voltage of 7 V validating the drop-off curve of Fig. 16.7. It then continues to drop to about 5 pF at a reverse voltage of 10 V. For varactor diodes the tuning ratio is important in the sense that it gives a quick idea of how much the capacitance will change between typical operating ranges of applied voltage. As shown in the electrical characteristics the capacitance will typically drop by a factor of 13 when the reverse voltage is changed from 1.25 V to 7 V. For the change from 2 V to 10 V the change in capacitance is in the range of 10 to 17, depending on the unit. The change in capacitance is plotted in Fig. 16.10(a) for the full range of anticipated application. For the range of reverse voltage shown, the capacitance drops from about 130 pF (log scale) at $V_r = 0.1$ V to about 4 pF $V_r = 15$ V. The quality factor Q is defined as introduced for resonant circuits in earlier sections of this text. It is an important factor when the varactor is used in oscillator design because it can have a pronounced effect on the noise performance level. A high Q will result in a high-selectivity response curve and a rejection of frequencies associated with noise. At a reverse voltage of 2 V and a typical operating frequency of 10 MHz the Q factor is quite high at a typical level of 140 and minimum level of 75. Note the provided curve for Q versus reverse voltage for a fixed frequency of 10 MHz. It increases rapidly with reverse voltage because the total junction capacitance drops with reverse voltage.

Typical Performance



Q $V_r = 2$ Vdc		V_{br} (Vdc) $I_r = 10$ μ Adc	I_r (nAdc) $V_r = 10$ Vdc	Part number
$F = 1$ MHz MIN/TYP	$F = 10$ MHz MIN/TYP	MIN/TYP	TYP/MAX	
–	75/140	12/20	10/50	TV1401
200/700	–	12/20	50/100	TV1402
200/700	–	12/20	100/1000	TV1403

(a)

Electrical Characteristics

Total capacitance, C_t $F = 1$ MHz (pF)				Tuning ratio, T_r $F = 1$ MHz		Part number
$V_r = 2$ Vdc MIN/TYP/MAX	$V_r = 7$ Vdc TYP	$V_r = 10$ Vdc MIN/TYP/MAX	$V_r = 125$ Vdc TYP	C(1.25V)/C(7V) TYP	C(2V)/C(10V) MIN/TYP/MAX	
46/57/68	6.1	4.2/4.7/5.2	81.5	13	10/12/17	TV1401
46/57/68	6.1	4.2/4.7/5.2	81.5	13	10/12/17	TV1402
46/57/-	6.1	-/4.7/5.2	81.5	13	10/12/-	TV1403

(b)

FIG. 16.10

Micrometrics TV 1400 series of varactor diodes: (a) typical performance; (b) electrical characteristics.

Some of the high-frequency (as defined by the small capacitance levels) areas of application include FM modulators, automatic-frequency-control devices, adjustable bandpass filters, and parametric amplifiers.

Application

In Fig. 16.11, the varactor diode is employed in a tuning network. That is, the resonant frequency of the parallel LC combination is determined by $f_p = 1/2\pi\sqrt{L_2C'_T}$ (high-Q system) with the level of $C'_T = C_T + C_C$ determined by the applied reverse-bias potential V_{DD}. The coupling capacitor C_C is present to provide isolation between the shorting effect of L_2 and the applied bias. The selected frequencies of the tuned network are then passed on to the high-input amplifier for further amplification.

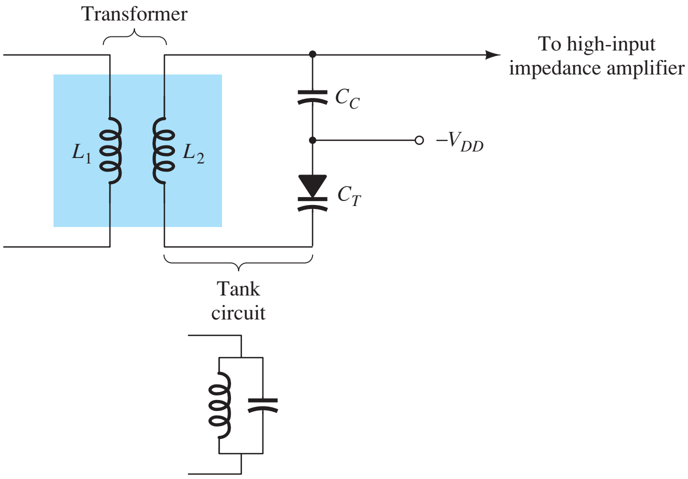


FIG. 16.11
Tuning network employing a varactor diode.

16.4 SOLAR CELLS

In recent years, there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mW/cm^2 (1 kW/m^2), it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy.

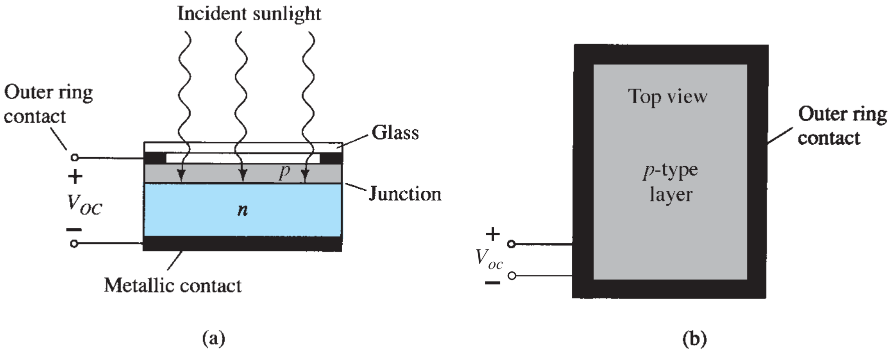


FIG. 16.12
Solar cell: (a) cross section; (b) top view.

The basic construction of a silicon *p–n* junction solar cell appears in Fig. 16.12. As shown in the top view, every effort is made to ensure that the surface area perpendicular to the sun is a maximum. Also note that the metallic conductor connected to the *p*-type material and the thickness of the *p*-type material are such that they ensure that a maximum number of photons of light energy will reach the junction. A photon of light energy in this region may collide with a valence electron and impart to it sufficient energy to leave the parent atom. The result is a generation of free electrons and holes. This phenomenon will occur on each side of the junction. In the *p*-type material, the newly generated electrons are minority carriers and will move rather freely across the junction as explained for the basic *p–n* junction with no applied bias. A similar discussion is true for the holes generated in the *n*-type material. The result is an increase in the minority-carrier flow, which is opposite in direction to the conventional forward current of a *p–n* junction. The current for a single-cell silicon solar cell will increase in an almost linear fashion with the intensity of the incident light as shown in Fig. 16.13. Double the incident light will double the resulting current and so on. The plot is for the maximum current generated for a particular level of incident light. Since maximum conditions result when the output is short-circuited as shown in Fig. 16.13, the label for the resulting current is I_{SC}. Under short-circuit conditions the output voltage is 0 V as shown in the same figure.

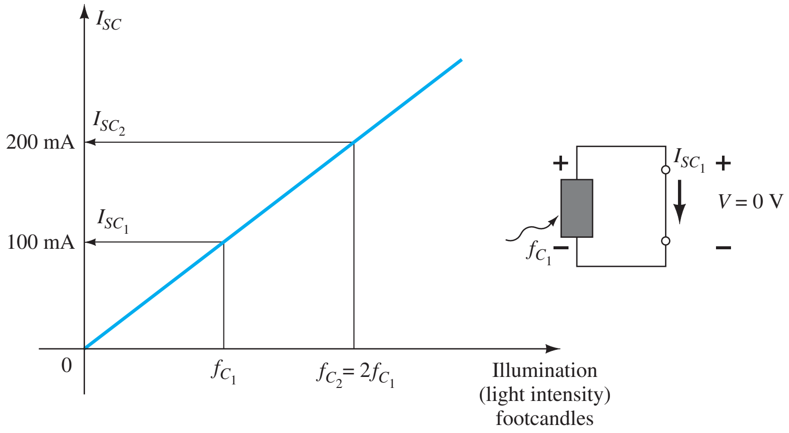


FIG. 16.13

Effect of light intensity on the short-circuit current.

A plot of the open-circuit voltage for the same levels of incident light is provided in Fig. 16.14. Note that it increases very rapidly to a level that stays within the boundaries of 0.5 V to 0.6 V. That is, for the broad range of incident light in Fig. 16.14, the terminal voltage is fairly constant. Since the output voltage is the open-circuit voltage as shown in the same figure, the label for the resulting voltage at each level of incident light is V_{OC}.

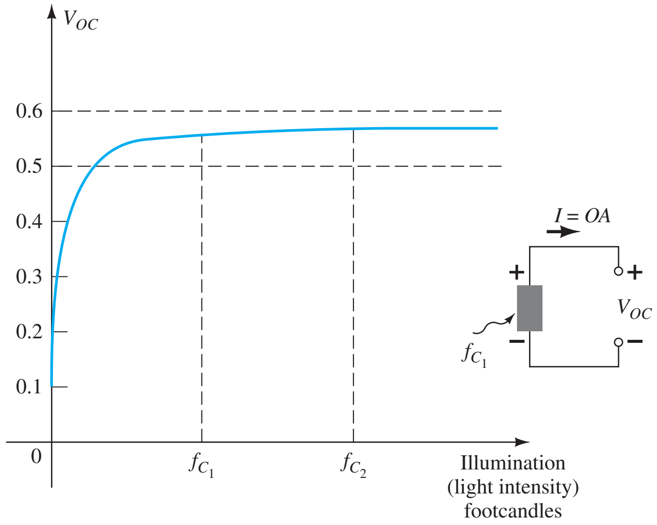


FIG. 16.14

Effect of light intensity on the open-circuit voltage.

In general, therefore,

The open-circuit potential generated by a solar cell is fairly constant, while the short-circuit maximum current will increase in a linear fashion.

Since the voltage is fairly constant, higher output voltages can be established by connecting the solar cells in a series. The current generated in a series configuration will be the same as generated by a single cell. For increased current levels at a single cell open-circuit voltage, solar cells can be connected in parallel.

If a plot of current versus voltage is generated as shown in Fig. 16.15 for a particular incident light, a curve for the power associated with the solar cell can be generated by simply using the equation $P = VI$.

Note in Fig. 16.15 that the short-circuit current is the maximum current with the level of current decreasing with increasing terminal voltage. Also take note that the level of voltage is fairly constant for the range of current from 0 A to just short of the maximum power point. Since the current curve is fairly level for the lower voltage levels, the increase in power is

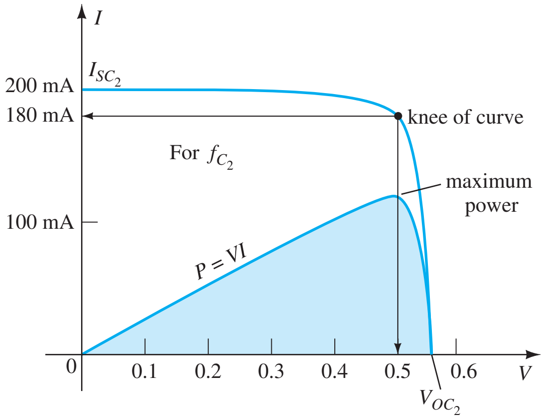


FIG. 16.15

Sketching the power curve for the light intensity f_{C_2}.

due primarily to the increasing levels of voltage using the power equation $P = VI$. Eventually, however, even though the voltage continues to increase, the current drops dramatically near V_{OC} and the power curve drops accordingly. The maximum power occurs in the knee region of the I–V curve as shown in Fig. 16.15. For this cell at f_{C_2} it is approximately

$$P = VI = (0.5\text{ V})(180\text{ mA}) = \mathbf{90\text{ mW}}$$

The level of current that results in a solar cell is directly related to the absorption characteristics of the material (referred to as the absorption coefficient), the wavelength of the incident light, and the intensity of the incident light.

Materials

The most common material in use today in the full range of bulk and thin-film solar cells is silicon in its various forms. Each form to be described is manufactured using a different process. The **single-crystal** silicon structure has an atomic lattice that is uniform, perfectly ordered, and of the highest purity. The typical range of efficiency extends from 14% to 17% with experimental levels of over 20%. **Polycrystalline** silicon solar cells are manufactured in a different, cheaper process but have lower levels of efficiency (9%–14%). However the reduced manufacturing cost and the fact that it can be cut into thinner layers than the single-crystal lattice make such cells a viable alternative. In recent years the introduction of **thin-film** technology has had a broad impact on the cost and range of application of solar cells. The very thin (less than 1 μm in many cases) semiconductor layers are deposited (using various spraying techniques) on a supporting structure such as glass, plastic, or metal. A compound, **amorphous silicon (a-Si),** is currently the most extensively used thin-film material. The reduced production costs, along with the high light absorption characteristics, balance out the efficiency levels that are reduced to single digits (6%–9%).

Another single-crystal compound, **gallium arsenide** (GaAs), is commonly used in bulk solar cells because of its high rate of absorption and higher energy conversion rate in the range 20%–30%. Additional thin-film materials include **cadmium telluride** (CdTe) and **copper indium diseelenide** ($CuInSe_2$ or CIS). CdTe has a very high light absorption level and is less expensive to manufacture with the same conversion efficiency as silicon. CIS is used in leading-edge research with conversion levels approaching 18% with high absorption and conversion rates.

Wavelength

The energy associated with each photon is directly related to the frequency of the traveling wave and determined by the following equation:

$$\boxed{W = \hbar f} \qquad (\text{joules}) \qquad \mathbf{(16.5)}$$

where $\hbar$ is called Planck's constant and is equal to 6.624×10^{-34} joule-seconds. You may recall from Section 1.16 that the frequency is related to the wavelength (distance between successive peaks) of the wave by the following equation:

$$\boxed{\lambda = \frac{v}{f}} \quad \text{(nm, angstrom units Å)} \tag{16.6}$$

where λ = wavelength in meters
v = velocity of light, 3×10^8 m/s
f = frequency of traveling wave in hertz

and $\text{Å} = 10^{-10}$ m, 1 nm $= 10^{-9}$ m

Substituting Eq. (16.6) into Eq. (16.5) we find

$$\boxed{W = \frac{\hbar v}{\lambda}} \quad \text{(joules)} \tag{16.7}$$

and find that the energy associated with a discrete package of photons is inversely proportional to the wavelength.

Clearly, therefore

The energy associated with the photons being absorbed by the semiconductor layer of a solar cell is a function of the wavelength of the incident light, and the longer the wavelength, the less the associated energy levels.

In addition it is important to realize that

Each photon can only cause the generation of one electron-hole pair. Any photon with energy levels higher than that required to release an electron will simply contribute to the heating of the solar cell.

For silicon, the absorption curve is provided as Fig. 16.16, showing that it peaks around 850 nm. As noted above, since the wavelength is shorter, the energy level associated with the color blue of the visible spectrum is significantly higher than that of green, red, or yellow. Take particular note of the wavelength 1200 nm corresponding with the point where the curve drops to the horizontal axis. This is the highest wavelength that will provide photons with sufficient energy to liberate electrons in the silicon material. In other words, at this wavelength the energy associated with the incident light is just enough to release an electron-hole pair. Any photon associated with longer wavelengths will not have sufficient energy associated with it to release an electron and will simply contribute to the heating of the solar cell.

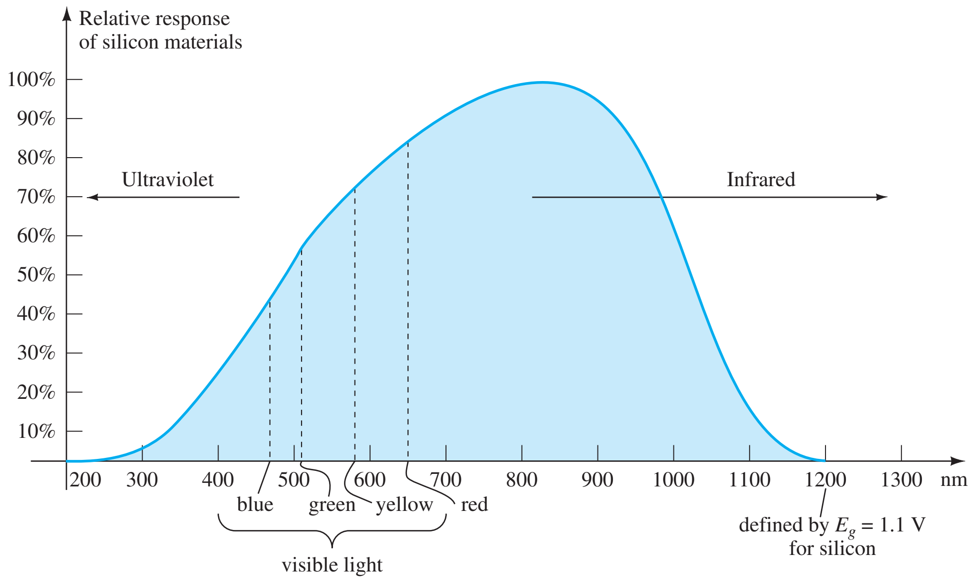


FIG. 16.16

Relative response of silicon versus the wavelength of the incident light.

Light Intensity

The third factor of major importance in the design of solar cells is the light intensity. The more intense the incident light, the greater the number of photons and resulting number of released electron-hole pairs. Light intensity is a measure of the amount of luminous flux falling on a particular surface area. Luminous flux is normally measured in lumens (lm) or watts. The two units are related by

$$\boxed{1 \text{ lumen} = 1 \text{ lm} = 1.496 \times 10^{-10} \text{ W}} \tag{16.8}$$

The light intensity is normally measured in lm/ft, footcandles (fc), or W/m, where

$$\boxed{1 \text{ lm/ft}^2 = 1\, fc = 1.609 \times 10^{-9} \text{ W/m}^2} \tag{16.9}$$

As noted earlier in this section the light intensity of the sun at sea level is about 100 mW/cm^2 or 1 kW/m^2, which gives us a good idea of the maximum levels that can be expected from the sun.

Current Maximum Levels of Efficiency

In recent years solar cell efficiencies at research institutes have passed the 40% plateau. In fact in 2011 an efficiency level of 43.5% was achieved. For thin-film technologies the maximum remains about 20%, whereas single-crystal GaAs cells are at 29% and single-crystal Si at 25%.

Applications

In Fig. 16.17 a commercially available Edmund Scientific Multi-Volt Output Solar can be used to provide a solar output of 3 V at 200 mA, 6 V at 100 mA, 9 V at 50 mA, and 12 V at 50 mA. Assuming a terminal voltage of 0.5 V for each cell the 3-V level would require six cells in a series, the 6-V level would require 12 cells in a series, and so on. The switch position will simply select which series combination of cells is part of the output voltage. The supply can be used to charge mobile phones, MP3 players, flashlights, and video games. The current levels are not sufficiently high to charge a 12-V car battery, which is charged by currents in the ampere range. Take note of the relatively small size of the unit for its range of applications.

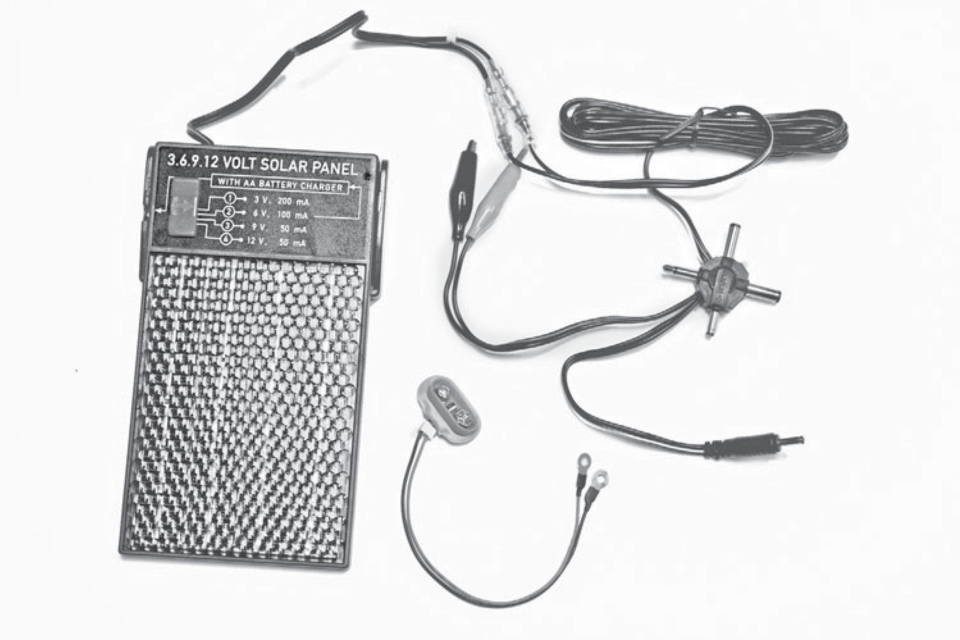
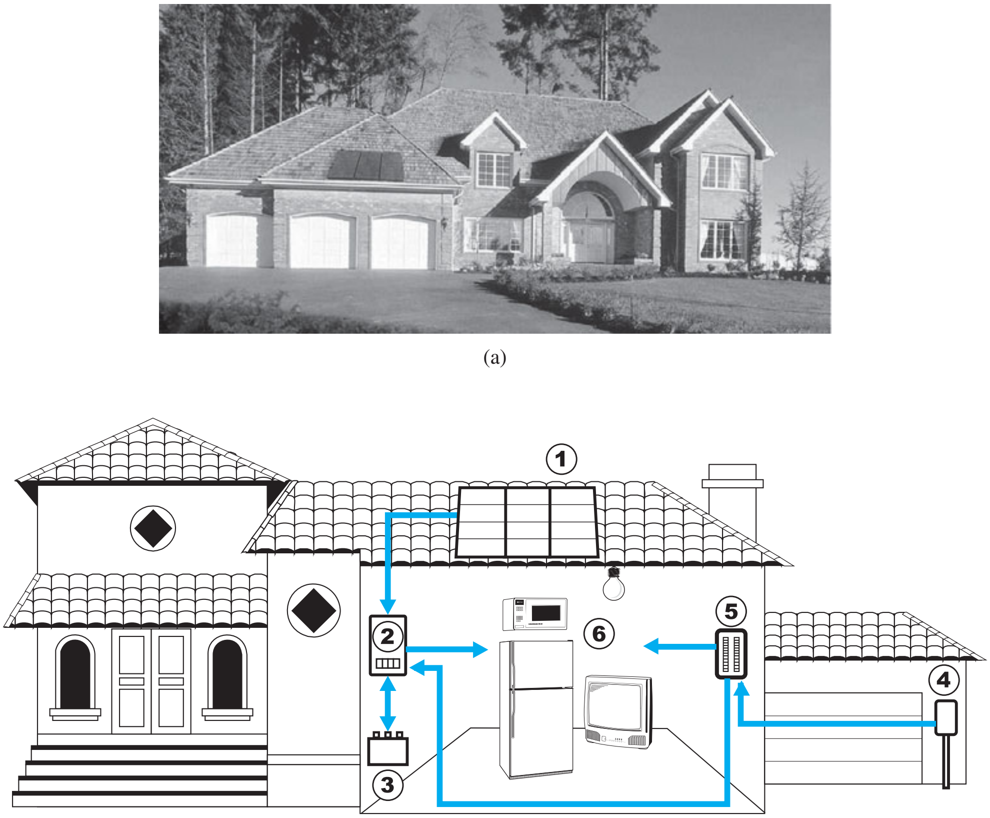


FIG. 16.17

Edmund Scientific multi-volt output solar panel.

(Photo by Dan Trudden/Pearson.)

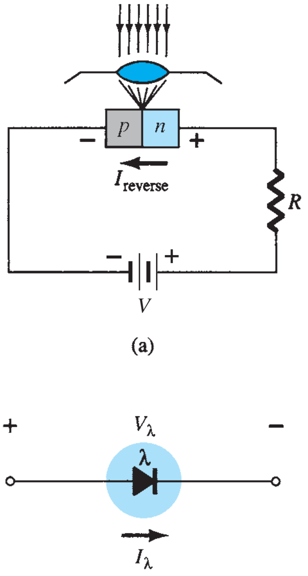


(b)

FIG. 16.18

Solar System: (a) panels on roof of garage; (b) system operation.
(Courtesy of SolarDirect.com)

Thin-film solar cell panels have led to widespread use of solar panels in the home. The solar panels appearing on the roof of the home of Fig. 16.18a are sufficient in power to run an energy-efficient refrigerator for 24 hours a day, while simultaneously running a color TV for 7 hours, a microwave for 15 minutes, a 60-W bulb for 10 hours, and an electric clock for 10 hours. The basic system operates as shown in Fig. 16.18b. The solar panels (1) convert sunlight into dc electric power. An inverter (2) converts the dc power into the standard ac power for use in the home (6). The batteries (3) can store energy from the sun for use if there is insufficient sunlight or a power failure. At night or on dark days when the demand exceeds the solar panel and battery supply, the local utility company (4) can provide power to the appliances (6) through a special hookup in the electrical panel (5). Although there is an initial expense to setting up the system, it is vitally important to realize that the source of energy is free—no monthly bill for sunlight to contend with—and will provide a significant amount of energy for a very long period of time.



(b)

FIG. 16.19

Photodiode: (a) basic biasing arrangement and construction; (b) symbol.

16.5 PHOTODIODES

The photodiode is a semiconductor *p*–*n* junction device whose region of operation is limited to the reverse-bias region. The basic biasing arrangement, construction, and symbol for the device appear in Fig. 16.19.

Recall from Chapter 1 that the reverse saturation current is normally limited to a few microamperes. It is due solely to the thermally generated minority carriers in the *n*- and *p*-type materials. The application of light to the junction will result in a transfer of energy from the incident traveling light waves (in the form of photons) to the atomic structure, resulting in an increased number of minority carriers and an increased level of reverse current. This is clearly shown in Fig. 16.20 for different intensity levels. The *dark* current is that current that will exist with no applied illumination. Note that the current will only return to zero with a positive applied bias equal to V_T. In addition, Fig. 16.19a demonstrates the use of a lens to concentrate the light on the junction region. Commercially available photodiodes appear in Fig. 16.21.

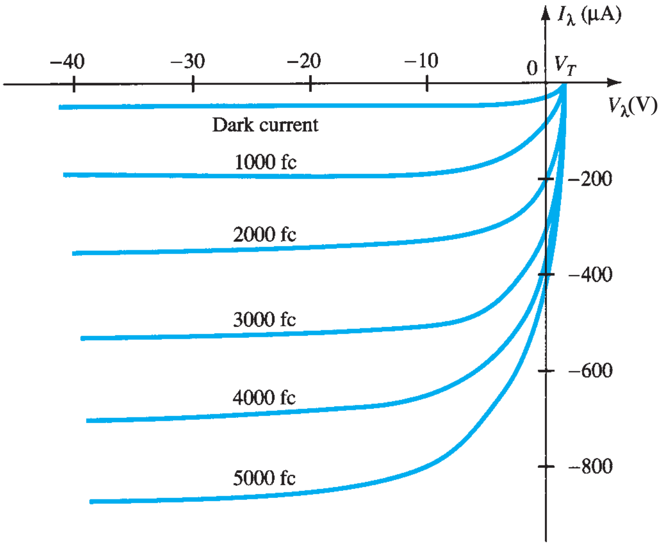


FIG. 16.20
Photodiode characteristics.

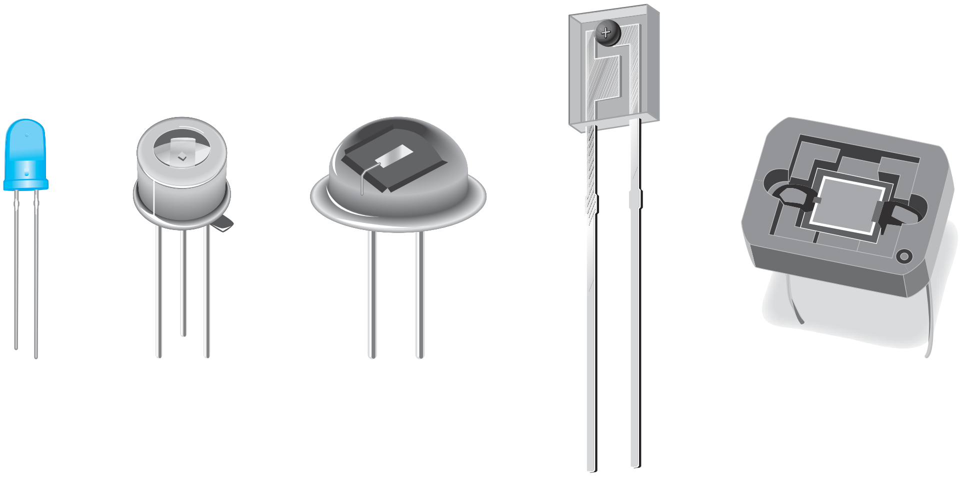


FIG. 16.21
Photodiodes

The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse current and the luminous flux are almost linearly related. In other words, an increase in light intensity will result in a similar increase in reverse current. A plot of the two to show this linear relationship appears in Fig. 16.22 for a fixed voltage V_λ of 20 V. On a relative basis, we can assume that the reverse current is essentially zero in the absence of incident light. Since the rise and fall times (change-of-state parameters) are very small for this device (in the nanosecond range), the device can be used for high-speed counting or switching applications. Germanium encompasses a wider spectrum of wavelengths than Si, making it suitable for incident light in the infrared region as provided by lasers and IR (infrared) light sources, to be described shortly. Germanium has a higher dark current than Si, but it also has a higher level of reverse current. The level of current generated by the incident light on a photodiode is not such that it could be used as a direct control, but it can be amplified for this purpose.

Applications

In Fig. 16.23, the photodiode is employed in an alarm system. The reverse current I_λ will continue to flow as long as the light beam is not broken. If the beam is interrupted, I_λ drops

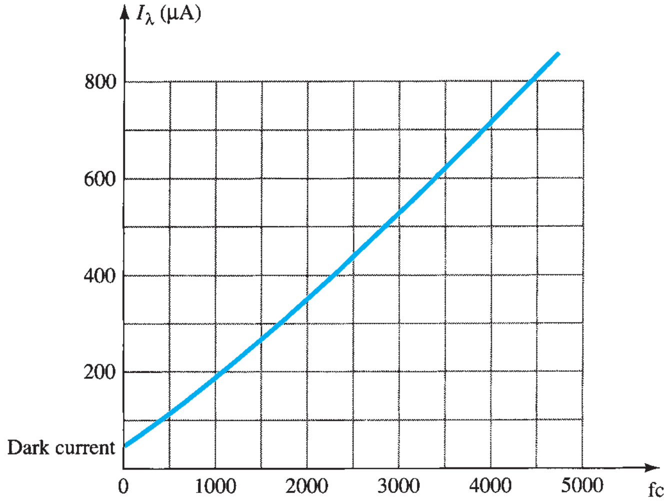


FIG. 16.22
I_λ (μA) versus f_C (at $V_\lambda = 20$ V) for the photodiode of Fig. 16.20.

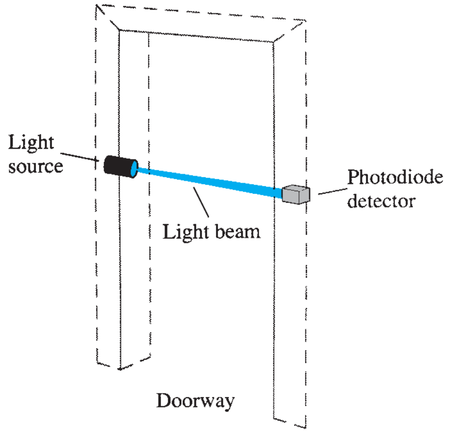

Light source
Light beam
Photodiode detector
Doorway

FIG. 16.23
Using a photodiode in an alarm system.

to the dark current level and sounds the alarm. In Fig. 16.24, a photodiode is used to count items on a conveyor belt. As each item passes, the light beam is broken, I_λ drops to the dark current level, and the counter is increased by one.

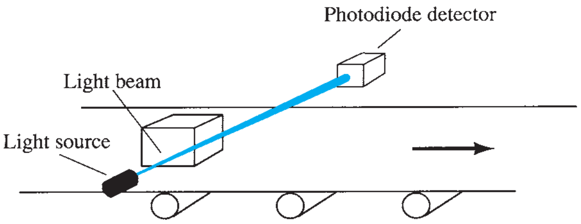
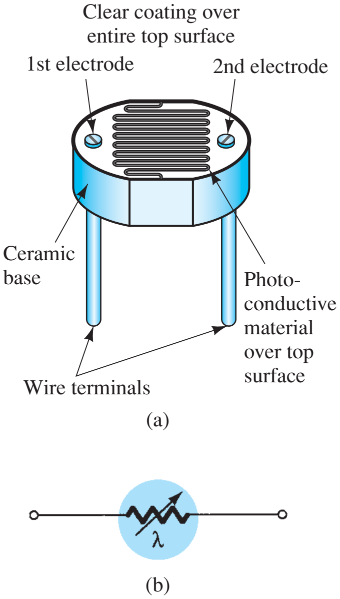

Photodiode detector
Light beam
Light source

FIG. 16.24
Using a photodiode in a counter operation.


Clear coating over entire top surface
1st electrode
2nd electrode
Ceramic base
Photo-conductive material over top surface
Wire terminals
λ
(a)

(b)

FIG. 16.25
Photoconductive cell:
(a) construction; (b) symbol.

16.6 PHOTOCONDUCTIVE CELLS

The photoconductive cell is a two-terminal semiconductor device whose terminal resistance varies (linearly) with the intensity of the incident light. For obvious reasons, it is frequently called a *photoresistive device.* The typical construction of a photoconductive cell is provided in Fig. 16.25 with the most common graphical symbol.

The photoconductive materials most frequently used include cadmium sulfide (CdS) and cadmium selenide (CdSe). The peak spectral response occurs at approximately 5100 Å for CdS and at 6150 Å for CdSe. The response time of CdS units is about 100 ms and of CdSe cells is 10 ms. The photoconductive cell does not have a junction like the photodiode. A thin layer of the material connected between terminals is simply exposed to the incident light energy.

As the illumination on the device increases in intensity, the energy state of a larger number of electrons in the structure will also increase because of the increased availability of the photon packages of energy. The result is an increasing number of relatively "free" electrons in the structure and a decrease in the terminal resistance. The sensitivity curve for a typical photoconductive device appears in Fig. 16.26. Note the linearity (when plotted using a log–log scale) of the resulting curve and the large change in resistance (100 kΩ → 100 Ω) for the indicated change in illumination.

To see the wealth of material available on each device from manufacturers, consider the CdS (cadmium sulfide) photoconductive cell described in Fig. 16.27. Note again the concern with temperature and response time.

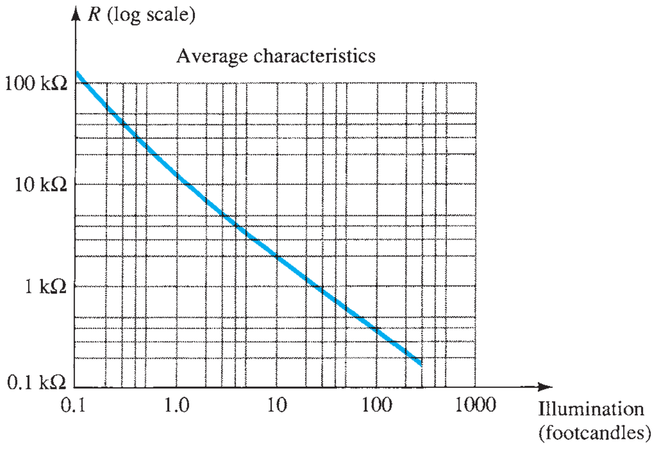
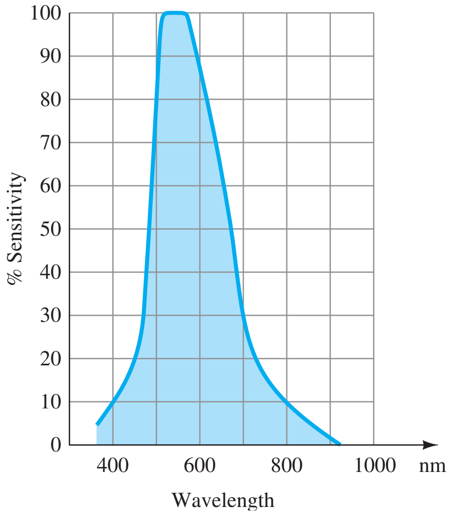


FIG. 16.26
Photoconductive cell-terminal characteristics.



Variation of Conductance with Temperature and Light

Footcandles	*0.01*	*0.1*	*1.0*	*10*	*100*
Temperature			*% Conductance*		
−25°C	103	104	104	102	106
0	98	102	102	100	103
25°C	100	100	100	100	100
50°C	98	102	103	104	99
75°C	90	106	108	109	104

Response Time versus Light

Footcandles	*0.01*	*0.1*	*1.0*	*10*	*100*
Rise (seconds)	0.5	0.095	0.022	0.005	0.002
Decay (seconds)	0.125	0.021	0.005	0.002	0.001

FIG. 16.27
Characteristics of a Clairex CdS photoconductive cell.

Application

One rather simple but interesting application of the device appears in Fig. 16.28. The purpose of the system is to maintain V_o at a fixed level even though V_i may fluctuate from its rated value. As indicated in the figure, the photoconductive cell, bulb, and resistor all form part of this voltage-regulator system. If V_i should drop in magnitude for any of a number of reasons, the brightness of the bulb would also decrease. The decrease in illumination

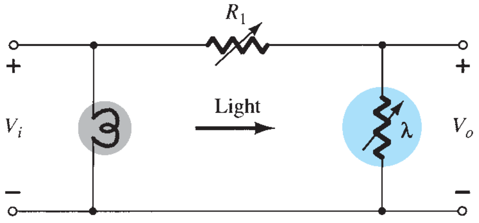


FIG. 16.28
Voltage regulator employing a photoconductive cell.

would result in an increase in the resistance (R_λ) of the photoconductive cell to maintain V_o at its rated level as determined by the voltage-divider rule, that is,

$$\boxed{V_o = \frac{R_\lambda V_i}{R_\lambda + R_1}} \tag{16.10}$$

16.7 IR EMITTERS

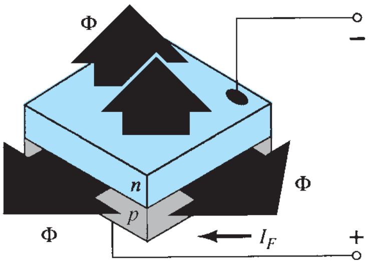


FIG. 16.29
General structure of a semiconductor IR-emitting diode.

Infrared-emitting diodes are solid-state gallium arsenide devices that emit a beam of radiant flux when forward-biased. The basic construction of the device is shown in Fig. 16.29. When the junction is forward-biased, electrons from the *n*-region recombine with excess holes of the *p*-material in a specially designed recombination region sandwiched between the *p*- and *n*-type materials. During this recombination process, energy is radiated away from the device in the form of photons. The generated photons are either reabsorbed in the structure or leave the surface of the device as radiant energy, as shown in Fig. 16.29.

The radiant flux in milliwatts versus the dc forward current for a typical device appears in Fig. 16.30. Note the almost linear relationship between the two. An interesting pattern for such devices is provided in Fig. 16.31. Note the very narrow pattern for devices with an internal collimating system. One such device appears in Fig. 16.32, with its internal construction and graphical symbol. Areas of application for such devices include card and paper-tape readers, shaft encoders, data-transmission systems, and intrusion alarms.

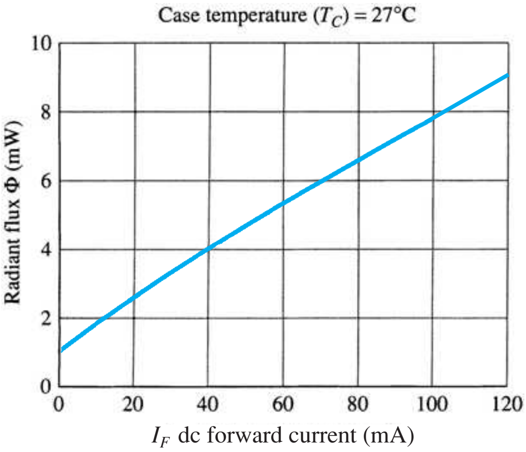


FIG. 16.30
Typical radiant flux versus dc forward current for an IR-emitting diode.

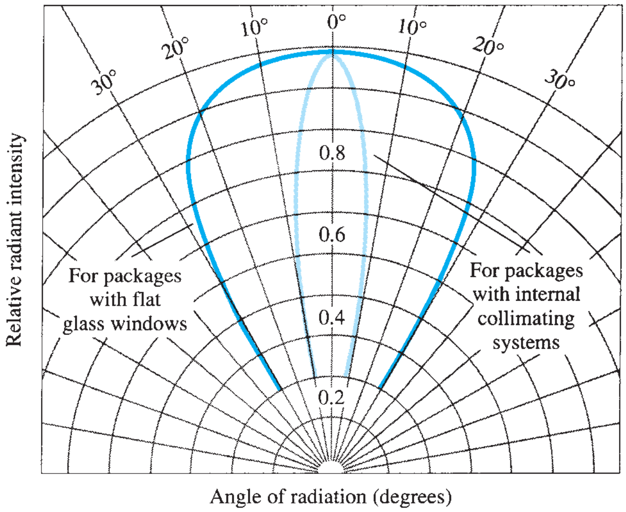


FIG. 16.31
Typical radiant intensity patterns of an IR-emitting diode.

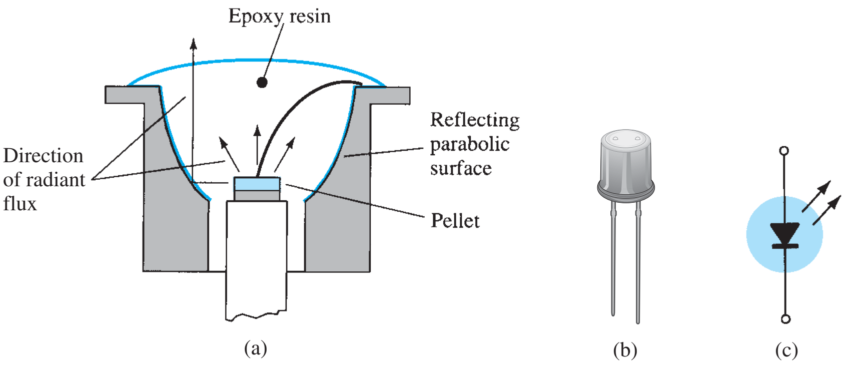


FIG. 16.32
IR-emitting diode: (a) construction; (b) photo; (c) symbol.

16.8 LIQUID-CRYSTAL DISPLAYS

The liquid-crystal display (LCD) has the distinct advantage of having a lower power requirement than the LED, typically on the order of microwatts for the display, compared to the order of milliwatts for LEDs. It does, however, require an external or internal light source, and is limited to a temperature range of about 0°C to 60°C. Lifetime is an area of concern because LCDs can chemically degrade. The types of unit of major interest are field-effect and dynamic-scattering units. Each will be covered in some detail in this section.

A liquid crystal is a material (normally organic for LCDs) that flows like a liquid but whose molecular structure has some properties normally associated with solids. For light-scattering units, the greatest interest is in *nematic liquid crystal,* which has the crystal structure shown in Fig. 16.33. The individual molecules have a rodlike appearance as shown in the figure. The indium oxide conducting surface is transparent, and under the condition shown in the figure, incident light will simply pass through and the liquid-crystal structure will appear clear. If a voltage (for commercial units the threshold level is usually between 6 V and 20 V) is applied across the conducting surfaces, as shown in Fig. 16.34, the molecular arrangement is disturbed, with the result that regions are established with different indices of refraction. The incident light is therefore reflected in different directions at the interface between regions of different indices of refraction (referred to as *dynamic scattering*—first studied by RCA in 1968), with the result that the scattered light has a frosted-glass appearance. Note in Fig. 16.34, however, that the frosted look occurs only where the conducting surfaces are opposite each other; the remaining areas remain translucent.

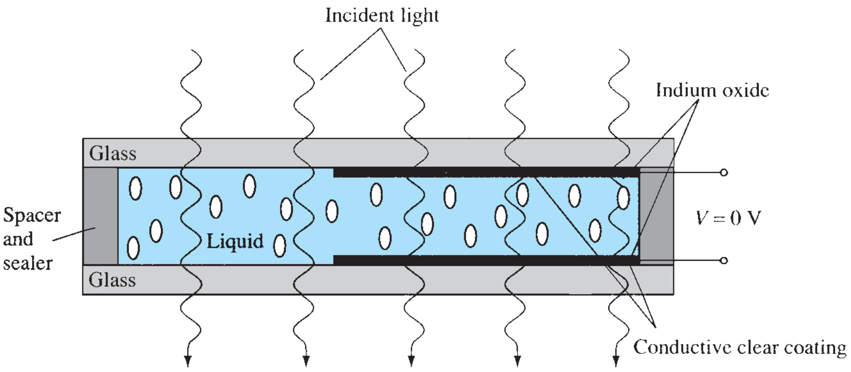


FIG. 16.33
Nematic liquid crystal with no applied bias.

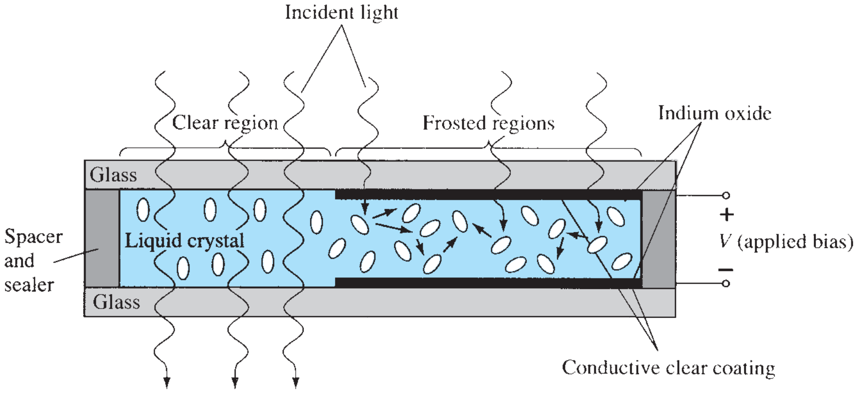


FIG. 16.34
Nematic liquid crystal with applied bias.

A numeral on an LCD display may have the segmented appearance shown in Fig. 16.35. The black area is actually a clear conducting surface connected to the terminals below for external control. Two similar masks are placed on opposite sides of a sealed, thick layer of liquid-crystal material. If the number 2 were required, the terminals 8, 7, 3, 4, and 5 would

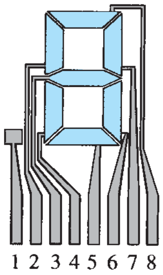


FIG. 16.35
LCD eight-segment digit display.

be energized, and only those regions would be frosted, whereas the other areas would remain clear.

As indicated earlier, the LCD does not generate its own light, but depends on an external or internal source. Under dark conditions, it would be necessary for the unit to have its own internal light source either behind or to the side of the LCD. During the day, or in lighted areas, a reflector can be put behind the LCD to reflect the light back through the display for maximum intensity. For optimum operation, watch manufacturers use a combination of the transmissive (own light source) and reflective modes called *transflective* operation.

The *field-effect* or *twisted nematic* LCD has the same segmented appearance and thin layer of encapsulated liquid crystal, but its mode of operation is very different. Similar to the dynamic-scattering LCD, the field-effect LCD can be operated in the reflective or the transmissive mode with an internal source. The transmissive display appears in Fig. 16.36. The internal light source is on the right, and the viewer is on the left. This figure is most noticeably different from Fig. 16.33 in that there is an addition of a *light polarizer*. Only the vertical component of the entering light on the right can pass through the vertical-light polarizer on the right. In the field-effect LCD, either the clear conducting surface to the right is chemically etched or an organic film is applied to orient the molecules in the liquid crystal in the vertical plane, parallel to the cell wall. Note the rods to the far right in the liquid crystal. The opposite conducting surface is also treated to ensure that the molecules are 90° out of phase in the direction shown (horizontal) but still parallel to the cell wall. In between the two walls of the liquid crystal there is a general drift from one polarization to the other, as shown in the figure. The left-hand light polarizer is also such that it permits the passage of only the vertically polarized incident light. If there is no applied voltage to the conducting surfaces, the vertically polarized light enters the liquid-crystal region and follows the 90° bending of the molecular structure. Its horizontal polarization at the left-hand vertical light polarizer does not allow it to pass through, and the viewer sees a uniformly dark pattern across the entire display. When a threshold voltage is applied (for commercial units from 2 V to 8 V), the rodlike molecules align themselves with the field (perpendicular to the wall) and the light passes directly through without the 90° shift. The vertically incident light can then pass directly through the second vertically polarized screen, and a light area is seen by the viewer. Through proper excitation of the segments of each digit, the pattern will appear as shown in Fig. 16.37. The reflective-type field-effect LCD is shown in Fig. 16.38. In this case, the horizontally polarized light at the far left encounters a horizontally polarized filter and passes through to the reflector, where it is reflected back into the liquid crystal, bent back to the other vertical polarization, and returned to the observer. If there is no applied voltage, there is a uniformly lit display. The application of a voltage results in a vertically incident light encountering a horizontally polarized filter at the left, through which it will not be able to pass, and so it will be reflected. A dark area results on the crystal, and the pattern shown in Fig. 16.39 appears.

Field-effect LCDs are normally used when a source of energy is a prime factor (e.g., in watches, portable instrumentation, etc.) since they absorb considerably less power than the

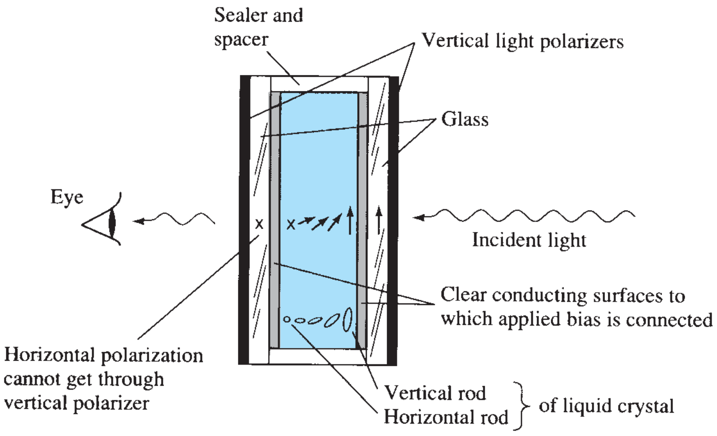

Sealer and spacer
Vertical light polarizers
Glass
Eye
x
x
Incident light
Clear conducting surfaces to which applied bias is connected
Horizontal polarization cannot get through vertical polarizer
Vertical rod
Horizontal rod
of liquid crystal

FIG. 16.36
Transmissive field-effect LCD with no applied bias.

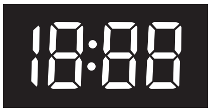


FIG. 16.37
Reflective-type LCD.

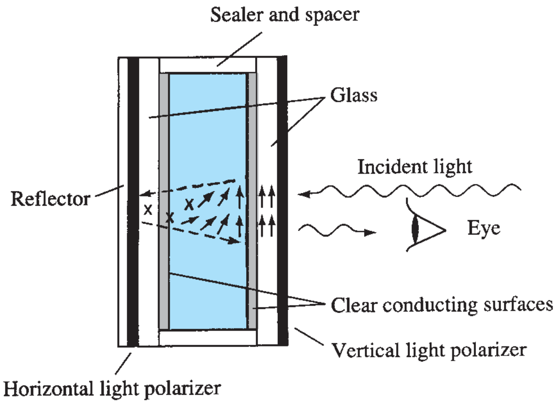


FIG. 16.38

Reflective field-effect LCD with no applied bias.

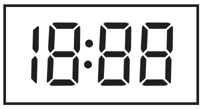


FIG. 16.39

Transmissive-type LCD.

light-scattering types—the microwatt range compared to the low-milliwatt range. The cost is typically higher for field-effect units, and their height is limited to about 2 in., whereas light-scattering units are available up to 8 in. in height.

A further consideration in displays is turn-on and turn-off time. LCDs are characteristically much slower than LEDs. LCDs typically have response times in the range 100 ms to 300 ms, whereas LEDs are available with response times below 100 ns. However, there are numerous applications, such as in a watch, where the difference between 100 ns and 100 ms ($\frac{1}{10}$ of a second) is of little consequence. For such applications, the lower power demand of LCDs is a very attractive characteristic. The lifetime of LCD units is steadily increasing beyond the 10,000+-hour limit. Since the color generated by LCD units is dependent on the source of illumination, there is a greater range of color choice.

16.9 THERMISTORS

The thermistor is, as the name implies, a temperature-sensitive resistor; that is, its terminal resistance is related to its body temperature. It is not a junction device and is constructed of germanium, silicon, or a mixture of oxides of cobalt, nickel, strontium, or manganese. The compound employed determines whether the device has a positive or a negative temperature coefficient.

The characteristics of a typical thermistor with a negative temperature coefficient are provided in Fig. 16.40, which also shows the commonly used symbol for the device. Note in

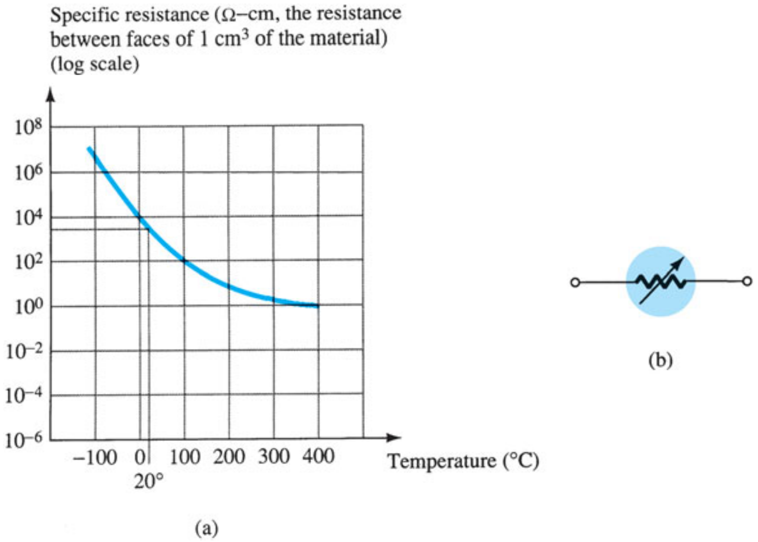


FIG. 16.40

Thermistor: (a) typical set of characteristics; (b) symbol.

particular that at room temperature (20°C) the resistance of the thermistor is approximately 5000 Ω, whereas at 100°C (212°F) the resistance decreases to 100 Ω. A temperature span of 80°C therefore results in a 50:1 change in resistance. The change in resistance is typically 3% to 5% per degree change in temperature. There are fundamentally two ways to change the temperature of the device: internally and externally. A simple change in current through the device will result in an internal change in temperature. A small applied voltage will result in a current too small to raise the body temperature above that of the surroundings. In this region, as shown in Fig. 16.41, the thermistor will act like a resistor and have a positive temperature coefficient. However, as the current increases, the temperature will rise to the point where the negative temperature coefficient will appear as shown in Fig. 16.41. The fact that the rate of internal flow can have such an effect on the resistance of the device introduces a wide vista of applications in control, measuring techniques, and so on. An external change requires changing the temperature of the surrounding medium or immersing the device in a hot or a cold solution.

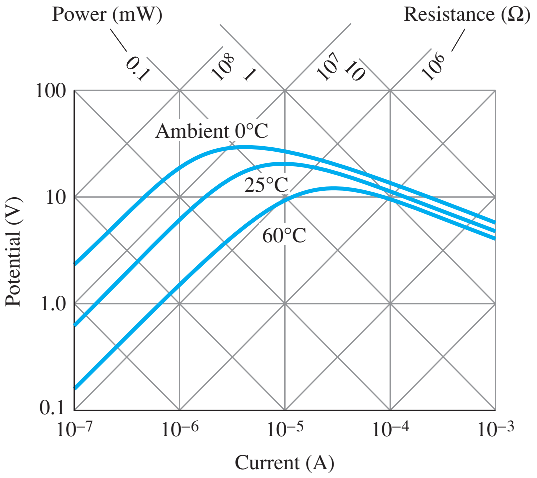
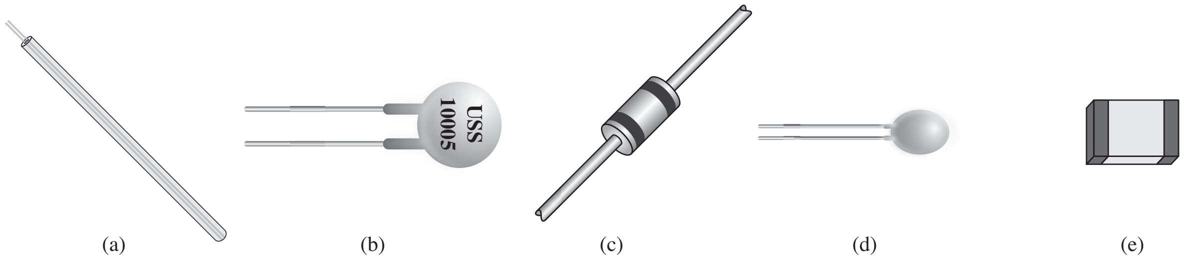


FIG. 16.41

Steady-state voltage–current characteristics of a thermistor.

A few of the most popular packaging techniques for U.S. sensor thermistor elements are provided in Fig. 16.42. The probe of Fig. 16.42a has a high stability factor and is rugged and very precise for applications ranging from laboratory applications to severe environmental conditions. The power thermistors of Fig. 16.42b have the unique ability to limit any in-rush current to an acceptable level until the capacitors are charged. The resistance of the device will then drop to a level where the drop across the device is negligible. They can handle currents up to 20 A with a resistance as low as 1 Ω. The glass encapsulated thermistor of Fig. 16.42c is small in size, is very rugged and very stable, and can be used at temperatures up to 300°C. The bead type thermistor of Fig. 16.42d is also very small in size, very accurate, and stable and has a fast thermal response. The chip thermistor of Fig. 16.42e is designed for use on hybrid substrates, integrated circuits, or printed circuit boards.



(a) Probe

(b) High power

(c) Glass

(d) Bead

(e) Surface mount

FIG. 16.42

Various types of packaging for U.S. sensor thermistors.

Application

A simple temperature-indicating circuit appears in Fig. 16.43. Any increase in the temperature of the surrounding medium will result in a decrease in the resistance of the thermistor and an increase in the current I_T. An increase in I_T will produce an increased movement deflection, which when properly calibrated will accurately indicate the higher temperature. The variable resistance was added for calibration purposes.

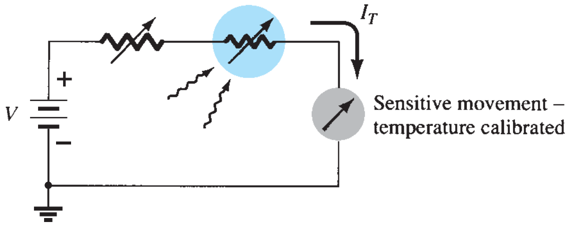


FIG. 16.43
Temperature-indicating circuit.

16.10 TUNNEL DIODES

The tunnel diode was first introduced by Leo Esaki in 1958. Its characteristics, shown in Fig. 16.44, are different from any diode discussed thus far in that it has a negative-resistance region. In this region, an increase in terminal voltage results in a reduction in diode current.

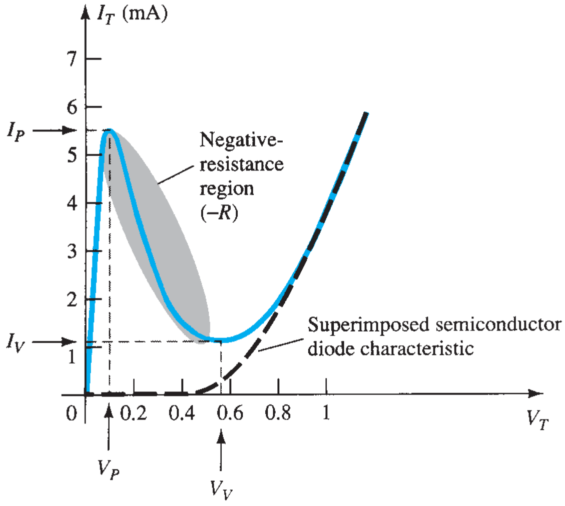


FIG. 16.44
Tunnel diode characteristics.

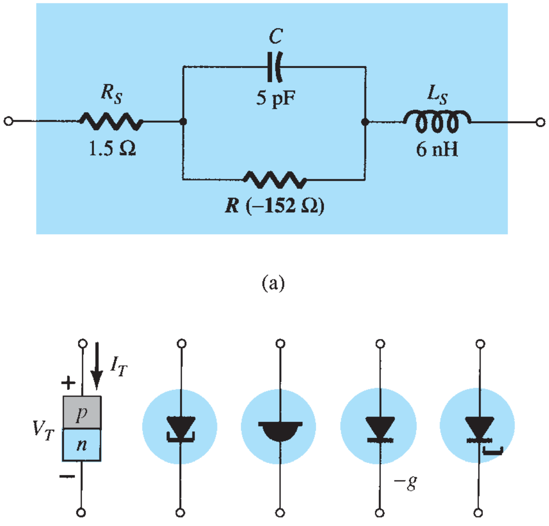
The tunnel diode is fabricated by doping the semiconductor materials that will form the *p–n* junction at a level 100 to several thousand times that of a typical semiconductor diode. This results in a greatly reduced depletion region, of the order of magnitude of 10^{-6} cm, or typically about $\frac{1}{100}$ the width of this region for a typical semiconductor diode. It is this thin depletion region, through which many carriers can "tunnel" rather than attempt to surmount, at low forward-bias potentials that accounts for the peak in the curve of Fig. 16.44. For comparison purposes, a typical semiconductor diode characteristic is superimposed on the tunnel-diode characteristic of Fig. 16.44.

This reduced depletion region results in carriers "punching through" at velocities that far exceed those available with conventional diodes. The tunnel diode can therefore be used in high-speed applications such as in computers, where switching times in the order of nanoseconds or picoseconds are desirable.

Recall from Section 1.15 that an increase in the doping level reduces the Zener potential. Note the effect of a very high doping level on this region in Fig. 16.44. The semiconductor materials most frequently used in the manufacture of tunnel diodes are germanium and gallium arsenide. The ratio I_P/I_V is very important for computer applications. For germanium, it is typically 10:1, and for gallium arsenide, it is closer to 20:1.

The peak current I_P of a tunnel diode can vary from a few microamperes to several hundred amperes. The peak voltage, however, is limited to about 600 mV. For this reason, a simple VOM with an internal dc battery potential of 1.5 V can severely damage a tunnel diode if applied improperly.

The tunnel-diode equivalent circuit in the negative-resistance region is provided in Fig. 16.45, with the symbols most frequently employed for tunnel diodes. The values for the parameters are typical for today's commercial units. The inductor L_S is due mainly to the terminal leads. The resistor R_S is due to the leads, the ohmic contact at the lead–semiconductor junction, and the semiconductor materials themselves. The capacitance C is the junction diffusion capacitance, and the R is the negative resistance of the region. The negative resistance finds application in oscillators to be described later.



(a)

(b)

FIG. 16.45
Tunnel diode: (a) equivalent circuit; (b) symbols.

The packaging for an Advanced Semiconductor planar tunnel diode appears in Fig. 16.46 while the maximum ratings and characteristics for the device are provided in Fig. 16.47. Note that there is a range of peak values for each device, so the design process has to be

Electrical Characteristics $T_C = 25°C$

Device	Symbol	Test Conditions	Min	Typ	Max	Units
ASTD1020	I_P		100		200	μA
ASTD2030			200		300	
ASTD3040			300		400	
ASTD1020	V_P				135	mV
ASTD2030					130	mV
ASTD3040					125	mV
ASTD1020	R_V	$f = 10$ GHz, $R_L = 10$ kΩ		−180		Ω
ASTD2030		$P_m = -20$ dBm		−130		Ω
ASTD3040				−80		Ω
All	R_S	$I = 10$ mA, $f = 100$ MHz		7		Ω

FIG. 16.47
Electrical characteristics for the Advanced Semiconductor planar tunnel diode of Fig. 16.46.

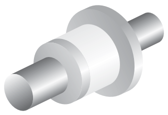


FIG. 16.46
Advanced Semiconductor planar tunnel diode.

satisfactory for the full range of values. One can never tell which peak value will result for a particular device. This range of peak values is common for most tunnel diodes, so the designers are well aware of this concern. Interestingly enough, the valley voltage is fairly constant at about 0.13 V, which is significantly less than the typical turn-on voltage for a silicon diode. For this series of diodes, the negative resistance has a range of -80 to $-180\ \Omega$, which is a fairly large range for this important parameter. A number of tunnel diodes simply state a constant value such as $-250\ \Omega$ for a particular series.

Although the use of tunnel diodes in present-day high-frequency systems has been dramatically stalled because of the availability of manufacturing techniques for alternative devices, its simplicity, linearity, low power drain, and reliability ensure its continued life and application.

In Fig. 16.48, the chosen supply voltage and load resistance define a load line that intersects the tunnel diode characteristics at three points. Keep in mind that the load line is determined solely by the network and the characteristics of the device. The intersections at *a* and *b* are referred to as *stable* operating points, due to the positive-resistance characteristic. That is, at either of these operating points, a slight disturbance in the network will not set the network into oscillations or result in a significant change in the location of the *Q*-point. For instance, if the defined operating point is at *b,* a slight increase in supply voltage *E* will move the operating point up the curve since the voltage across the diode will increase. Once the disturbance has passed, the voltage across the diode and the associated diode current will return to the levels defined by the *Q*-point at *b*. The operating point defined by *c* is an *unstable* one because a slight change in the voltage across or current through the diode will result in the *Q*-point moving to either *a* or *b*. For instance, the slightest increase in *E* will cause the voltage across the tunnel diode to increase above its level at *c*. In this region, however, an increase in V_T will cause a decrease in I_T and a further increase in V_T. This increased level in V_T will result in a continuing decrease in I_T, and so on. The result is an increase in V_T and a change in I_T until the stable operating point at *b* is established. A slight drop in supply voltage would result in a transition to stability at point *a*. In other words, point *c* can be defined as the operating point using the load-line technique, but once the system is energized, it will eventually stabilize at location *a* or *b*.

The availability of a negative-resistance region can be put to good use in the design of oscillators, switching networks, pulse generators, and amplifiers.

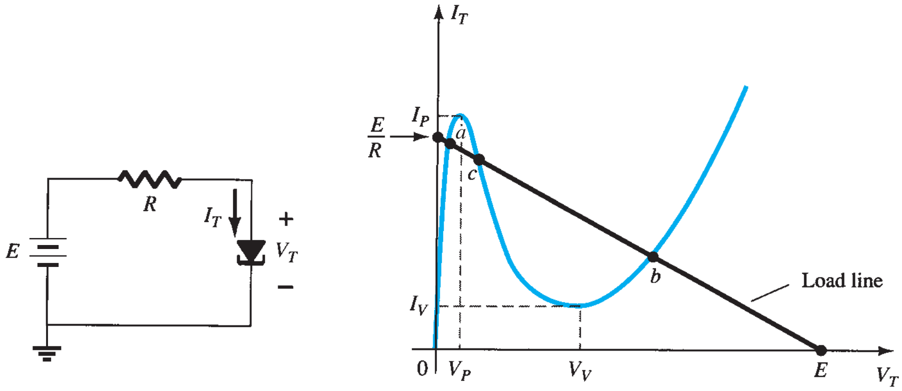


FIG. 16.48

Tunnel diode and resulting load line.

Applications

In Fig. 16.49a, a *negative-resistance oscillator* is shown as constructed using a tunnel diode. The choice of network elements is designed to establish a load line such as shown in Fig. 16.49b. Note that the only intersection with the characteristics is in the unstable negative-resistance region—a stable operating point is not defined. When the power is turned on, the terminal voltage of the supply will build up from 0 V to a final value of *E* volts. Initially, the current I_T will increase from 0 mA to I_P, resulting in a storage of energy in the inductor in the form of a magnetic field. However, once I_P is reached, the diode

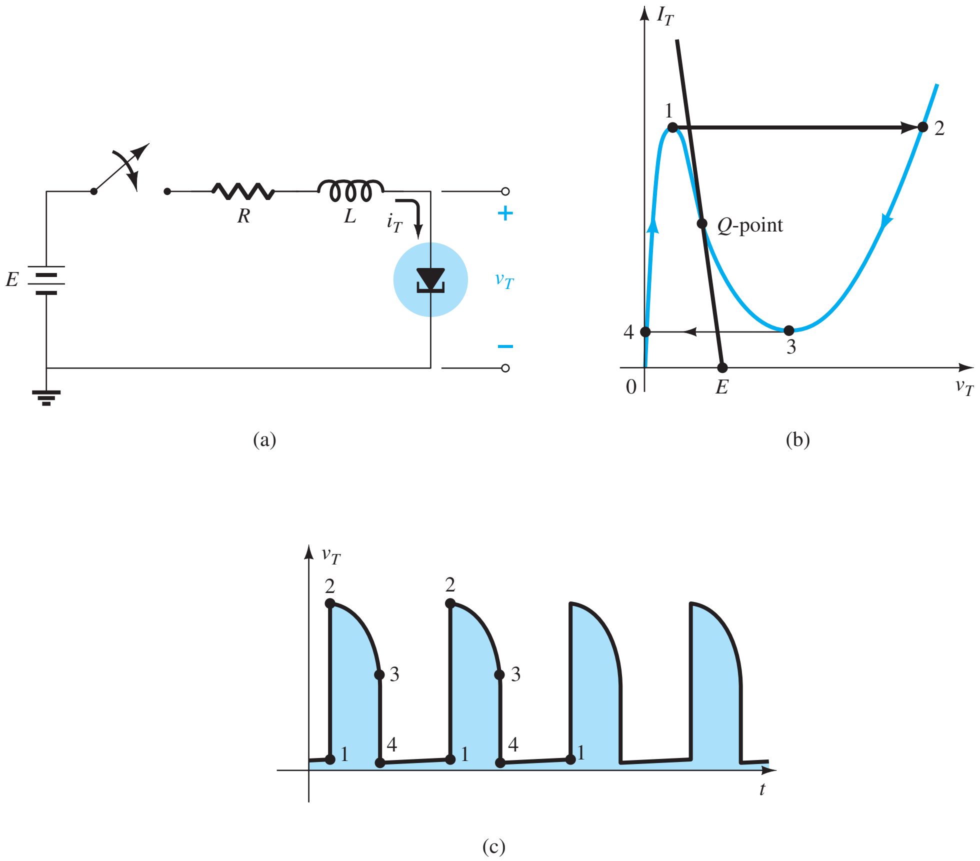


FIG. 16.49

Negative-resistance oscillator.

characteristics suggest that the current I_T must now decrease with increase in voltage across the diode. This contradicts the fact that

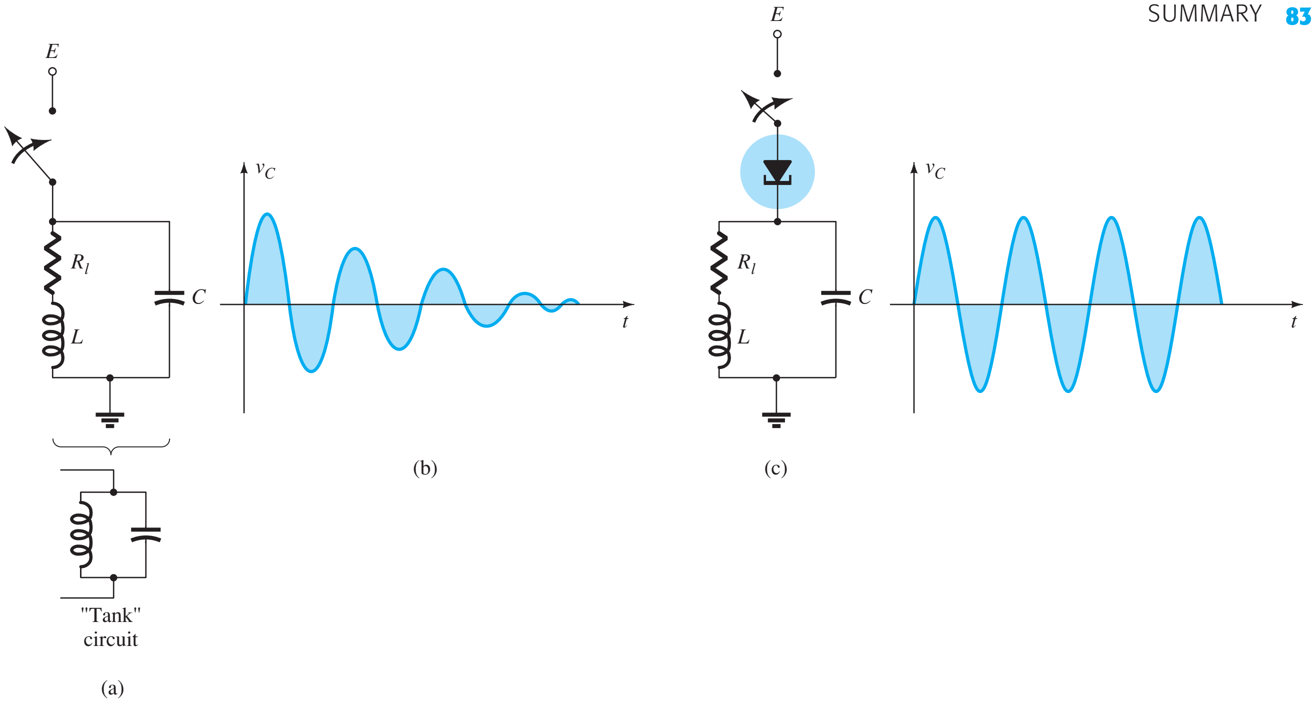
$$E = I_T R + I_T(-R_T)$$

and

$$E = \underbrace{I_T}_{\text{less}}\underbrace{(R - R_T)}_{\text{less}}$$

If both elements of the equation above were to decrease, it would be impossible for the supply voltage to reach its set value. Therefore, for the current I_T to continue rising, the point of operation must shift from point 1 to point 2. However, at point 2, the voltage V_T has jumped to a value greater than the applied voltage (point 2 is to the right of any point on the network load line). To satisfy Kirchhoff's voltage law, the polarity of the transient voltage across the coil must reverse and the current begin to decrease as shown from 2 to 3 on the characteristics. When V_T drops to V_V, the characteristics suggest that the current I_T will begin to increase again. This is unacceptable since V_T is still more than the applied voltage and the coil is discharging through the series circuit. The point of operation must shift to point 4 to permit a continuation of the decrease in I_T. However, once at point 4, the potential levels are such that the tunnel current can again increase from 0 mA to I_P as shown on the characteristics. The process will repeat itself again and again, never settling in on the operating point defined for the unstable region. The resulting voltage across the tunnel diode appears in Fig. 16.49c and will continue as long as the dc supply is energized. The result is an oscillatory output established by a fixed supply and a device with a negative-resistance characteristic. The waveform of Fig. 16.49c has extensive application in timing and computer logic circuitry.

A tunnel diode can also be used to generate a sinusoidal voltage using simply a dc supply and a few passive elements. In Fig. 16.50a, the closing of the switch will result in a sinusoidal voltage that will decease in amplitude with time as shown in Fig. 16.50b. Depending on the elements employed, the time period can be from one almost instantaneous to one measurable in minutes using typical parameter values. This *damping* of the oscillatory output with time is due to the dissipative characteristics of the resistive elements. By placing a tunnel diode in series with the tank circuit as shown in Fig. 16.50c, we can have the negative resistance of the



(a)

(b)

(c)

FIG. 16.50

Sinusoidal oscillator.

tunnel diode offset the resistive characteristics of the tank circuit, resulting in the *undamped* response appearing in the same figure. The design must continue to result in a load line that will intersect the characteristics only in the negative-resistance region. In another light, the sinusoidal generator of Fig. 16.50 is simply an extension of the pulse oscillator of Fig. 16.49, with the addition of the capacitor to permit an exchange of energy between the inductor and the capacitor during the various phases of the cycle depicted in Fig. 16.49b.

16.11 SUMMARY

Important Conclusions and Concepts

1. The Schottky barrier (hot-carrier) diode has a **lower threshold voltage** (about 0.2 V), a **larger reverse saturation current**, and a **smaller PIV** than the conventional *p–n* junction variety. It can also be used at higher frequencies because of the reduced reverse recovery time.
2. The varactor (varicap) diode has a **transition capacitance** sensitive to the applied reverse-bias potential that is a maximum at 0 V and that **decreases exponentially** with increasing reverse-bias potentials.
3. The **current capability** of power diodes can be increased by placing two or more in **parallel**, and the **PIV rating** can be increased by stacking the diodes in series.
4. The chassis itself can be used as a **heat sink** for power diodes.
5. **Tunnel diodes** are unique in that they have a **negative-resistance region** at voltage levels less than the typical *p–n* junction threshold voltage. This characteristic is particularly useful in oscillators to establish an oscillating waveform from a switched dc power supply. Due to its reduced depletion region, it is also considered a **high-frequency device** for applications where switching times in nanoseconds or picoseconds are required.
6. The region of operation for **photodiodes** is the **reverse-bias region**. The resulting diode current increases almost **linearly** with an increase in incident light. The **wavelength** of the incident light determines which material will result in the best response; selenium has a good match with the naked eye, and silicon is better for incident light of higher wavelengths.
7. A photoconductive cell is one whose terminal resistance **decreases exponentially** with an **increase in incident light**.
8. An **infrared-emitting diode** emits a beam of radiant flux when **forward-biased**. The strength of the emitted flux pattern is almost **linearly related** to the dc forward current through the device.

9. **LCDs** have a much **lower power absorption level** than LEDs, but their lifetime is much **shorter**, and they require an **internal or external light source**.
10. The **solar cell** is capable of converting light energy in the form of photons into electrical energy in the form of a difference in potential or **voltage**. The terminal voltage will **initially increase quite rapidly** with the application of light, but then the increase will occur at an increasingly **slower rate**. In other words, the terminal voltage will reach a **saturation level** at some point where any further increase in incident light will have little effect on the magnitude of the terminal voltage.
11. A **thermistor** can have regions of **positive or negative temperature coefficients** determined by the construction material or the temperature of the material. The change in temperature can be due to **internal effects** such as caused by the current through the thermistor or due to **external effects** of heating or cooling.

Equations

Varactor diode:

$$C_T(V_R) = \frac{C(0)}{(1 + |V_R/V_T|)^n}$$

where $n = 1/2$ alloy junction
$n = 1/3$ diffused junction

$$TC_C = \frac{\Delta C}{C_0(T_1 - T_0)} \times 100\% \qquad \%/^\circ\text{C}$$

Photodiodes:

$$\lambda = \frac{v}{f} = \frac{3 \times 10^8\ \text{m/s}}{f}$$

$$1\text{Å} = 10^{-10}\text{m} \qquad \text{and} \qquad 1\ \text{lm} = 1.496 \times 10^{-10}\ \text{W}$$

$$1\ \text{fc} = 1\ \text{lm/ft}^2 = 1.609 \times 10^{-9}\ \text{W/m}^2$$

Solar cells:

$$\eta = \frac{P_{o(\text{electrical})}}{P_{i(\text{light energy})}} \times 100\%$$

$$= \frac{P_{\max(\text{device})}}{(\text{area in cm}^2)(100\ \text{mW/cm}^2)} \times 100\%$$

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

16.2 Schottky Barrier (Hot-Carrier) Diodes

1. **a.** Describe in your own words how the construction of the hot-carrier diode is significantly different from the conventional semiconductor diode.
   b. In addition, describe its mode of operation.
2. **a.** Consult Fig. 16.2. Compare the dynamic resistances of the diodes in the forward-bias regions.
   b. How do the levels of I_s and V_Z compare?
3. Using the data of Fig. 16.5, determine the reverse leakage current at a temperature of 50°C. Assume a linear relationship between the two quantities.
4. (a) Using the electrical characteristics of Fig. 16.5, find the reactance of the capacitor at a frequency of 1 MHz and a reverse voltage of 1 V. (b) Find the forward dc resistance of the diode at 10 mA.
5. **a.** Using the data from Fig. 16.5 plot the forward current versus forward voltage for the Schottky diode.
   b. Determine the piecewise equivalent resistance for the vertical rise section of the characteristics.
   c. What is the resulting vertical break voltage for the diode as compared to the 0.7 V value typically used for a *p–n* junction diode.
6. Using the plot of Fig. 16.6a,
   a. What is the forward voltage at a current of 50 mA (note the log scale) at room temperature (25°C).
   b. What is the forward voltage at the same current as part (a) but a temperature of 125°C?
   c. What can be said about the effect of temperature on the resulting voltage drop across a Schottky diode as the temperature increases?

7. Using the characteristics of Fig. 16.6(c), determine the reactance of the diode capacitor at a frequency of 1 MHz and a reverse bias potential of 1 V. Is it significant?

16.3 Varactor (Varicap) Diodes

8. **a.** Determine the transition capacitance of a diffused junction varicap diode at a reverse potential of 4.2 V if $C(0) = 80$ pF and $V_r = 0.7$ V.
   b. From the information of part (a), determine the constant K in Eq. (16.2).

9. **a.** For a varicap diode having the characteristics of Fig. 16.7, determine the difference in capacitance between reverse-bias potentials of -3 V and -12 V.
   b. Determine the incremental rate of change $(\Delta C/\Delta V_r)$ at $V = -8$ V. How does this value compare with the incremental change determined at -2 V?

***10.** Using Fig. 16.10a, determine the total capacitance at a reverse potential of 1 V and 8 V and find the tuning ratio between these two levels. How does it compare to the tuning ratio for the ratio between reverse bias potentials of 1.25 V and 7 V?

11. At a reverse-bias potential of 4 V, determine the total capacitance for the varactor from Fig. 16.10a and calculate the Q value from $Q = 1/(2\pi f R_S C_t)$ using a frequency of 10 MHz and $R_s = 3\ \Omega$. Compare to the Q value determined from the chart of Fig. 16.10a.

12. Determine T_1 for a varactor diode if $C_0 = 22$ pF, $TC_C = 0.02\%/°\text{C}$, and $\Delta C = 0.11$ pF due to an increase in temperature above $T_0 = 25°\text{C}$.

13. What region of V_R would appear to have the greatest change in capacitance per change in reverse voltage for the diode of Fig. 16.10? Be aware that it is a log-log scale. Then, for this region, determine the ratio of the change in capacitance to the change in voltage.

***14.** Using Fig. 16.10a, compare the Q levels at a reverse bias potential of 1 V and 10 V. What is the ratio between the two? If the resonant frequency is 10 MHz, what is the bandwidth for each bias voltage? Compare the bandwidths obtained and compare their ratio to the ratio of Q levels.

15. Referring to Fig. 16.11, if $V_{DD} = 2$ V for the varactor of Fig. 16.10, find the resonant frequency of the tank circuit if $C_C = 40$ pF and $L_T = 2$ mH.

16.4 Solar Cells

16. A 1-cm by 2-cm solar cell has a conversion efficiency of 9%. Determine the maximum power rating of the device.

***17.** If the power rating of a solar cell is determined on a very rough scale by the product $V_{OC} I_{SC}$, is the greatest rate of increase obtained at lower or higher levels of illumination? Explain your reasoning.

18. **a.** For the solar cell of Fig. 16.13, determine the ratio $\Delta I_{SC}/\Delta fc$ if $fc_1 = 20 fc$.
   b. Using the results of part (a), find the level of I_{SC} resulting from a light intensity of 28 footcandles.

19. **a.** For the solar cell of Fig. 16.14, determine the ratio $\Delta IV_{OC}/\Delta fc$ for the range of 20 fc to 100 fc if $fc_1 = 40 fc$.
   b. Using the results of part (a), determine the expected level of V_{OC} at a light intensity of 60 fc.

20. **a.** Plot the 1-V curve for the same solar cell of Fig. 16.15 but with a light intensity of fc_1.
   b. Plot the resulting power curve from the results of part (a).
   c. What is the maximum power rating? How dews it compare to the maximum power rating for a light intensity fc_2?

21. **a.** What is the energy in joules associated with photons that have a wavelength matching that of the color blue in the visible spectrum?
   b. Repeat part (a) for the color red.
   c. Do the results confirm the fact that the shorter the wavelength the higher the energy level?
   d. Is light in the ultraviolet range more dangerous in regard to skin cancer than those in the infrared range? Why?
   e. Can you guess why fluorescent lights are used for growing plants in a dark environment?

16.5 Photodiodes

22. Referring to Fig. 16.20, determine I_λ if $V_\lambda = 30$ V and the light intensity is $4 \times 10^{-9}\ \text{W/m}^2$.

***23.** Determine the voltage drop across the resistor of Fig. 16.19 if the incident flux is 3000 fc, $V_\lambda = 25$ V, and $R = 100\ \text{k}\Omega$. Use the characteristics of Fig. 16.20.

24. Write an equation for the diode current of Fig. 16.22 versus the applied light intensity in footcandles.

16.6 Photoconductive Cells

***25.** What is the approximate rate of change of resistance with illumination for a photoconductive cell with the characteristics of Fig. 16.26 for the ranges (a) $0.1 \rightarrow 1\ \text{k}\Omega$, (b) $1 \rightarrow 10\ \text{k}\Omega$, and (c) $10 \rightarrow \text{k}\Omega$? (Note that this is a log scale.) Which region has the greatest rate of change in resistance with illumination?

26. What is the "dark current" of a photodiode?

27. If the illumination on the photoconductive diode in Fig. 16.28 is 10 fc, determine the magnitude of V_i to establish 6 V across the cell if R_1 is equal to 5 kΩ. Use the characteristics of Fig. 16.26.

***28.** Using the data provided in Fig. 16.27, sketch a curve of percentage conductance versus temperature for 0.01, 1.0, and 100 fc. Are there any noticeable effects?

***29.** **a.** Sketch a curve of rise time versus illumination using the data from Fig. 16.27.
  b. Repeat part (a) for the decay time.
  c. Discuss any noticeable effects of illumination in parts (a) and (b).

30. Which colors is the CdS unit of Fig. 16.27 most sensitive to?

16.7 IR Emitters

31. **a.** Determine the radiant flux at a dc forward current of 70 mA for the device of Fig. 16.30.
  b. Determine the radiant flux in lumens at a dc forward current of 45 mA.

***32.** **a.** Through the use of Fig. 16.31, determine the relative radiant intensity at an angle of 25° for a package with a flat glass window.
  b. Plot a curve of relative radiant intensity versus degrees for the flat package.

***33.** If 60 mA of dc forward current is applied to an SG1010A IR emitter, what will be the incident radiant flux in lumens 5° off the center if the package has an internal collimating system? Refer to Figs. 16.30 and 16.31.

16.8 Liquid-Crystal Displays

34. Referring to Fig. 16.35, which terminals must be energized to display number 7?

35. In your own words, describe the basic operation of an LCD.

36. Discuss the relative differences in mode of operation between an LED and an LCD display.

37. What are the relative advantages and disadvantages of an LCD display as compared to an LED display?

16.9 Thermistors

***38.** For the thermistor of Fig. 16.40, determine the dynamic rate of change in specific resistance with temperature at $T = 20°\text{C}$. How does this compare to the value determined at $T = 300°\text{C}$? From the results, determine whether the greatest change in resistance per unit change in temperature occurs at lower or higher levels of temperature. Note the vertical log scale.

39. Using the information provided in Fig. 16.40, determine the total resistance of a 2-cm length of the material having a perpendicular surface area of 1 cm^2 at a temperature of 0°C. Note the vertical log scale.

40. **a.** Referring to Fig. 16.41, determine the current at which a 25°C sample of the material changes from a positive to a negative temperature coefficient. (Figure 16.41 is a log scale.)
  b. Determine the power and resistance levels of the device (Fig. 16.41) at the peak of the 0°C curve.
  c. At a temperature of 25°C, determine the power rating if the resistance level is 1 MΩ.

41. In Fig. 16.43, $V = 0.2$ V and $R_{\text{variable}} = 10\ \Omega$. If the current through the sensitive movement is 2 mA and the voltage drop across the movement is 0 V, what is the resistance of the thermistor?

16.10 Tunnel Diodes

42. What are the essential differences between a semiconductor junction diode and a tunnel diode?

***43.** Note in the equivalent circuit of Fig. 16.45 that the capacitor appears in parallel with the negative resistance. Determine the reactance of the capacitor at 1 MHz and 100 MHz if $C = 5$ pF, and determine the total impedance of the parallel combination (with $R = -152\ \Omega$) at each frequency. Is the magnitude of the inductive reactance anything to be overly concerned about at either of these frequencies if $L_S = 6$ nH?

***44.** Why do you believe the maximum reverse current rating for the tunnel diode can be greater than the forward current rating? (*Hint:* Note the characteristics and consider the power rating.)

45. Determine the negative resistance for the tunnel diode of Fig. 16.44 between $V_T = 0.1$ V and $V_T = 0.3$ V.

46. Determine the stable operating points for the network of Fig. 16.48 if $E = 2$ V, $R = 0.39$ kΩ, and the tunnel diode of Fig. 16.44 is employed.

***47.** For $E = 0.5$ V and $R = 51\ \Omega$, sketch v_T for the network of Fig. 16.49 and the tunnel diode of Fig. 16.44.

48. Determine the frequency of oscillation for the network of Fig. 16.50 if $L = 5$ mH, $R_l = 10\ \Omega$, and $C = 1\ \mu$F.

17

pnpn and Other Devices

CHAPTER OBJECTIVES

To become familiar with the characteristics and areas of application of

- Silicon-controlled rectifiers (SCRs)
- Silicon-controlled switches (SCSs)
- Gate turn-off switches (GTO)
- Light-activated SCRs (LSCR)
- Shockley diodes and diacs
- Triacs
- Phototransistors and opto-isolators
- Unijunction and programmable unijunction transistors

17.1 INTRODUCTION

In Chapter 17, a number of important devices not discussed in detail in earlier chapters are introduced. The two-layer semiconductor diode has led to three-, four-, and even five-layer devices. A family of four-layer *pnpn* devices will first be considered: the SCR (silicon-controlled rectifier), the SCS (silicon-controlled switch), the GTO (gate turn-off switch), the LASCR (light-activated SCR), and then an increasingly important device—the UJT (unijunction transistor). Those four-layer devices with a control mechanism are commonly referred to as *thyristors*, although the term is most frequently applied to the SCR. The chapter closes with an introduction to the phototransistor, opto-isolators, and the PUT (programmable unijunction transistor).

pnpn DEVICES

17.2 SILICON-CONTROLLED RECTIFIER

Within the family of *pnpn* devices, the silicon-controlled rectifier is of greatest interest. It was first introduced in 1956 by Bell Telephone Laboratories. Some of the more common areas of application for SCRs include relay controls, time-delay circuits, regulated power suppliers, static switches, motor controls, choppers, inverters, cycloconverters, battery chargers, protective circuits, heater controls, and phase controls.

In recent years, SCRs have been designed to *control* powers as high as 10 MW with individual ratings as high as 2000 A at 1800 V. Its frequency range of application has also been extended to about 50 kHz, permitting some high-frequency applications such as induction heating and ultrasonic cleaning.

17.3 BASIC SILICON-CONTROLLED RECTIFIER OPERATION

As the terminology indicates, the SCR is a rectifier constructed of silicon material with a third terminal for control purposes. Silicon was chosen because of its high temperature and power capabilities. The basic operation of the SCR is different from that of the fundamental two-layer semiconductor diode in that a third terminal, called a *gate*, determines when the rectifier switches from the open-circuit to the short-circuit state. It is not enough to simply forward-bias the anode-to-cathode region of the device. In the conduction region, the dynamic resistance of the SCR is typically 0.01 Ω to 0.1 Ω. The reverse resistance is typically 100 kΩ or more.

The graphic symbol for the SCR is shown in Fig. 17.1 with the corresponding connections to the four-layer semiconductor structure. As indicated in Fig. 17.1a, if forward conduction is to be established, the anode must be positive with respect to the cathode. This is not, however, a sufficient criterion for turning the device on. A pulse of sufficient magnitude must also be applied to the gate to establish a turn-on gate current, represented symbolically by I_{GT}.

A more detailed examination of the basic operation of an SCR is best effected by splitting the four-layer *pnpn* structure of Fig. 17.1b into two three-layer transistor structures as shown in Fig. 17.2a and then considering the resultant circuit of Fig. 17.2b.

Note that one transistor for Fig. 17.2 is an *npn* device, whereas the other is a *pnp* transistor. For discussion purposes, the signal shown in Fig. 17.3a will be applied to the gate of the circuit of Fig. 17.2b. During the interval $0 \rightarrow t_1$, $V_{\text{gate}} = 0$ V, the circuit of Fig. 17.2b will appear as shown in Fig. 17.3b ($V_{\text{gate}} = 0$ V is equivalent to the gate terminal being grounded as shown in the figure). For $V_{BE_2} = V_{\text{gate}} = 0$ V, the base current $I_{B_2} = 0$, and I_{C_2} will be approximately I_{CO}. The base current of Q_1, $I_{B_1} = I_{C_2} = I_{CO}$, is too small to turn Q_1 on. Both transistors are therefore in the "off" state, resulting in a high impedance between the collector and the emitter of each transistor and the open-circuit representation for the controlled rectifier as shown in Fig. 17.3c.

At $t = t_1$, a pulse of V_G volts will appear at the SCR gate. The circuit conditions established with this input are shown in Fig. 17.4a. The potential V_G was chosen sufficiently large to turn Q_2 on ($V_{BE_2} = V_G$). The collector current of Q_2 will then rise to a value sufficiently large to turn Q_1 on ($I_{B_1} = I_{C_2}$). As Q_1 turns on, I_{C_1} will increase, resulting in a corresponding increase in I_{B_2}. The increase in base current for Q_2 will result in a further increase in I_{C_2}. The net result is a regenerative increase in the collector current of each transistor. The resulting anode-to-cathode resistance ($R_{SCR} = V/I_A$) is then small because I_A is large, resulting in the short-circuit representation for the SCR as indicated in Fig. 17.4b. The regenerative action described above results in SCRs having typical turn-on times of 0.1 μs to 1 μs. However, high-power devices in the range 100 A to 400 A may have 10- to 25-μs turn-on times.

In addition to gate triggering, SCRs can also be turned on by significantly raising the temperature of the device or raising the anode-to-cathode voltage to the breakover value shown on the characteristics of Fig. 17.7.

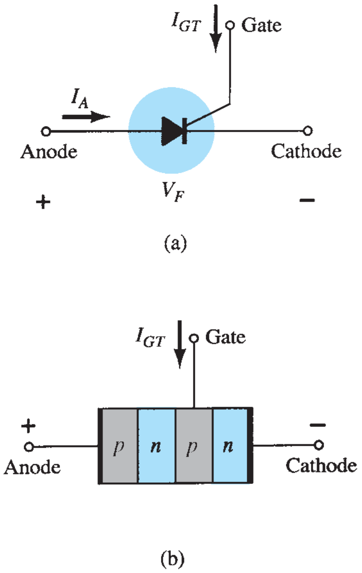


FIG. 17.1
(a) SCR symbol; (b) basic construction.

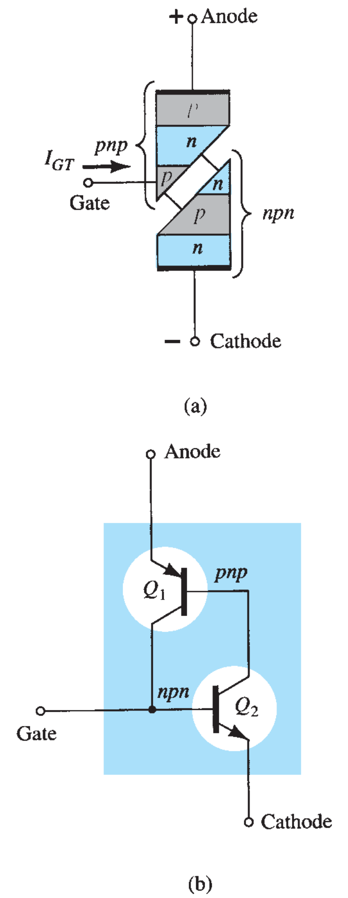


FIG. 17.2
SCR two-transistor equivalent circuit.

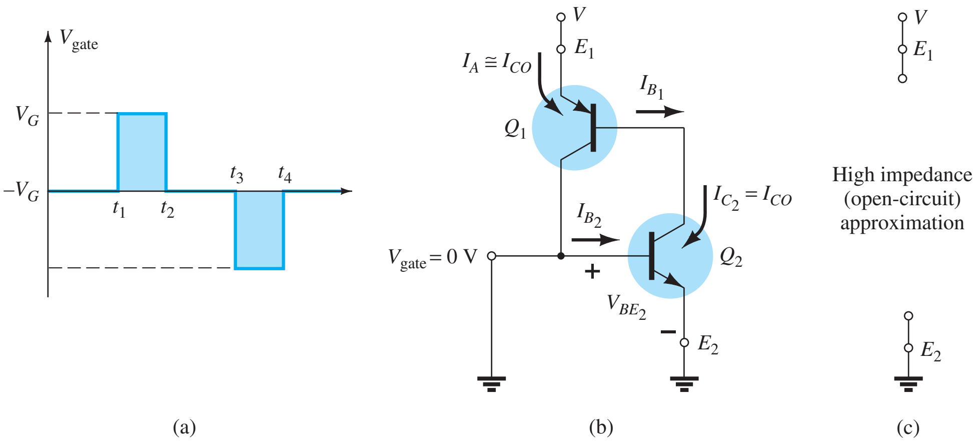


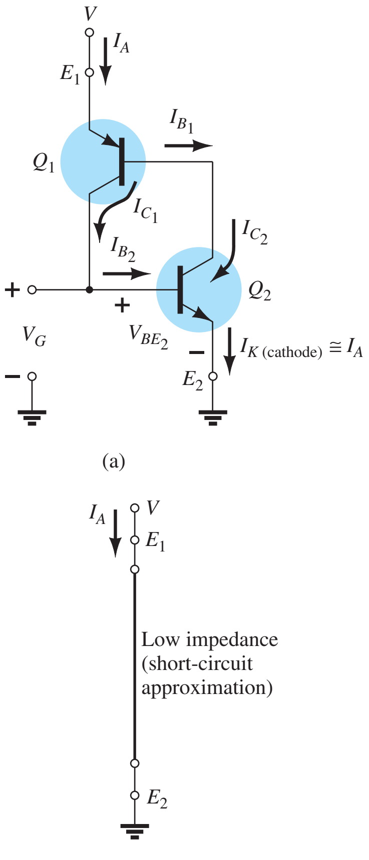
FIG. 17.3
"Off" state of the SCR.

The next question of concern is: How long is the turn-off time and how is turn-off accomplished? An SCR *cannot* be turned off by simply removing the gate signal, and only a special few can be turned off by applying a negative pulse to the gate terminal as shown in Fig. 17.3a at $t = t_3$.

The two general methods for turning off an SCR are categorized as anode current interruption and forced commutation.

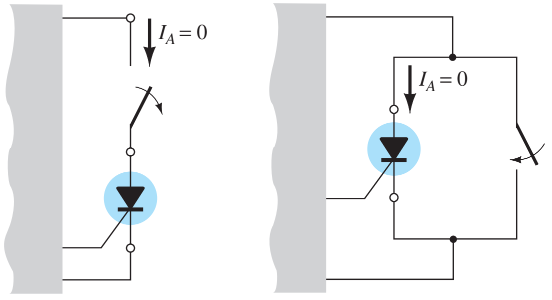
The two possibilities for current interruption are shown in Fig. 17.5. In Fig. 17.5a, I_A is zero when the switch is opened (series interruption), whereas in Fig. 17.5b, the same condition is established when the switch is closed (shunt interruption).

Forced commutation is the "forcing" of current through the SCR in the direction opposite to forward conduction. There is a wide variety of circuits for performing this function, a number of which can be found in the manuals of major manufacturers in this area. One of the more basic types is shown in Fig. 17.6. As indicated in the figure, the turn-off circuit consists of an *npn* transistor, a dc battery V_B, and a pulse generator. During SCR conduction, the transistor is in the "off" state, that is, $I_B = 0$, and the collector-to-emitter impedance is very high (for all practical purposes an open circuit). This high impedance will isolate the turn-off circuitry from affecting the operation of the SCR. For turn-off conditions, a positive pulse is applied to the base of the transistor, turning it heavily on, resulting in a very low impedance from collector to emitter (short-circuit representation). The battery potential will then appear directly across the SCR as shown in Fig. 17.6b, forcing current through it in the reverse direction for turn-off. Turn-off times of SCRs are typically 5 μs to 30 μs.



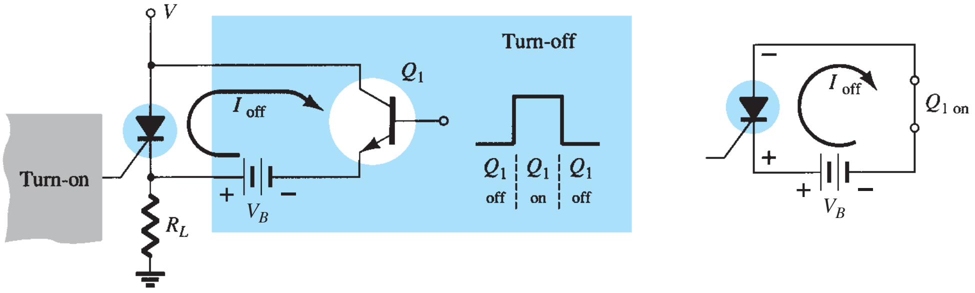
(b)

FIG. 17.4
"On" state of the SCR.



(a) (b)

FIG. 17.5
Anode current interruption.



(a) (b)

FIG. 17.6
Forced-commutation technique.

17.4 SCR CHARACTERISTICS AND RATINGS

The characteristics of an SCR are provided in Fig. 17.7 for various values of gate current. The currents and voltages of usual interest are indicated on the characteristic. A brief description of each follows.

1. *Forward breakover voltage* $V_{(BR)F^*}$ is the voltage above which the SCR enters the conduction region. The asterisk (*) denotes the letter to be added, which is dependent

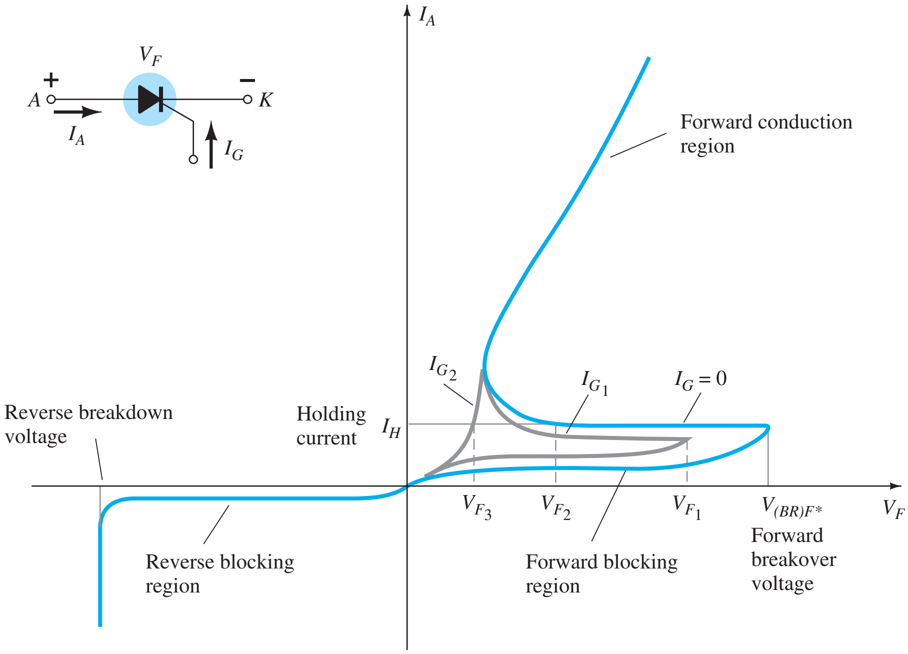


FIG. 17.7

SCR characteristics.

on the condition of the gate terminal as follows:

O = open circuit from G to K
S = short circuit from G to K
R = resistor from G to K
V = fixed bias (voltage) from G to K

2. *Holding current* I_H is the value of current below which the SCR switches from the conduction state to the forward blocking region under stated conditions.
3. *Forward and reverse blocking regions* are the regions corresponding to the open-circuit condition for the controlled rectifier that *block* the flow of charge (current) from anode to cathode.
4. *Reverse breakdown voltage* is equivalent to the Zener or avalanche region of the fundamental two-layer semiconductor diode.

It should be immediately obvious that the SCR characteristics of Fig. 17.7 are very similar to those of the basic two-layer semiconductor diode except for the horizontal offshoot before entering the conduction region. It is this horizontal jutting region that gives the gate control over the response of the SCR. For the characteristic having the solid blue line in Fig. 17.7 ($I_G = 0$), V_F must reach the largest required breakover voltage ($V_{(BR)F^*}$) before the "collapsing" effect results and the SCR can enter the conduction region corresponding to the *on* state. If the gate current is increased to I_{G_1}, as shown in the same figure by applying a bias voltage to the gate terminal, the value of V_F required for the conduction (V_{F_1}) is considerably less. Note also that I_H drops with increase in I_G. If increased to I_{G_2}, the SCR will fire at very low values of voltage (V_{F_3}) and the characteristics will begin to approach those of the basic *p–n* junction diode. Looking at the characteristics in a completely different sense, for a particular V_F voltage, say V_{F_2} (Fig. 17.7), we see that if the gate current is increased from $I_G = 0$ to I_{G_1} or more, the SCR will fire.

The gate characteristics are provided in Fig. 17.8. The characteristics of Fig. 17.8b are an expanded version of the shaded region of Fig. 17.8a. In Fig. 17.8a, the three gate ratings of greatest interest, P_{GFM}, I_{GFM}, and V_{GFM}, are indicated. Each is included on the characteristics in the same manner employed for the transistor. Except for portions of the shaded region, any combination of gate current and voltage that falls within this region will fire any SCR in the series of components for which these characteristics are provided. Temperature will determine which sections of the shaded region must be avoided. At −65°C the minimum current that will trigger the series of SCRs is 100 mA, whereas at +150°C only

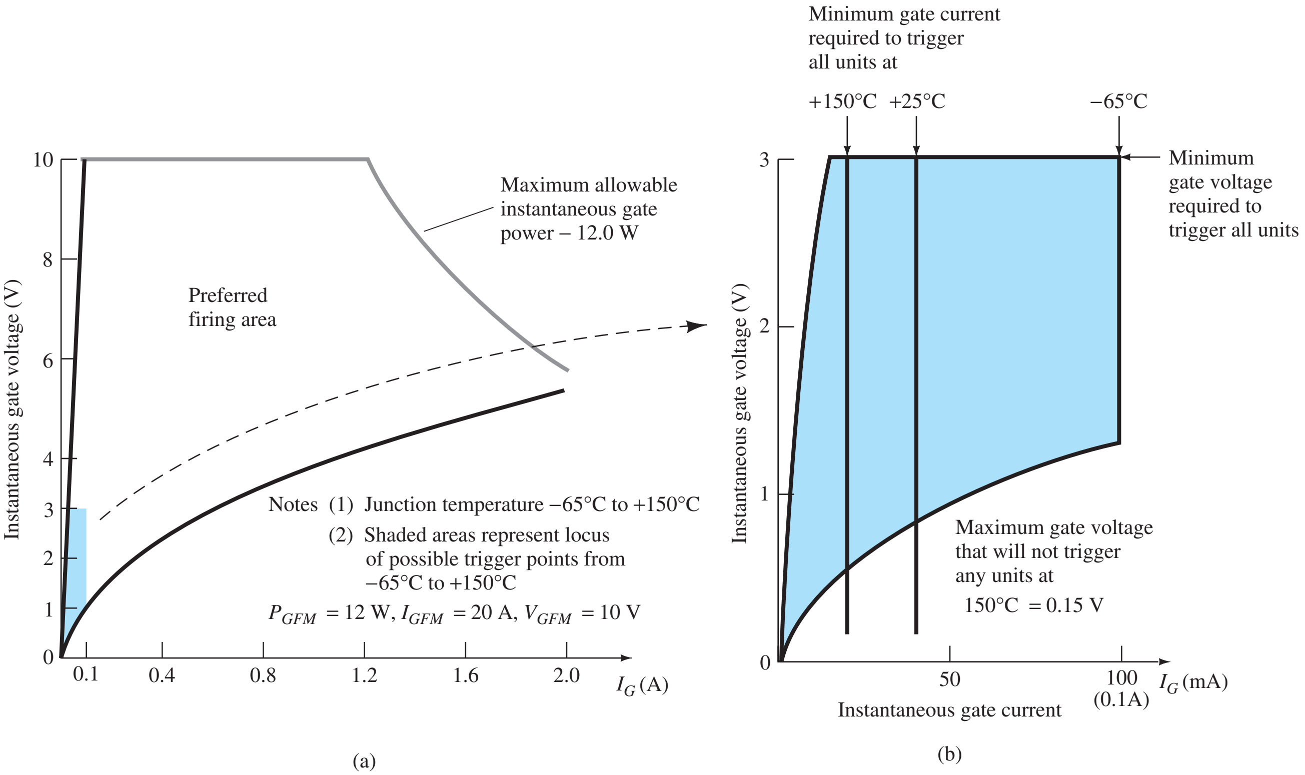


FIG. 17.8

SCR gate characteristics (GE series C38).

20 mA is required. The effect of temperature on the minimum gate voltage is usually not indicated on curves of this type since gate potentials of 3 V or more are usually obtained easily. As indicated on Fig. 17.8b, a minimum of 3 V is indicated for all units for the temperature range of interest.

Other parameters usually included on the specification sheet of an SCR are the turn-on time t_{on}, turn-off time t_{off}, junction temperature T_J, and case temperature T_C, all of which by now should be to some extent self-explanatory.

The case construction and terminal identification of SCRs vary with the application. The case-construction techniques and the terminal identification of a number of SCRs are provided in Fig. 17.9.

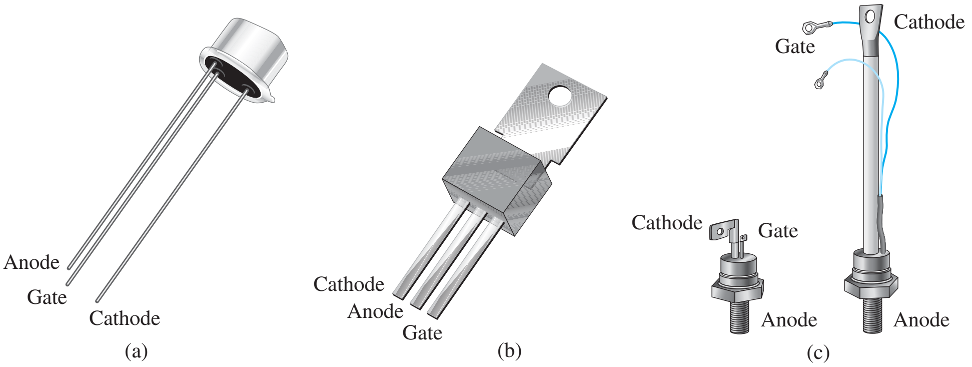


FIG. 17.9

SCR case construction and terminal identification.

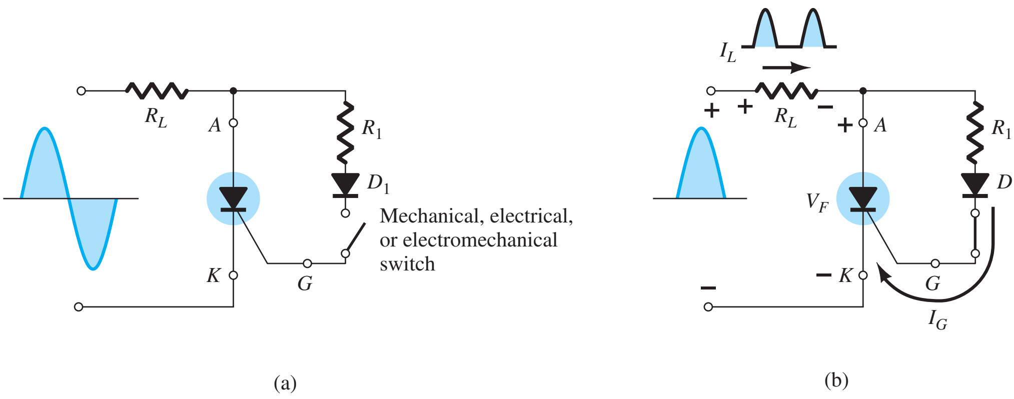
17.5 SCR APPLICATIONS

Some of the possible applications for the SCR are listed in the introduction to the SCR (Section 17.2). In this section, we consider five: a static switch, a phase-control system, a battery charger, a temperature controller, and a single-source emergency-lighting system.

Series Static Switch

A half-wave *series static switch* is shown in Fig. 17.10a. If the switch is closed as shown in Fig. 17.10b, a gate current will flow during the positive portion of the input signal, turning the SCR on. Resistor R_1 limits the magnitude of the gate current. When the SCR turns on, the anode-to-cathode voltage (V_F) will drop to the conduction value, resulting in a greatly reduced gate current and very little loss in the gate circuitry. For the negative region of the input signal, the SCR will turn off since the anode is negative with respect to the cathode. The diode D_1 is included to prevent a reversal in gate current.

The waveforms for the resulting load current and voltage are shown in Fig. 17.10b. The result is a half-wave-rectified signal through the load. If less than 180° conduction is desired, the switch can be closed at any phase displacement during the positive portion of the input signal. The switch can be electronic, electromagnetic, or mechanical, depending on the application.



(a)

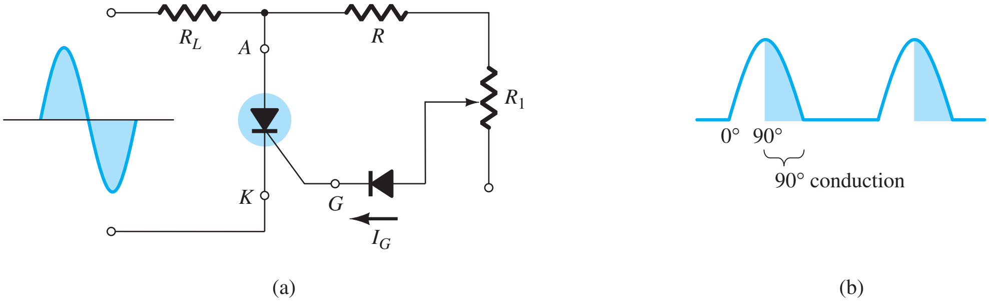
(b)

FIG. 17.10

Half-wave series static switch.

Variable-Resistance Phase Control

A circuit capable of establishing a conduction angle between 90° and 180° is shown in Fig. 17.11a. The circuit is similar to that of Fig. 17.10a except for the addition of a variable resistor and the elimination of the switch. The combination of the resistors R and R_1 will limit the gate current during the positive portion of the input signal. If R_1 is set to its maximum value, the gate current may never reach turn-on magnitude. As R_1 is decreased from the maximum, the gate current will increase from the same input voltage. In this way, the required turn-on gate current can be established in any point between 0° and 90° as shown in Fig. 17.11b. If R_1 is low, the SCR will fire almost immediately, resulting in the same action as that obtained from the circuit of Fig. 17.10a (180° conduction). However, as indicated above, if R_1 is increased, a larger input voltage (positive) will be required to fire the SCR. As shown in Fig. 17.11b, the control cannot be extended past a 90° phase displacement since the input is at its maximum at this point. If it fails to fire at this and lesser values of input voltage on the positive slope of the input, the same response must be



(a)

(b)

FIG. 17.11

Half-wave variable-resistance phase control.

expected from the negatively sloped portion of the signal waveform. The operation here is normally referred to in technical terms as *half-wave variable-resistance phase control.* It is an effective method of controlling the rms current and therefore power to the load.

Battery-Charging Regulator

A third popular application of the SCR is in a *battery-charging regulator.* The fundamental components of the circuit are shown in Fig. 17.12. The control circuit has been blocked off for discussion purposes.

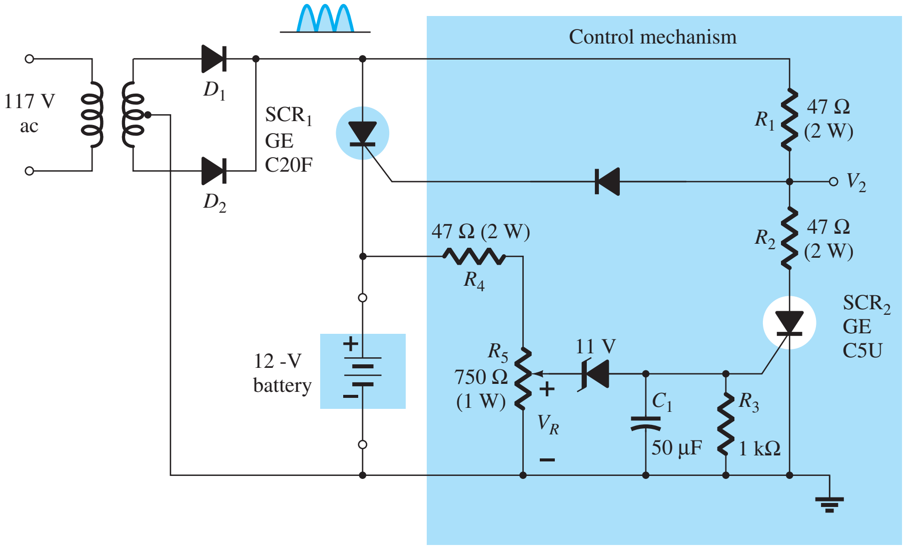


FIG. 17.12

Battery-charging regulator.

As indicated in the figure, D_1 and D_2 establish a full-wave-rectified signal across SCR_1 and the 12-V battery to be charged. At low battery voltages, SCR_2 is in the "off" state for reasons to be explained shortly. With SCR_2 open, the SCR_1 controlling circuit is exactly the same as the series static switch control discussed earlier in this section. When the full-wave-rectified input is sufficiently large to produce the required turn-on gate current (controlled by R_1), SCR_1 will turn on and charging of the battery will commence. At the start of charging, the low battery voltage will result in a low voltage V_R as determined by the simple voltage-divider circuit. Voltage V_R is in turn too small to cause 11.0-V Zener conduction. In the "off" state, the Zener is effectively an open circuit, maintaining SCR_2 in the "off" state since the gate current is zero. The capacitor C_1 is included to prevent any voltage transients in the circuit from accidentally turning on SCR_2. Recall from your fundamental study of circuit analysis that the voltage cannot change instantaneously across a capacitor. In this way, C_1 prevents transient effects from affecting the SCR.

As charging continues, the battery voltage rises to a point where V_R is sufficiently high to both turn on the 11.0-V Zener and fire SCR_2. Once SCR_2 has fired, the short-circuit representation for SCR_2 will result in a voltage-divider circuit determined by R_1 and R_2 that will maintain V_2 at a level too small to turn SCR_1 on. When this occurs, the battery is fully charged and the open-circuit state of SCR_1 will cut off the charging current. Thus the regulator recharges the battery whenever the voltage drops and prevents overcharging when it is fully charged.

Temperature Controller

The schematic diagram of a 100-W heater control using an SCR appears in Fig. 17.13. It is designed such that the 100-W heater will turn on and off as determined by thermostats. Mercury-in-glass thermostats are very sensitive to temperature change. In fact, they can sense changes as small as 0.1°C. They are limited in application, however, in that they can

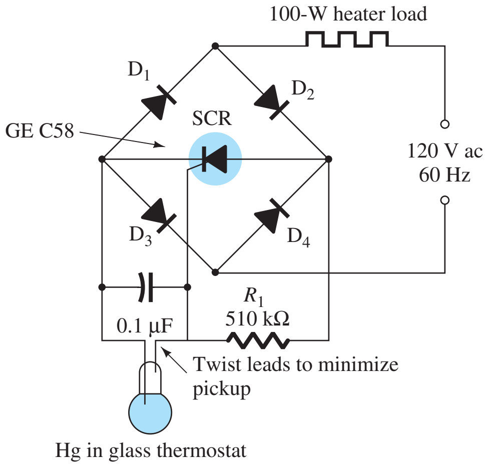

100-W heater load
D1
D2
SCR
GE C58
120 V ac
60 Hz
D3
D4
R1
510 kΩ
0.1 μF
Twist leads to minimize pickup
Hg in glass thermostat

FIG. 17.13

Temperature controller.

handle only very low levels of current—below 1 mA. In this application, the SCR serves as a current amplifier in a load-switching element. It is not an amplifier in the sense that it magnifies the current level of the thermostat. Rather, it is a device whose higher current level is controlled by the behavior of the thermostat.

It should be clear that the bridge network is connected to the ac supply through the 100-W heater. This will result in a full-wave-rectified voltage across the SCR. When the thermostat is open, the voltage across the capacitor will charge to a gate-firing potential through each pulse of the rectified signal. The charging time constant is determined by the *RC* product. This will trigger the SCR during each half-cycle of the input signal, permitting a flow of charge (current) to the heater. As the temperature rises, the conductive thermostat will short-circuit the capacitor, eliminating the possibility of the capacitor charging to the firing potential and triggering the SCR. The 510-kΩ resistor will then contribute to maintaining a very low current (less than 250 μA) through the thermostat.

Emergency-Lighting System

The last application for the SCR to be described is shown in Fig. 17.14. It is a single-source emergency-lighting system that will maintain the charge on a 6-V battery to ensure its availability and also provide dc energy to a bulb if there is a power shortage. A full-wave-rectified signal will appear across the 6-V lamp due to diodes D_2 and D_1. The capacitor C_1 will charge to a voltage slightly less than a difference between the peak value of the full-wave-rectified signal and the dc voltage across R_2 established by the 6-V battery. In any event, the cathode of SCR_1 is higher than the anode, and the gate-to-cathode voltage is negative, ensuring that the SCR is nonconducting. The battery is charged

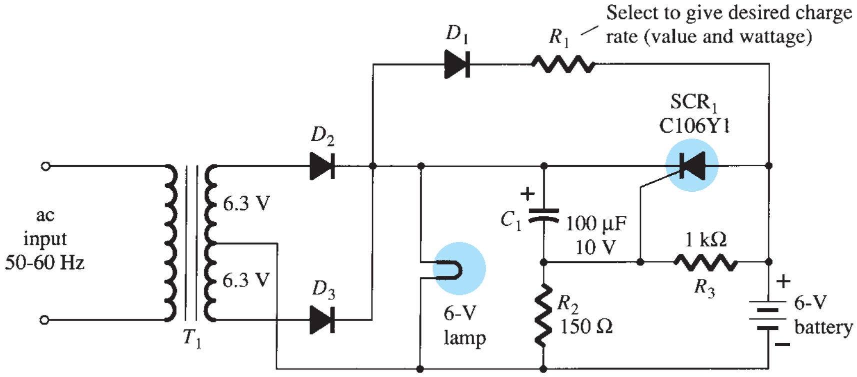

D1
R1
Select to give desired charge rate (value and wattage)
SCR1
C106Y1
D2
ac input 50-60 Hz
6.3 V
6.3 V
T1
D3
+
C1
100 μF
10 V
1 kΩ
R3
6-V lamp
R2
150 Ω
+
6-V battery
−

FIG. 17.14

Single-source emergency-lighting system.

through R_1 and D_1 at a rate determined by R_1. Charging will only take place when the anode of D_1 is more positive than its cathode. The dc level of the full-wave-rectified signal will ensure that the bulb is lit when the power is on. If the power should fail, the capacitor C_1 will discharge through D_1, R_1, and R_3 until the cathode of SCR_1 is less positive than the anode. At the same time, the junction of R_2 and R_3 will become positive and establish sufficient gate-to-cathode voltage to trigger the SCR. Once fired, the 6-V battery discharges through the SCR_1 and energizes the lamp and maintains its illumination. Once power is restored, the capacitor C_1 recharges and reestablishes the nonconducting state of SCR_1 as described above.

17.6 SILICON-CONTROLLED SWITCH

The silicon-controlled switch (SCS), like the silicon-controlled rectifier, is a four-layer *pnpn* device. All four semiconductor layers of the SCS are available due to the addition of an anode gate, as shown in Fig. 17.15a. The graphic symbol and transistor equivalent circuit are shown in the same figure. The characteristics of the device are essentially the same as those for the SCR. The effect of an anode gate current is very similar to that demonstrated by the gate current in Fig. 17.7. The higher the anode gate current, the lower is the required anode-to-cathode voltage to turn the device on.

The anode gate connection can be used to turn the device either on or off. To turn on the device, a negative pulse must be applied to the anode gate terminal, whereas a positive pulse is required to turn off the device. The need for the type of pulse indicated above can be demonstrated using the circuit of Fig. 17.15c. A negative pulse at the anode gate will forward-bias the base-to-emitter junction of Q_1, turning it on. The resulting heavy collector current I_{C_1} will turn on Q_2, resulting in a regenerative action and the "on" state for the SCS device. A positive pulse at the anode gate will reverse-bias the base-to-emitter junction of Q_1, turning it off, resulting in the open-circuit "off" state of the device. In general, the triggering (turn-on) anode gate current is larger in magnitude than the required cathode gate current. For one representative SCS device, the triggering anode gate current is 1.5 mA, whereas the required cathode gate current is 1 μA. The required turn-on gate current at either terminal is affected by many factors, including the operating temperature, the anode-to-cathode voltage, the load placement, and the type of cathode, gate-to-cathode, and anode gate-to-anode connection (short-circuit, open-circuit, bias, load, etc.). Tables, graphs, and curves are normally available for each device to provide the type of information indicated above.

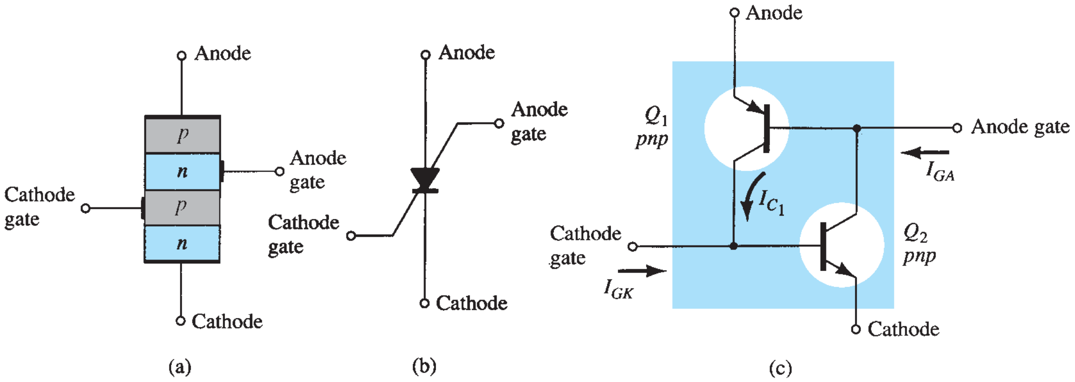
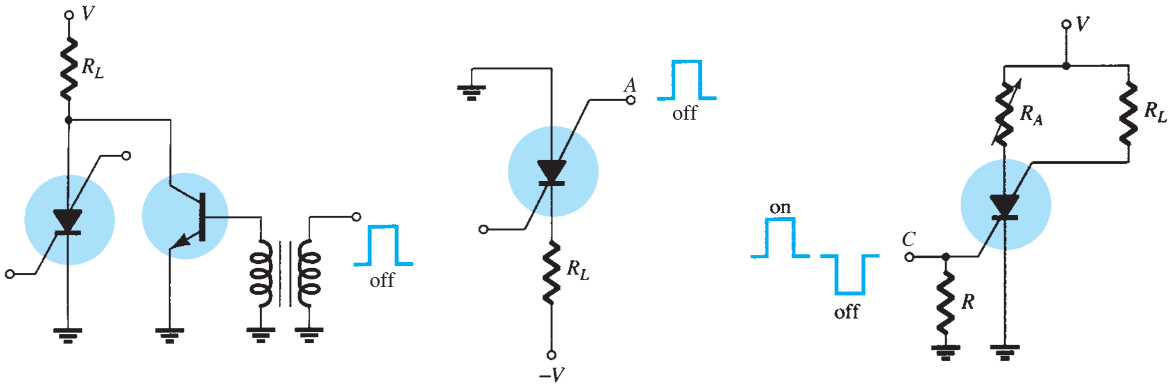


FIG. 17.15

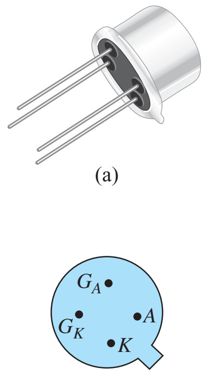
Silicon-controlled switch (SCS): (a) basic construction; (b) graphic symbol; (c) equivalent transistor circuit.

Three of the more fundamental types of turn-off circuits for the SCS are shown in Fig. 17.16. When a pulse is applied to the transformer of Fig. 17.16a, the transistor conducts heavily, resulting in a low-impedance (≅ short-circuit) characteristic between collector and emitter. This low-impedance branch diverts anode current away from the SCS, dropping it below the holding value and consequently turning it off. Similarly, the positive pulse at the anode gate of Fig. 17.16b will turn the SCS off by the mechanism described earlier in this section. The circuit of Fig. 17.16c can be turned either off *or* on by a pulse of the proper magnitude



(a) (b) (c)

FIG. 17.16
SCS turn-off techniques.



(a)

(b)

FIG. 17.17
Silicon-controlled switch (SCS): (a) device; (b) terminal identification.

at the cathode gate. The turn-off characteristic is possible only if the correct value of R_A is employed. It will control the amount of regenerative feedback, the magnitude of which is critical for this type of operation. Note the variety of positions in which the load resistor R_L can be placed. There are a number of other possibilities, which can be found in any comprehensive semiconductor handbook or manual.

An advantage of the SCS over a corresponding SCR is the reduced turn-off time, typically within the range 1 μs to 10 μs for the SCS and 5 μs to 30 μs for the SCR. Some of the remaining advantages of the SCS over an SCR include increased control and triggering sensitivity and a more predictable firing situation. At present, however, the SCS is limited to low power, current, and voltage ratings. Typical maximum anode currents range from 100 mA to 300 mA with dissipation (power) ratings of 100 mW to 500 mW.

The terminal identification of an SCS is shown in Fig. 17.17 with a packaged SCS.

Voltage Sensor

Some of the more common areas of application include a wide variety of computer circuits (counters, registers, and timing circuits), pulse generators, voltage sensors, and oscillators. One simple application for an SCS as a voltage-sensing device is shown in Fig. 17.18. It is an alarm system with *n* inputs from various stations. Any single input will turn that particular SCS on, resulting in an energized alarm relay and light in the anode gate circuit to indicate the location of the input (disturbance).

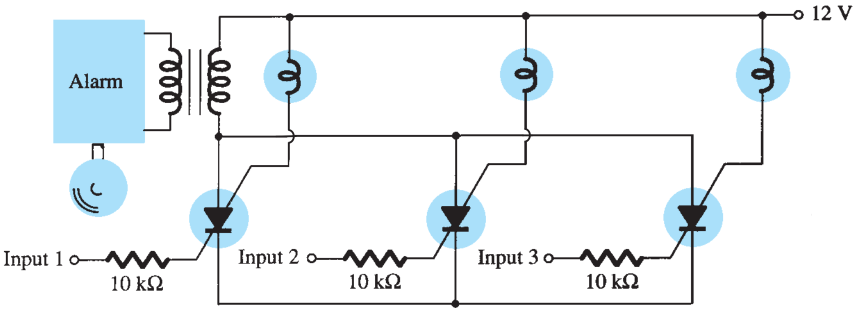


FIG. 17.18
SCS alarm circuit.

Alarm Circuit

One additional application of the SCS is in the alarm circuit of Fig. 17.19. R_S represents a temperature-, light-, or radiation-sensitive resistor, that is, an element whose resistance will decrease with the application of any of the three energy sources listed above. The cathode gate potential is determined by the divider relationship established by R_S and the variable resistor. Note that the gate potential is at approximately 0 V if R_S equals the value set by the variable resistor since both resistors will have 12 V across them. However, if R_S decreases, the potential of the junction will increase until the SCS is forward-biased, causing the SCS to turn on and energize the alarm relay.

The 100-kΩ resistor is included to reduce the possibility of an accidental triggering of the device through a phenomenon known as the *rate effect.* It is caused by the stray capacitance levels between gates. A high-frequency transient can establish sufficient base current to turn the SCS on accidentally. The device is reset by pressing the reset button, which opens the conduction path of the SCS and reduces the anode current to zero.

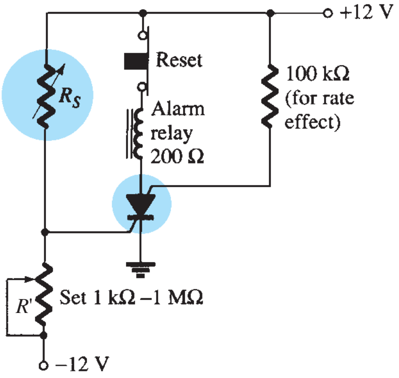


FIG. 17.19
Alarm circuit.

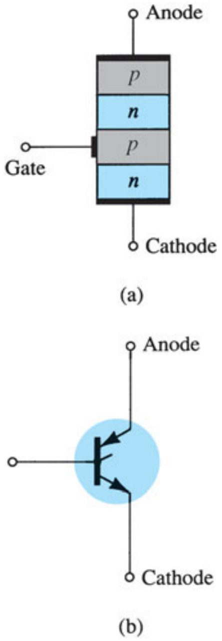
17.7 GATE TURN-OFF SWITCH

The gate turn-off switch (GTO) is the third *pnpn* device to be introduced in this chapter. Like the SCR, however, it has only three external terminals, as indicated in Fig. 17.20a. Its graphical symbol is shown in Fig. 17.20b. Although the graphical symbol is different from that of either the SCR or the SCS, the transistor equivalent is exactly the same and the characteristics are similar.

The most obvious advantage of the GTO over the SCR or SCS is the fact that it can be turned on *or* off by applying the proper pulse to the cathode gate (without the anode gate and associated circuitry required for the SCS). A consequence of this turn-off capability is an increase in the magnitude of the required gate current for triggering. For an SCR and GTO of similar maximum rms current ratings, the gate-triggering current of a particular SCR is 30 μA, whereas the triggering current of the GTO is 20 mA. The turn-off current of a GTO is slightly larger than the required triggering current. The maximum rms current and dissipation ratings of GTOs manufactured today are limited to about 3 A and 20 W, respectively.

A second very important characteristic of the GTO is improved switching characteristics. The turn-on time is similar to that of the SCR (typically 1 μs), but the turn-off time of about the *same* duration (1 μs) is much smaller than the typical turn-off time of an SCR (5 μs to 30 μs). The fact that the turn-off time is similar to the turn-on time rather than considerably larger permits the use of this device in high-speed applications.

A typical GTO and its terminal identification are shown in Fig. 17.21. The GTO gate input characteristics and turn-off circuits can be found in a comprehensive manual or specification sheet. The majority of the SCR turn-off circuits can also be used for GTOs.



(a)

(b)

FIG. 17.20
Gate turn-off switch (GTO): (a) basic construction; (b) symbol.

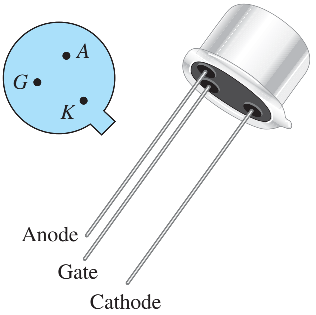


FIG. 17.21
Typical GTO and its terminal identification.

Sawtooth Generator

Some of the areas of application for the GTO include counters, pulse generators, multivibrators, and voltage regulators. Figure 17.22 is an illustration of a simple sawtooth generator employing a GTO and a Zener diode.

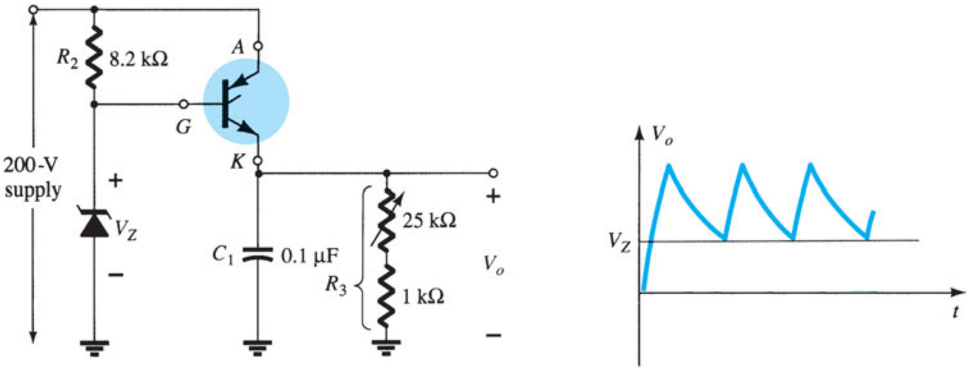


FIG. 17.22
GTO sawtooth generator.

When the supply is energized, the GTO will turn on, resulting in the short-circuit equivalent from anode to cathode. The capacitor C_1 will then begin to charge toward the supply voltage as shown in Fig. 17.22. As the voltage across the capacitor C_1 charges above the Zener potential, a reversal in gate-to-cathode voltage will result, establishing a reversal in gate current. Eventually, the negative gate current will be large enough to turn the GTO off. Once the GTO turns off, resulting in the open-circuit representation, the capacitor C_1 will discharge through the resistor R_3. The discharge time will be determined by the circuit time constant $\tau = R_3C_1$. The proper choice of R_3 and C_1 will result in the sawtooth waveform of Fig. 17.22. Once the output potential V_o drops below V_Z, the GTO will turn on and the process will repeat.

17.8 LIGHT-ACTIVATED SCR

The next in the series of *pnpn* devices is the light-activated SCR (LASCR). As indicated by the terminology, it is an SCR whose state is controlled by the light falling on a silicon semiconductor layer of the device. The basic construction of an LASCR is shown in Fig. 17.23a. As indicated in Fig. 17.23a, a gate lead is also provided to permit triggering the device using typical SCR methods. Note also in the figure that the mounting surface for the silicon pellet is the anode connection for the device. The graphical symbols most commonly employed for the LASCR are provided in Fig. 17.23b. The terminal identification and a typical LASCR appear in Fig. 17.24a.

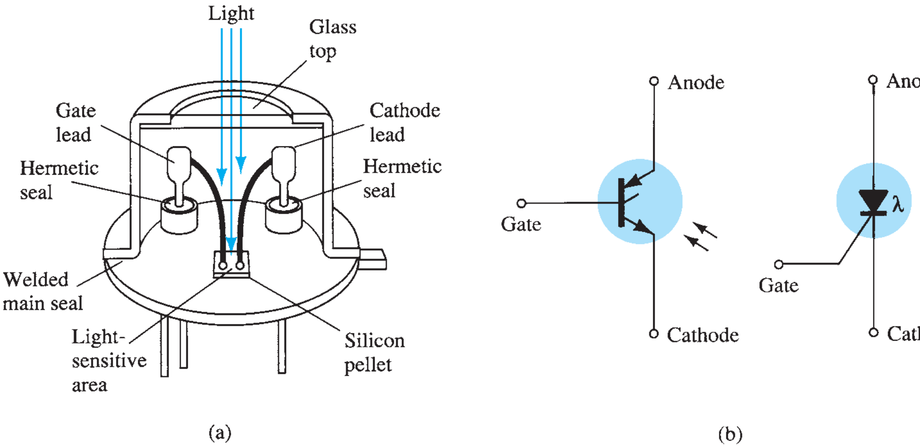


FIG. 17.23

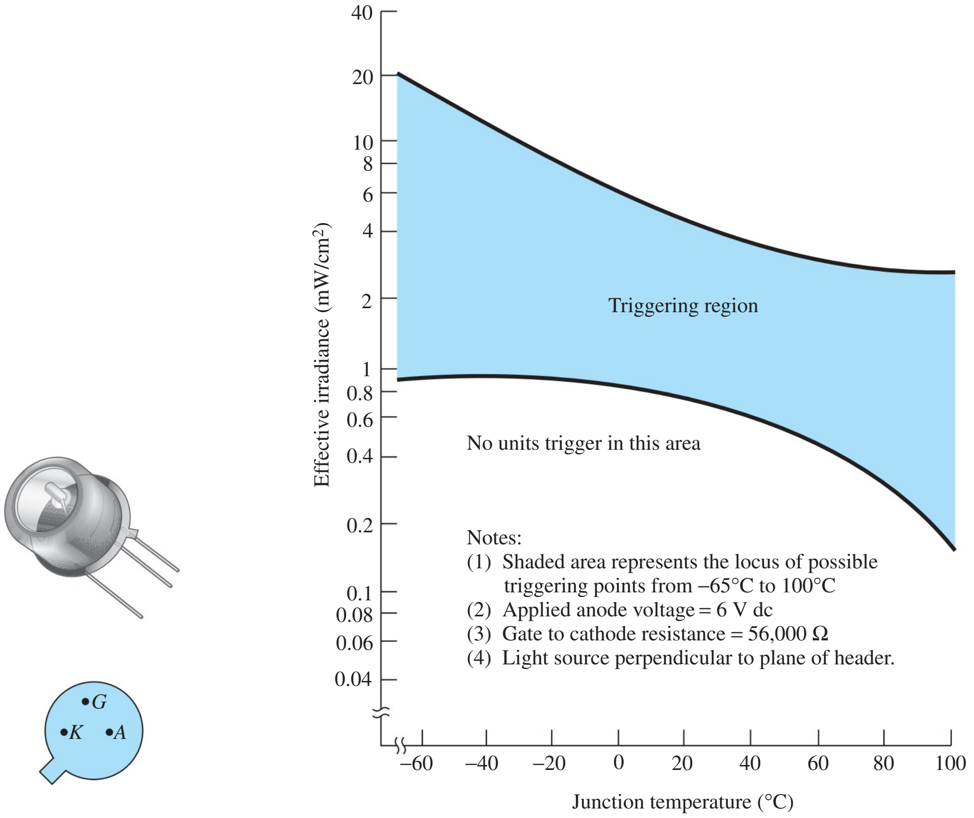
Light-activated SCR (LASCR): (a) basic construction; (b) symbols.

Some of the areas of application for the LASCR include optical light controls, relays, phase control, motor control, and a variety of computer applications. The maximum current (rms) and power (gate) ratings for commercially available LASCRs are about 3 A and 0.1 W, respectively. The characteristics (light triggering) of a representative LASCR are provided in Fig. 17.24b. Note in this figure that an increase in junction temperature results in a reduction in light energy required to activate the device.

AND/OR Circuits

One interesting application of an LASCR is in the AND and OR circuits of Fig. 17.25. Only when light falls on LASCR_1 *and* LASCR_2 will the short-circuit representation for each be applicable and the supply voltage appear across the load. For the OR circuit, light energy applied to LASCR_1 *or* LASCR_2 will result in the supply voltage appearing across the load.

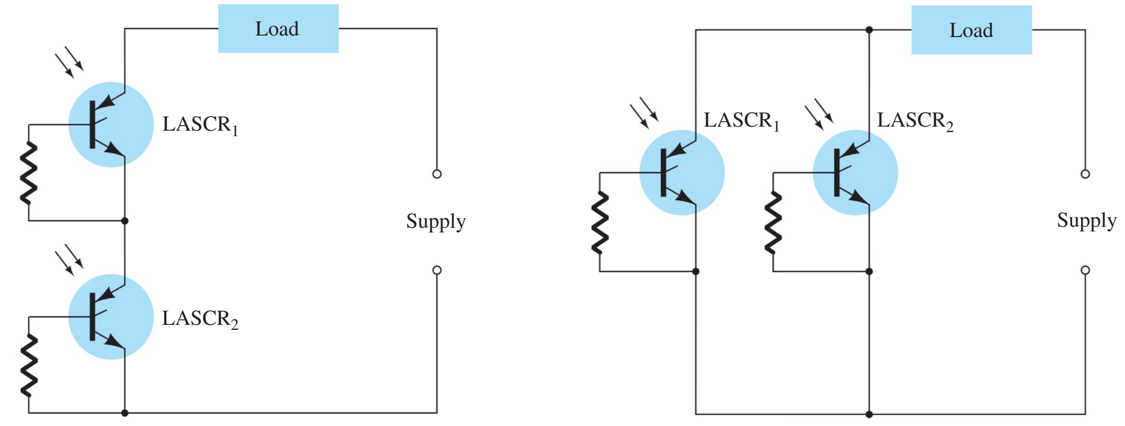
The LASCR is most sensitive to light when the gate terminal is open. Its sensitivity can be reduced and controlled somewhat by the insertion of a gate resistor, as shown in Fig. 17.25.



(a) (b)

FIG. 17.24

LASCR: (a) appearance and terminal identification; (b) light-triggering characteristics.



(a) (b)

FIG. 17.25

LASCR optoelectronic logic circuitry: (a) AND gate: input to LASCR$_1$ *and LASCR*$_2$ *is required for energization of the load; (b) OR gate: input to either LASCR*$_1$ *or LASCR*$_2$ *will energize the load.*

Latching Relay

A second application of the LASCR appears in Fig. 17.26. It is the semiconductor analog of an electromechanical relay. Note that it offers complete isolation between the input and the switching element. The energizing current can be passed through a light-emitting diode or a lamp, as shown in the figure. The incident light will cause the LASCR to turn on and permit a flow of charge (current) through the load as established by the dc supply. The

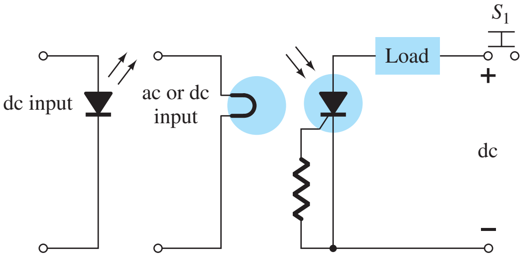


FIG. 17.26
Latching relay.

LASCR can be turned off using the reset switch S_1. This system offers the additional advantages over an electromechanical switch of long life, microsecond response, small size, and the elimination of contact bounce.

17.9 SHOCKLEY DIODE

The Shockley diode is a four-layer *pnpn* diode with only two external terminals, as shown in Fig. 17.27a with its graphical symbol. The characteristics (Fig. 17.27b) of the device are exactly the same as those encountered for the SCR with $I_G = 0$. As indicated by the characteristics, the device is in the "off" state (open-circuit representation) until the breakover voltage is reached, at which time avalanche conditions develop and the device turns on (short-circuit representation).

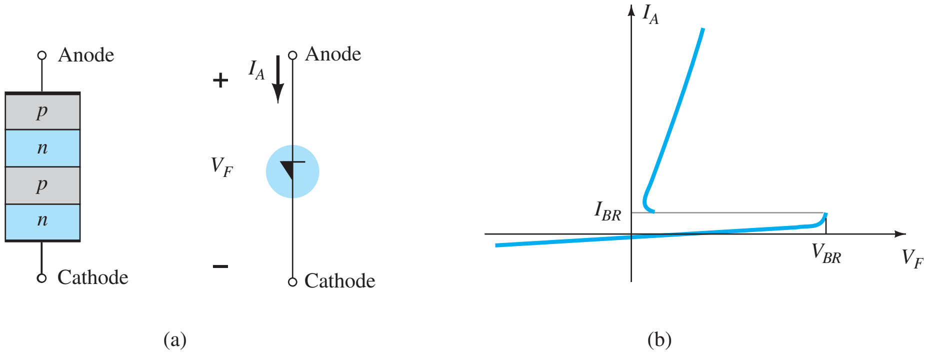


FIG. 17.27
Shockley diode: (a) basic construction and symbol; (b) characteristics.

Trigger Switch

One common application of the Shockley diode is shown in Fig. 17.28, where it is employed as a trigger switch for an SCR. When the circuit is energized, the voltage across the capacitor will begin to change toward the supply voltage. Eventually, the voltage across the capacitor will be sufficiently high to first turn on the Shockley diode and then the SCR.

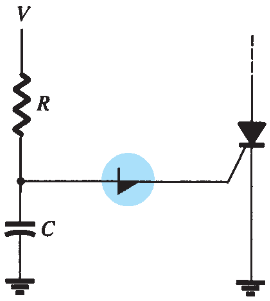
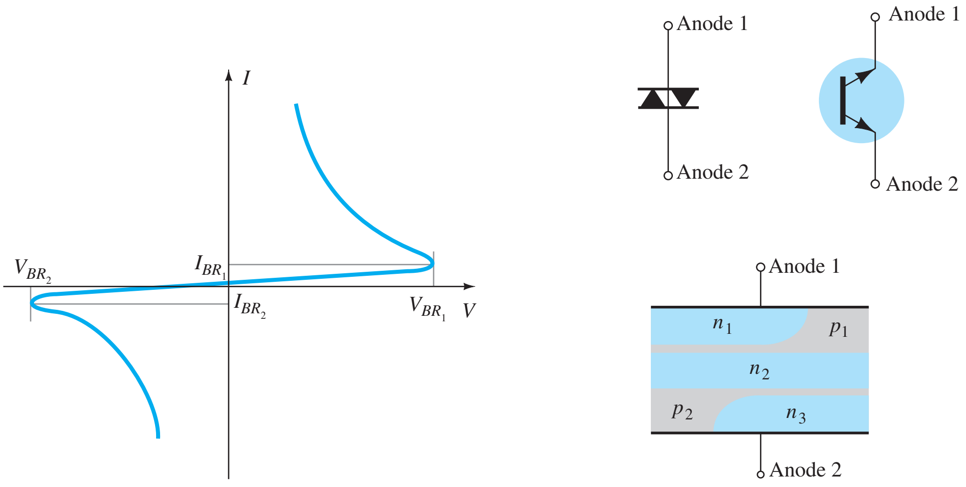


FIG. 17.28
Shockley diode application—trigger switch for an SCR.

17.10 DIAC

The diac is basically a two-terminal parallel-inverse combination of semiconductor layers that permits triggering in either direction. The characteristics of the device, presented in Fig. 17.29a, clearly demonstrate that there is a breakover voltage in either direction. This possibility of an *on* condition in either direction can be used to its fullest advantage in ac applications.

The basic arrangement of the semiconductor layers of the diac is shown in Fig. 17.29b, along with its graphical symbol. Note that neither terminal is referred to as the cathode. Instead, there is an anode 1 (or electrode 1) and an anode 2 (or electrode 2). When anode 1 is positive with respect to anode 2, the semiconductor layers of particular interest are $p_1n_2p_2$ and n_3. For anode 2 positive with respect to anode 1, the applicable layers are $p_2n_2p_1$ and n_1.


I
V_{BR_2}
I_{BR_1}
I_{BR_2}
V_{BR_1}
V
Anode 1
Anode 2
Anode 1
Anode 2
Anode 1
n_1
p_1
n_2
p_2
n_3
Anode 2

(a) (b)

FIG. 17.29

The diac: (a) characteristics; (b) symbols and basic construction.

For the unit appearing in Fig. 17.29, the breakdown voltages are very close in magnitude but may vary from a minimum of 28 V to a maximum of 42 V. They are related by the following equation provided in the specification sheet:

$$\boxed{V_{BR_1} = V_{BR_2} \pm 0.1V_{BR_2}} \qquad \textbf{(17.1)}$$

The current levels (I_{BR_1} and I_{BR_2}) are also very close in magnitude for each device. For the unit of Fig. 17.29, both current levels are about 200 μA = 0.2 mA.

Proximity Detector

The use of the diac in a proximity detector is shown in Fig. 17.30. Note the use of an SCR in series with the load and the programmable unijunction transistor (to be described in Section 17.12) connected directly to the sensing electrode.

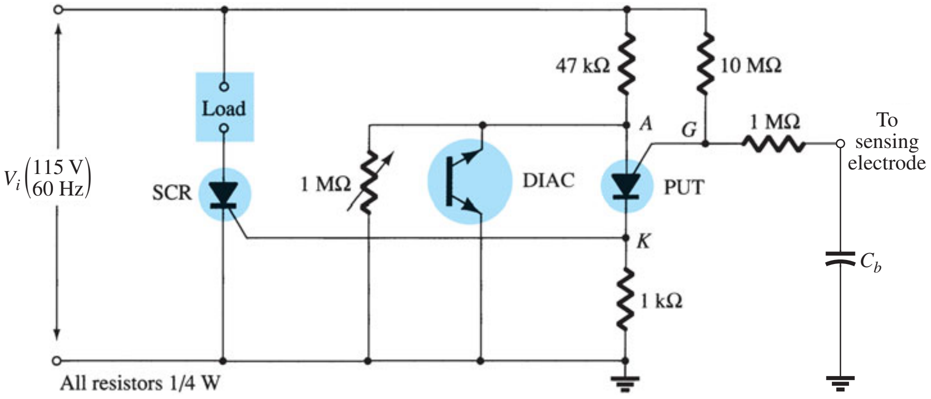

47 kΩ
10 MΩ
Load
A
G
1 MΩ
To sensing electrode
$V_i \left(\begin{matrix}115 \text{ V} \\ 60 \text{ Hz}\end{matrix}\right)$
SCR
1 MΩ
DIAC
PUT
K
C_b
1 kΩ
All resistors 1/4 W

FIG. 17.30

Proximity detector or touch switch.

As a human body approaches the sensing electrode, the capacitance between the electrode and the ground (C_b) increases. The programmable UJT (PUT) is a device that will fire (enter the short-circuit state) when the anode voltage (V_A) is at least 0.7 V (for silicon) greater than the gate voltage (V_G). Before the programmable device turns on, the system is essentially as shown in Fig. 17.31. As the input voltage rises, the diac voltage v_A will follow as shown in the figure until the firing potential is reached. It will then turn on and the diac voltage will drop substantially, as shown. Note that the diac is in essentially an open-circuit state until it fires. Before the capacitive element is introduced, the voltage v_G will be the

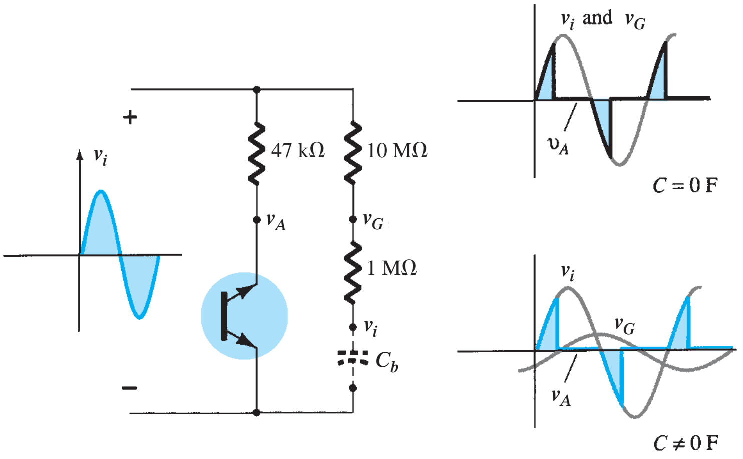

+
v_i
47 kΩ
10 MΩ
v_A
v_G
1 MΩ
v_i
C_b
−
v_i and v_G
v_A
$C = 0$ F
v_i
v_G
v_A
$C \neq 0$ F

FIG. 17.31

Effect of capacitive element on the behavior of the network of Fig. 17.30.

same as the input. As indicated in the figure, since both v_A and v_G follow the input, v_A can never be greater than v_G by 0.7 V and turn on the device. However, as the capacitive element is introduced, the voltage v_G will begin to lag the input voltage by an increasing angle, as indicated in the figure. There is therefore a point established where v_A can exceed v_G by 0.7 V and cause the programmable device to fire. A heavy current is established through the PUT at this point, raising the voltage v_G and turning on the SCR. A heavy SCR current will then exist through the load, reacting to the presence of the approaching person.

A second application of the diac appears in the next section (Fig. 17.33) as we consider an important power-control device: the triac.

17.11 TRIAC

The triac is fundamentally a diac with a gate terminal for controlling the turn-on conditions of the bilateral device in either direction. In other words, for either direction the gate current can control the action of the device in a manner very similar to that demonstrated for an SCR. The characteristics, however, of the triac in the first and third quadrants are somewhat different from those of the diac, as shown in Fig. 17.32c. Note the holding current in each direction not present in the characteristics of the diac.

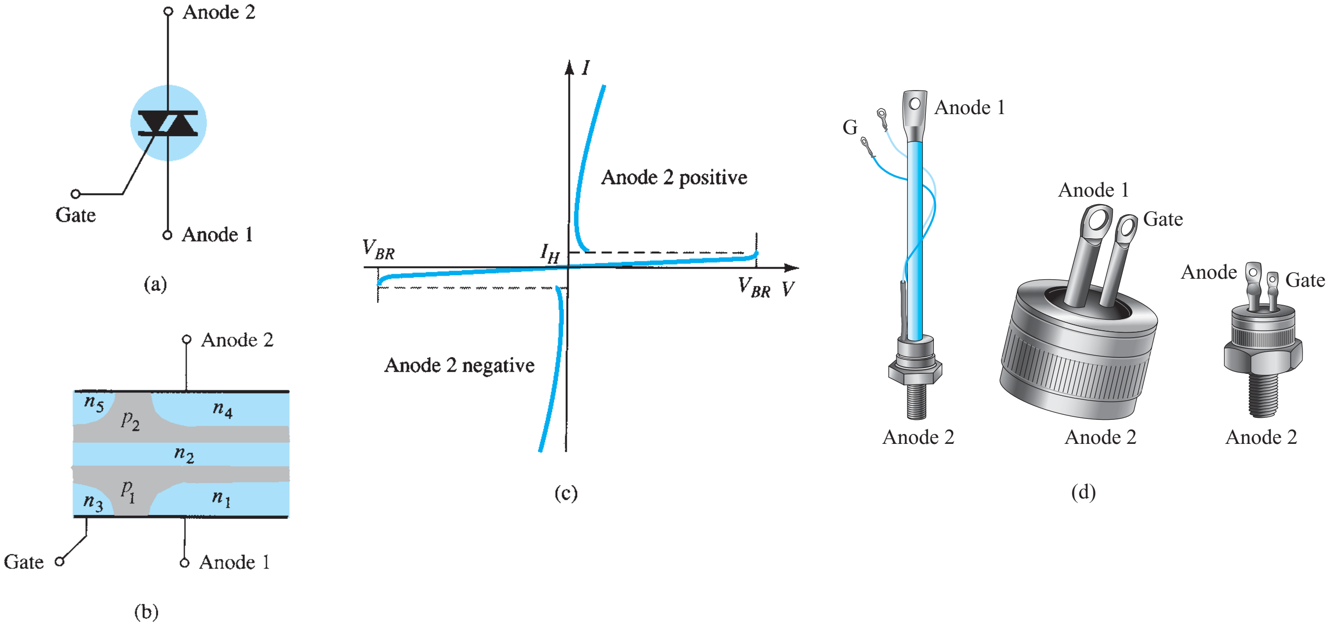

Anode 2
Gate
Anode 1
(a)
Anode 2
n_5
p_2
n_4
n_2
p_1
n_3
n_1
Gate
Anode 1
(b)
I
Anode 2 positive
V_{BR}
I_H
V_{BR} V
Anode 2 negative
(c)
G
Anode 1
Anode 1
Gate
Anode
Gate
Anode 2
Anode 2
Anode 2
(d)

FIG. 17.32

The triac: (a) symbol; (b) basic construction; (c) characteristics; (d) drawings.

The graphical symbol for the device and the distribution of the semiconductor layers are provided in Fig. 17.32 with photographs of the device. For each possible direction of conduction, there is a combination of semiconductor layers whose state will be controlled by the signal applied to the gate terminal.

Phase (Power) Control

One fundamental application of the triac is presented in Fig. 17.33. In this capacity, it is controlling the ac power to the load by switching on and off during the positive and negative regions of the input sinusoidal signal. The action of this circuit during the positive portion of the input signal is very similar to that encountered for the Shockley diode in Fig. 17.28. The advantage of this configuration is that during the negative portion of the input signal, the same type of response will result since both the diac and the triac can fire in the reverse direction. The resulting waveform for the current through the load is provided in Fig. 17.33. By varying the resistor R, one can control the conduction angle. There are units available that can handle in excess of 10-kW loads.

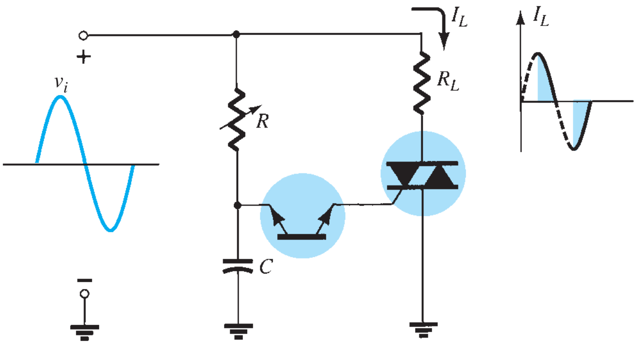


FIG. 17.33
Application of a triac: phase (power) control.

OTHER DEVICES

17.12 UNIJUNCTION TRANSISTOR

Recent interest in the unijunction transistor (UJT) has, like that for the SCR, been increasing at a remarkable rate. Although first introduced in 1948, the device did not become commercially available until 1952. The low cost per unit combined with the excellent characteristics of the device have warranted its use in a wide variety of applications, including oscillators, trigger circuits, sawtooth generators, phase control, timing circuits, bistable networks, and voltage- or current-regulated supplies. The fact that this device is, in general, a low-power-absorbing device under normal operating conditions is a tremendous aid in the continual effort to design relatively efficient systems.

The UJT is a three-terminal device having the basic construction shown in Fig. 17.34. A slab of lightly doped (increased resistance characteristic) n-type silicon material has two base

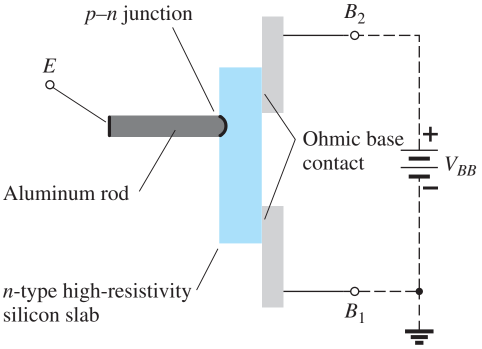


FIG. 17.34
Unijunction transistor (UJT): basic construction.

contacts attached to both ends of one surface and an aluminum rod alloyed to the opposite surface. The *p–n* junction of the device is formed at the boundary of the aluminum rod and the *n*-type silicon slab. The single *p–n* junction accounts for the terminology *unijunction*. It was originally called a duo (double) base diode due to the presence of two base contacts. Note in Fig. 17.34 that the aluminum rod is alloyed to the silicon slab at a point closer to the base 2 contact than the base 1 contact and that the base 2 terminal is made positive with respect to the base 1 terminal by V_{BB} volts. The effect of each will become evident in the paragraphs to follow.

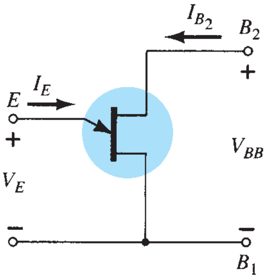
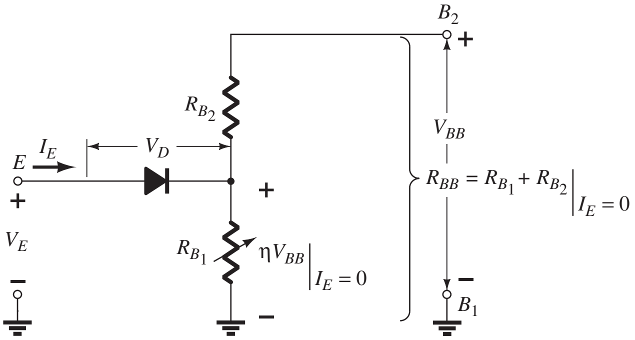


FIG. 17.35
Symbol and basic biasing arrangement for the unijunction transistor.

The symbol for the unijunction transistor is provided in Fig. 17.35. Note that the emitter leg is drawn at an angle to the vertical line representing the slab of *n*-type material. The arrowhead is pointing in the direction of conventional current (hole) flow when the device is in the forward-biased, active, or conducting state.

The circuit equivalent of the UJT is shown in Fig. 17.36. Note the relative simplicity of this equivalent circuit: two resistors (one fixed, one variable) and a single diode. The resistance R_{B_1} is shown as a variable resistor since its magnitude will vary with the current I_E. In fact, for a representative unijunction transistor, R_{B_1} may vary from 5 kΩ down to 50 Ω for a corresponding change of I_E from 0 μA to 50 μA. The interbase resistance R_{BB} is the resistance of the device between terminals B_1 and B_2 when $I_E = 0$. In equation form,

$$\boxed{R_{BB} = (R_{B_1} + R_{B_2})\big|_{I_E=0}} \tag{17.2}$$



B_2
+
R_{B_2}
V_{BB}
I_E
V_D
E
+
$R_{BB} = R_{B_1} + R_{B_2}\big|_{I_E=0}$
+
V_E
R_{B_1}
$\eta V_{BB}\big|_{I_E=0}$
–
–
–
B_1

FIG. 17.36
UJT equivalent circuit.

(R_{BB} is typically within the range of 4 kΩ to 10 kΩ.) The position of the aluminum rod of Fig. 17.34 will determine the relative values of R_{B_1} and R_{B_2} with $I_E = 0$. The magnitude of $V_{R_{B1}}$ (with $I_E = 0$) is determined by the voltage-divider rule in the following manner:

$$\boxed{V_{R_{B1}} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \cdot V_{BB} = \eta V_{BB}\Big|_{I_E=0}} \tag{17.3}$$

The Greek letter η (eta) denotes the *intrinsic stand-off* ratio of the device, which is defined by

$$\boxed{\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}\Big|_{I_E=0} = \frac{R_{B_1}}{R_{BB}}} \tag{17.4}$$

For applied emitter potentials V_E greater than $V_{R_{B1}}(= \eta V_{BB})$ by the forward voltage drop of the diode V_D (0.35 → 0.70 V), the diode will fire. Assume the short-circuit representation (on an ideal basis); I_E will begin to flow through R_{B_1}. In equation form, the emitter firing potential is given by

$$\boxed{V_P = \eta V_{BB} + V_D} \tag{17.5}$$

The characteristics of a representative unijunction transistor are shown for $V_{BB} = 10$ V in Fig. 17.37. Note that for emitter potentials to the left of the peak point, the magnitude of I_E is never greater than I_{EO} (measured in microamperes). The current I_{EO} corresponds very closely to the reverse leakage current I_{CO} of the conventional bipolar transistor. This region, as indicated in the figure, is called the cutoff region. Once conduction is established at $V_E = V_P$,

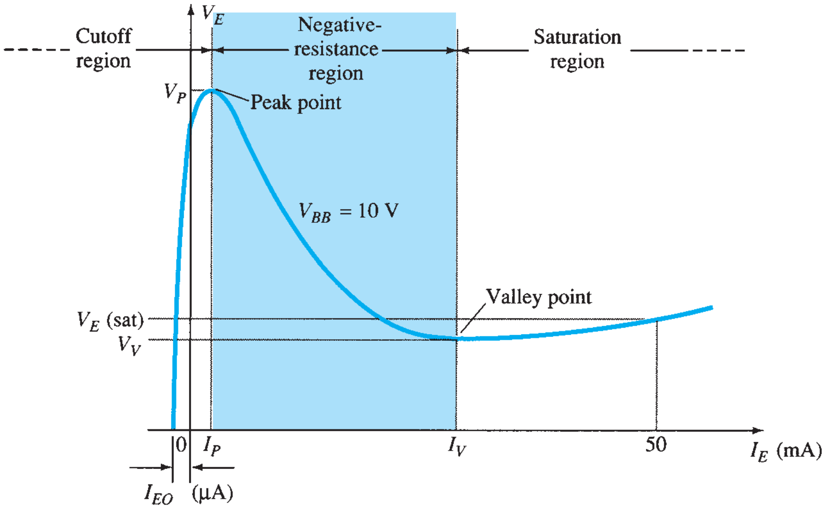


FIG. 17.37
UJT static emitter characteristic curve.

the emitter potential V_E will drop with increase in I_E. This corresponds exactly to the decreasing resistance R_{B_1} for increasing current I_E, as discussed earlier. This device, therefore, has a *negative-resistance* region that is stable enough to be used with a great deal of reliability in the areas of application listed earlier. Eventually, the valley point will be reached, and any further increase in I_E will place the device in the saturation region. In this region, the characteristics approach those of the semiconductor diode in the equivalent circuit of Fig. 17.36.

The decrease in resistance in the active region is due to the holes injected into the *n*-type slab from the aluminum *p*-type rod when conduction is established. The increased hole content in the *n*-type material will result in an increase in the number of free electrons in the slab, producing an increase in conductivity G and a corresponding drop in resistance $(R\downarrow = 1/G\uparrow)$. Three other important parameters for the unijunction transistor are I_P, V_V, and I_V. Each is indicated on Fig. 17.37. They are all self-explanatory.

The emitter characteristics as they normally appear are provided in Fig. 17.38. Note that I_{EO} (μA) is not in evidence since the horizontal scale is in milliamperes. The intersection

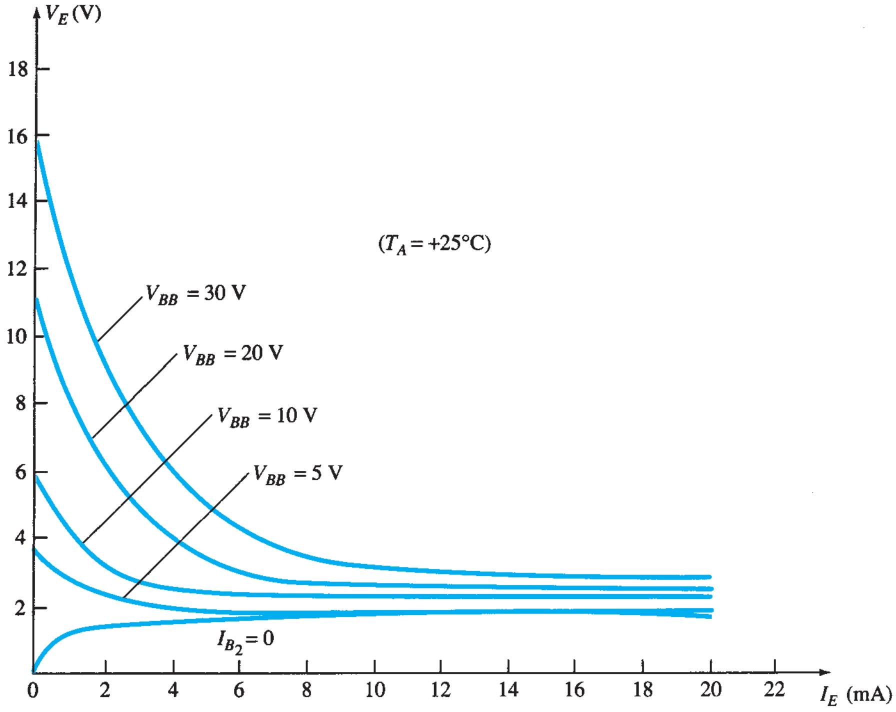
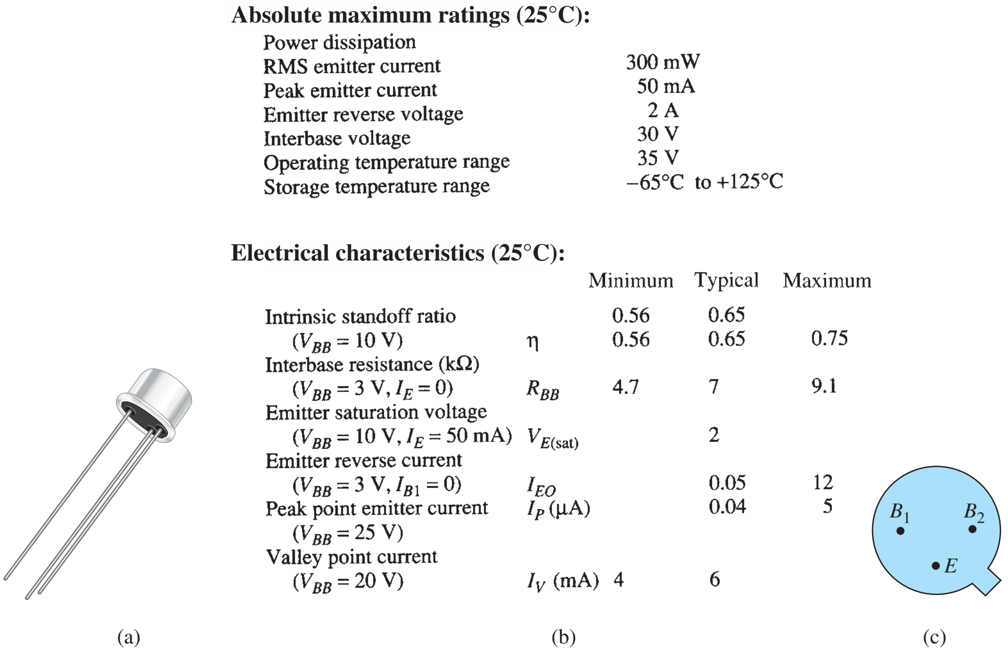


FIG. 17.38
Typical static emitter characteristic curves for a UJT.

of each curve with the vertical axis is the corresponding value of V_P. For fixed values of η and V_D, the magnitude of V_P will vary as V_{BB}, that is,

$$V_P \uparrow = \underbrace{\eta V_{BB}\uparrow + V_D}_{\text{fixed}}$$

A typical set of specifications for the UJT is provided in Fig. 17.39b. The discussion of the last few paragraphs should make each quantity readily recognizable. The terminal identification is provided in Fig. 17.39c and a photograph of a representative UJT in Fig. 17.39a. Note that the base terminals are opposite each other, whereas the emitter terminal is between the two. In addition, the base terminal to be tied to the higher potential is closer to the extension on the lip of the casing.



Absolute maximum ratings (25°C):

Power dissipation	300 mW
RMS emitter current	50 mA
Peak emitter current	2 A
Emitter reverse voltage	30 V
Interbase voltage	35 V
Operating temperature range	−65°C to +125°C
Storage temperature range	

Electrical characteristics (25°C):

		Minimum	Typical	Maximum
Intrinsic standoff ratio		0.56	0.65	
($V_{BB} = 10$ V)	η	0.56	0.65	0.75
Interbase resistance (kΩ)				
($V_{BB} = 3$ V, $I_E = 0$)	R_{BB}	4.7	7	9.1
Emitter saturation voltage				
($V_{BB} = 10$ V, $I_E = 50$ mA)	$V_{E(\text{sat})}$		2	
Emitter reverse current				
($V_{BB} = 3$ V, $I_{B1} = 0$)	I_{EO}		0.05	12
Peak point emitter current	I_P (μA)		0.04	5
($V_{BB} = 25$ V)				
Valley point current				
($V_{BB} = 20$ V)	I_V (mA)	4	6	

(a) (b) (c)

FIG. 17.39

UJT: (a) appearance; (b) specification sheet; (c) terminal identification.

SCR Triggering

One rather common application of the UJT is in the triggering of other devices such as the SCR. The basic elements of such a triggering circuit are shown in Fig. 17.40. The resistor R_1 must be chosen to ensure that the load line determined by R_1 passes through the device characteristics in the negative-resistance region, that is, to the right of the peak point but to the left of the valley point, as shown in Fig. 17.41. If the load line fails to pass to the right

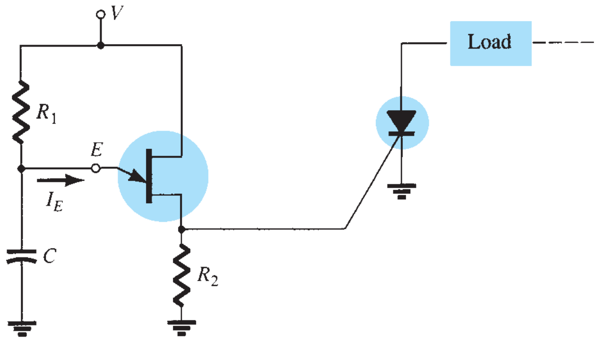


FIG. 17.40

UJT triggering of an SCR.

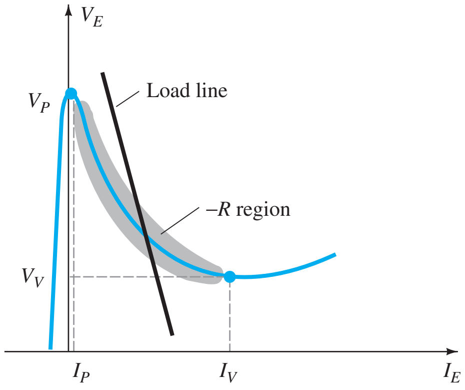


FIG. 17.41

Load line for a triggering application.

of the peak point, the device cannot turn on. An equation for R_1 that will ensure a turn-on condition can be established if we consider the peak point at which $I_{R_1} = I_P$ and $V_E = V_P$. (The equality $I_{R_1} = I_P$ is valid since the charging current of the capacitor at this instant is zero. That is, at this particular instant the capacitor is changing from a charging to a discharging state.) Then $V - I_{R_1}R_1 = V_E$ and $R_1 = (V - V_E)/I_{R_1} = (V - V_P)/I_P$ at the peak point. To ensure firing, the condition is

$$\boxed{R_1 < \frac{V - V_P}{I_P}} \tag{17.6}$$

At the valley point $I_E = I_V$ and $V_E = V_V$, so that

$$V - I_{R_1}R_1 = V_E$$

becomes

$$V - I_V R_1 = V_V$$

and

$$R_1 = \frac{V - V_V}{I_V}$$

or, to ensure turning off,

$$\boxed{R_1 > \frac{V - V_V}{I_V}} \tag{17.7}$$

The range of R_1 is therefore limited by

$$\boxed{\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P}} \tag{17.8}$$

The resistance R_2 must be chosen small enough to ensure that the SCR is not turned on by the voltage V_{R_2} of Fig. 17.42 when $I_E \cong 0$ A. The voltage V_{R_2} is then given by

$$\boxed{V_{R_2} \cong \left.\frac{R_2 V}{R_2 + R_{BB}}\right|_{I_E = 0\text{ A}}} \tag{17.9}$$

The capacitor C will determine, as we shall see, the time interval between triggering pulses and the time span of each pulse.

At the instant the dc supply voltage V is applied, the voltage $v_E = v_C$ will charge toward V volts from V_V as shown in Fig. 17.43 with a time constant $\tau = R_1C$.

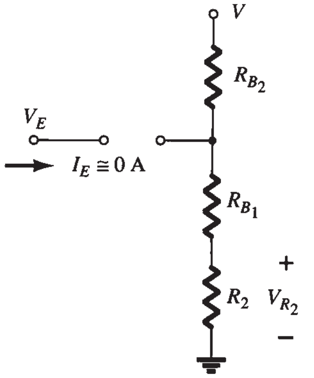


FIG. 17.42
Triggering network when $I_E \cong 0$ A.

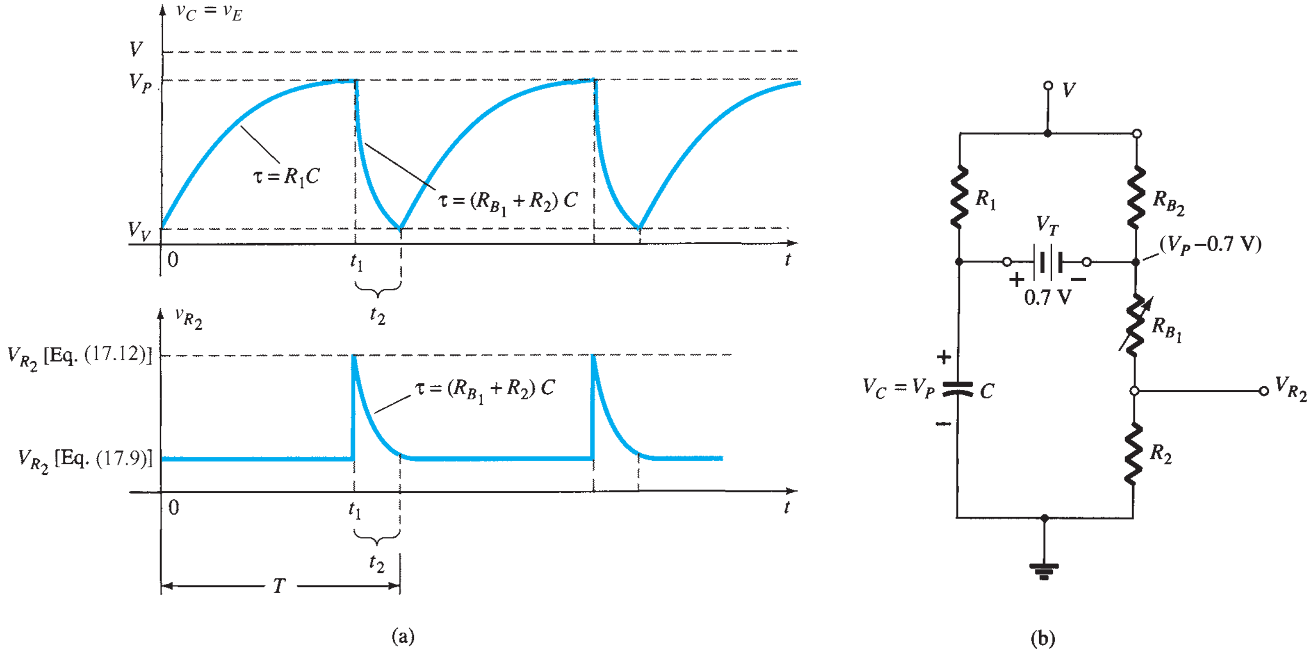


FIG. 17.43
(a) Charging and discharging phases for trigger network of Fig. 17.40; (b) equivalent network when UJT turns on.

The general equation for the charging period is

$$\boxed{v_C = V_V + (V - V_V)(1 - e^{-t/R_1C})} \qquad \textbf{(17.10)}$$

As noted in Fig. 17.43, the voltage across R_2 is determined by Eq. (17.9) during this charging period. When $v_C = v_E = V_P$, the UJT will enter the conduction state and the capacitor will discharge through R_{B_1} and R_2 at a rate determined by the time constant $\tau = (R_{B_1} + R_2)C$.

The discharge equation for the voltage $v_C = v_E$ is

$$\boxed{v_C \cong V_P e^{-t/(R_{B_1}+R_2)C}} \qquad \textbf{(17.11)}$$

Equation (17.11) is complicated somewhat by the fact that R_{B_1} will decrease with increasing emitter current and the other elements of the network, such as R_1 and V, will affect the discharge rate and final level. However, the equivalent network appears as shown in Fig. 17.43 and the magnitudes of R_1 and R_{B_2} are typically such that a Thévenin network for the network surrounding the capacitor C will be only slightly affected by these two resistors. Even though V is a reasonably high voltage, the voltage-divider contribution to the Thévenin voltage can be ignored on an approximate basis.

Using the reduced equivalent of Fig. 17.44 for the discharge phase results in the following approximation for the peak value of V_{R_2}:

$$\boxed{V_{R_2} \cong \frac{R_2(V_P - 0.7)}{R_2 + R_{B_1}}} \qquad \textbf{(17.12)}$$

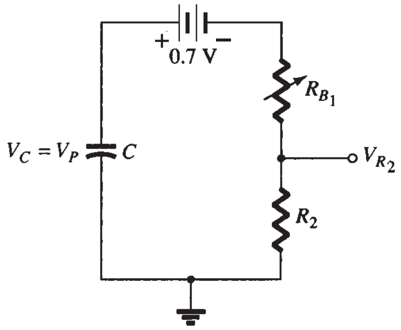


FIG. 17.44
Reduced equivalent network when UJT turns on.

The period t_1 of Fig. 17.43 can be determined in the following manner:

$$\begin{aligned} v_C\,(\text{charging}) &= V_V + (V - V_V)(1 - e^{-t/R_1C}) \\ &= V_V + V - V_V - (V - V_V)e^{-t/R_1C} \\ &= V - (V - V_V)e^{-t/R_1C} \end{aligned}$$

when $v_C = V_P$, $t = t_1$, and $V_P = V - (V - V_V)e^{-t_1/R_1C}$, or

$$\frac{V_P - V}{V - V_V} = -e^{-t_1/R_1C}$$

and

$$e^{-t_1/R_1C} = \frac{V - V_P}{V - V_V}$$

Using logs, we have

$$\log_e e^{-t_1/R_1C} = \log_e \frac{V - V_P}{V - V_V}$$

and

$$\frac{-t_1}{R_1C} = \log_e \frac{V - V_P}{V - V_P}$$

with

$$\boxed{t_1 = R_1C \log_e \frac{V - V_V}{V - V_P}} \qquad \textbf{(17.13)}$$

For the discharge period the time between t_1 and t_2 can be determined from Eq. (17.11) as follows:

$$v_C\,(\text{discharging}) = V_P\, e^{-t/(R_{B_1}+R_2)C}$$

Establishing t_1 as $t = 0$ gives us

$$v_C = V_V \qquad \text{at} \qquad t = t_2$$

and

$$V_V = V_P e^{-t_2/(R_{B_1}+R_2)C}$$

or

$$e^{-t_2/(R_{B_1}+R_2)C} = \frac{V_V}{V_P}$$

Using logs yields

$$\frac{-t_2}{(R_{B_1} + R_2)C} = \log_e \frac{V_V}{V_P}$$

and

$$\boxed{t_2 = (R_{B_1} + R_2)C \log_e \frac{V_P}{V_V}} \tag{17.14}$$

The period of time to complete one cycle is defined by T in Fig. 17.43. That is,

$$\boxed{T = t_1 + t_2} \tag{17.15}$$

Relaxation Oscillator

If the SCR were dropped from the configuration, the network would behave as a *relaxation oscillator*, generating the waveform of Fig. 17.43. The frequency of oscillation is determined by

$$\boxed{f_{\text{osc}} = \frac{1}{T}} \tag{17.16}$$

In many systems, $t_1 \gg t_2$, and

$$T \cong t_1 = R_1 C \log_e \frac{V - V_V}{V - V_P}$$

Since $V \gg V_V$ in many instances,

$$\begin{aligned} T \cong t_1 &= R_1 C \log_e \frac{V}{V - V_P} \\ &= R_1 C \log_e \frac{1}{1 - V_P/V} \end{aligned}$$

but $\eta = V_P/V$ if we ignore the effects of V_D in Eq. (17.5), and

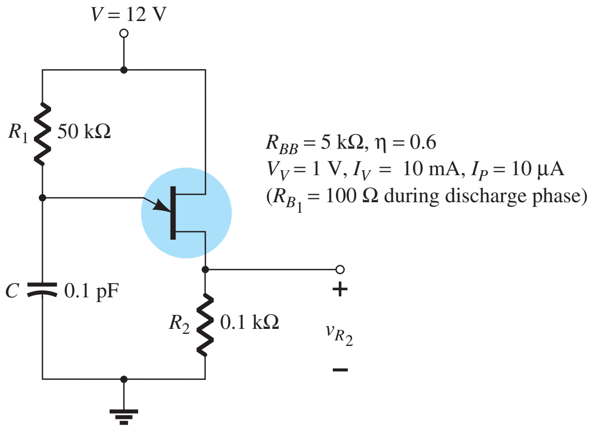
$$T \cong R_1 C \log_e \frac{1}{1 - \eta}$$

or

$$\boxed{f \cong \frac{1}{R_1 C \log_e [1/(1 - \eta)]}} \tag{17.17}$$

EXAMPLE 17.1 Given the relaxation oscillator of Fig. 17.45:

a. Determine R_{B_1} and R_{B_2} at $I_E = 0$ A.
b. Calculate V_P, the voltage necessary to turn on the UJT.



$V = 12$ V
R_1
50 kΩ
$R_{BB} = 5$ kΩ, $\eta = 0.6$
$V_V = 1$ V, $I_V = 10$ mA, $I_P = 10$ µA
($R_{B_1} = 100$ Ω during discharge phase)
C
0.1 pF
R_2
0.1 kΩ
+
v_{R_2}
−

FIG. 17.45
Example 17.1.

c. Determine whether R_1 is within the permissible range of values as determined by Eq. (17.8) to ensure firing of the UJT.
d. Determine the frequency of oscillation if $R_{B_1} = 100\ \Omega$ during the discharge phase.
e. Sketch the waveform of v_C for a full cycle.
f. Sketch the waveform of v_{R_2} for a full cycle.

Solution:

a.
$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$
$$0.6 = \frac{R_{B_1}}{R_{BB}}$$
$$R_{B_1} = 0.6R_{BB} = 0.6(5\text{ k}\Omega) = \mathbf{3\text{ k}\Omega}$$
$$R_{B_2} = R_{BB} - R_{B_1} = 5\text{ k}\Omega - 3\text{ k}\Omega = \mathbf{2\text{ k}\Omega}$$

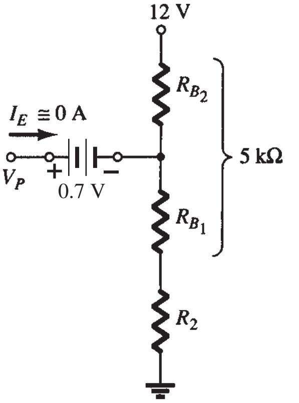


FIG. 17.46
Network for determining V_P, the voltage required to turn on the UJT.

b. At the point where $v_C = V_P$, if we continue with $I_E = 0$ A, the network of Fig. 17.46 results, where

$$V_P = 0.7\text{ V} + \frac{(R_{B_1} + R_2)12\text{ V}}{\underbrace{R_{B_1} + R_{B_2}}_{R_{BB}} + R_2}$$
$$= 0.7\text{ V} + \frac{(3\text{ k}\Omega + 0.1\text{ k}\Omega)12\text{ V}}{5\text{ k}\Omega + 0.1\text{ k}\Omega} = 0.7\text{ V} + 7.294\text{ V}$$
$$\cong \mathbf{8\text{ V}}$$

c.
$$\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P}$$
$$\frac{12\text{ V} - 1\text{ V}}{10\ m\text{A}} < R_1 < \frac{12\text{ V} - 8\text{ V}}{10\ \mu\text{A}}$$
$$1.1\text{ k}\Omega < R_1 < 400\text{ k}\Omega$$

The resistance $R_1 = 50\text{ k}\Omega$ falls within this range.

d.
$$t_1 = R_1C\log_e\frac{V - V_V}{V - V_P}$$
$$= (50\text{ k}\Omega)(0.1\text{ pF})\log_e\frac{12\text{ V} - 1\text{ V}}{12\text{ V} - 8\text{ V}}$$
$$= 5 \times 10^{-3}\log_e\frac{11}{4} = 5 \times 10^{-3}(1.01)$$
$$= 5.05\text{ ms}$$
$$t_2 = (R_{B_1} + R_2)C\log_e\frac{V_P}{V_V}$$
$$= (0.1\text{ k}\Omega + 0.1\text{ k}\Omega)(0.1\text{ pF})\log_e\frac{8}{1}$$
$$= (0.02 \times 10^{-6})(2.08)$$
$$= 41.6\ \mu\text{s}$$

and
$$T = t_1 + t_2 = 5.05\text{ ms} + 0.0416\text{ ms}$$
$$= 5.092\text{ ms}$$

with
$$f_{\text{osc}} = \frac{1}{T} = \frac{1}{5.092\text{ ms}} \cong \mathbf{196\text{ Hz}}$$

Using Eq. (17.17) gives

$$f \cong \frac{1}{R_1C\log_e[1/(1 - \eta)]}$$
$$= \frac{1}{5 \times 10^{-3}\log_e 2.5}$$
$$= \mathbf{218\text{ Hz}}$$

e. See Fig. 17.47.

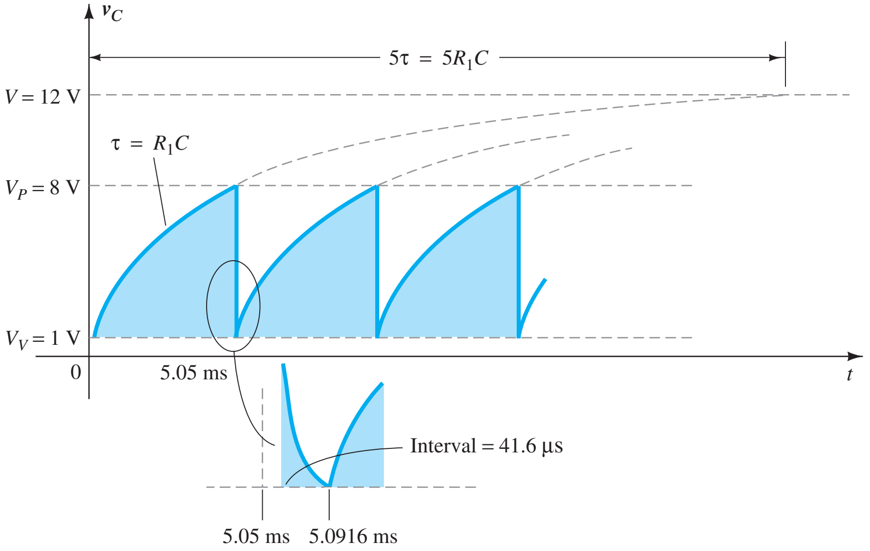


FIG. 17.47
The voltage v_C for the relaxation oscillator of Fig. 17.45.

f. During the charging phase, from (Eq. 17.9), we have

$$V_{R_2} = \frac{R_2V}{R_2 + R_{BB}} = \frac{0.1\text{ k}\Omega(12\ V)}{0.1\text{ k}\Omega + 5\text{ k}\Omega} = \mathbf{0.235\ V}$$

When $v_C = V_P$, from (Eq. 17.12), we have

$$V_{R_2} \cong \frac{R_2(V_P - 0.7\text{ V})}{R_2 + R_{B_1}} = \frac{0.1\text{ k}\Omega(8\text{ V} - 0.7\text{ V})}{0.1\text{ k}\Omega + 0.1\text{ k}\Omega}$$
$$= \mathbf{3.65\ V}$$

The plot of v_{R_2} appears in Fig. 17.48.

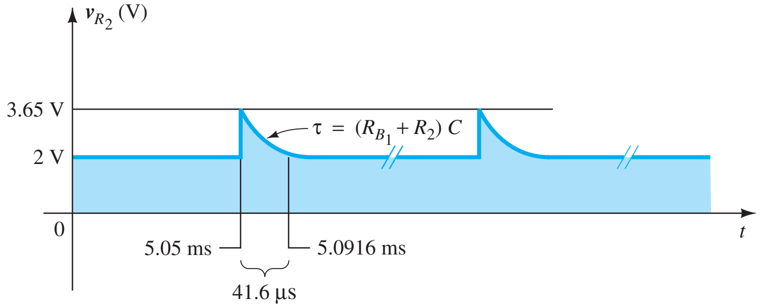


FIG. 17.48
The voltage v_{R_2} for the relaxation oscillator of Fig. 17.45.

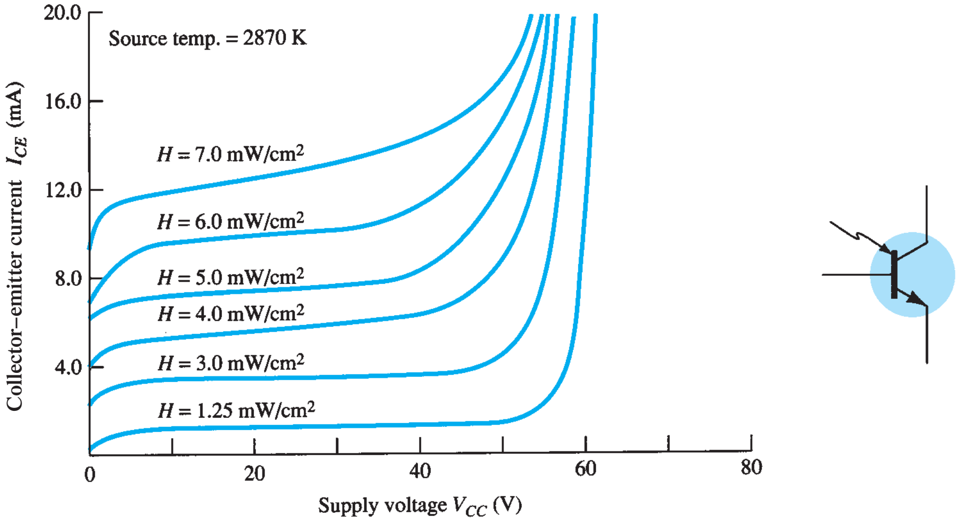
17.13 PHOTOTRANSISTORS

The fundamental behavior of photoelectric devices was introduced earlier with the description of the photodiode. This discussion will now be extended to include the phototransistor, which has a photosensitive collector–base *p–n* junction. The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I_λ for the photoinduced base current, the resulting collector current, on an approximate basis, is

$$\boxed{I_C \cong h_{fe} I_\lambda} \qquad \textbf{(17.18)}$$

A representative set of characteristics for a phototransistor is provided in Fig. 17.49 along with the symbolic representation of the device. Note the similarities between these curves and those of a typical bipolar transistor. As expected, an increase in light intensity corresponds to an increase in collector current. To provide a greater degree of familiarity with the light-intensity unit of measurement, milliwatts per square centimeter, we give a curve of base current versus flux density in Fig. 17.50a. Note the exponential increase in base current with increasing flux density. In the same figure, a sketch of the phototransistor is provided with the terminal identification and the angular alignment.

Some of the areas of application for the phototransistor include computer logic circuitry, lighting control (highways, etc.), level indication, relays, and counting systems.



(a) (b)

FIG. 17.49

Phototransistor: (a) collector characteristics; (b) symbol.

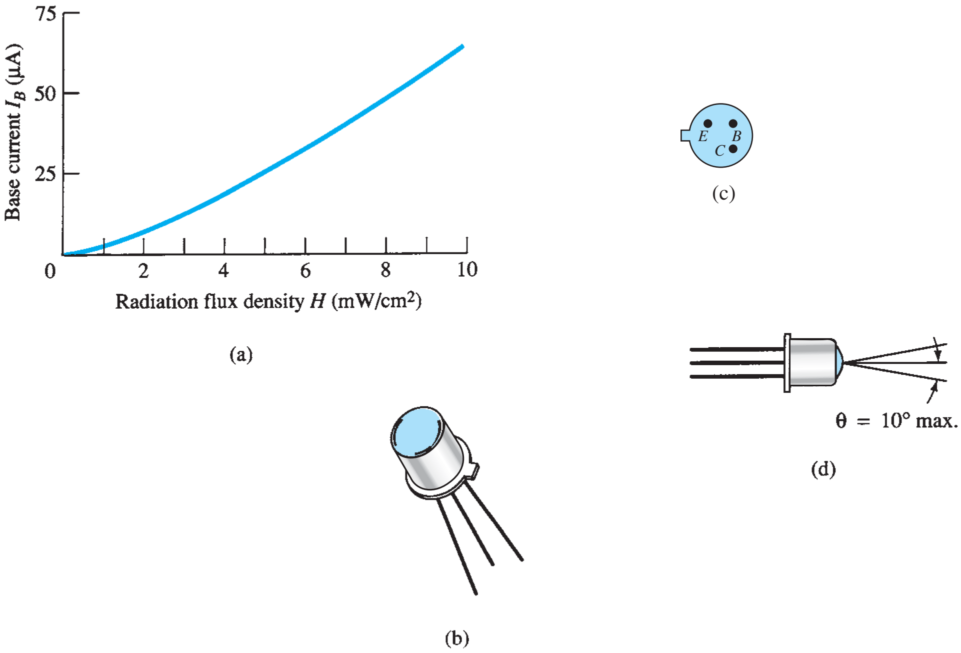


FIG. 17.50

Phototransistor: (a) base current versus flux density; (b) device; (c) terminal identification; (d) angular alignment.

High-Isolation AND Gate

A high-isolation AND gate is shown in Fig. 17.51 using three phototransistors and three LEDs (light-emitting diodes). The LEDs are semiconductor devices that emit light at an intensity determined by the forward current through the device. With the aid of discussions in Chapter 1, the circuit behavior should be relatively easy to understand. The terminology *high isolation* simply refers to the lack of an electrical connection between the input and output circuits.

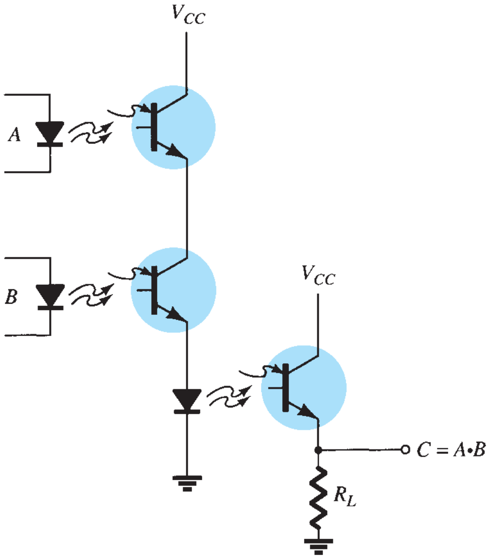
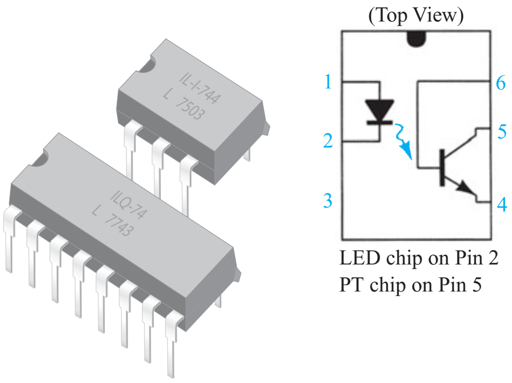


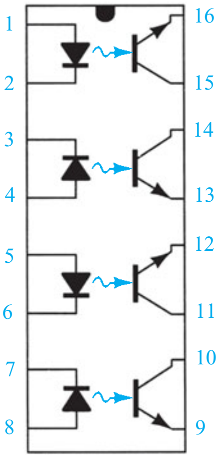
FIG. 17.51
High-isolation AND gate employing phototransistors and light-emitting diodes (LEDs).

17.14 OPTO-ISOLATORS

The *opto-isolator* is a device that incorporates many of the characteristics described in the preceding section. It is simply a package that contains both an infrared LED and a photodetector such as a silicon diode, transistor Darlington pair, or SCR. The wavelength response of each device is tailored to be as identical as possible to permit the highest measure of coupling possible. In Fig. 17.52, two possible chip configurations are provided,



Pin No.	*Function*
1	anode
2	cathode
3	nc
4	emitter
5	collector
6	base



Pin No.	*Function*
1	anode
2	cathode
3	cathode
4	anode
5	anode
6	cathode
7	cathode
8	anode
9	emitter
10	collector
11	collector
12	enitter
13	emitter
14	collector
15	collector
16	emitter

FIG. 17.52
Two Litronix opto-isolators.

with a drawing of each. There is a transparent insulating cap between each set of elements embedded in the structure (not visible) to permit the passage of light. They are designed with response times so small that they can be used to transmit data in the megahertz range.

The maximum ratings and electrical characteristics for the 6-pin model are provided in Fig. 17.53. Note that I_{CEO} is measured in nanoamperes and that the power dissipation of the LED and transistor are about the same.

Maximum Ratings

Gallium arsenide LED (each channel)	
Power dissipation @ 25°C	200 mW
Derate linearly from 25°C	2.6 mW/°C
Continuous forward current	150 mA
Detector silicon phototransistor (each channel)	
Power dissipation @ 25°C	200 mW
Derate linearly from 25°C	2.6 mW/°C
Collector-emitter breakdown voltage	30 V
Emitter-collector breakdown voltage	7 V
Collector-base breakdown voltage	70 V

Electrical Characteristics per Channel (at 25°C Ambient)

Parameter	*Min.*	*Typ.*	*Max.*	*Unit*	*Test Conditions*
Gallium arsenide LED					
Forward voltage		1.3	1.5	V	$I_F = 60$ mA
Reverse current		0.1	10	μA	$V_R = 3.0$ V
Capacitance		100		pF	$V_R = 0$ V
Phototransistor detector					
BV_{CEO}	30			V	$I_C = 1$ mA
I_{CEO}		5.0	50	nA	$V_{CE} = 10$ V, $I_F = 0$ A
Collector-emitter capacitance		2.0		pF	$V_{CE} = 0$ V
BV_{ECO}	7			V	$I_E = 100$ μA
Coupled characteristics					
dc current transfer ratio	0.2	0.35			$I_F = 10$ mA, $V_{CE} = 10$ V
Capacitance, input to output		0.5		pF	
Breakdown voltage	2500			V	DC
Resistance, input to output		100		GΩ	
V_{sat}			0.5	V	$I_C = 1.6$ mA, $I_F = 16$ mA
Propagation delay					
$t_{D\text{ on}}$		6.0		μs	$R_L = 2.4$ kΩ, $V_{CE} = 5$ V
$t_{D\text{ off}}$		25		μs	$I_F = 16$ mA

FIG. 17.53
Opto-isolator characteristics.

The typical optoelectronic characteristic curves for each channel are provided in Figs. 17.54 through 17.58. Note the very pronounced effect of temperature on the output current at low temperatures but the fairly level response at or above room temperature (25°C). As mentioned earlier, the level of I_{CEO} is improving steadily with improved design and construction techniques (the lower the better). In Fig. 17.54, we do not reach 1 μA until the temperature rises above 75°C. The transfer characteristics of Fig. 17.55 compare the input LED current (which establishes the luminous flux) to the resulting collector current of the output transistor (whose base current is determined by the incident flux). In fact, Fig. 17.56 demonstrates that the V_{CE} voltage affects the resulting collector current only very slightly. It is interesting to note in Fig. 17.57 that the switching time of an opto-isolator decreases with increased current, whereas for many devices it is exactly the reverse. Consider that it is only 2 μs for a collector current of 6 mA and a load R_L of 100 Ω. The relative output versus temperature appears in Fig. 17.58.

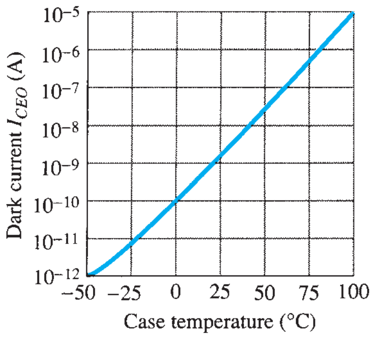


FIG. 17.54
Dark current I_{CEO} versus temperature.

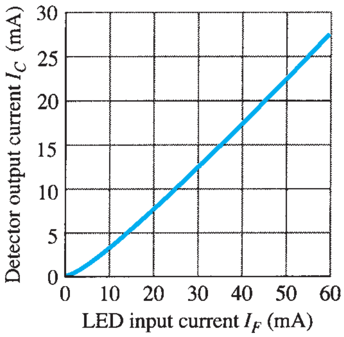


FIG. 17.55
Transfer characteristics.

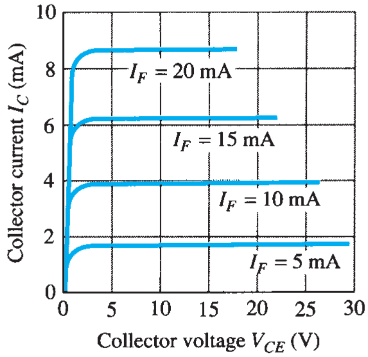


FIG. 17.56
Detector output characteristics.

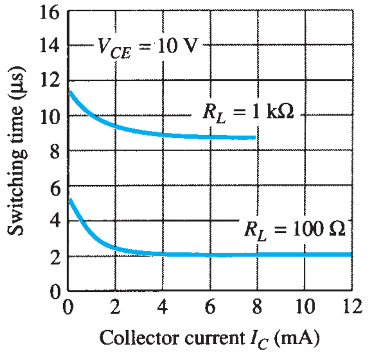


FIG. 17.57
Switching time versus collector current.

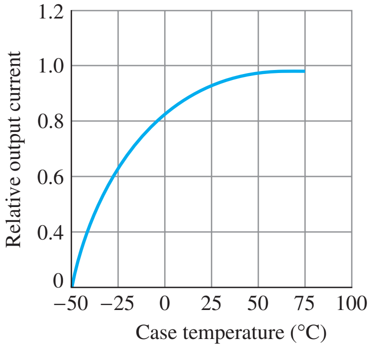


FIG. 17.58
Relative output versus temperature.

The schematic representation for a transistor coupler appears in Fig. 17.52. The schematic representations for a photodiode, a photo-Darlington, and a photo-SCR opto-isolator appear in Fig. 17.59.

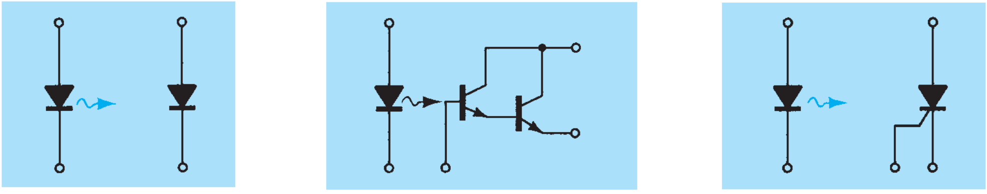

(a) (b) (c)

FIG. 17.59
Opto-isolators: (a) photodiode; (b) photo-Darlington; (c) photo-SCR.

17.15 PROGRAMMABLE UNIJUNCTION TRANSISTOR

Although there is a similarity in name, the actual construction and mode of operation of the programmable unijunction transistor (PUT) are quite different from those of the unijunction transistor. The fact that the *I–V* characteristics and applications of each are similar prompted the choice of labels.

As indicated in Fig. 17.60, the PUT is a four-layer *pnpn* device with a gate connected directly to the sandwiched *n*-type layer. The symbol for the device and the basic biasing arrangement appear in Fig. 17.61. As the symbol suggests, it is essentially an SCR with

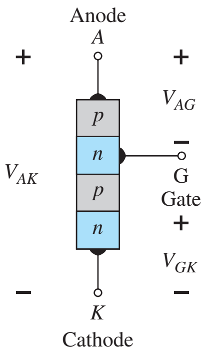


FIG. 17.60
Programmable UJT (PUT).

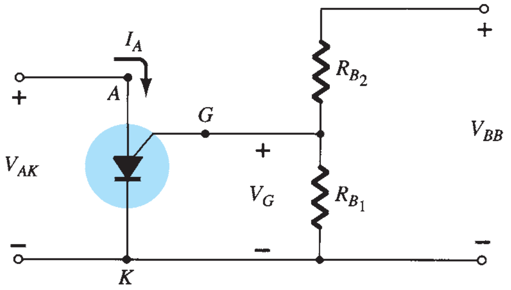


FIG. 17.61

Basic biasing arrangement for the PUT.

a control mechanism that permits a duplication of the characteristics of the typical SCR. The term *programmable* is applied because R_{BB}, η, and V_P as defined for the UJT can be controlled through the resistors R_{B_1}, R_{B_2}, and the supply voltage V_{BB}. Note in Fig. 17.61 that through an application of the voltage-divider rule, when $I_G = 0$,

$$\boxed{V_G = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} V_{BB} = \eta V_{BB}} \tag{17.19}$$

where
$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

as defined for the UJT.

The characteristics of the device appear in Fig. 17.62. As noted on the diagram, the "off" state (I low, V between 0 and V_P) and the "on" state ($I \geq I_V$, $V \geq V_V$) are separated by the unstable region as occurred for the UJT. That is, the device cannot stay in the unstable state—it will simply shift to either the "off" or the "on" stable state.

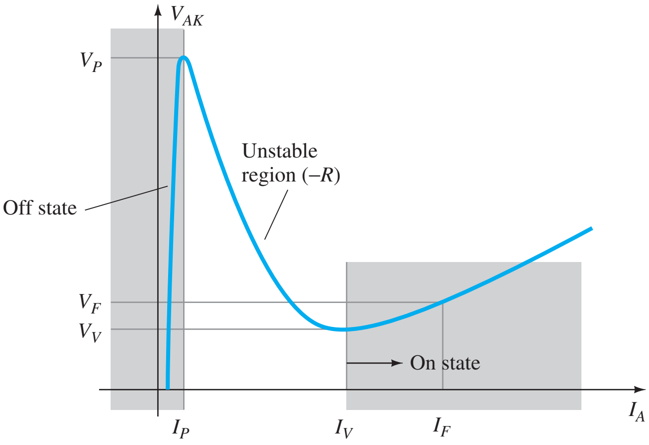


FIG. 17.62

PUT characteristics.

The firing potential V_P, or voltage necessary to "fire" the device, is given by

$$\boxed{V_P = \eta V_{BB} + V_D} \tag{17.20}$$

as defined for the UJT. However, V_P represents the voltage drop V_{AK} in Fig. 17.60 (the forward voltage drop across the conducting diode). For silicon, V_D is typically 0.7 V. Therefore,

$$V_{AK} = V_{AG} + V_{GK}$$
$$V_P = V_D + V_G$$

and
$$\boxed{V_P = \eta V_{BB} + 0.7\text{ V}} \quad \text{silicon} \tag{17.21}$$

We noted above, however, that $V_G = \eta V_{BB}$, with the result that

$$\boxed{V_P = V_G + 0.7} \quad \text{silicon} \tag{17.22}$$

Recall that for the UJT, R_{B_1} and R_{B_2} represent the bulk resistance and the ohmic base contacts of the device—both inaccessible. In the development above, we note that R_{B_1} and R_{B_2} are external to the device, permitting an adjustment of η and hence V_G above. In other words, the PUT provides a measure of control on the level of V_P required to turn on the device.

Although the characteristics of the PUT and UJT are similar, the peak and valley currents of the PUT are typically lower than those of a similarly rated UJT. In addition, the minimum operating voltage is also less for a PUT.

If we take a Thévenin equivalent of the network to the right of the gate terminal in Fig. 17.61, the network of Fig. 17.63 results. The resulting resistance R_S is important because it is often included in specification sheets since it affects the level of I_V.

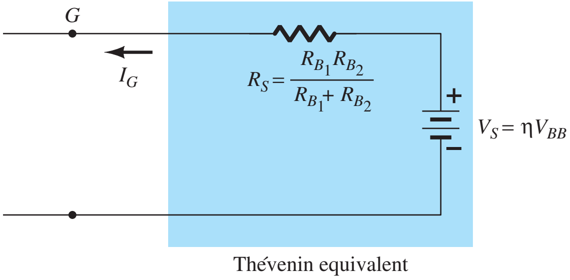


FIG. 17.63
Thévenin equivalent for the network to the right of the gate terminal in Fig. 17.61.

The basic operation of the device can be reviewed through reference to Fig. 17.62. A device in the "off" state will not change state until the voltage V_P as defined by V_G and V_D is reached. The level of current until I_P is reached is very low, resulting in an open-circuit equivalent since $R = V(\text{high})/I(\text{low})$ will result in a high resistance level. When V_P is reached, the device will switch through the unstable region to the "on" state, where the voltage is lower but the current higher, resulting in a terminal resistance $R = V(\text{low})/I(\text{high})$, which is quite small, representing a short-circuit equivalent on an approximate basis. The device has therefore switched from essentially an open-circuit to a short-circuit state at a point determined by the choice of R_{B_1}, R_{B_2}, and V_{BB}. Once the device is in the "on" state, the removal of V_G will not turn the device off. The level of voltage V_{AK} must be dropped sufficiently to reduce the current below a holding level.

EXAMPLE 17.2 Determine R_{B_1} and V_{BB} for a silicon PUT if it is determined that $\eta = 0.8$, $V_P = 10.3$ V, and $R_{B_2} = 5\text{ k}\Omega$.

Solution:

$$\begin{aligned}
\text{Eq. (17.4):}\quad \eta &= \frac{R_{B_2}}{R_{B_1} + R_{B_2}} = 0.8 \\
R_{B_1} &= 0.8(R_{B_1} + R_{B_2}) \\
0.2R_{B_1} &= 0.8R_{B_2} \\
R_{B_1} &= 4R_{B_2} \\
R_{B_1} &= 4(5\text{ k}\Omega) = \mathbf{20\text{ k}\Omega} \\
\text{Eq. (17.20):}\quad V_P &= \eta V_{BB} + V_D \\
10.3\text{ V} &= (0.8)(V_{BB}) + 0.7\text{ V} \\
9.6\text{ V} &= 0.8V_{BB} \\
V_{BB} &= \mathbf{12\text{ V}}
\end{aligned}$$

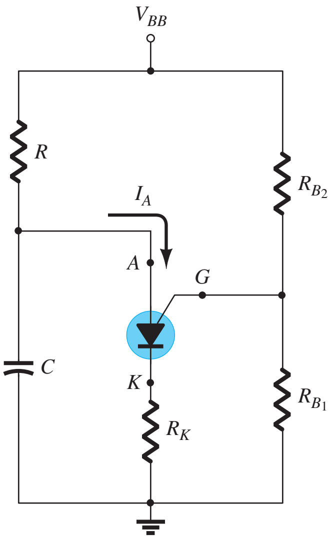


FIG. 17.64

PUT relaxation oscillator.

Relaxation Oscillator

One popular application of the PUT is in the relaxation oscillator of Fig. 17.64. The instant the supply is connected, the capacitor will begin to charge toward V_{BB} volts since there is no anode current at this point. The charging curve appears in Fig. 17.65. The period T required to reach the firing potential V_P is given approximately by

$$\boxed{T \cong RC \log_e \frac{V_{BB}}{V_{BB} - V_P}} \tag{17.23}$$

or, when $V_P \cong \eta V_{BB}$,

$$\boxed{T \cong RC \log_e \left(1 + \frac{R_{B_1}}{R_{B_2}}\right)} \tag{17.24}$$

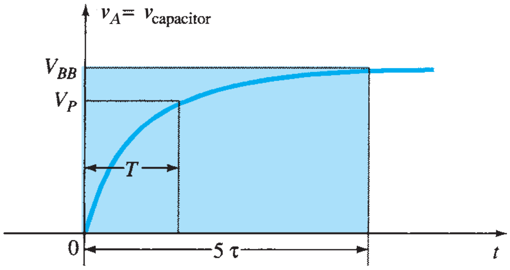


FIG. 17.65

Charging wave for the capacitor C of Fig. 17.64.

The instant the voltage across the capacitor equals V_P, the device will fire and a current $I_A = I_P$ will be established through the PUT. If R is too large, the current I_P cannot be established and the device will not fire. At the point of transition,

$$I_P R = V_{BB} - V_P$$

and

$$\boxed{R_{\max} = \frac{V_{BB} - V_P}{I_P}} \tag{17.25}$$

The subscript is included to indicate that any R greater than $R_{\max}$ will result in a current less than I_P. The level of R must also be such as to ensure it is less than I_V if oscillations are to occur. In other words, we want the device to enter the unstable region and then return to the "off" state. From reasoning similar to that above, we obtain

$$\boxed{R_{\min} = \frac{V_{BB} - V_V}{I_V}} \tag{17.26}$$

The discussion above requires that R be limited to the following for an oscillatory system:

$$R_{\min} < R < R_{\max}$$

The waveforms of v_A, v_G, and v_K appear in Fig. 17.66. Note that T determines the maximum voltage that v_A can charge to. Once the device fires, the capacitor will rapidly discharge through the PUT and R_K, producing the drop shown. Of course, v_K will peak at the same time due to the brief but heavy current. The voltage v_G will rapidly drop from V_G to a level just greater than 0 V. When the capacitor voltage drops to a low level, the PUT will once again turn off and the charging cycle will be repeated. The effect on V_G and V_K is shown in Fig. 17.66.

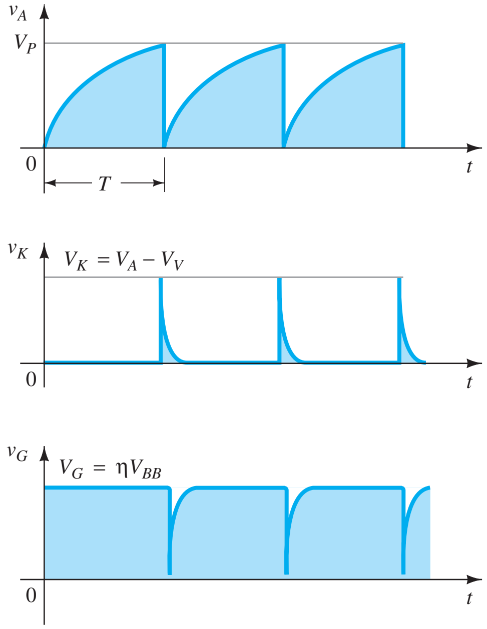


FIG. 17.66
Waveforms for PUT oscillator of Fig. 17.64.

EXAMPLE 17.3 For the network of Fig. 17.64, if $V_{BB} = 12\text{ V}$, $R = 20\text{ k}\Omega$, $C = 1\ \mu\text{F}$, $R_K = 100\ \Omega$, $R_{B_1} = 10\text{ k}\Omega$, $R_{B_2} = 5\text{ k}\Omega$, $I_P = 100\ \mu\text{A}$, $V_V = 1\text{ V}$, and $I_V = 5.5\text{ mA}$, determine:

a. V_P.
b. R_{max} and R_{min}.
c. T and frequency of oscillation.
d. The waveforms of v_A, v_G, and v_K.

Solution:

a. Eq. (17.20): $$V_P = \eta V_{BB} + V_D$$

$$= \frac{R_{B_1}}{R_{B_1} + R_{B_2}} V_{BB} + 0.7\text{ V}$$

$$= \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 5\text{ k}\Omega}(12\text{ V}) + 0.7\text{ V}$$

$$= (0.67)(12\text{ V}) + 0.7\text{ V} = \mathbf{8.7\ V}$$

b. From Eq. (17.25): $$R_{\text{max}} = \frac{V_{BB} - V_P}{I_P}$$

$$= \frac{12\text{ V} - 8.7\text{ V}}{100\ \mu\text{A}} = \mathbf{33\ k\Omega}$$

From Eq. (17.26): $$R_{\text{min}} = \frac{V_{BB} - V_V}{I_V}$$

$$= \frac{12\text{ V} - 1\text{ V}}{5.5\text{ mA}} = \mathbf{2\ k\Omega}$$

$$R\text{:}\quad 2\text{ k}\Omega < 20\text{ k}\Omega < 33\text{ k}\Omega$$

c. Eq. (17.23): $$T = RC \log_e \frac{V_{BB}}{V_{BB} - V_P}$$

$$= (20\text{ k}\Omega)(1\ \mu\text{F}) \log_e \frac{12\text{ V}}{12\text{ V} - 8.7\text{ V}}$$

$$= 20 \times 10^{-3} \log_e (3.64)$$

$$= 20 \times 10^{-3}(1.29)$$
$$= \mathbf{25.8\ ms}$$
$$f = \frac{1}{T} = \frac{1}{25.8\ \text{ms}} = \mathbf{38.8\ Hz}$$

d. Indicated in Fig. 17.67.

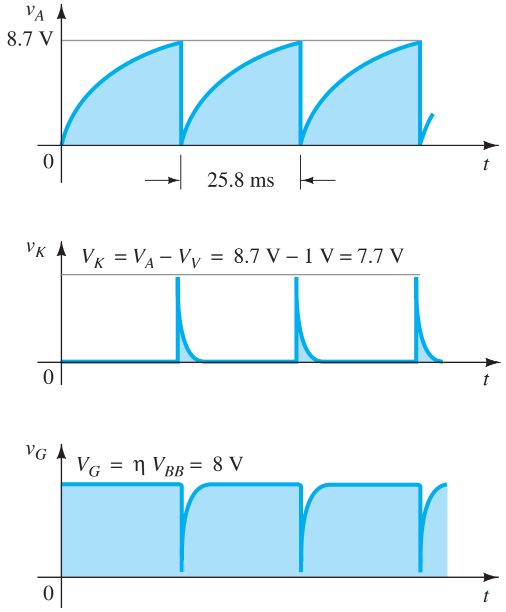


FIG. 17.67
Waveforms for the oscillator of Example 17.3.

17.16 SUMMARY

Important Conclusions and Concepts

1. The **silicon-controlled rectifier** (SCR) is a rectifier whose state **is controlled by the magnitude of the gate current**. The forward-bias voltage across the device will determine the level of gate current required to “fire” (turn on) the device. The **higher** the level of biasing voltage, the **less** is the required gate current.
2. In addition to gate triggering, an SCR can be **turned on with zero gate current** simply by applying **sufficient voltage** across the device. The higher the gate current, however, the less is the required biasing voltage to turn the SCR on.
3. The **silicon-controlled switch** has both **an anode gate and a cathode gate** for controlling the state of the device, although the anode gate is now connected to an *n*-type layer and the cathode gate to a *p*-type layer. The result is that **a negative pulse at the anode gate will turn the device on**, **whereas a positive pulse will turn it off**. The reverse is true for the cathode gate.
4. A **gate turn-off switch** (GTO) looks similar in construction to the SCR with only **one gate connection**, but the GTO has the added advantage of being able to turn the device **off and on** at the gate terminal. However, this added option of being able to turn the device off at the gate results in a much **higher gate current** to turn the device on.
5. The **LASCR** is a light-activated SCR whose state can be controlled by **light falling on a semiconductor layer** of the device **or by triggering the gate terminal** in a manner described for SCRs. The higher the junction temperature of the device, the less is the required incident light to turn the device on.
6. The **Shockley diode** has essentially the **same characteristics as an SCR with zero gate current**. It is turned on by simply increasing the forward-bias voltage across the device beyond the breakover level.

7. The **diac** is essentially a **Shockley diode that can fire in either direction**. The application of sufficient voltage of either polarity will turn the device on.
8. The **triac** is fundamentally a **diac with a gate terminal to control the action of the device** in either direction.
9. The **unijunction transistor** is a three-terminal device with a *p–n* junction formed between an aluminum rod and an *n*-type silicon slab. Once the emitter firing potential is reached, the emitter voltage will drop with an increase in emitter current, establishing a **negative-resistance region** excellent for oscillator applications. Once the valley point is reached, the characteristics of the device **take on those of a semiconductor diode**. The higher the applied voltage across the device, the higher is the emitter firing potential.
10. The **phototransistor** is a three-terminal device having characteristics **very similar to those of a BJT** with a base and collector current sensitive to the incident light intensity. The base current that results is essentially **linearly related to the applied light** with a level almost independent of the voltage across the device until breakdown results.
11. **Opto-isolators** contain an **infrared LED** and a **photodetector** to provide a linkage between systems that does not require a direct connection. The output detector current **is less than but linearly related to the applied input LED current**. Furthermore, the collector current is essentially independent of the collector-to-emitter voltage.
12. The **PUT** (programmable unijunction transistor) is, as the name implies, a device with the **characteristics of a UJT** but with the added capability of **being able to control the firing potential**. In general, the peak, valley, and minimum operating voltages of PUTs are less than those of UJTs.

Equations

Diac:

$$V_{BR_1} = V_{BR_2} \pm 0.1V_{BR_2}$$

UJT:

$$R_{BB} = (R_{B_1} + R_{B_2})\big|_{I_E=0}$$

$$V_{R_{B_1}} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \cdot V_{BB} = \eta V_{BB}\bigg|_{I_E=0}$$

$$\eta = \frac{R_{B_1}}{R_{BB}}$$

$$V_P = \eta V_{BB} + V_D$$

Phototransistor:

$$I_C \cong h_{fe} I_\lambda$$

PUT:

$$V_G = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \cdot V_{BB} = \eta V_{BB}$$

$$V_P = \eta V_{BB} + V_D$$

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

17.3 Basic Silicon-Controlled Rectifier Operation

1. Describe in your own words the basic behavior of the SCR using the two-transistor equivalent circuit.

2. Describe two techniques for turning an SCR off.

3. Consult a manufacturer's manual or specification sheet and obtain a turn-off network. If possible, describe the turn-off action of the design.

17.4 SCR Characteristics and Ratings

***4. a.** At high levels of gate current, the characteristics of an SCR approach those of what two-terminal device?

b. At a fixed anode-to-cathode voltage less than $V_{(BR)F^*}$, what is the effect on the firing of the SCR as the gate current is reduced from its maximum value to the zero level?

c. At a fixed gate current greater than $I_G = 0$, what is the effect on the firing of the SCR as the gate voltage is reduced from $V_{(BR)F^*}$?

d. For increasing levels of I_G, what is the effect on the holding current?

5. a. Based on Fig. 17.8, will a gate current of 50 mA fire the device at room temperature (25°C)?

b. Repeat part (a) for a gate current of 10 mA.

c. Will a gate voltage of 2.6 V trigger the device at room temperature?

d. Is $V_G = 6\text{ V}, I_G = 800\text{ mA}$ a good choice for firing conditions? Would $V_G = 4\text{ V}$, $I_G = 1.6\text{ A}$ be preferred? Explain.

17.5 SCR Applications

6. In Fig. 17.10b, why is there very little loss in potential across the SCR during conduction?

7. Fully explain why reduced values of R_1 in Fig. 17.11 will result in an increased angle of conduction.

***8.** Refer to the charging network of Fig. 17.12.

a. Determine the dc level of the full-wave rectified signal if a 1:1 transformer is employed.

b. If the battery in its uncharged state is sitting at 11 V, what is the anode-to-cathode voltage drop across SCR_1?

c. What is the maximum possible value of V_R ($V_{GK} \cong 0.7\text{ V}$)?

d. At the maximum value of part (c), what is the gate potential of SCR_2?

e. Once SCR_2 has entered the short-circuit state, what is the level of V_2?

9. Refer to the temperature controller of Fig. 17.13.

a. Sketch the waveform of the full-wave rectified waveform across the SCR.

b. What is the peak current through the heater when the SCR is "on" and has a short-circuit equivalent between anode and cathode? Assume each diode has a drop of 0.7 V when conducting.

c. When the SCR is on, what is the maximum current through the thermostat?

d. What is the total time for the rise time of the positive pulse of the applied ac voltage from 0 V to the maximum voltage of the rectified signal?

e. What is the time constant of the capacitor that is charging during the same period of part (d)? How do they compare? Why is this a concern?

f. What is the state of the SCR during this charging period? Why?

g. If the gate-firing potential is 40 V, what is the time period between successive triggering of the SCR?

h. Once the thermostat reaches its set temperature and assumes the short-circuit state, how will the SCR react?

i. What method was used to turn the SCR off: anode current interruption or forced commutation?

10. Refer to the emergency-lighting system of Fig. 17.14.

a. Sketch the waveform of the full-wave rectified signal across the bulb using a drop of 0.7 V during conduction of each diode.

b. Determine the peak voltage across the capacitor C_1 when the SCR_1 is off.

c. What is the peak voltage across R_1 during the charging phase if the battery voltage drops to 5 V?

d. What is the voltage across the lamp when the SCR turns on and the battery is fully charged at 6 V?

e. What is the current drawn from the battery if the lamp is dissipating 2 W of power?

17.6 Silicon-Controlled Switch

11. Fully describe in your own words the behavior of the networks of Fig. 17.16.

12. What is the suggested turn-off procedure for the network of Fig. 17.18?

13. For the network of Fig. 17.19

a. Write an equation for the voltage from gate to ground for the SCR.

b. What is the voltage V_{GK} when $R_S = R'$?

c. Find R_S to establish a turn-on voltage of 2 V if $R' = 10\text{ k}\Omega$.

d. When the alarm turns on, what is the current through the relay?

e. At $V_A = 0\text{ V}$, the maximum dc current through the rate-effect resistor will be established. What is its value?

f. When the reset button is activated, is there any reason for concern about spikes in voltage anywhere in the network? How could they be suppressed?

17.7 Gate Turn-Off Switch

14. a. In Fig. 17.22, if $V_Z = 50\text{ V}$, determine the maximum possible value the capacitor C_1 can charge to ($V_{GK} \cong 0.7\text{ V}$).

b. Determine the approximate discharge time (5τ) for $R_3 = 20\ \text{k}\Omega$.
c. Determine the internal resistance of the GTO if the rise time is one-half the decay period determined in part (b).

17.8 Light-Activated SCR

15. a. Using Fig. 17.24b, determine the minimum irradiance required to fire the device at room temperature (25°C).
b. What percentage reduction in irradiance is allowable if the junction temperature is increased from 0°C (32°F) to 100°C (212°F)?

17.9 Shockley Diode

16. For the network of Fig. 17.28, if $V_{BR} = 6\ \text{V}$, $\text{V} = 40\ \text{V}$, $R = 10\ \text{k}\Omega$, $C = 0.2\ \mu\text{F}$, and V_{GK} (firing potential) $= 3\ \text{V}$, determine the time period between energizing the network and the turning on of the SCR.

17.10 Diac

17. Using whatever reference you require, find an application of a diac and explain the network behavior.

18. If V_{BR_2} is 6.4 V, determine the range for V_{BR_1} using Eq. (17.1).

19. Find the level of human body capacitance C_b that would result in a 45-degree phase shift between v_i and v_G for the network of Fig. 17.30.

17.11 Triac

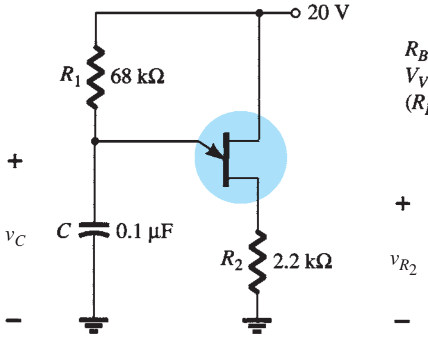
20. For the network of Fig. 17.33, if $C = 1\ \mu\text{F}$, find the level of R that will result in a 50% conduction period for the load in either direction if the turn-on voltage for the diac in either direction is 12 V and the applied sinusoidal signal has a peak value of 170 V ($= 1.414 \times 120$ V) at 60 Hz.

17.12 Unijunction Transistor

21. For the network of Fig. 17.40, in which $V = 40\ \text{V}$, $\eta = 0.6$, $V_V = 1\ \text{V}$, $I_V = 8\ \text{mA}$, and $I_P = 10\ \mu\text{A}$, determine the range of R_1 for the triggering network.

22. For a unijunction transistor with $V_{BB} = 20\ \text{V}$, $\eta = 0.65$, $R_{B_1} = 2\ \text{k}\Omega$ ($I_E = 0$), and $V_D = 0.7\ \text{V}$, determine:
a. R_{B_2}.
b. R_{BB}.
c. $V_{R_{B_1}}$.
d. V_P.

***23.** Given the relaxation oscillator of Fig. 17.68:
a. Find R_{B_1} and R_{B_2} at $I_E = 0\ \text{A}$.
b. Determine V_P, the voltage necessary to turn on the UJT.
c. Determine whether R_1 is within the permissible range of values defined by Eq. (17.8).
d. Determine the frequency of oscillation if $R_{B_1} = 200\ \Omega$ during the discharge phase.
e. Sketch the waveform of v_C for two full cycles.
f. Sketch the waveform of v_{R_2} for two full cycles.
g. Determine the frequency using Eq. (17.17) and compare to the value determined in part (d). Account for any major differences.



$R_{BB} = 10\ \text{k}\Omega$, $\eta = 0.55$
$V_V = 1.2\ \text{V}$, $I_V = 5\ \text{mA}$, $I_P = 50\ \mu\text{A}$
($R_{B_1} = 200\ \Omega$ during discharge phase)

FIG. 17.68
Problem 23.

17.13 Phototransistors

24. For a phototransistor having the characteristics of Fig. 17.50, determine the photoinduced base current for a radiant flux density of 5 mW/cm^2. If $h_{fe} = 40$, find I_C.

***25.** Design a high-isolation OR-gate employing phototransistors and LEDs.

17.14 Opto-Isolators

26. **a.** Determine an average derating factor from the curve of Fig. 17.58 for the region defined by temperatures between $-25°\text{C}$ and $+50°\text{C}$.
b. Is it fair to say that for temperatures greater than room temperature (up to 100°C), the output current is somewhat unaffected by temperature?

27. **a.** Determine from Fig. 17.54 the average change in I_{CEO} per degree change in temperature for the range 25°C to 50°C.
b. Can the results of part (a) be used to determine the level of I_{CEO} at 35°C? Test your theory.

28. Determine from Fig. 17.55 the ratio of LED output current to detector input current for an output current of 20 mA. Would you consider the device to be relatively efficient in its purpose?

***29.** **a.** Sketch the maximum-power curve of $P_D = 200$ mW on the graph of Fig. 17.56. List any noteworthy conclusions.
b. Determine β_{dc} (defined by I_C/I_F) for the system at $V_{CE} = 15$ V, $I_F = 10$ mA.
c. Compare the results of part (b) with those obtained from Fig. 17.55 at $I_F = 10$ mA. Do they compare? Should they? Why?

***30.** **a.** Referring to Fig. 17.57, determine the collector current above which the switching time does not change appreciably for $R_L = 1\ \text{k}\Omega$ and $R_L = 100\ \Omega$.
b. At $I_C = 6$ mA, how does the ratio of switching times for $R_L = 1\ \text{k}\Omega$ and $R_L = 100\ \Omega$ compare to the ratio of resistance levels?

17.15 Programmable Unijunction Transistor

31. Determine η and V_G for a PUT with $V_{BB} = 20$ V and $R_{B_1} = 3R_{B_2}$.

32. Using the data provided in Example 17.3, determine the impedance of the PUT at the firing and valley points. Are the approximate open- and short-circuit states verified?

33. Can Eq. (17.24) be derived exactly as shown from Eq. (17.23)? If not, what element is missing in Eq. (17.24)?

***34.** **a.** Will the network of Example 17.3 oscillate if V_{BB} is changed to 10 V? What minimum value of V_{BB} is required (V_V a constant)?
b. Referring to the same example, what value of R would place the network in the stable "on" state and remove the oscillatory response of the system?
c. What value of R would make the network a 2-ms time-delay network? That is, would provide a pulse v_K at 2 ms after the supply is turned on and then stay in the "on" state.

Appendix A

Hybrid Parameters—Graphical Determinations and Conversion Equations (Exact and Approximate)

A.1 GRAPHICAL DETERMINATION OF THE *h*-PARAMETERS

Using partial derivatives (calculus), it can be shown that the magnitude of the *h*-parameters for the small-signal transistor equivalent circuit in the region of operation for the common-emitter configuration can be found using the following equations:*

$$\boxed{h_{ie} = \frac{\partial v_i}{\partial i_i} = \frac{\partial v_{be}}{\partial i_b} \cong \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE}=\text{constant}}} \quad \text{(ohms)} \tag{A.1}$$

$$\boxed{h_{re} = \frac{\partial v_i}{\partial v_o} = \frac{\partial v_{be}}{\partial v_{ce}} \cong \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B=\text{constant}}} \quad \text{(unitless)} \tag{A.2}$$

$$\boxed{h_{fe} = \frac{\partial i_o}{\partial i_i} = \frac{\partial i_c}{\partial i_b} \cong \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE}=\text{constant}}} \quad \text{(unitless)} \tag{A.3}$$

$$\boxed{h_{oe} = \frac{\partial i_o}{\partial v_o} = \frac{\partial i_c}{\partial v_{ce}} \cong \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B=\text{constant}}} \quad \text{(siemens)} \tag{A.4}$$

In each case, the symbol Δ refers to a small change in that quantity around the quiescent point of operation. In other words, the *h*-parameters are determined in the region of operation for the applied signal so that the equivalent circuit will be the most accurate available. The constant values of V_{CE} and I_B in each case refer to a condition that must be met when the various parameters are determined from the characteristics of the transistor. For the common-base and common-collector configurations, the proper equation can be obtained by simply substituting the proper values of v_i, v_o, i_i, and i_o.

The parameters h_{ie} and h_{re} are determined from the input or base characteristics, whereas the parameters h_{fe} and h_{oe} are obtained from the output or collector characteristics. Since h_{fe} is usually the parameter of greatest interest, we shall discuss the operations involved with equations, such as Eqs. (A.1) through (A.4), for this parameter first. The first step in determining any of the four hybrid parameters is to find the quiescent point of operation as

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*The partial derivative $\partial v_i/\partial i_i$ provides a measure of the instantaneous change in v_i due to an instantaneous change in i_i.

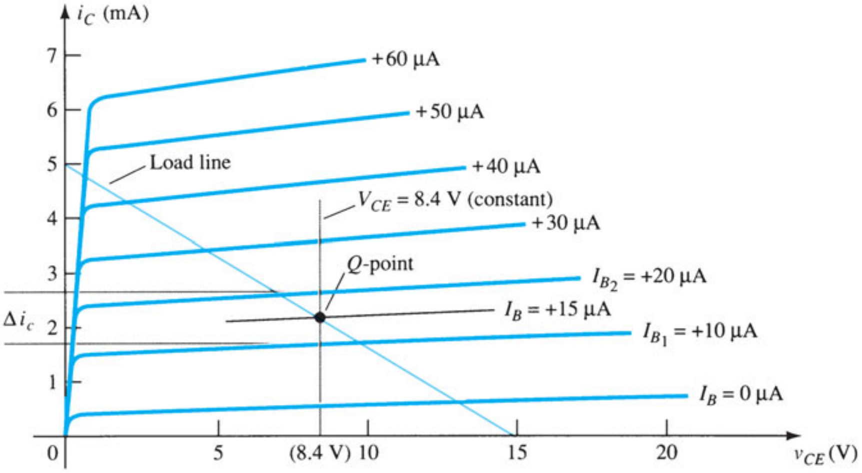


FIG. A.1

h_{fe} determination.

indicated in Fig. A.1. In Eq. (A.3) the condition V_{CE} = constant requires that the changes in base current and collector current be taken along a vertical straight line drawn through the *Q*-point representing a fixed collector-to-emitter voltage. Equation (A.3) then requires that a small change in collector current be divided by the corresponding change in base current. For the greatest accuracy, these changes should be made as small as possible.

In Fig. A.1, the change in i_b is chosen to extend from I_{B_1} to I_{B_2} along the perpendicular straight line at V_{CE}. The corresponding change in i_c is then found by drawing the horizontal lines from the intersections of I_{B_1} and I_{B_2} with V_{CE} = constant to the vertical axis. All that remains is to substitute the resultant changes of i_b and i_c into Eq. (A.3). That is,

$$|h_{fe}| = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE}=\text{constant}} = \left.\frac{(2.7 - 1.7)\text{ mA}}{(20 - 10)\ \mu\text{A}}\right|_{V_{CE}=8.4\text{ V}}$$

$$= \frac{10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

In Fig. A.2, a straight line is drawn tangent to the curve I_B through the *Q*-point to establish a line I_B = constant as required by Eq. (A.4) for h_{oe}. A change in v_{CE} was then chosen and the corresponding change in i_C determined by drawing the horizontal lines to the vertical axis at

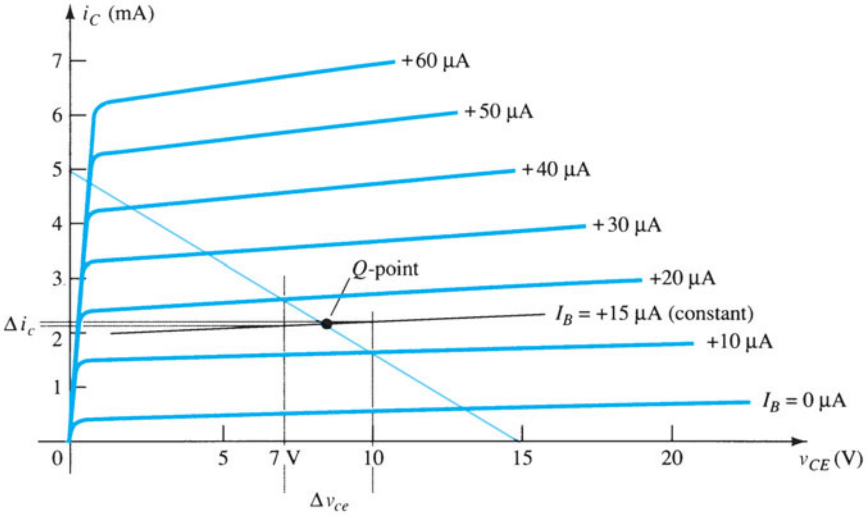


FIG. A.2

h_{oe} determination.

the intersections on the $I_B =$ constant line. Substituting into Eq. (A.4), we get

$$|h_{oe}| = \frac{\Delta i_c}{\Delta v_{ce}}\bigg|_{I_B=\text{constant}} = \frac{(2.2 - 2.1)\text{ mA}}{(10 - 7)\ V}\bigg|_{I_B=+15\ \mu\text{A}}$$

$$= \frac{0.1 \times 10^{-3}}{3} = \mathbf{33\ \mu A/V = 33 \times 10^{-6}\,S = 33\ \mu S}$$

To determine the parameters h_{ie} and h_{re} the Q-point must first be found on the input or base characteristics as indicated in Fig. A.3. For h_{ie}, a line is drawn tangent to the curve $V_{CE} = 8.4$ V through the Q-point to establish a line $V_{CE} =$ constant as required by Eq. (A.1). A small change in v_{be} is then chosen, resulting in a corresponding change in i_b. Substituting into Eq. (A.1), we get

$$|h_{ie}| = \frac{\Delta v_{be}}{\Delta i_b}\bigg|_{V_{CE}=\text{constant}} = \frac{(733 - 718)\text{ mV}}{(20 - 10)\ \mu\text{A}}\bigg|_{V_{CE}=8.4\text{ V}}$$

$$= \frac{15 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1.5\ k\Omega}$$

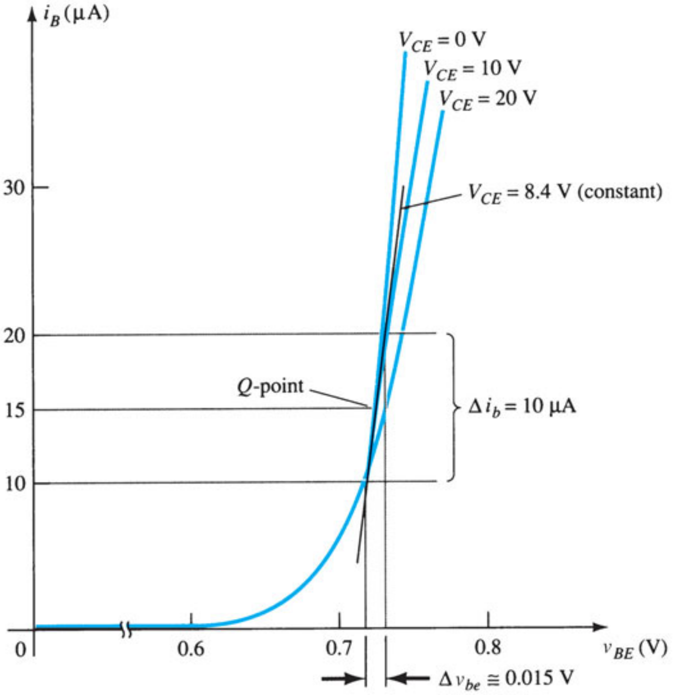


FIG. A.3
h_{ie} determination.

The last parameter, h_{re}, can be found by first drawing a horizontal line through the Q-point at $I_B = 15\ \mu$A. The natural choice then is to pick a change in v_{CE} and find the resulting change in v_{BE} as shown in Fig. A.4.

Substituting into Eq. (A.2), we get

$$|h_{re}| = \frac{\Delta v_{be}}{\Delta v_{ce}}\bigg|_{I_B=\text{constant}} = \frac{(733 - 725)\text{ mV}}{(20 - 0)\text{ V}} = \frac{8 \times 10^{-3}}{20} = \mathbf{4 \times 10^{-4}}$$

For the transistor whose characteristics appear in Figs. A.1 through A.4, the resulting hybrid small-signal equivalent circuit is shown in Fig. A.5.

As mentioned earlier, the hybrid parameters for the common-base and common-collector configurations can be found using the same basic equations with the proper variables and characteristics.

Table A.1 lists typical parameter values in each of the three configurations for the broad range of transistors available. The minus sign indicates that in Eq. (A.3) as one quantity increases in magnitude within the change chosen, the other decreases in magnitude.

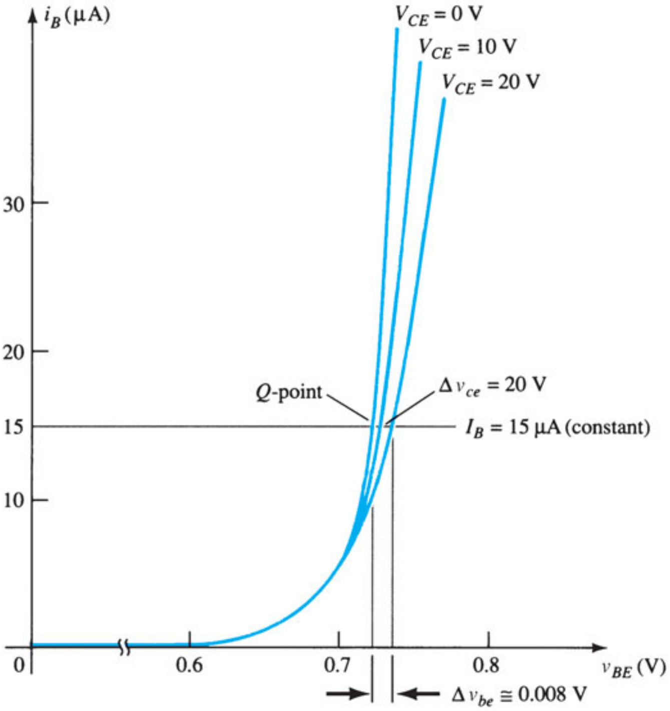


FIG. A.4
h_{re} determination.

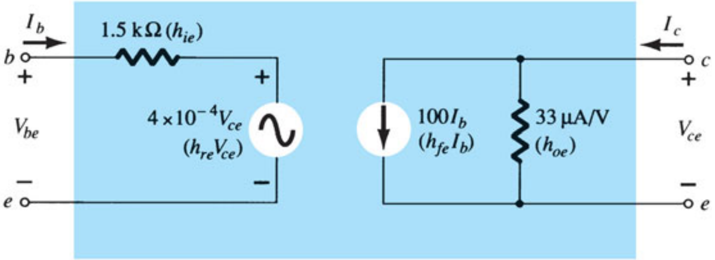

I_b
b
+
V_{be}
–
e
1.5 kΩ (h_{ie})
+
$4 \times 10^{-4} V_{ce}$
($h_{re} V_{ce}$)
–
$100 I_b$
($h_{fe} I_b$)
33 μA/V
(h_{oe})
I_c
c
+
V_{ce}
–
e

FIG. A.5
Complete hybrid equivalent circuit for a transistor having the characteristics that appear in Figs. A.1 through A.4.

TABLE A.1
Typical Parameter Values for the CE, CC, and CB Transistor Configurations

Parameter	CE	CC	CB
h_i	1 kΩ	1 kΩ	20 Ω
h_r	2.5×10^{-4}	≅ 1	3.0×10^{-4}
h_f	50	−50	−0.98
h_o	25 μA/V	25 μA/V	0.5 μA/V
$1/h_o$	40 kΩ	40 kΩ	2 MΩ

A.2 EXACT CONVERSION EQUATIONS

Common-Emitter Configuration

$$h_{ie} = \frac{h_{ib}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = h_{ic}$$

$$h_{re} = \frac{h_{ib}h_{ob} - h_{rb}(1 + h_{fb})}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = 1 - h_{rc}$$

$$h_{fe} = \frac{-h_{fb}(1 - h_{rb}) - h_{ob}h_{ib}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = -(1 + h_{fc})$$

$$h_{oe} = \frac{h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = h_{oc}$$

Common-Base Configuration

$$h_{ib} = \frac{h_{ie}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}} = \frac{h_{ic}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{rb} = \frac{h_{ie}h_{oe} - h_{re}(1 + h_{fe})}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}} = \frac{h_{fc}(1 - h_{rc}) + h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{fb} = \frac{-h_{fe}(1 - h_{re}) - h_{ie}h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}} = \frac{h_{rc}(1 + h_{fc}) - h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{ob} = \frac{h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}} = \frac{h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

Common-Collector Configuration

$$h_{ic} = \frac{h_{ib}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = h_{ie}$$

$$h_{rc} = \frac{1 + h_{fb}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = 1 - h_{re}$$

$$h_{fc} = \frac{h_{rb} - 1}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = -(1 + h_{fe})$$

$$h_{oc} = \frac{h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}} = h_{oe}$$

A.3 APPROXIMATE CONVERSION EQUATIONS

Common-Emitter Configuration

$$h_{ie} \cong \frac{h_{ib}}{1 + h_{fb}} \cong \beta r_e$$

$$h_{re} \cong \frac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{rb}$$

$$h_{fe} \cong \frac{-h_{fb}}{1 + h_{fb}} \cong \beta$$

$$h_{oe} \cong \frac{h_{ob}}{1 + h_{fb}}$$

Common-Base Configuration

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} \cong \frac{-h_{ic}}{h_{fc}} \cong r_e$$

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} \cong h_{rc} - 1 - \frac{h_{ic}h_{oc}}{h_{fc}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} \cong - \frac{(1 + h_{fc})}{h_{fc}} \cong - \alpha$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} \cong \frac{-h_{oc}}{h_{fc}}$$

Common-Collector Configuration

$$h_{ic} \cong \frac{h_{ib}}{1 + h_{fb}} \cong \beta r_e$$

$$h_{rc} \cong 1$$

$$h_{fc} \cong \frac{-1}{1 + h_{fb}} \cong -\beta$$

$$h_{oc} \cong \frac{h_{ob}}{1 + h_{fb}}$$

Appendix B

Ripple Factor and Voltage Calculations

B.1 RIPPLE FACTOR OF RECTIFIER

The ripple factor of a voltage is defined by

$$r = \frac{\text{rms value of ac component of signal}}{\text{average value of signal}}$$

which can be expressed as

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}}$$

Since the ac voltage component of a signal containing a dc level is

$$v_{\text{ac}} = v - V_{\text{dc}}$$

the rms value of the ac component is

$$\begin{aligned} V_r(\text{rms}) &= \left[\frac{1}{2\pi}\int_0^{2\pi} v_{\text{ac}}^2\, d\theta\right]^{1/2} \\ &= \left[\frac{1}{2\pi}\int_0^{2\pi} (v - V_{\text{dc}})^2\, d\theta\right]^{1/2} \\ &= \left[\frac{1}{2\pi}\int_0^{2\pi} (v^2 - 2vV_{\text{dc}} + V_{\text{dc}}^2)\, d\theta\right]^{1/2} \\ &= [V^2(\text{rms}) - 2V_{\text{dc}}^2 + V_{\text{dc}}^2]^{1/2} \\ &= [V^2(\text{rms}) - V_{\text{dc}}^2]^{1/2} \end{aligned}$$

where $V(\text{rms})$ is the rms value of the total voltage. For the half-wave rectified signal,

$$\begin{aligned} V_r(\text{rms}) &= [V^2(\text{rms}) - V_{\text{dc}}^2]^{1/2} \\ &= \left[\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2\right]^{1/2} \\ &= V_m\left[\left(\frac{1}{2}\right)^2 - \left(\frac{1}{\pi}\right)^2\right]^{1/2} \end{aligned}$$

$$\boxed{V_r(\text{rms}) = 0.385V_m \qquad \text{(half-wave)}} \qquad \textbf{(B.1)}$$

For the full-wave rectified signal,

$$\begin{aligned}V_r(\text{rms}) &= [V^2(\text{rms}) - V_{\text{dc}}^2]^{1/2} \\ &= \left[\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2\right]^{1/2} \\ &= V_m\left(\frac{1}{2} - \frac{4}{\pi^2}\right)^{1/2}\end{aligned}$$

$$\boxed{V_r(\text{rms}) = 0.308V_m \qquad \text{(full-wave)}} \tag{B.2}$$

B.2 RIPPLE VOLTAGE OF CAPACITOR FILTER

Assuming a triangular ripple waveform approximation as shown in Fig. B.1, we can write (see Fig. B.2)

$$V_{\text{dc}} = V_m - \frac{V_r(\text{p-p})}{2} \tag{B.3}$$

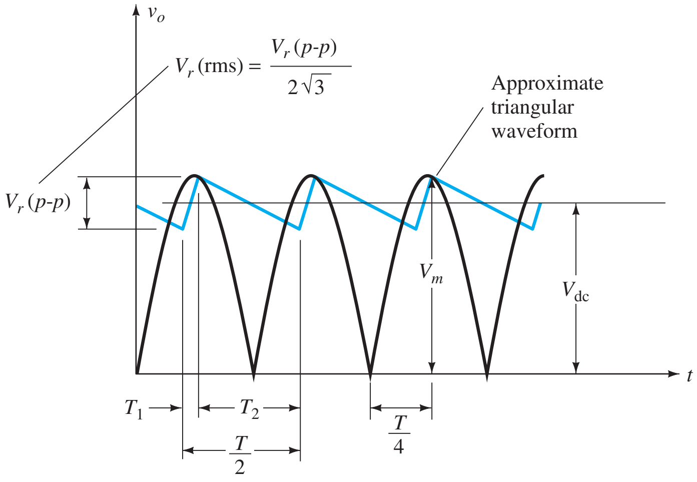
During capacitor discharge, the voltage change across C is

$$V_r(\text{p-p}) = \frac{I_{\text{dc}}T_2}{C} \tag{B.4}$$

From the triangular waveform in Fig. B.1,

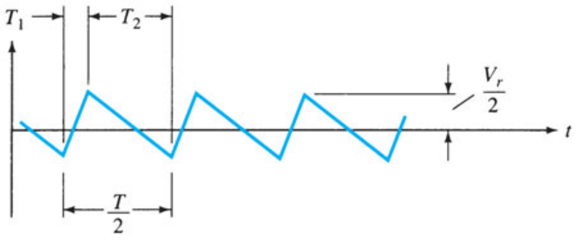
$$V_r(\text{rms}) = \frac{V_r(\text{p-p})}{2\sqrt{3}} \tag{B.5}$$

(obtained by calculations not shown).



v_o
$V_r(\text{rms}) = \frac{V_r(p\text{-}p)}{2\sqrt{3}}$
Approximate triangular waveform
$V_r(p\text{-}p)$
V_m
V_{dc}
t
T_1
T_2
$\frac{T}{2}$
$\frac{T}{4}$

FIG. B.1
Approximate triangular ripple voltage for capacitor filter.



T_1
T_2
$\frac{V_r}{2}$
t
$\frac{T}{2}$

FIG. B.2
Ripple voltage.

Using the waveform details of Fig. B.1 results in

$$\frac{V_r(\text{p-p})}{T_1} = \frac{V_m}{T/4}$$

$$T_1 = \frac{V_r(\text{p-p})(T/4)}{V_m}$$

Also, $$T_2 = \frac{T}{2} - T_1 = \frac{T}{2} - \frac{V_r(\text{p-p})(T/4)}{V_m} = \frac{2TV_m - V_r(\text{p-p})T}{4V_m}$$

$$T_2 = \frac{2V_m - V_r(\text{p-p})}{V_m}\frac{T}{4} \tag{B.6}$$

Since Eq. (B.3) can be written as

$$V_{\text{dc}} = \frac{2V_m - V_r(\text{p-p})}{2}$$

we can combine the last equation with Eq. (B.6) to obtain

$$T_2 = \frac{V_{\text{dc}}}{V_m}\frac{T}{2}$$

which, inserted into Eq. (B.4), gives

$$V_r(\text{p-p}) = \frac{I_{\text{dc}}}{C}\left(\frac{V_{\text{dc}}}{V_m}\frac{T}{2}\right)$$

$$T = \frac{1}{f}$$

$$V_r(\text{p-p}) = \frac{I_{\text{dc}}}{2fC}\frac{V_{\text{dc}}}{V_m} \tag{B.7}$$

Combining Eqs. (B.5) and (B.7), we solve for V_r (rms):

$$\boxed{V_r(\text{rms}) = \frac{V_r(\text{p-p})}{2\sqrt{3}} = \frac{I_{\text{dc}}}{4\sqrt{3}fC}\frac{V_{\text{dc}}}{V_m}} \tag{B.8}$$

B.3 RELATION OF V_{dc} AND V_m TO RIPPLE r

The dc voltage developed across a filter capacitor from a transformer providing a peak voltage V_m can be related to the ripple as follows:

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} = \frac{V_r(\text{p-p})}{2\sqrt{3}V_{\text{dc}}}$$

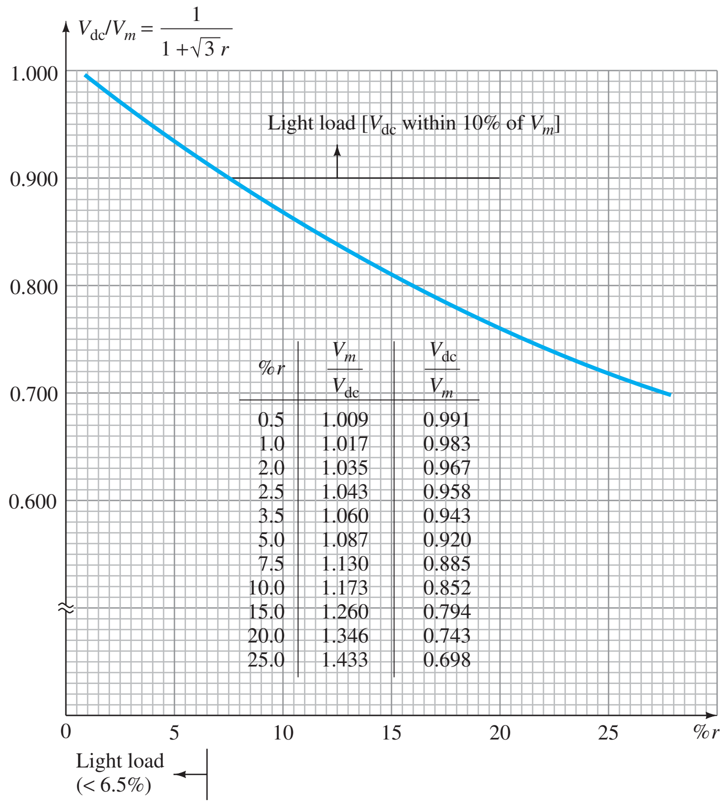
$$V_{\text{dc}} = \frac{V_r(\text{p-p})}{2\sqrt{3}r} = \frac{V_r(\text{p-p})/2}{\sqrt{3}r} = \frac{V_r(\text{p})}{\sqrt{3}r} = \frac{V_m - V_{\text{dc}}}{\sqrt{3}r}$$

$$V_m - V_{\text{dc}} = \sqrt{3}rV_{\text{dc}}$$

$$V_m = (1 + \sqrt{3}r)V_{\text{dc}}$$

$$\boxed{\frac{V_m}{V_{\text{dc}}} = 1 + \sqrt{3}r} \tag{B.9}$$

Equation (B.9) applies to both half-wave and full-wave rectifier-capacitor filter circuits and is plotted in Fig. B.3. As an example, at a ripple of 5% the dc voltage is $V_{\text{dc}} = 0.92V_m$, or within 10% of the peak voltage, whereas at 20% ripple the dc voltage drops to only $0.74V_m$, which is more than 25% less than the peak value. Note that V_{dc} is within 10% of V_m for ripple less than 6.5%. This amount of ripple represents the borderline of the light-load condition.



%r	$\frac{V_m}{V_{dc}}$	$\frac{V_{dc}}{V_m}$
0.5	1.009	0.991
1.0	1.017	0.983
2.0	1.035	0.967
2.5	1.043	0.958
3.5	1.060	0.943
5.0	1.087	0.920
7.5	1.130	0.885
10.0	1.173	0.852
15.0	1.260	0.794
20.0	1.346	0.743
25.0	1.433	0.698

FIG. B.3

Plot of V_{dc}/V_m as a function of %r.

B.4 RELATION OF V_r(rms) AND V_m TO RIPPLE r

We can also obtain a relation connecting V_r(rms), V_m, and the amount of ripple for both half-wave and full-wave rectifier-capacitor filter circuits as follows:

$$\frac{V_r(\text{p-p})}{2} = V_m - V_{dc}$$

$$\frac{V_r(\text{p-p})/2}{V_m} = \frac{V_m - V_{dc}}{V_m} = 1 - \frac{V_{dc}}{V_m}$$

$$\frac{\sqrt{3}V_r(\text{rms})}{V_m} = 1 - \frac{V_{dc}}{V_m}$$

Using Eq. (B.9), we get

$$\frac{\sqrt{3}V_r(\text{rms})}{V_m} = 1 - \frac{1}{1 + \sqrt{3}r}$$

$$\frac{V_r(\text{rms})}{V_m} = \frac{1}{\sqrt{3}}\left(1 - \frac{1}{1 + \sqrt{3}r}\right) = \frac{1}{\sqrt{3}}\left(\frac{1 + \sqrt{3}r - 1}{1 + \sqrt{3}r}\right)$$

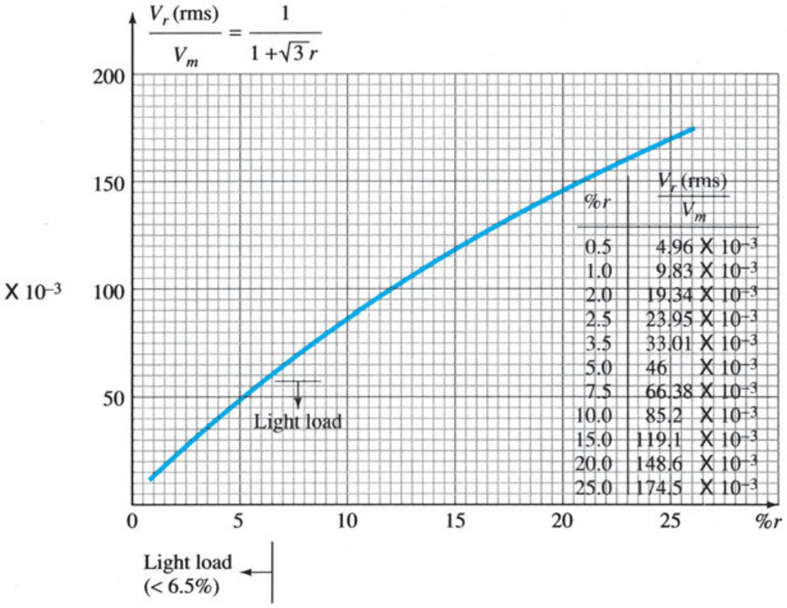
$$\boxed{\frac{V_r(\text{rms})}{V_m} = \frac{r}{1 + \sqrt{3}r}} \qquad \textbf{(B.10)}$$

Equation (B.10) is plotted in Fig. B.4.

Since V_{dc} is within 10% of V_m for ripple $\leq$ 6.5%,

$$\frac{V_r(\text{rms})}{V_m} \cong \frac{V_r(\text{rms})}{V_{dc}} = r \qquad \text{(light load)}$$

and we can use $V_r(\text{rms})/V_m = r$ for ripple $\leq$ 6.5%.



$\%r$	$\frac{V_r(\text{rms})}{V_m}$
0.5	4.96 X 10^{-3}
1.0	9.83 X 10^{-3}
2.0	19.34 X 10^{-3}
2.5	23.95 X 10^{-3}
3.5	33.01 X 10^{-3}
5.0	46 X 10^{-3}
7.5	66.38 X 10^{-3}
10.0	85.2 X 10^{-3}
15.0	119.1 X 10^{-3}
20.0	148.6 X 10^{-3}
25.0	174.5 X 10^{-3}

FIG. B.4

Plot of $V_r(\text{rms})/V_m$ as a function of $\%r$.

B.5 RELATION CONNECTING CONDUCTION ANGLE, PERCENTAGE RIPPLE, AND $I_{\text{peak}}/I_{\text{dc}}$ FOR RECTIFIER-CAPACITOR FILTER CIRCUITS

Using Fig. B.1, we can determine the angle θ_1 at which the diode starts to conduct as follows: Since

$$v = V_m \sin\theta = V_m - V_r(\text{p-p}) \qquad \text{at} \qquad \theta = \theta_1$$

we have

$$\theta_1 = \sin^{-1}\left[1 - \frac{V_r(\text{p-p})}{V_m}\right]$$

Using Eq. (B.10) and $V_r(\text{rms}) = V_r(\text{p-p})/2\sqrt{3}$ gives

$$\frac{V_r(\text{p-p})}{V_m} = \frac{2\sqrt{3}V_r(\text{rms})}{V_m}$$

so that

$$1 - \frac{V_r(\text{p-p})}{V_m} = 1 - \frac{2\sqrt{3}V_r(\text{rms})}{V_m} = 1 - 2\sqrt{3}\left(\frac{r}{1 + \sqrt{3}r}\right)$$

$$= \frac{1 - \sqrt{3}r}{1 + \sqrt{3}r}$$

and

$$\boxed{\theta_1 = \sin^{-1}\frac{1 - \sqrt{3}r}{1 + \sqrt{3}r}} \qquad \textbf{(B.11)}$$

where θ_1 is the angle at which conduction starts.

When the current becomes zero after charging the parallel impedances R_L and C, we can determine that

$$\theta_2 = \pi - \tan^{-1}\omega R_L C$$

An expression for $\omega R_L C$ can be obtained as follows:

$$r = \frac{V_r(\text{rms})}{V_{\text{dc}}} = \frac{(I_{\text{dc}}/4\sqrt{3}fC)(V_{\text{dc}}/V_m)}{V_{\text{dc}}} = \frac{V_{\text{dc}}/R_L}{4\sqrt{3}fC}\frac{1}{V_m}$$

$$= \frac{V_{\text{dc}}/V_m}{4\sqrt{3}fCR_L} = \frac{2\pi\left(\frac{1}{1 + \sqrt{3}r}\right)}{4\sqrt{3}\omega CR_L}$$

so that
$$\omega R_L C = \frac{2\pi}{4\sqrt{3}\,(1 + \sqrt{3}r)r} = \frac{0.907}{r(1 + \sqrt{3}r)}$$

Thus conduction stops at an angle

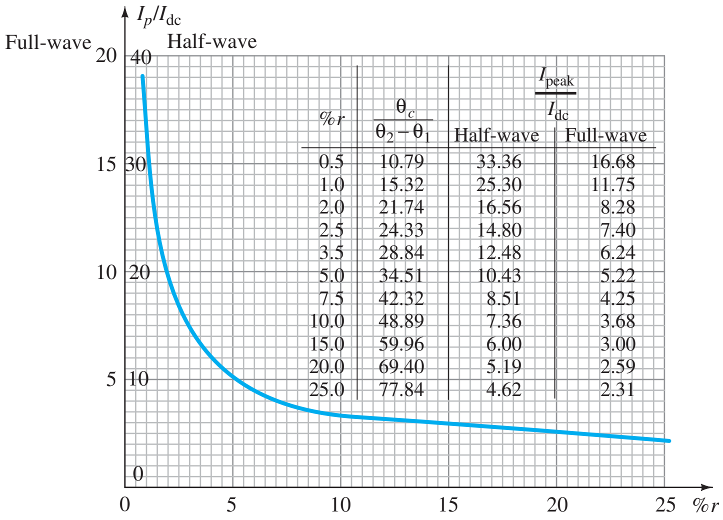
$$\boxed{\theta_2 = \pi - \tan^{-1}\frac{0.907}{(1 + \sqrt{3}r)r}} \qquad \textbf{(B.12)}$$

From Eq. (15.10b), we can write

$$\frac{I_{\text{peak}}}{I_{\text{dc}}} = \frac{I_p}{I_{\text{dc}}} = \frac{T}{T_1} = \frac{180^\circ}{\theta} \qquad \text{(full-wave)}$$

$$= \frac{360^\circ}{\theta} \qquad \text{(half-wave)} \qquad \textbf{(B.13)}$$

A plot of I_p/I_{dc} as a function of ripple is provided in Fig. B.5 for both half-wave and full-wave operation.



%r	θ_c $\theta_2 - \theta_1$	$\frac{I_{\text{peak}}}{I_{\text{dc}}}$ Half-wave	Full-wave
0.5	10.79	33.36	16.68
1.0	15.32	25.30	11.75
2.0	21.74	16.56	8.28
2.5	24.33	14.80	7.40
3.5	28.84	12.48	6.24
5.0	34.51	10.43	5.22
7.5	42.32	8.51	4.25
10.0	48.89	7.36	3.68
15.0	59.96	6.00	3.00
20.0	69.40	5.19	2.59
25.0	77.84	4.62	2.31

$$\theta_1 = \sin^{-1}\left(\frac{1 - \sqrt{3}\,r}{1 + \sqrt{3}\,r}\right) \qquad \theta_2 = \pi - \tan^{-1}\left[\frac{0.907}{r\,(1 + \sqrt{3}\,r)}\right] \qquad \theta_c = \theta_2 - \theta_1$$

FIG. B.5

Plot of I_p/I_{dc} versus %r for half-wave and full-wave operation.

Appendix C

Charts and Tables

TABLE C.1

Greek Alphabet

Name	Capital	Lowercase
alpha	Α	α
beta	Β	β
gamma	Γ	γ
delta	Δ	δ
epsilon	Ε	ε
zeta	Ζ	ζ
eta	Η	η
theta	Θ	θ
iota	Ι	ι
kappa	Κ	κ
lambda	Λ	λ
mu	Μ	μ
nu	Ν	ν
xi	Ξ	ξ
omicron	Ο	ο
pi	Π	π
rho	Ρ	ρ
sigma	Σ	σ
tau	Τ	τ
upsilon	Υ	υ
phi	Φ	ϕ
chi	Χ	χ
psi	Ψ	ψ
omega	Ω	ω

TABLE C.2

Standard Values of Commercially Available Resistors

Ohms (Ω)					Kilohms (kΩ)		Megohms (MΩ)	
0.10	**1.0**	**10**	**100**	**1000**	**10**	**100**	**1.0**	**10.0**
0.11	1.1	11	110	1100	11	110	1.1	11.0
0.12	**1.2**	**12**	**120**	**1200**	**12**	**120**	**1.2**	**12.0**
0.13	1.3	13	130	1300	13	130	1.3	13.0
0.15	**1.5**	**15**	**150**	**1500**	**15**	**150**	**1.5**	**15.0**
0.16	1.6	16	160	1600	16	160	1.6	16.0
0.18	**1.8**	**18**	**180**	**1800**	**18**	**180**	**1.8**	**18.0**
0.20	2.0	20	200	2000	20	200	2.0	20.0
0.22	**2.2**	**22**	**220**	**2200**	**22**	**220**	**2.2**	**22.0**
0.24	2.4	24	240	2400	24	240	2.4	
0.27	**2.7**	**27**	**270**	**2700**	**27**	**270**	**2.7**	
0.30	3.0	30	300	3000	30	300	3.0	
0.33	**3.3**	**33**	**330**	**3300**	**33**	**330**	**3.3**	
0.36	3.6	36	360	3600	36	360	3.6	
0.39	**3.9**	**39**	**390**	**3900**	**39**	**390**	**3.9**	
0.43	4.3	43	430	4300	43	430	4.3	
0.47	**4.7**	**47**	**470**	**4700**	**47**	**470**	**4.7**	
0.51	5.1	51	510	5100	51	510	5.1	
0.56	**5.6**	**56**	**560**	**5600**	**56**	**560**	**5.6**	
0.62	6.2	62	620	6200	62	620	6.2	
0.68	**6.8**	**68**	**680**	**6800**	**68**	**680**	**6.8**	
0.75	7.5	75	750	7500	75	750	7.5	
0.82	**8.2**	**82**	**820**	**8200**	**82**	**820**	**8.2**	
0.91	9.1	91	910	9100	91	910	9.1	

TABLE C.3

Typical Capacitor Component Values

pF				μF				
10	100	1000	10,000	0.10	1.0	10	100	1000
12	120	1200						
15	150	1500	15,000	0.15	1.5	18	180	1800
22	220	2200	22,000	0.22	2.2	22	220	2200
27	270	2700						
33	330	3300	33,000	0.33	3.3	33	330	3300
39	390	3900						
47	470	4700	47,000	0.47	4.7	47	470	4700
56	560	5600						
68	680	6800	68,000	0.68	6.8			
82	820	8200						

Appendix D

Answers ~~Solutions~~ to Selected Odd-Numbered Problems

Chapter 1

5. 2.4×10^{-18} C
15. **(a)** 25.27 mV **(b)** 11.84 mA
17. **(a)** 25.27 mV **(b)** 0.1 μA
19. 0.41 V
21. 1.6 μA
23. −75°C: 1.1 V, 0.01 pA; 25°C: 0.85 V, 1 pA; 125°C: 1.1 V, 105 μA
27. 175 Ω
29. −10 V: 100 MΩ; −30 V: 300 MΩ
31. **(a)** 3 Ω **(b)** 2.6 Ω **(c)** quite close
33. 1 mA: 52 Ω, 15 mA: 1.73 Ω
35. 22.5 Ω
37. $r_d = 4\ \Omega$
39. **(a)** −25 V: 0.75 pF; −10 V: 1.25 pF; $\Delta C_T/\Delta V_R = 0.033$ pF/V
43. 2.81 pF
45. $t_s = 3$ ns, $t_t = 6$ ns
47. **(b)** 6 pF **(c)** 0.58
49. 25°C: 0.5 nA; 100°C: 60 nA; 60 nA: 0.5 nA = 120:1
51. 25°C: 500 mW; 100°C: 260 mW; 25°C: 714.29 mA; 100°C: 371.43 mA
55. 0.053%/°C
57. 13 Ω
59. 2 V
61. 2.3 V
63. **(a)** 75° **(b)** 40°

Chapter 2

1. **(a)** $I_{D_Q} \cong 15$ mA, $V_{D_Q} \cong 0.85$ V, $V_R = 11.15$ V **(b)** $I_{D_Q} \cong 15$ mA, $V_{D_Q} = 0.71$ V, $V_R = 11.3$ V **(c)** $I_{D_Q} = 16$ mA, $V_{D_Q} = 0$ V, $V_R = 12$ V
3. $R = 0.62$ kΩ
5. **(a)** $I = 0$ mA **(b)** $I = 2.895$ A **(c)** $I = 1$ A
7. **(a)** $V_o = 9.17$ V **(b)** $V_o = 10$ V
9. **(a)** $V_{o_1} = 11.3$ V, $V_{o_2} = 1.2$ V **(b)** $V_{o_1} = 0$ V, $V_{o_2} = 0$ V
11. **(a)** $V_o = 0.3$ V, $I = 0.3$ mA **(b)** $V_o = 14.6$ V, $I = 3.96$ mA
13. $V_o = 6.03$ V, $I_D = 1.635$ mA
15. $V_o = 9.3$ V

17. $V_o = 10$ V
19. $V_o = -0.7$ V
21. $V_o = 4.7$ V
23. v_i: $V_m = 6.98$ V: r_d: pos. max = 0.7 V, neg. peak = −6.98 V: i_d: pos. pulse of 3.14 mA
25. Pos. pulse, peak = 169.68 V, $V_{\text{dc}} = 5.396$ V
27. **(a)** $I_{D_{\max}} = 20$ mA **(b)** $I_{\max} = 40$ mA **(c)** $I_D = 18.1$ mA **(d)** $I_D = 36.2 \text{ mA} > I_{D_{\max}} = 20$ mA
29. Full rectified waveform, peak = −100 V; PIV = 100 V, $I_{\max} = 45.45$ mA
31. Full rectified waveform, peak = 56.67 V; $V_{\text{dc}} = 36.04$ V
33. **(a)** Pos. pulse of 5.09 V **(b)** Pos. pulse of 15.3 V
35. **(a)** Clipped at 4.7 V **(b)** Pos. clip at 0.7 V, neg. peak = −11 V
37. **(a)** 0 V to 40 V swing **(b)** −5 V to 35 V swing
39. **(a)** 28 ms **(b)** 56:1 **(c)** −1.3 V to −25.3 V swing
41. Network of Fig. 2.179 with battery reversed
43. **(a)** $R_s = 20\ \Omega$, $V_Z = 12$ V **(b)** $P_{Z_{\max}} = 2.4$ W
45. $R_s = 0.5\ \text{k}\Omega$, $I_{ZM} = 40$ mA
47. $V_o = 339.36$ V

Chapter 3

3. Forward- and reverse-biased
9. $I_C = 7.921$ mA, $I_B = 79.21\ \mu$A
11. $V_{CB} = 1$ V: $V_{BE} = 800$ mV
$V_{CB} = 10$ V: $V_{BE} = 770$ mV
$V_{CB} = 20$ V: $V_{BE} = 750$ mV
Only slight
13. **(a)** $I_C \cong 3.5$ mA **(b)** $I_C \cong 3.5$ mA **(c)** Negligible **(d)** $I_C = I_E$
15. **(a)** $I_C = 3.992$ mA **(b)** $\alpha = 0.946$
19. **(a)** $\beta_{\text{dc}} = 111.11$ **(b)** $\alpha_{\text{dc}} = 0.991$ **(c)** $I_{CEO} = 0.3$ mA **(d)** $I_{CBO} = 2.7$ mA
21. **(a)** $\beta_{\text{dc}} = 87.5$ **(b)** $\beta_{\text{dc}} = 108.3$ **(c)** $\beta_{\text{dc}} = 135$
23. $\beta_{\text{dc}} = 116$, $\alpha_{\text{dc}} = 0.991$, $I_E = 2.93$ mA
29. $I_C = I_{C_{\max}}$, $V_{CB} = 6$ V
$V_{CB} = V_{CB_{\max}}$, $I_C = 2.1$ mA
$I_C = 4$ mA, $V_{CB} = 10.5$ V
$V_{CB} = 10$ V, $I_C = 4.2$ mA
31. $I_C = I_{C_{\max}}$, $V_{CE} = 3.125$ V
$V_{CE} = V_{CE_{\max}}$, $I_C = 20.83$ mA
$I_C = 100$ mA, $V_{CE} = 6.25$ mA
$V_{CE} = 20$ V, $I_C = 31.25$ mA
33. h_{FE}: $I_C = 0.1$ mA, $h_{FE} \cong 43$
$I_C = 10$ mA, $h_{FE} \cong 98$
h_{fe}: $I_C = 0.1$ mA, $h_{fe} \cong 72$
$I_C = 10$ mA, $h_{fe} \cong 160$
35. $I_C = 1$ mA, $h_{fe} \cong 120$
$I_C = 10$ mA, $h_{fe} \cong 160$
37. **(a)** $\beta_{\text{ac}} = 190$ **(b)** $\beta_{\text{dc}} = 201.7$ **(c)** $\beta_{\text{ac}} = 200$ **(d)** $\beta_{\text{dc}} = 230.77$ **(f)** Yes

Chapter 4

1. **(a)** $I_{B_Q} = 30\ \mu$A **(b)** $I_{CO} = 3.6$ mA **(c)** $V_{CE_Q} = 9.52$ V **(d)** $V_C = 9.52$ V **(e)** $V_B = 0.7$ V **(f)** $V_E = 0$ V
3. **(a)** $I_C = 3.98$ mA **(b)** $V_{CC} = 15.96$ V **(c)** $\beta = 199$ **(d)** $R_B = 763\ \text{k}\Omega$
5. **(b)** $R_B = 812\ \text{k}\Omega$ **(c)** $I_{C_Q} = 3.4$ mA, $V_{CE_Q} = 10.75$ V **(d)** $\beta_{\text{dc}} = 136$ **(e)** $\alpha = 0.992$ **(f)** $I_{C_{sat}} = 7$ mA **(h)** $P_D = 36.55$ mW **(i)** $P_s = 71.92$ mW **(j)** $P_R = 35.37$ mW
7. $I_{C_Q} = 2.4$ mA, $V_{CE_Q} = 11.5$ V
9. **(b)** $I_{C_Q} = 4.7$ mA, $V_{CE_Q} = 7.5$ V **(c)** 133.25 **(d)** reasonably close
11. **(a)** 154.5 **(b)** 17.74 V **(c)** 747 kΩ
13. **(a)** 2.33 kΩ **(b)** 133.33 **(c)** 616.67 kΩ **(d)** 40 mW **(e)** 37.28 mW
15. **(a)** 21.42 μA **(b)** 1.71 mA **(c)** 8.17 V **(d)** 9.33 V **(e)** 1.16 V **(f)** 1.86 V

17. **(a)** $I_C = 1.28$ mA **(b)** $V_E = 1.54$ V **(c)** $V_B = 2.24$ V **(d)** $R_1 = 39.4$ kΩ

19. $I_{C_{\text{sat}}} = 3.49$ mA

21. **(a)** 2.43 mA **(b)** 7.55 V **(c)** 20.25 μA **(d)** 2.43 V **(e)** 3.13 V

23. **(a)** 1.99 mA **(b)** $I_{C_Q} = 1.71$ mA, $V_{CE_Q} = 8.17$ V, $I_{B_Q} = 21.42$ μA

25. **(a)** $I_C = 1.71$ mA, $V_{CE} = 8.17$ V **(b)** $I_C = 1.8$ mA, $V_{CE} = 7.76$ V **(c)** $\% \Delta I_C = 5.26$, $\% \Delta V_{CE} = 5.02$ **(e)** Voltage-divider

27. **(a)** 18.09 μA **(b)** 2.17 mA **(c)** 8.19 V

29. **(a)** 2.24 mA **(b)** 11.63 V **(c)** 4.03 V **(d)** 7.6 V

31. **(a)** $I_C = 0.91$ mA, $V_{CE} = 5.44$ V **(b)** $I_C = 0.983$ mA, $V_{CE} = 4.11$ V **(c)** $\% \Delta I_C = 8.02$, $\% \Delta V_{CE} = 24.45$ **(d)** Voltage-divider

33. **(a)** 3.3 V **(b)** 2.75 mA **(c)** 11.95 V **(d)** 8.65 V **(e)** 24.09 μA **(f)**114.16

35. **(a)** $I_B = 65.77$ μA, $I_C = 7.23$ mA, $I_E = 7.3$ mA **(b)** $V_B = 9.46$ V, $V_C = 12$ V, $V_E = 8.76$ V **(c)** $V_{BC} = -2.54$ V, $V_{CE} = 3.24$ V

37. **(a)** $I_E = 3.32$ mA, $V_C = 4.02$ V, $V_{CE} = 4.72$ V

39. **(a)** $R_{\text{Th}} = 255$ kΩ, $E_{\text{Th}} = 0$ V, $I_B = 13.95$ μA **(b)** $I_C = 1.81$ mA **(c)** $V_E = -4.42$ V **(d)** $V_{CE} = 5.95$ V

41. $R_B = 361.6$ kΩ, $R_C = 2.4$ kΩ
Standard values: $R_B = 360$ kΩ, $R_C = 2.4$ kΩ

43. $R_E = 0.75$ kΩ, $R_C = 3.25$ kΩ, $R_2 = 7.5$ kΩ, $R_1 = 41.15$ kΩ, Standard values: $R_E = 0.75$ kΩ, $R_C = 3.3$ kΩ, $R_2 = 8.2$ kΩ, $R_1 = 43$ kΩ

45. **(a)** $V_{B_1} = 4.14$ V, $V_{E_1} = 3.44$ V, $I_{C_1} = I_{E_1} = 3.44$ mA, $V_{C_1} = 12.43$ V, $V_{B_2} = 2.61$ V, $V_{E_2} = 1.91$ V, $I_{E_2} = I_{C_2} = 1.59$ mA, $V_{C_2} = 16.5$ V
(b) $I_{B_1} = 21.5$ μA, $I_{C_1} \cong I_{E_1} = 3.44$ mA, $I_{B_2} = 17.67$ μA, $I_{C_2} \cong I_{E_2} = 1.59$ mA

47. **(a)** $I_{B_1} = 57.33$ μA, $I_{C_1} = 3.44$ mA, $I_{B_2} = 28.67$ μA, $I_{C_2} = 3.44$ mA
(b) $V_{B_1} = 4.48$ V, $V_{B_2} = 10.86$ V, $V_{E_1} = 3.78$ V, $V_{C_1} = 10.16$ V, $V_{E_2} = 10.16$ V, $V_{C_2} = 14.43$ V

49. $I = 8.65$ mA

51. $I = 2.59$ mA

53. $I_E = 3.67$ μA

55. $I_B = 17.5$ μA, $V_C = -13.53$ V

57. $I_{C_{sat}} = 4.167$ mA, $V_o = 9.76$ V

59. **(a)** $t_{on} = 168$ ns, $t_{off} = 148$ ns **(b)** $t_{on} = 37$ ns, $t_{off} = 132$ ns

63. **(a)** $V_C\downarrow$ **(b)** $V_{CE}\downarrow$ **(c)** $I_C\downarrow$ **(d)** $V_{CE} \cong 20$ V **(e)** $V_{CE} \cong 20$ V

65. **(a)** $S(I_{CO}) = 120$ **(b)** $S(V_{\beta E}) = -235 \times 10^{-6}$S **(c)** $S(\beta) = 30 \times 10^{-6}$ A **(d)** $\Delta I_C \cong 2.12$ mA

67. **(a)** $S(I_{CO}) = 11.06$ **(b)** $S(V_{BE}) = -1280 \times 10^{-6}$ S **(c)** $S(\beta) = 2.43 \times 10^{-6}$ A **(d)** $\Delta I_C = 0.313$ mA

Chapter 5

1. **(c)** 80.4%

7. **(a)** 20 Ω **(b)** 0.588 V **(c)** 58.8 **(d)** ∞ Ω **(e)** 0.98 **(f)** 10 μA

9. 8.57 Ω **(b)** 25 μA **(c)** 3.5 mA **(d)** 132.84 **(e)** −298.89

11. **(a)** $Z_i = 497.47$ Ω, $Z_o = 2.2$ kΩ **(b)** −264.74 **(c)** $Z_i = 497.47$ Ω, $Z_o = 1.98$ kΩ, $A_v = -238.27$

13. **(a)** $I_B = 18.72$ μA, $I_C = 1.87$ mA, $r_e = 13.76$ Ω **(b)** $Z_i = 1.38$ kΩ, $Z_o = 5.6$ kΩ **(c)** −406.98 **(d)** −343.03

15. **(a)** 30.56 Ω **(b)** $Z_i = 1.77$ kΩ, $Z_o = 3.9$ kΩ **(c)** −127.6 **(d)** $Z_i = 1.77$ kΩ, $Z_o = 3.37$ kΩ, $A_v = -110.28$

17. **(a)** 18.95 Ω **(b)** $V_B = 3.72$ V, $V_C = 13.59$ V **(c)** $Z_i = 3.17$ kΩ, $A_v = -298.15$

19. **(a)** 5.34 Ω **(b)** $Z_i = 118.37$ kΩ, $Z_o = 2.2$ kΩ **(c)** −1.81 **(d)** $Z_i = 105.95$ kΩ, $Z_o = 2.2$ kΩ, $A_v = -1.81$

21. $R_E = 0.82$ kΩ, $R_B = 242.09$ kΩ

23. **(a)** 15.53 Ω **(b)** $V_B = 2.71$ V, $V_{CE} = 6.14$ V, $V_{CB} = 5.44$ V **(c)** $Z_i = 67.45$ kΩ, $Z_o = 4.7$ kΩ **(d)** −3.92 **(e)** 56.26

25. **(a)** $Z_i = 236.1$ kΩ, $Z_o = 31.2$ Ω **(b)** 0.994 **(c)** 0.994 mV

27. **(a)** 33.38 Ω **(b)** $Z_i = 33.22$ Ω, $Z_o = 4.7$ kΩ **(c)** 140.52

29. **(a)** 13.08 Ω **(b)** $Z_i = 501.98$ Ω, $Z_o = 3.83$ kΩ **(c)** −298

31. **(c)** $A_v = -1.83$, $Z_i = 40.8$ kΩ, $Z_o = 2.16$ kΩ

33. **(a)** $Z_i = 12.79\ \text{k}\Omega$, $Z_o = 1.75\ \text{k}\Omega$, $A_v = -2.65$

35. **(a)** $R_L = 4.7\ \text{k}\Omega$, $A_{v_L} = -191.65$; $R_L = 2.2\ \text{k}\Omega$, $A_{v_L} = -130.49$; $R_L = 0.5\ \text{k}\Omega$, $A_{v_L} = -42.92$ **(b)** No change

37. **(a)** $A_{v_{NL}} = -557.36$, $Z_i = 616.52\ \Omega$, $Z_o = 4.3\ \text{k}\Omega$ **(c)** $A_{v_L} = -214.98$, $A_{v_s} = -81.91$ **(d)** 49.04 **(e)** -120.12 **(f)** A_{v_s} the same **(g)** No change

39. **(a)** $R_L = 4.7\ \text{k}\Omega$, $A_{v_L} = -154.2$; $R_L = 2.2\ \text{k}\Omega$, $A_{v_L} = -113.2$; $R_L = 0.5\ \text{k}\Omega$, $A_{v_L} = -41.93$ **(b)** No change

41. **(a)** $A_{v_{NL}} = 0.983$, $Z_i = 9.89\ \text{k}\Omega$, $Z_o = 20.19\ \Omega$ **(c)** $A_{v_L} = 0.976$, $A_{v_s} = 0.92$ **(d)** $A_{v_L} = 0.976$, $A_{v_s} = 0.886$ **(e)** No change **(f)** $A_{v_L} = 0.979$, $A_{v_s} = 0.923$ **(g)** $A_i = 3.59$

43. **(a)** $A_{v_1} = -97.67$, $A_{v_2} = -189$ **(b)** $A_{v_L} = 18.46 \times 10^3$, $A_{v_s} = 11.54 \times 10^3$ **(c)** $A_{i_1} = 97.67$, $A_{i_2} = 70$ **(d)** $A_{i_L} = 6.84 \times 10^3$ **(e)** No effect **(f)** No effect **(g)** In phase

45. $V_B = 3.08$ V, $V_E = 2.38$ V, $I_E \cong I_C = 1.59$ mA, $V_C = 6.89$ V

47. $V_{B_1} = 4.4$ V, $V_{B_2} = 11.48$ V, $V_{E_1} = 3.7$ V, $I_{C_1} \cong I_{E_1} = 3.7$ mA $\cong I_{E_2} \cong I_{C_2}$, $V_{C_2} = 14.45$ V, $V_{C_1} = 10.78$ V

49. -1.86 V

51. **(a)** $V_{B_1} = 9.59$ V, $V_{C_1} = 16$ V, $V_{E_2} = 8.17$ V, $V_{CB_1} = 6.41$ V, $V_{CE_2} = 7.83$ V **(b)** $I_{B_1} = 2.67\ \mu\text{A}$, $I_{B_2} = 133.5\ \mu\text{A}$, $I_{E_2} = 16.02$ mA **(c)** $Z_i = 1.13\ \text{M}\Omega$, $Z_o = 3.21\ \Omega$ **(d)** $A_v \cong 1$, $A_i = 3.16 \times 10^3$

53. **(a)** $V_{B_1} = 8.22$ V, $V_{E_2} = 6.61$ V, $V_{CE_2} = 3.3$ V, $V_{CB_1} = 1.69$ V **(b)** $Z_i \cong 8\ \text{k}\Omega$, $Z_o = 470\ \Omega$ **(d)** -235 **(e)** 4×10^3

55. **(a)** $V_{B_1} = 6.24$ V, $V_{B_2} = 3.63$ V, $V_{C_1} = 3.63$ V, $V_{C_2} = 6.95$ V, $V_{E_1} = 6.95$ V, $V_{E_2} = 2.93$ V **(b)** $I_{B_1} = 4.16\ \mu\text{A}$, $I_{C_1} = 0.666$ mA, $I_{B_2} = 0.666$ mA, $I_{C_2} = 133.12$ mA, $I_{E_2} = 135.12$ mA **(c)** $Z_i = 0.887\ \text{M}\Omega$, $Z_o = 68\ \Omega$ **(d)** $\cong 1$ **(e)** -13.06×10^3

57. $r_e = 21.67\ \Omega$, $\beta r_e = 2.6\ \text{k}\Omega$

63. % difference = 4.2, ignore effects

65. % difference = 4.8, ignore effects

67. **(a)** $8.31\ \Omega$ **(b)** $h_{fe} = 60$, $h_{ie} = 498.6\ \Omega$ **(c)** $Z_i = 497.47\ \Omega$, $Z_o = 2.2\ \text{k}\Omega$ **(d)** $A_v = -264.74$, $A_i \cong 60$ **(e)** $Z_i = 497.47\ \Omega$, $Z_o = 2.09\ \text{k}\Omega$ **(f)** $A_v = -250.90$, $A_i = 56.73$

69. **(a)** $Z_i = 9.38\ \Omega$, $Z_o = 2.7\ \text{k}\Omega$ **(b)** $A_v = 284.43$, $A_i \cong -1$ **(c)** $\alpha = 0.992$, $\beta = 124$, $r_e = 9.45\ \Omega$, $r_o = 1\ \text{M}\Omega$

71. **(a)** $814.8\ \Omega$ **(b)** -357.68 **(c)** 132.43 **(d)** $72.9\ \text{k}\Omega$

75. **(a)** 75% **(b)** 70%

77. **(a)** $200\ \mu\text{S}$ **(b)** $5\ \text{k}\Omega$ versus $8.6\ \text{k}\Omega$, not a good approximation

79. **(a)** h_{fe} **(b)** h_{oe} **(c)** $30\ \mu\text{S}$ to $0.1\ \mu\text{S}$ **(d)** Mid-region

81. **(a)** Yes **(b)** R_2 not connected as base.

Chapter 6

5. **(a)** 3.5 mA **(b)** 2.5 mA **(c)** 1.5 mA **(d)** 0.5 mA **(e)** As $V_{GS}\downarrow$, $\Delta I_D\downarrow$ **(f)** Nonlinear

15. **(a)** 1.852 mA **(b)** -1.318 V

19. 525 mW

21. 5.5 mA

23. -3 V

25. **(a)** $175\ \Omega$ **(b)** $233\ \Omega$ **(c)** $252\ \Omega$

29. $V_{GS} = 0$ V, $I_D = 6$ mA; $V_{GS} = -1$ V, $I_D = 2.66$ mA; $V_{GS} = +1$ V, $I_D = 10.67$ mA, $V_{GS} = 2$ V, $I_D = 16.61$ mA; $\Delta I_D = 3.34$ mA versus 6 mA

31. -4.67 V

33. 8.13 V

37. **(a)** $k = 1\ \text{mA/V}^2$, $I_D = 1 \times 10^{-3}\,(V_{GS} - 4\ \text{V})^2$ **(c)** $V_{GS} = 2$ V, $I_D = 0$ mA; $V_{GS} = 5$ V, $I_D = 1$ mA; $V_{GS} = 10$ V, $I_D = 36$ mA

39. 1.261

41. $dI_D/dV_{GS} = 2k\,(V_{GS} - V_T)$

Chapter 7

1. **(c)** $I_{D_Q} \cong 4.7$ mA, $V_{DS_Q} \cong 5.54$ V
(d) $I_{D_Q} = 4.69$ mA, $V_{DS_Q} = 5.56$ V

3. **(a)** $I_D = 2.727$ mA **(b)** $V_{DS} = 6$ V **(c)** $V_{GG} = 1.66$ V
5. $V_D = 18$ V, $V_{GS} = -4$ V
7. $I_{D_Q} = 2.6$ mA
9. **(a)** $I_{D_Q} = 3.33$ mA **(b)** $V_{GS_Q} \cong -1.7$ V **(c)** $I_{DSS} = 10.06$ mA **(d)** $V_D = 11.34$ V **(e)** $V_{DS} = 9.64$ V
11. $V_S = 1.4$ V
13. **(a)** $V_G = 2.16$ V $I_{D_Q} \cong 5.8$ mA, $V_{GS_Q} \cong -0.85$ V $V_D = 7.24$ V, $V_S = 6.38$ V $V_{DS_Q} = 0.86$ V **(b)** $V_{GS} = 0$ V, $V_G = I_D R_S = I_{DSS} R_S$ and $R_S = 216\ \Omega$
15. $R_S = 2.67$ kΩ
17. **(a)** $I_D = 3.33$ mA **(b)** $V_D = 10$ V, $V_S = 6$ V **(c)** $V_{GS} = -6$ V
19. $V_D = 8.8$ V, $V_{GS} = 0$ V
21. **(a)** $I_{D_Q} \cong 9$ mA, $V_{GS_Q} \cong 0.5$ V **(b)** $V_{DS} = 7.69$ V, $V_S = -0.5$ V
23. **(a)** $I_{D_Q} \cong 5$ mA, $V_{GS_Q} \cong 6$ V
25. **(a)** $V_B = V_G = 3.2$ V **(b)** $V_E = 2.5$ V **(c)** $I_E = 2.08$ mA, $I_C = 2.08$ mA, $I_D = 2.08$ mA **(d)** $I_B = 20.8\ \mu$A **(e)** $V_C = 5.67$ V, $V_S = 5.67$ V, $V_D = 11.42$ V **(f)** $V_{CE} = 3.17$ V **(g)** $V_{DS} = 5.75$ V
27. $V_{GS} = -2$ V, $R_S = 2.4$ kΩ, $R_D = 6.2$ kΩ, $R_2 = 4.3$ MΩ
29. **(a)** JFET in saturation **(b)** JFET nonconducting **(c)** Short from gate to drain (JFET or circuit)
31. JFET in saturation, open circuit between gate and voltage-divider network
33. **(a)** $I_{D_Q} \cong 4.4$ mA, $V_{GS_Q} \cong -7.25$ V **(b)** $V_{DS} = -7.25$ V **(c)** $V_D = -7.25$ V
35. **(a)** $V_{GS_Q} = -1.96$ V, $I_{D_Q} = 2.7$ mA **(b)** $V_{DS} = 11.93$ V, $V_D = 13.95$ V, $V_G = 0$ V, $V_S = 2.03$ V
37. **(a)** $I_{D_Q} = 2.76$ mA, $V_{GS_Q} = -2.04$ V **(b)** $V_{DS} = 7.86$ V, $V_S = 2.07$ V

Chapter 8

1. 6 mS
3. 10 mA
5. 12.5 mA
7. 2.4 mS
9. $Z_o = 40$ kΩ, $A_v = -180$
11. **(a)** 4 mS **(b)** 3.64 mS **(c)** 3.6 mS **(d)** 3 mS **(e)** 3.2 mS
13. **(a)** 0.75 mS **(b)** 100 kΩ
15. $g_m = 5.6$ mS, $r_d = 66.67$ kΩ
17. $Z_i = 1$ MΩ, $Z_o = 1.72$ kΩ, $A_v = -4.8$
19. **(a)** $Z_i = 2$ MΩ, $Z_o = 3.81$ kΩ, $A_v = -7.14$ **(b)** $Z_i = 2$ MΩ, $Z_o = 4.21$ kΩ, (increased), $A_v = -7.89$ (increased)
21. $Z_i = 10$ MΩ, $Z_o = 730\ \Omega$, $A_v = -2.19$
23. **(a)** 3.83 kΩ, **(b)** 3.41 kΩ
25. $Z_i = 9.7$ MΩ, $Z_o = 1.92$ kΩ, $V_o = -210$ mV
27. $Z_i = 9.7$ MΩ, $Z_o = 1.82$ kΩ, $V_o = -198.8$ mV
29. $Z_i = 356.3\ \Omega$, $Z_o = 3.3$ kΩ, $V_o = 28.24$ mV
31. $Z_i = 275.5\ \Omega$, $Z_o = 2.2$ kΩ, $A_v = 5.79$
33. $Z_i = 10$ MΩ, $Z_o = 506.4\ \Omega$, $A_v = 0.745$
35. 11.73 mV
37. $Z_i = 10$ MΩ, $Z_o = 1.68$ kΩ, $A_v = -9.07$
39. $Z_i = 9$ MΩ, $Z_o = 197.6\ \Omega$, $A_v = 0.816$
41. $Z_i = 1.73$ MΩ, $Z_o = 2.15$ kΩ, $A_v = -4.77$
43. -203 mV
45. -3.51 mV
47. $R_S = 180\ \Omega$, $R_D = 2$ kΩ (standard values)
49. **(a)** $Z_i = 2$ MΩ, $Z_o = 0.72$ kΩ, $A_{v_{NL}} = 0.733$ **(c)** $A_{v_L} = 0.552$, $A_{v_s} = 0.552$ **(d)** $A_{v_L} = 0.670$, A_{v_s} the same **(e)** A_{v_L} the same, $A_{v_s} = 0.546$ **(f)** Z_i and Z_o the same
51. From graph $V_{GS_Q} \cong -1.45$ V, $I_{D_Q} \cong 3.7$ mA, $V_D = 9.86$ V, $V_S = 1.44$ V, $V_{DS} = 8.42$ V, $V_G = 0$ V
53. From graph $V_{GS_Q} \cong -1.4$ V, $I_{D_Q} \cong 3.6$ mA, $V_D = 10.08$ V, $V_S = 1.4$ V, $V_{DS} = 8.68$ V, $V_G = 0$ V

55. $Z_i = 10\text{ M}\Omega$, $Z_o = 2.7\text{ k}\Omega$

57. $A_{v_1} = -3.77$, $A_{v_2} = -87.2$, $A_{v_T} = 328.74$

Chapter 9

1. **(a)** 3,1.699, −1.151 **(b)** 6.908, 3.912, −0.347 **(c)** Results differ by 2.3

3. **(a)** Same 22.92 **(b)** Same 23.98 **(c)** Same 0.903

5. $G_{dBm} = 43.98\text{ dBm}$

7. $G_{dB} = 67.96\text{ dB}$

9. **(a)** $G_{dB} = 69.83\text{ dB}$ **(b)** $G_v = 82.83\text{ dB}$ **(c)** $R_i = 2\text{ k}\Omega$ **(d)** $P_o = 1385.64\text{ V}$

11. **(a)** $f_L = 1/\sqrt{1 + (1950.43\text{ Hz}/f)^2}$ **(b)** 100 Hz: $|A_v| = 0.051$; 1k Hz: $|A_v| = 0.456$; 2k Hz: $|A_v| = 0.716$; 5k Hz: $|A_v| = 0.932$; 10k Hz: $|A_v| = 0.982$ **(c)** $f_L \cong 1950\text{ Hz}$

13. **(a)** 10k Hz **(b)** 1k Hz **(c)** 5k Hz **(d)** 100k Hz

15. **(a)** $r_e = 28.48\ \Omega$ **(b)** $A_{v_{\text{mid}}} = -72.91$ **(c)** $Z_i = 2.455\text{ k}\Omega$ **(d)** $f_{L_s} = 137.93\text{ Hz}$, $f_{L_C} = 38.05\text{ Hz}$, $f_{L_E} = 85.30\text{ Hz}$ **(e)** $f_L = f_{L_s} = 137.93\text{ Hz}$

17. **(a)** $r_e = 30.23\ \Omega$ **(b)** $A_{v_{\text{mid}}} = 0.983$ **(c)** $Z_i = 21.13\text{ k}\Omega$ **(d)** $f_{L_s} = 75.32\text{ Hz}$, $f_{L_C} = 188.57\text{ Hz}$ **(e)** $f_L = f_{L_C} = 188.57\text{ Hz}$

19. **(a)** $r_e = 28.48\ \Omega$ **(b)** $A_{v_{\text{mid}}} = -72.91$ **(c)** $Z_i = 2.455\text{ k}\Omega$ **(d)** $f_{L_s} = 103.4\text{ Hz}$, $f_{L_C} = 38.05\text{ Hz}$, $f_{L_E} = 235.79\text{ Hz}$ **(e)** $f_L = f_{L_E} = 235.79\text{ Hz}$

21. **(a)** $r_e = 30.23\Omega$ **(b)** $A_{v_{\text{mid}}} = 0.983$ **(c)** $Z_i = 21.13\text{ k}\Omega$ **(d)** $f_{L_s} = 71.92\text{ Hz}$, $f_{L_C} = 193.16\text{ Hz}$ **(e)** $f_L = f_{L_C} = 193.16\text{ Hz}$

23. **(a)** $V_{GS_Q} = -2.45\text{ V}$, $I_{D_Q} = 2.1\text{ mA}$ **(b)** $g_m = 1.18\text{ mS}$ **(c)** $A_{v_{\text{mid}}} = -2$ **(d)** $Z_i = 1\text{ M}\Omega$ **(e)** $A_{v_s} = -2$ **(f)** $f_{L_G} = 1.59\text{ Hz}$, $f_{L_C} = 4.91\text{ Hz}$, $f_{L_S} = 32.04\text{ Hz}$ **(g)** $f_L = f_{L_S} = 32\text{ Hz}$

25. **(a)** $V_{GS_Q} = -2.55\text{ V}$, $I_{D_Q} = 3.3\text{ mA}$ **(b)** $g_m = 1.91\text{ mS}$ **(c)** $A_{v_{\text{mid}}} = -4.39$ **(d)** $Z_i = 51.94\text{ k}\Omega$ **(e)** $A_{v_s} = -4.27$ **(f)** $f_{L_G} = 2.98\text{ Hz}$, $f_{L_C} = 2.46\text{ Hz}$, $f_{L_S} = 41\text{ Hz}$ **(g)** $f_L = f_{L_S} = 41\text{ Hz}$

27. **(a)** $f_{H_i} = 277.89\text{ kHz}$, $f_{H_o} = 2.73\text{ mHz}$ **(b)** $f_\beta = 895.56\text{ kHz}$, $f_T = 107.47\text{ MHz}$ **(d)** GBP = 18.23 MHz

29. **(a)** $f_{H_i} = 2.87\text{ MHz}$, $f_{H_o} = 127.72\text{ mHz}$ **(b)** $f_\beta = 1.05\text{ MHz}$, $f_T = 105\text{ MHz}$ **(d)** GBP = 786.4 kHz

31. **(a)** $g_{m0} = 2\text{ mS}$, $g_m = 1.18\text{ mS}$ **(b)** $A_{v_{\text{mid}}} = A_{v_s} = -2$ **(c)** $f_{H_i} = 7.59\text{ MHz}$, $f_{H_o} = 7.82\text{ MHz}$ **(e)** GBP = 12 MHz

33. $A_{v_T} = 16 \times 10^4$

35. $f'_L = 91.96\text{ Hz}$

Chapter 10

1. $V_o = -18.75\text{ V}$

3. $V_1 = -40\text{ mV}$

5. $V_o = -9.3\text{ V}$

7. V_o ranges from 5.5 V to 10.5 V

9. $V_o = -3.39\text{ V}$

11. $V_o = 0.5\text{ V}$

13. $V_2 = -2\text{V}$, $V_1 = 4.2\text{ V}$

15. $V_o = 6.4\text{ V}$

17. $I_{\text{IB}} = 22\text{ nA}$, $I_{\text{IB}} = 18\text{ nA}$

19. $A_{\text{CL}} = 80$

21. V_o (offset) = 105 mV

23. CMRR = 75.56 dB

Chapter 11

1. $V_o = -175\text{ mV}$, rms

3. $V_o = 412\text{ mV}$

7. $V_o = -2.5\text{ V}$

11. $I_L = 6\text{ mA}$

13. $I_o = 0.5\text{ mA}$

13. $I_o = 0.5$ mA
15. $f_{OH} = 1.45$ kHz
17. $f_{OL} = 318.3$ Hz, $f_{OH} = 397.9$ Hz

Chapter 12

1. $P_o = 10.4$ W, $P_o = 640$ mW
3. $P_o = 2.1$ W
5. $R(\text{eff}) = 2.5$ kΩ
7. $a = 44.7$
9. $\%\eta = 37\%$
13. **(a)** Maximum $P_1 = 49.7$ W **(b)** Maximum $P_o = 39.06$ W **(c)** Maximum $\%\eta = 78.5\%$
17. **(a)** $P_o = 27$ W **(b)** $P_o = 8$ W **(c)** $\%\eta = 29.6\%$ **(d)** $P_{2Q} = 19$ W
19. $\%D_2 = 14.3\%$, $\%D_3 = 4.8\%$, $\%D_4 = 2.4\%$
21. $\%D_2 = 6.8\%$
23. $P_D = 25$ W
25. $P_D = 3$ W

Chapter 13

9. $V_o = 13$ V
13. Period $= 204.8\ \mu$s
17. $f_o = 60$ kHz
19. $C = 133$ pF
21. $C_1 = 300$ pF

Chapter 14

1. $A_f = -9.95$
3. $A_f = -14.3$, $R_{of} = 31.5$ kΩ, $R_{of} = 2.4$ kΩ
5. Without feedback: $A_i = -303.2$, $Z_i = 1.18$ kΩ, $Z_o = 4.7$ kΩ
   With feedback: $A_{of} = -3.82$, $Z_{of} = 45.8$ kΩ
7. $f_o = 4.2$ kHz
9. $f_o = 1.05$ MHz
11. $f_o = 159.2$ kHz

Chapter 15

1. Ripple factor $= 0.028$
3. Ripple voltage $= 24.2$ V
5. $V_r = 1.2$ V
7. $V_r = 0.6$ V rms, $V_{dc} = 17$ V
9. $V_r = 0.12$ V rms
11. $V_m = 13.7$ V
13. $\%r = 7.2\%$
15. $\%r = 8.3\%$, $\%r = 3.1\%$
17. $V_r = 0.325$ V rms
19. $V_o = 7.6$ V, $I_z = 3.66$ mA
21. $V_o = 24.6$ V
25. $I_{dc} = 225$ mA
27. $V_o = 9.9$ V

Chapter 16

3. 33.25 μA
7. $C_D \cong 6.2$ pF, $X_C = 25.67$ kΩ
9. **(a)** -3 V: 40 pF, -12V: 20 pF, $\Delta C = 20$ pF **(b)** -8 V: $\Delta C/\Delta V_R = 2$ pF/V, -2 V: $\Delta C/\Delta V_R = 6.67$ pF/V
11. $C_t \cong 15$ pF, $Q = 354.61$ versus 350 on chart

15. $\cong$ 739.5 kHz
19. **(a)** $\Delta V_{OC}/\Delta f_C = 0.375$ mV$/f_C$ **(b)** 547.5 mV
21. **(a)** 422.8×10^{-21} J **(b)** 305.72×10^{-21} J **(c)** yes
23. 50 V
25. **(a)** $\cong$ 0.9 Ω/fc **(b)** $\cong$ 380 Ω/fc **(c)** $\cong$ 78 kΩ/fc, low-illumination region
27. $V_i = 21$ V
29. As fc increases, t_r and t_d decrease exponentially
31. **(a)** $\phi \cong 5$ mW **(b)** 2.27 lm
33. $\phi = 3.44$ mW
37. Lower levels
39. $R = 20$ kΩ
41. R (thermistor) $= 90\ \Omega$
43. 1 MHz: 31.83 kΩ; 100 MHz: 318.3 Ω; 1 MHz: $Z_T = -152\ \Omega\angle 0°$; 100 MHz: $Z_T = -137.16\ \Omega\ \angle 26°$; L_S very little effect
45. $-62.5\ \Omega$

Chapter 17

5. **(a)** Yes **(b)** No **(c)** No **(d)** Yes, No
9. **(a)** $V_{\text{peak}} = 168.28$ V **(b)** $I_{\text{peak}} = 1.19$ A **(c)** 1.19 A **(d)** 4.17 ms **(e)** 51 ms **(f)** Open **(g)** 23.86 ms **(h)** Turn on **(i)** Forced commutation
13. **(a)** $V_{GK} = -12\text{ V} + \dfrac{R'(24\text{ V})}{R' + R_S}$
(b) 0 V **(c)** 14 kΩ **(d)** 60 mA **(e)** 0.12 mA **(f)** Yes, inductive element in alarm; install protective capacitive element.

15. **(a)** $\cong 0.7$ MW/cm^2 **(b)** 80.5%
19. 241 pF
21. $153\text{ M}\Omega > R_1 > 4.875\text{ k}\Omega$
23. **(a)** $R_{B_1} = 5.5$ kΩ, $R_{B_2} = 4.5$ kΩ **(b)** 11.7 V **(c)** OK, 68 kΩ < 166 kΩ
27. **(a)** 1.12 nA/°C
29. **(b)** $\beta_{\text{dc}} = 0.4$
31. $\eta = 0.75$, $V_G = 15$ V

INDEX

A
Acceptor ion, 9
ac millivoltmeter, 664
ac resistance, 23–26, 35
Active filters, 667
Active region, 133, 137, 162
Adjustable voltage regulator, 802
Alarm circuit, 850–851
Alarm system with a CCS, 229–231
Alpha, 134–135
Amplifier,
  analog-digital conversion, 729
  distortion, 705
  op-amp, 607
AND gates, 70–72
AND/OR circuit, 852–853
Angstrom, 43
Anode, 47
Antilogarithm, 547
Applications. *See* Practical applications
Arsenic, 2–19
Astable operation, 732–734
Audio mixer, 342–345, 524
Avalanche breakdown region, 16
Average ac resistance, 26–27
Axial luminous intensity, 44

B
Band frequencies, 557
Bandpass filter, 670
Bandwidth, 557
Bardeen, John, 129
Battery charger, 101–103
Battery charging regulator, 847
Bel, 550
Beta, 138–141
Biasing, 10–13, 160–252, 422–480
  BJTs, 160–252
  FETs, 422–480
BiFET amplifier, 617
BiMOS amplifier, 617
Bipolar, 378
BJTs (bipolar junction transistors)
  ac analysis, 253–377
  active region, 137, 162
  alpha, 134–135
  applications, 226–233, 342–349
  beta, 138–141
  Bode plot, 562
  break frequencies, 577
  cascade configuration, 303–304
  cascaded systems, 300–305, 521
  collector dc feedback configuration, 284–286
  collector feedback configuration, 279–283, 359–360
  combination networks, 449–452
  common-base configuration, 131–135, 187–189, 260–261, 277–279, 329–330
  common-collector configuration, 143–144, 189–190, 262, 273, 279–283
  common-emitter configuration, 136–143, 257–259, 262–265, 321, 322, 579, 580
  computer analysis, 155–157, 181, 235–238, 271–272, 352–361, 592–601
  construction, 130
  current gain, 286–287
  current mirror configuration, 205–208
  current source, 208–209
  curve tracer, 149–150
  cutoff, 132–133, 137–138, 145, 161–163, 211–213, 231
  Darlington configuration, 305–314, 359
  dc biasing, 135, 141–142, 160–252
  depletion region, 130
  design, 194–199
  direct-coupled amplifier, 554–557
  effect of R_S and R_L, 286–291
  emitter-bias configuration, 169–175, 196, 219–220, 222–223, 224–225, 267–273, 327–328
  emitter follower configuration, 186–187, 273–277, 328–329
  feedback pair, 314–318
  fixed-bias configuration, 163–169, 194, 216, 219, 222, 224, 226, 236–237, 262–265, 273, 289, 293, 325–326
  frequency response, 545–606
  gain-bandwidth product, 581–582
  Giacoletto model, 579
  high-frequency analysis, 583–586
  hybrid equivalent circuit, 254, 319–336
  hybrid parameter variation, 338–340
  hybrid pi model, 255, 337–338, 579
  inverting amplifier, 574–576
  leakage current, 131
  limits of operation, 144–145
  linear region, 162
  load-line analysis, 166–169, 173–175, 185–186
  low frequency analysis, 559–574
  majority carriers, 130–131
  Miller effect capacitance, 574–576
  minority carriers, 130–131
  miscellaneous bias configurations, 189–193
  modeling, 254–262
  normalization, 148–149
  npn transistor, 130
  operation, 130–131
  phase relationship, 264, 266, 268, 275, 278, 281, 285
  pnp transistor, 130–151
  quiescent point, 161–163
  RC-coupled amplifier, 302–303, 556

BJTs (*continued*)
  r_e model, 255, 257–262, 265–267
  reverse saturation current, 217–226
  saturation, 133, 144, 161–163, 165–166, 173, 181, 185, 211–212
  self-bias configuration, 427–431, 492–496
  specification sheets, 145–149
  stabilization, 172–173, 217–226
  summary table, 292
  switching networks, 211–215
  temperature effects, 217–218
  terminal identification, 151–152
  testing, 149–151
  transformer-coupled amplifier, 556
  troubleshooting, 215, 340–342
  two-port system approach, 292–300
  unbypassed emitter-bias configuration, 327–328
  voltage-divider bias configuration, 175–181, 196, 220, 225, 233, 265–267, 292, 326–327, 352–357, 431–436, 497–498
  voltage feedback dc biasing, 181–186, 220, 224
Bode plot, 559–564
Body resistance, 15, 25
Bohr model, 3–4
Brattain, Walter H., 129
Break frequency, 557

C
Candela, 44
Capacitance, 30–31, 105
  diffusion, 30–31
  transition, 30–31
Capacitor filter, 786–789
Cascade configuration, 300–305, 518–521
Cascode configuration, 303–305
Cathode, 47
Center-tapped transformer, 77–78
Clampers, 85–88
Class A amplifier, 685
Class B amplifier operation, 695–699
Class C amplifier, 712
Clippers, 78–85
  parallel, 82–84
  series, 79–84
Clipping, 106
CMOS amplifier, 411–412, 617
Collector dc feedback configuration, 284–286
Collector feedback configuration, 279–283, 369–370
Colpitts oscillator, 771–773
Common-base configuration, 131–135, 187–189, 260–261, 277–279, 329–330
Common-base, short-circuit, amplification factor, 135
Common-collector configuration, 143–144, 262
Common-emitter configuration, 136–143, 257–259, 262–265, 321, 322, 579, 580
Common-emitter, forward-current, amplification factor, 139
Common-gate configuration, 436–438, 498–501
Common logarithm, 545–549
Common-mode operation, 609, 610, 615–616, 639
Common-mode rejection, 609–610, 637
Comparator unit operation, 722–729
Complementary-symmetry circuits, 701–702
Computer analysis
  Multisim, 50–51, 117–119, 237–238, 359–361, 472–473, 535–536, 597–599
  PSpice, 50, 155–157, 235–236, 352–357, 416–418, 471–472, 531–535, 596–597, 644–646, 745–747
Conservation of energy, 253
Constant-current source, 616–617
Constant-gain multiplier, 653–657
Constant-magnitude gain, 622
Contact resistance, 15, 25
Contributors
  Bardeen, John, 129
  Brattain, Walter H., 129
  Dacey, Dr. G. C., 379
  DeForest, Lee, 129
  Fleming, J. A., 129
  Kilby, Jack St. Clair, 1, 2
  Ohl, Russell, 19
  Ross, Dr. Ian, 379
  Shockley, William Bradford, 386
Control grid, 129
Controlled battery-powered backup, 108
Controlled sources, 661–663
Conventional flow, 9
Conversion efficiency, 254
Corner frequencies, 557
Covalent bonding, 3–5
Crystal oscillator, 774–776
Current-controlled current source, 662–663
Current-controlled voltage source, 662
Current gain, 286–287
Current mirror, 205–208, 247–248
Current series feedback, 755–756
Current source network, 208–209
Curve tracer, 37, 149–150, 394
Cutoff frequencies, 231, 557
Cutoff region, 132–133, 137–138, 145, 161–163, 211–213, 231

D
Dacey, Dr. G. C., 379
Darlington configuration, 305–314, 359
dB plots, 557
dc biasing
  BJTs, 160–252
  JFETs, 422–480
dc millivoltmeter, 664
dc resistance, 21–23
DDM, 36, 151
Decibels, 550–554
DeForest, Lee, 129
Depletion region, 10–13, 130–131, 399
Depletion-type MOSFETS. *See* MOSFETs
Design
  BJT, 194–199
  JFET, 452–454
  MOSFET, 456
Detector, 108–109
Diac, 854–856
Dielectric, 397
Differential amplifier circuit, 610–617
Differential-mode operation, 639
Differentiator, 627–628
Diffusion capacitance, 30
Digital-analog converters, 729–732
Digital display meter, 36, 151
Digital multimeter, 36, 151
Diodes, 1–128, 347
  acceptor ions, 9
  AND/OR gates, 70–72
  avalanche breakdown region, 16
  biasing, 10–15
  body resistance, 15, 25
  capacitance, 30–31
  characteristics, 13–19
  clampers, 85–88
  computer analysis, 49–54, 64–65, 112–119
  contact resistance, 15, 25
  covalent bonding, 3–5
  curve tracer, 37
  dc analysis, 55–128

  depletion region, 10–13
  diffusion capacitance, 30–31
  donor atoms, 7–8
  doping, 5, 7–8, 38
  electron flow, 9
  electron volt, 7
  energy levels, 5–7
  equivalent circuits, 27–30, 39
  extrinsic materials, 7–10
  free carriers, 4, 7, 10–13
  full-wave rectification, 75–78
  GaAs, 2–19, 41–48
  germanium, 2–19, 41
  half-wave rectification, 72–75
  hole, 8
  ideal, 20–21, 29, 61
  intrinsic materials, 3–5
  knee voltage, 17, 28–30
  LCDs, 41
  LEDs, 7, 41–48, 68–69, 92–93, 108–109, 232–233
  load line analysis, 56–61
  majority carrier, 9–10
  maximum power, 32
  minority carrier, 9–10
  multiplier networks, 98–101
  negative temperature coefficient, 5
  notation, 35
  n-type materials, 7–19
  Ohl, Russell, 19
  parallel diode configurations, 67–70
  PIV, 16, 75, 77, 78
  positive temperature coefficient, 5
  practical applications, 101–111
  p-type materials, 7–19
  quiescent point, 23, 57
  rectifiers, 32, 72–78, 101–103, 348
  regulator, 93–98
  relative mobility, 5
  resistance levels, 21–27, 28, 32
  reverse breakdown region, 16–19, 38–41, 46
  reverse recovery time, 31–32
  reverse saturation current, 11–19, 31
  semiconductors, 2–19
  series diode configurations, 61–67
  series-parallel diode configurations, 67–70
  Shockley's equation, 13–19
  silicon, 2–19, 42
  sinusoidal inputs, 72–78
  specification sheets, 32–35
  storage time, 31
  temperature effects, 5, 6, 18–19, 32–35, 40
  testing, 36–37
  thermal voltage, 13
  transition capacitance, 30–31
  valence electrons, 3–7
  Zener diodes, 38–41, 91–98, 111–112, 209, 410
Direct-coupled amplifier, 556
Display driver, 664–665
DMM, 36, 151
Donor atom, 7
Doping, 5, 7–8, 38
Double-ended input, 607–608
Double-ended output, 608–609
Doubler, 99–100
Dynamic resistance, 23–26

E
Efficacy, 45
Electric field, 378
Electron, 3–4
Electron flow, 9
Electron volt, 7
Electronic workbench. *See* Multisim
Emergency lighting system, 848–849
Emitter-bias configuration, 169–175, 196, 219–220, 222–223, 224–225, 267–273, 327–328
Emitter-follower configuration, 186–187, 273–277, 290, 305–308, 328–329
Energy gaps, 43–44
Energy levels, 5–7
Enhancement-type MOSFET. *See* MOSFETs
Equivalent models. *See* DIODES; BJTs; JFETs; MOSFETs
EWB. *See* Multisim
Exponential function, 13–15
Extrinsic materials, 7–10

F
Fall time, 215
Feedback amplifier—frequency and phase, 763–765
Feedback circuits, 752
Feedback connection types, 752–758
Feedback gain, 753
Feedback pair, 314–318
FET phase-shift oscillator, 768
Fiber optic system, 467–469
Field effect transistor. *See also* JFETs; MOSFETs
  ripple voltage, 784
  voltage regulation, 784–785
Filter, 346
Fixed-bias configuration, 163–169, 194–195, 216, 219, 222, 224 225–226, 236–237, 265, 289, 325–326, 423–427, 489–491
Fleming, J. A., 129
Flicker noise, 347–348
Footcandle, 44
Fourier series, 588–591
Free carriers, 10–13
Free electrons, 5, 7, 8
Frequency response. *See* BJTs; JFETs; MOSFETs
Full-wave rectification, 75–78
Fundamental frequency, 705

G
GaAs, 2–19, 41–48, 379
Gain–bandwidth product, 580–583
Gain margin, 765
Gallium arsenide, 2–19, 41–48, 379
Gate turn-off switch, 851–852
Germanium, 2–7, 41
Giacoletto model, 579

H
Half-power frequencies, 557
Half-wave rectification, 72–75, 79
Harmonic distortion, 706–708
Harmonics, 588, 705, 706
Hartley oscillator, 772–773
Heat sink, 103
High-frequency response
  BJTs, 576–583
  JFETs, 583–586
High-pass filter, 667
Hole, 8
Hybrid equivalent circuit, 254, 319–336
Hybrid pi model, 255, 337–338, 579

I
IC, 1
IC phase-shift oscillator, 769–770
IC voltage regulator, 798–802
Ideal diode, 20–21, 29, 61
Inductor, 104, 105
Infrared, 41

Input impedance with feedback, 754–755
Instrumentation amplifier, 665–666
Instrumentation circuits, 663–666
Integrated circuit, 1
Integrator, 625–627
Interfacing circuitry, 742–745
Intrinsic materials, 3–5
Inverter, 412, 413
Inverting amplifier, 574–576, 623
Ionization potential, 3
IR emitters, 828

J

JFETs
  ac analysis, 481–544
  applications, 461–470, 522–530
  break frequencies, 583–585
  cascade, 518–523
  case construction, 408
  combination networks, 449–452
  common-gate configuration, 498–501
  computer analysis, 416–418, 471–473, 531–536, 592–601
  construction, 379–380
  curve tracer, 394
  dc analysis, 422–480
  design, 452–454, 511–513
  effects of R_S and R_L, 516–518
  fixed-bias configuration, 423–427, 489–491, 531–533
  high-frequency analysis, 583–586
  input impedance, 487
  low-frequency analysis, 571–574
  Miller effect capacitance, 574–576
  n-channel, 379–384
Johnson noise, 346–348
Junction field-effect transistor. *See* JFET

K

Kilby, Jack St. Clair, 1, 2
Knee voltage, 17, 28–30

L

Ladder-network conversion, 731–732
Latching relay, 853–854
LCD, 41
Leakage current, 131
LEDs, 7, 41–48, 68–69, 92–93, 108–109, 232–233
  axial luminous intensity, 44
  candela, 44
  characteristics, 44
  construction, 41–42
  efficacy, 45
  energy gaps, 43–44
  footcandle, 44
  frequency spectrum, 42–43
  photons, 41
  wavelength, 42–44
Light-activated SCR, 841, 852–854
Light-emitting diodes. *See* LEDs
Linear-digital ICs, 722–750
Liquid crystal displays, 829–831
Load-line analysis
  BJT, 166–169, 173–174, 181, 185
  diodes, 56–61
Logarithms, 545–549
Logic gates, 231–232
Log scale, 34–35, 548–549
Low-frequency analysis, 559–574
  BJTs, 564–571
  break frequency, 557
  JFETs, 571–574
  log plot, 548, 549
  phase plot, 559
Low-pass filter, 667–668

M

Majority carrier, 9–10, 130–131
MESFET, 379, 413–415, 423
  characteristics, 414
  construction, 414–415
  operation, 415
  symbols, 415
Metal-oxide-semiconductor field-effect transistor. *See* MOSFET
Metal-semiconductor field-effect transistor. *See* MESFET
Microphone, 345–346
Miller effect capacitance, 574–576
Minority carrier, 9–10, 130–131
Mirror circuits, 205–208
Models. *See* Individual device
Monostable operation, 735
MOSFET relay driver, 469–470
MOSFETs, depletion type, 397–402, 439–443, 450, 456, 505–506
  characteristics, 398–399
  construction, 397–398
  effects of R_S and R_L, 516–518
  equivalent model, 505
  operation, 398–400
  p-channel, 455–457
  relay driver, 469–470
  self-bias configuration, 442
  specifications sheets, 402
  summary table, 449
  symbols, 408
  terminal identification, 408
  troubleshooting, 521–522
  voltage divider configuration, 439–442, 505–506
MOSFETs, enhancement type, 397, 403–410, 443–449, 506–507
  characteristics, 403–407
  CMOS, 412–413
  computer analysis, 471–473
  construction, 403
  design, 452–454
  drain feedback configuration, 507–510
  effects of R_S and R_L, 516–518
  equivalent model, 506–507
  feedback biasing, 444–447
  handling, 410
  operation, 403–407
  p-channel, 455–457
  specifications sheets, 408–409
  summary table, 449
  symbols, 407–409
  terminal identification, 408
  transfer characteristics, 406–407
  troubleshooting, 521–522
  VMOS, 411–412
  voltage-divider configuration, 447, 510–511
Motion detector system, 529–530
Multiplier circuits, 98–101
Multisim, 50–51, 117–119, 237–238, 359–361, 472–473, 535–536, 597–599
Multistage amplifier effects, 586–588

N

Natural logarithms, 546
Negative temperature coefficient, 5
Neutrons, 3–4
nMOS on/off operation, 617
Non-inverting amplifier, 623–624
Non-inverting opamp, 463–464
Normalization, 44, 148–149, 557–558
npn BJT transistor, 135

n-type materials, 7–19
Nucleus, 3
Nyquist criterion, 764–765

O

Octave, 563
Offset currents and voltages, 628–631, 636
Ohl, Russell, 19
Ohmmeter, 36–37, 151
Op-amp, 231, 463–464, 527, 607, 620–623, 638–639
  applications, 653–682
  specs, 643
Open-circuit, 69
Open-circuit output admittance parameter, 320
Open-circuit, reverse transfer, voltage ratio parameter, 320
Opto-isolators, 867–869
OR gates, 70–72
Oscillator circuits, 751–782
Oscillator operation, 766–767
Output impedance with feedback, 755–756

P

Parallel diode configurations, 67–70
Parallel-resonant circuit, 775–776
Peak inverse voltage, 16, 75, 78
Pentavalent, 3, 7
Phase-locked loop (PLL), 738–742
Phase margin, 765
Phase plot, 559
Phase relationship
  collector dc feedback configuration, 285
  collector feedback configuration, 281
  common-base configuration, 278
  common-emitter configuration, 264
  emitter-bias configuration, 268
  emitter-follower configuration, 275
  voltage-divider configuration, 267
Phase-shift networks, 527–528
Phase-shift oscillator, 767–770
Photoconductive cells, 826–828
Photodiodes, 824–826
Photons, 4, 41–42
Phototransistors, 865–867
Pink noise, 346–347
PIV rating, 16, 75, 78
Planck's constant, 44, 822
pMOS on/off operation, 618
pnpn devices, 841
pnp BJT transistor, 130–154, 210
Point-contact transistor, 129
Polarity detector, 108–109
Positive temperature coefficient, 5
Power amplifiers, 683–721
Power diodes, 818
Power supplies, 783
Power transistor heat sinking, 709–710
Practical applications
  alarm systems with a CCS, 229–231
  audio mixer, 342–345
  constant-current source, 228–229
  controlled battery-powered backup, 108
  fiber optic system, 467–469
  logic gates, 231–232
  MOSFET relay driver, 469–470
  motion detector system, 529–530
  noninverting opamp, 464–465
  phase-shift networks, 527–528
  polarity detector, 108–109
  polarity insurance, 107–108
  preamplifier, 345–346
  protective configuration, 104–107
  random noise generator, 346–348
  rectification, 101–104
  regulator, 110–111
  relay driver, 226–228
  silent switching, 524–527
  sound-modulated light source, 348–349
  square-wave generator, 110–111
  three-channel audio mixer, 522–524
  timer network, 466–467
  voltage controlled resistor, 461–466
  voltage-level indicator, 232–233
  voltage reference levels, 109
  voltmeter, 465–466
Practical feedback circuits, 758–763
Preamplifier, 345–346
Programmable unijunction transistor, 869–874
Protective configurations, 104–107
Proximity detector, 855–856
PRV, 16, 75, 78
PSpice, 50, 114–117, 155–157, 352–359, 416–418, 471–472, 531–535, 596–597, 599–600, 601
p-type materials, 7–19
Push–pull circuits, 701

Q

Quasi-complementary push–pull amplifier, 702–704

R

Random-noise generator, 346–348
RC-coupled amplifier, 302–303, 556
RC filter, 789–791
Rectification, 32, 101–103
Rectifiers, 32, 72–78
Reference voltage levels, 109
Region of operation, 144–145
Regulator, 93–98, 101, 110–111
Relative mobility, 5
Relay, 104–105
Relay driver, 226–228
Resistance levels, 21–27
Reverse breakdown voltage, 16–19, 46
Reverse recovery time, 31–32
Reverse saturation current, 11–19, 31, 217–218
Relaxation oscillator, 777, 863, 872–873
Rise time, 215
r_e model, 253, 257–262, 338–340
Ross, Dr. Ian, 379
RS-232C-TO-TTL converter, 743–745

S

Saturation, 133, 144, 161–163, 165–166, 173, 181, 185, 211–212
Saturation current, 382–383
Schottky barrier diodes, 811–815
SCR, 348–349
SCR triggering, 860–863
Shockley diode, 854
Self-bias configuration, 427–431, 458–461, 492–496
Semiconductor diodes, 1–54
Semiconductor materials, 2–19
  covalent bonding, 3–5
  energy levels, 5–7
  extrinsic, 7–10
  germanium, 2–7
  hole, 8
  intrinsic, 3–5
  majority carrier, 9–10
  minority carrier, 9–10
  n-type, 7–19

Semiconductor materials (*continued*)
  p-type, 7–19
  relative mobility, 5
Semi-log plot, 34, 35, 548–549
Series diode configurations, 61–67
Series-fed class A amplifier, 685–688
Series-parallel diode configurations, 67–70
Series static switch, 846
Series-resonant circuit, 774–775
Series voltage regulation, 791–795
Shockley, William Bradford, 386
Shockley's equation, 13–19, 386–390
Short-circuit, 64
Short-circuit-, forward transfer current ratio parameter, 320
Short-circuit input impedance parameter, 320
Shot noise, 346
Shunt voltage regulation, 795–797
Silent switching network, 524–527
Silicon, 2–19, 41
Silicon-controlled rectifiers (SCRs), 841
Silicon-controlled switch, 849–851
Single-ended input, 607
Slew rate, 632–633
Snubber, 104
Software, 50–51
Solar cells, 819–824
Sound-modulated light source, 348–349
Source-follower configuration, 501–505
Specification sheets
  BJTs, 145–149
  diodes, 32–35
  JFETs, 390–394
  LEDs, 44
Square-wave generator, 110–111
Square-wave testing, 588–591
Stability factor, 162, 172–173, 203–211
Stabilization, 172–173, 217–226
Storage time, 31, 215
Summary tables
  field effect transistors, 415
  loaded BJT transistor amplifiers including the effects of R, 292, 293–295
  switching regulation, 797–798
  unloaded BJT transistor amplifiers, 292
  Z_i, Z_o, and A_v for various FET configurations, 513–516
Summing amplifier, 624–625
Superposition, 254, 343
Switching networks, 211–215

T

Temperature coefficient, 40
Temperature controller, 847–848
Temperature effects, 5–6, 18–19, 32–35, 217–218
Testing
  BJTs, 149–151
  diodes, 36–37
Tetravalent, 3
Thermal voltage, 13
Thermistors, 831–833
Thévenin equivalent, 343–344
Timer IC operation, 732–736
Timer network, 466–467
Transconductance, 482–488
Transfer characteristics, 386–390, 482–489
Transformation
  current, 690
  impedance, 690
  voltage, 690
Transformer, 77–78, 99–103
Transformer-coupled amplifier, 556
Transformer-coupled class A amplifier, 688–695
Transistor phase-shift oscillator, 769
Transistor tester, 150–151
Transition capacitance, 30
Triac, 856–857
Triode, 129
Tripler, 100–101
Trivalent, 3
Troubleshooting
  BJTs, 215–217, 340–342
  JFETs, 455, 521–522
Tuned oscillator circuit, 771–773
Tunnel diodes, 833–837
Turns ratio, 101
Two-port systems approach, 292–300
Two-terminal devices, 811

U

Unbypassed emitter-bias configuration, 327–328
Unijunction oscillator, 777–778
Unijunction transistor, 857–865
Unity follower, 624
Unity gain, 622
Universal JFET bias curve, 458–461

V

Vacuum tube, 129
Valence electrons, 3–7
Varactor diodes, 817
Variable-resistance phase control, 846–847
Virtual ground, 622–623
VMOS, 411–412
Voltage buffer, 660–661
Voltage-controlled current source, 662
Voltage-controlled oscillator, 736–738
Voltage-controlled resistor, 384, 461–466
Voltage-controlled voltage source, 661–662
Voltage-divider bias configuration, 175–181, 196, 220, 225, 233, 265–267, 292, 326–327, 352–357, 431–436, 497–498
Voltage doubler, 99–100
Voltage feedback dc biasing, 181–186
Voltage-level indicator, 232–233
Voltage multiplier circuits, 98–101
Voltage reference levels, 109
Voltage regulators, 783–810
Voltage sensor, 850
Voltage-series feedback, 752, 753
Voltage-shunt feedback, 752, 753
Voltage summing, 657–660
Voltage subtraction, 658–660
Voltage tripler, 100–101

W

Wavelength, 42–44
White noise, 346–347
Wien bridge oscillator, 770–771

Z

Zener breakdown, 16
Zener diode, 16, 38–41, 91–98, 111–112, 209, 410
Zener region, 16